ZLP32300

Low-Voltage Infrared OTP

Programming Specification

PRS000303-1005

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Table of Contents

List of Figures

List of Tables

OTP Programming Specification

General Description

The ZLP32300 EPROM features 256K bits that are arranged as 32K x 8. Additional bit exist as option bits, shadow rows and shadow columns.

The EPM and VPP pins control the device to provide EPROM mode access (programming & read verify). When EPM or VPP are asserted, the device enters EPROM mode, otherwise the device is in User mode. Various programming modes are available in EPROM mode based on the internal mode register settings.

In EPROM mode, the ZLP32300 features an internal address generator that is incremented using the CLK input and is cleared using the CLR input.

Programming Algorithm: 3X Overprogram Intelligent

Table 1. Option Bit Table (Option Available Denoted by x)

Pin-count	20-DIP/SOIC/SSOP	28-DIP/SOIC/SSOP	40-DIP, 48-SSOP
Port 0: 0-3 Pull-ups	x	x	x
Port 0: 4-7 Pull-ups	x	x	x
Port 1: 0-3 Pull-ups			x
Port 1:4-7 Pull-ups			x
Port 2: 0-7 Pull-ups	x	x	x
WDT Perm	x	x	x
EPROM Protection	x	x	x

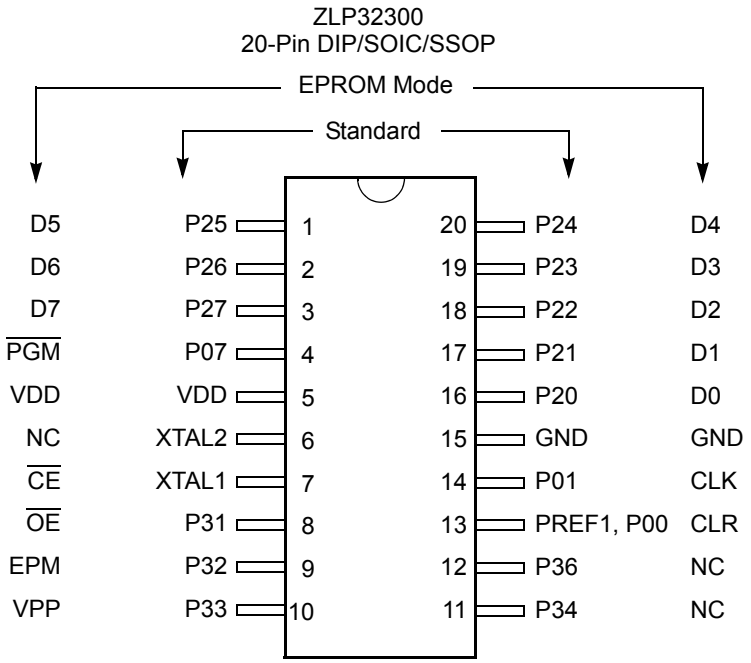


Figure 1. 20-Pin DIP/SOIC/SSOP Pin Assignments

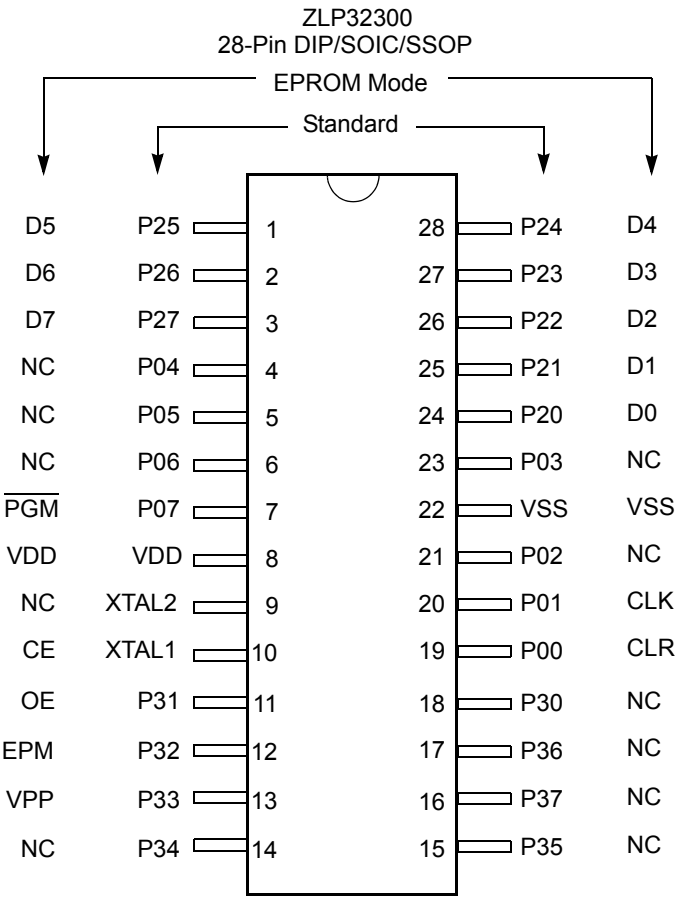


Figure 2. 28-Pin DIP/SOIC/SSOP Pin Assignments

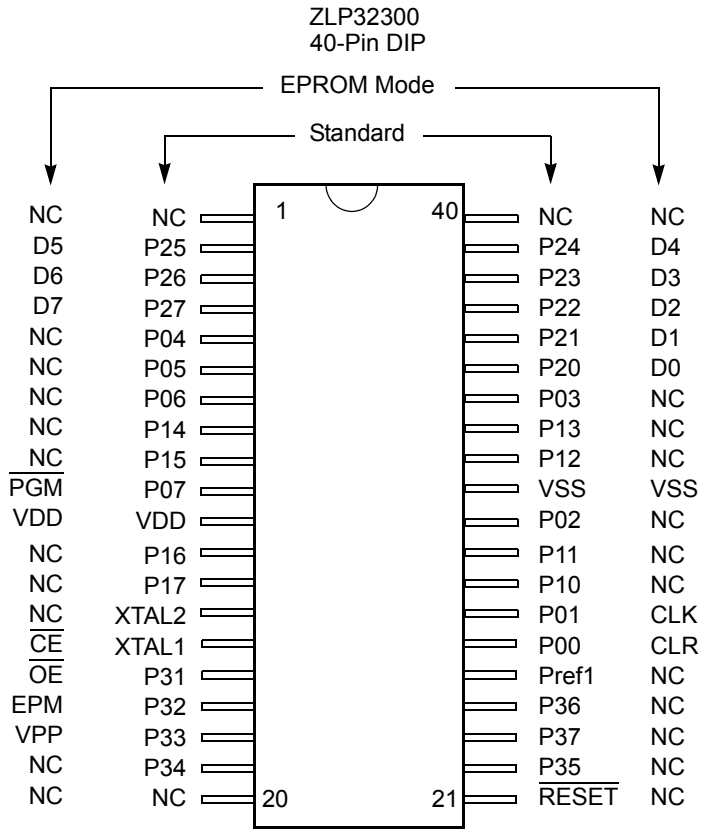


Figure 3. 40-Pin DIP Pin Assignments

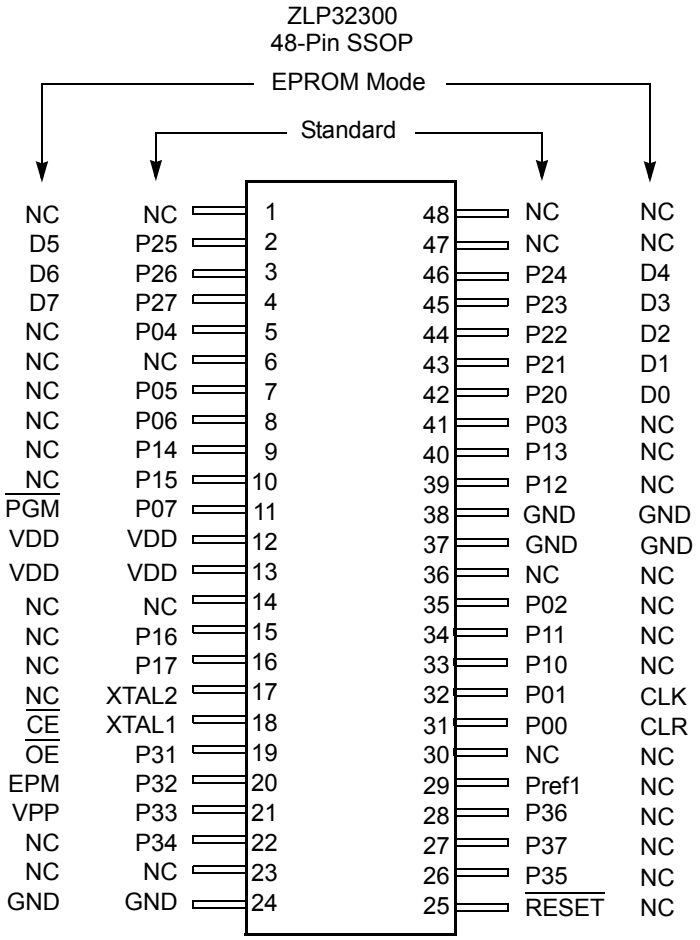


Figure 4. 48-Pin SSOP Pin Assignments

Detailed Pin Descriptions for EPROM Mode

The following is the description of the pinouts and functions for the pins when the part is placed in either EPROM or test modes. Two of the pins have what is called a High Voltage Detector (HVD) which is a circuit to detect input voltages higher than V_{DD}. This high voltage is referred to as "V_H" and is specified below. The output of the HVD is a logic 1 or 0 depending if the input is above or below V_H respectively. The pins which have the HVD are VPP and EPM and are included in the descriptions below.

Signal Descriptions

VPP

Input pin; supplies the EPROM cell gate programming voltage. This pin is also used to latch one of the EPROM modes described in the programming table. When VPP goes above V_H, the 4 LSB address bits are latched and become the mode (3:0) inputs to the EPROM. To enter normal program/ verify mode the EPM pin is raised to V_H and the address is cleared to zero with the CLR pin, then the VPP pin is raised to V_{PP}. To enter any other mode the address must be incremented with the CLK input to the appropriate address before the VPP pin is raised to V_{PP}.

EPM

Input pin; When this pin is raised above V_H it is used to place the EPROM in one of the EPROM modes. This pin enables the mode latch and switches the address muxes to EPROM mode. It must be raised to V_H before the VPP pin is raised to V_{PP}. To clear an EPROM mode both the VPP and EPM pin must be reduced below V_H.

$\overline{OE}$

Input pin; Active low output enable. When low the output data pins contain data from the EPROM. When high (V_{DD}) the data outputs are tristated. Of course, for this pin to control the output pins the part must be in an EPROM mode by having EPM above V_H.

$\overline{CE}$

Input pin; Enables the EPROM operation when low. When high (V_{IH}) the EPROM is disabled. When this pin is set High the EPROM is disabled regardless of the current EPROM mode setting.

$\overline{PGM}$

Input pin; The active Low programming pulse that applies VPP to the EPROM during programming.

CLK

Input pin; this pin increments the address counter. This pin sequences through the address during programming and reading the EPROM in EPROM mode.

CLR

Input pin; This pin clears the address counter. It is used at the beginning of programming or reading to initialize the counter to zero.

D(7:0)

I/O pins, contain data to the EPROM in program mode and from the EPROM in read mode. The most significant bit is used to program/read the shadow column when in that mode.

NC

No connection pins. These pins have a valid logic state when in EPROM mode to minimize the current in through the input buffers.

Various EPROM Mode Descriptions

The modes are set by setting EPM above V_H then incrementing the address counter until the correct mode number is on the least significant bits of the address and raising the VPP pin above V_H. The VPP pin can be left high or lowered below V_H depending on the mode. However, each time VPP is raised above V_H a new mode is latched. (Except for margin read mode. The only way exit margin read mode is to reduce both EPM and VPP below V_H and start over.)

All program/read cycles are the same for any mode. Address (3:0) map to mode(3:0) one for one. As an example if one were to set the R/W option bits mode the EPM pin would be set above V_H, the address would be incremented to 3 (0011h), then the VPP is raised to V_{PP}. This action would latch the mode and all subsequent program cycles would be in R/W OPTION BITS mode. It is important to remember to clear the address back to zero after latching the mode and before be-ginning the first program/read at address 0. If the address is not reset back to 0 the first few addresses may be missed.

Table 2. Programming Modes

	Standard Mode	Direction
Mode	Mode Number	Address bit (3:0)
R/W EPROM	0	0000
Reserved	1	0001
Reserved	2	0010
R/W Option bits	3	0011
Reserved	4	0100

Table 2. Programming Modes (Continued)

	Standard Mode	Direction
Mode	Mode Number	Address bit (3:0)
Reserved	5	0101
Reserved	6	0110
Reserved	7	0111
Reserved	8	1000
Reserved	9	1001
Reserved	10	1010
Reserved	11	1011
Reserved	12	1100
Reserved	13	1101
Reserved	14	1110
Reserved	15	1111

User Mode

The EPROM normally operates in the USER mode for Z8 operation. USER mode is the default mode when the VPP and EPM pins are both below V_H. When in USER mode, the mode register that controls EPROM programming modes is reset (all bits set to 0). The $\overline{PGM}$ input is also forced inactive so that no programming can occur.

R/W EPROM: #0

This mode provides access to the EPROM through the external pins. This mode is entered by raising EPM above V_H then clearing the address counter to 0 by pulsing CLR high, then raising VPP above V_H. The Mode register is always cleared while in USER mode, thus, the Mode register contains a reset value when entering EPROM mode by raising EPM above V_H.

R/W Options: #3

By selecting this mode the option bits are made available. The 16 bits in word 0 and 1 are employed as hardwired option bits. To program the option bits EPM is raised above V_H, then the address counter is cleared then incremented to 3. Then VPP is raised to V_{PP} to latch the option mode. The address counter is again cleared and the normal program cycle is started. The data, in the table below, is

placed on the data bus and the $\overline{PGM}$ input is pulsed low per the programming algorithm.

If the EPROM is protected (option bit 0, word 0) the EPROM is forced into the OPTION mode. No other EPROM mode can be accessed externally. During Power On Reset (POR) the option bits are read, latched and deployed.

Table 3. Option Bits

Word 0	**Bit Description (default)**
Bit 7	WDT @POR (disable)
Bit 6	Reserved
Bit 5	P20-27 Pull-up (disable)
Bit 4	P04-07 Pull-up (disable)
Bit 3	P00-03 Pull-up (disable)
Bit 2	Reserved
Bit 1	Reserved
Bit 0	EPROM protection (not protected)
Word 1	**Bit Description (default)**
Bit 7	Reserved
Bit 6	Reserved
Bit 5	Reserved
Bit 4	Reserved
Bit 3	Reserved
Bit 2	Reserved
Bit 1	P10-P13 Pull-up (disabled)
Bit 0	P14-P17 Pull-up (disabled)

Note: To program the data word a 0 is placed in the appropriate position. To leave a bit unprogrammed place a 1 in that position.

When the bits are read using the R/W OPTION BITS mode (Mode #3), programmed bits read 0 and unprogrammed read 1.

Option Bit Description

P10-13 Pull-ups (bit 1, word 1):

When programmed, the pull-up transistors are enabled at P10 to P13. The default is disable.

P14-17 Pull-ups (bit 0, word 1):

When programmed, the pull-up transistors are enabled at P14 to P17. The default is disable.

WDT Permanently Enabled (bit 7, word 0):

When programmed the WDT is enabled permanently. The default is that the WDT is not permanently enabled.

P20-27 Pull-ups (bit 5, word 0):

When programmed, the pull-up transistors are enabled at P20 to P27. The default is disable.

P04-07 Pull-ups (bit 4, word 0):

When programmed, the pull-up transistors are enabled at P04 to P07. The default is disable.

P00-03 Pull-ups (bit 3, word 0):

When programmed, the pull-up transistors are enabled at P00 to P03. The default is disable.

EPROM Protect (bit 0, word 0):

The purpose of the EPROM protect option bit is to disable any access to the EPROM data from the outside world, thereby protecting any proprietary code from being read. Once this bit is programmed the EPROM only enters the OPTION BIT mode. It is not allowed to enter any other EPROM mode. If a read is attempted while the EPROM is protected the data comes only from the option row. The default is not protected.

Note: Program/Verify of the EPROM data must be performed prior to setting this option bit.

DC CHARACTERISTICS

- Read Operating Temperature: T0 =0° to 70°C
- Programming Temperature: T_P = 20°C to 30°C

Table 4 lists the specifications for pins VPP, VDD and EPM. Table 5 lists the recommended levels of these same pins.

Table 4. Pin VPP, VDD and EPM Specifications

Symbol	Parameter	Conditions	Units	Minimum	Typical	Maximum	Notes
V_H	High Voltage Detect Active	V_{DD}=3.0V-5.5V	Volts	V_{DD}+4V		10.75V	VPP, EPM pins
V_{IH}	Input High Voltage	V_{DD}=5.5V	Volts	0.7V_{DD}		V_{DD}	VPP, EPM pins
V_{IL}	Input Low Voltage	V_{DD}=5.5V	Volts	V_{SS}-0.3		0.2V_{DD}	VPP, EPM pins
I_{IL}	Input Leakage	V_{IN} = 5.5V V_{IN} = 10.5V	µA µA	-1.0 80	 100	1.0 150	VPP, EPM pins
I_{PP}	Program Current	V_{IN} = 10.5V	mA	0	0.5	2	VPP pin
I_{DD}	Program Current	V_{IN} = 5.5V	mA	0	5	10	VDD pin
V_{PP}	Programming Voltage		Volts	10.25	10.5	10.75	VPP pin
V_{DD}	Read Voltage Supply		Volts	3.0		4.5	VDD pin
V_V	Program/Verify Supply Voltage		Volts	5.4	5.5	5.6	VDD pin

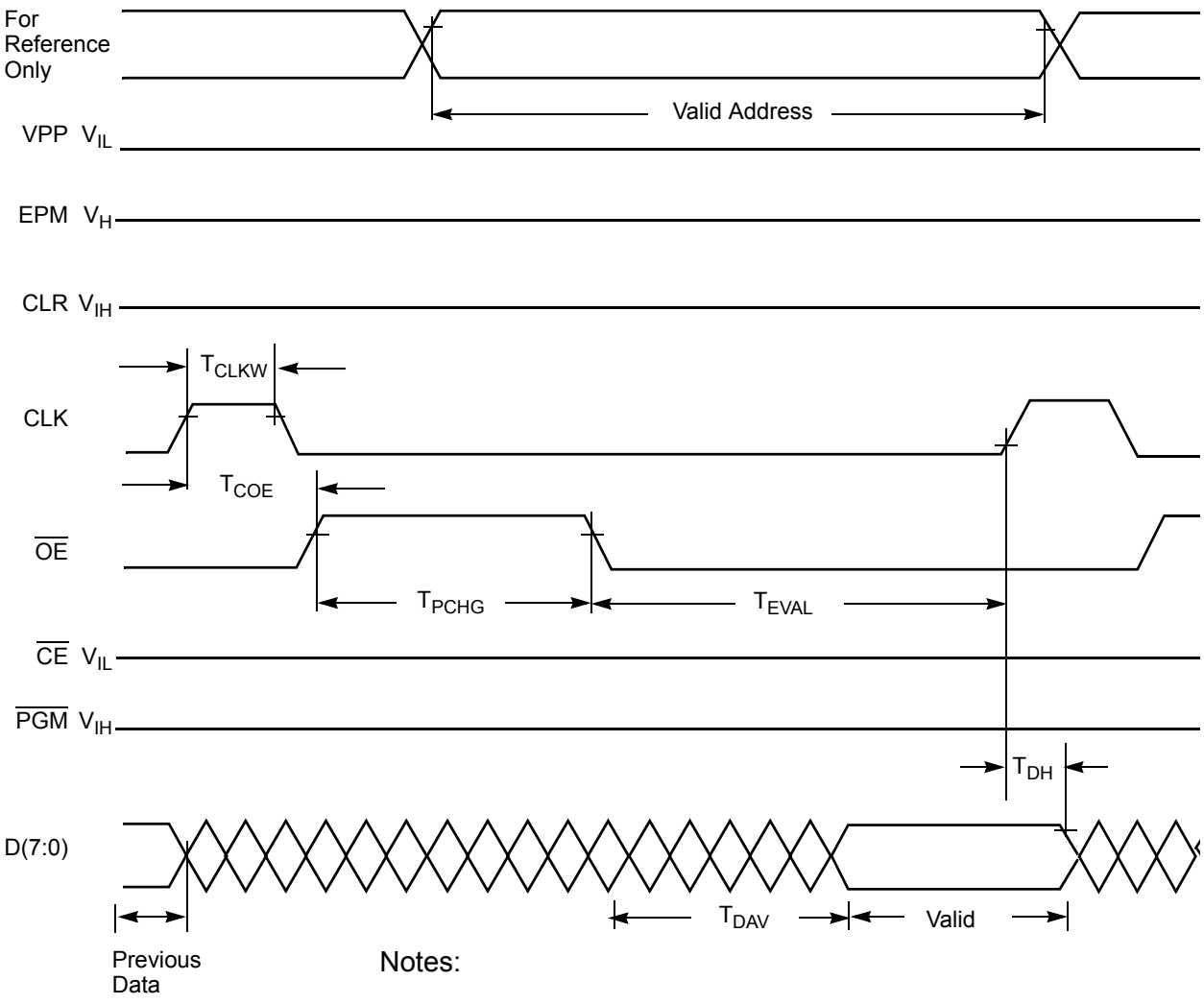
Note: The V_{PP} and V_H levels in this table represent the long-duration voltage level limits that the EPM and VPP inputs can sustain without damage. If short-duration spikes of the V_H and V_{PP} voltage levels cannot be prevented, the peak of the voltage spike should not exceed 1 Volt above the typical rating and should not have a duration of greater than 5 nanoseconds or potential damage to the EPM and/or VPP pins may occur.

Table 5. Recommended Levels for VDD, VPP and EPM

Recommended Levels:				
	V_{DD}/Read	**V_V/Program**	**V_{PP}**	**EPM**
Specs	3.0V-4.5V	5.5%+/-0.1V	10.5+/–0.25V	10.5+/–0.25V
3rd Party	3.0V	5.5V	10.5V	10.5V

AC Characteristics

- Read Operating Frequency: F0 = DC–1.67 MHz
- Read Operating Temperature: T0 =0° to 70°C
- Programming Temperature:T_P = 20°C to 30°C



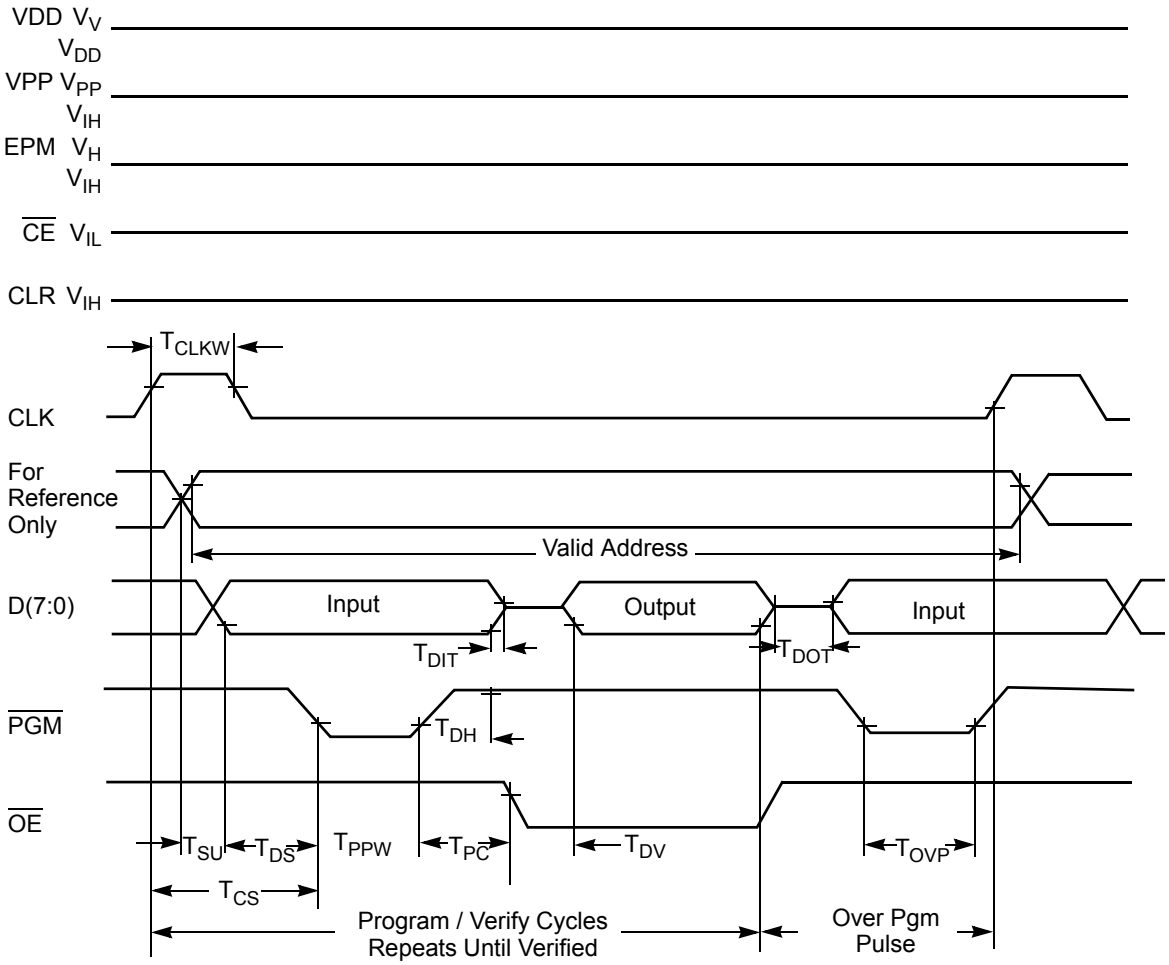
Notes:

1. Unless otherwise noted, all levels are V_{IL}, V_{IH}.
2. The power-on reset is assumed to be completed before EPM is raised to V_H.
3. Refer to the power up waveforms in Table 6 for initial timings.
4. The $\overline{OE}$ signal must make both transitions on each address.

Figure 5. Read Cycle Waveforms (Power-On Reset and Mode Select is Assumed Complete)

Table 6. Read Cycle Waveform Timing

Symbol	Parameter	Minimum	Maximum	Units
T_{COE}	CLK TO $\overline{OE}$	150	—	ns
T_{PCHG}	$\overline{OE}$ High to $\overline{OE}$ Low	250	—	ns
T_{DAV}	$\overline{OE}$ Low to Data Valid	—	200	ns
T_{EVAL}	$\overline{OE}$ Low to CLK High	375	—	ns
T_{CLKW}	CLK Pulse Width	125	—	ns
T_{DH}	Data Hold	0	—	ns



Note: Unless otherwise designated, all levels are V_{IL}, V_{IH}.

Figure 6. Program/Verify Cycle Waveforms

Table 7. Program/Verify Waveform Timing

Symbol	Parameter	Minimum	Maximum	Units
T_{CLKW}	CLK High to CLK Low	125	—	ns
T_{SU}	$\overline{OE}$ EPM VPP $\overline{CE}$ set up	1	n/a	µs
T_{CS}	Clock Set Up	1	n/a	µs
T_{DS}	Data Set Up	1	n/a	µs
TDH	Data Hold	100	n/a	ns
T_{PPW}	Program Pulse Width	0.10	1.05	ms
T_{OVP}	Overprogram Pulse	0.30	Note 2	ms
T_{PC}	$\overline{PGM}$ High to $\overline{OE}$ Low	1	n/a	µs
T_{OEW}	$\overline{OE}$ Low Width	250	n/a	ns
T_{DV}	$\overline{OE}$ Low to Data Valid	200	n/a	ns
T_{DIT}	Data Tristate before $\overline{OE}$ Low	100	n/a	ns
T_{DOT}	Data Tristate after $\overline{OE}$ High	100	n/a	ns

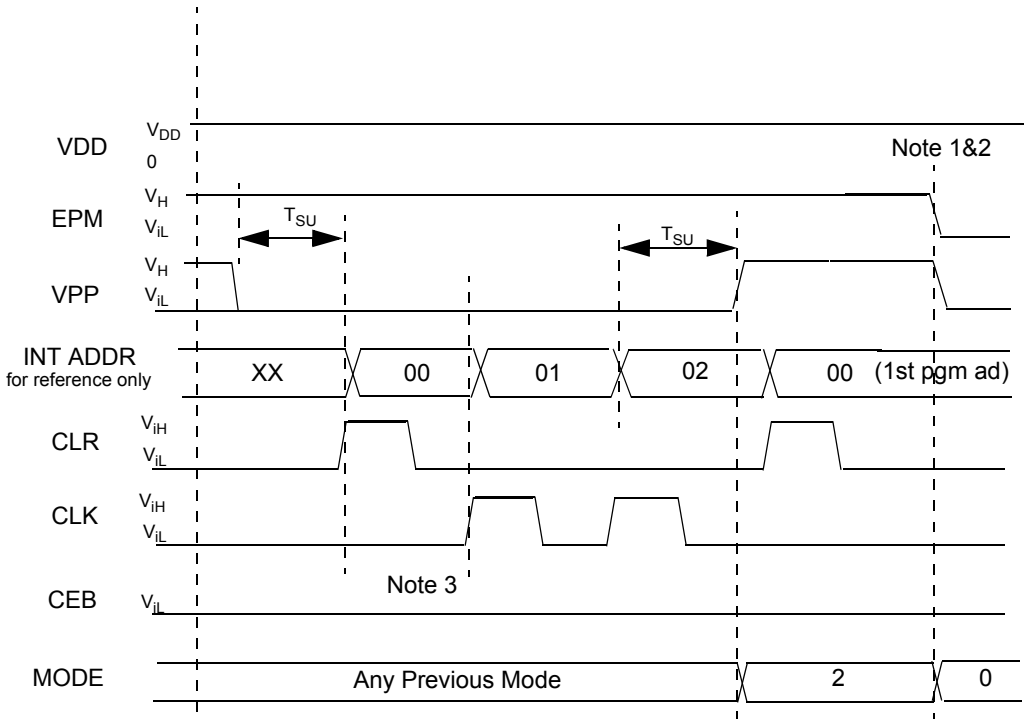
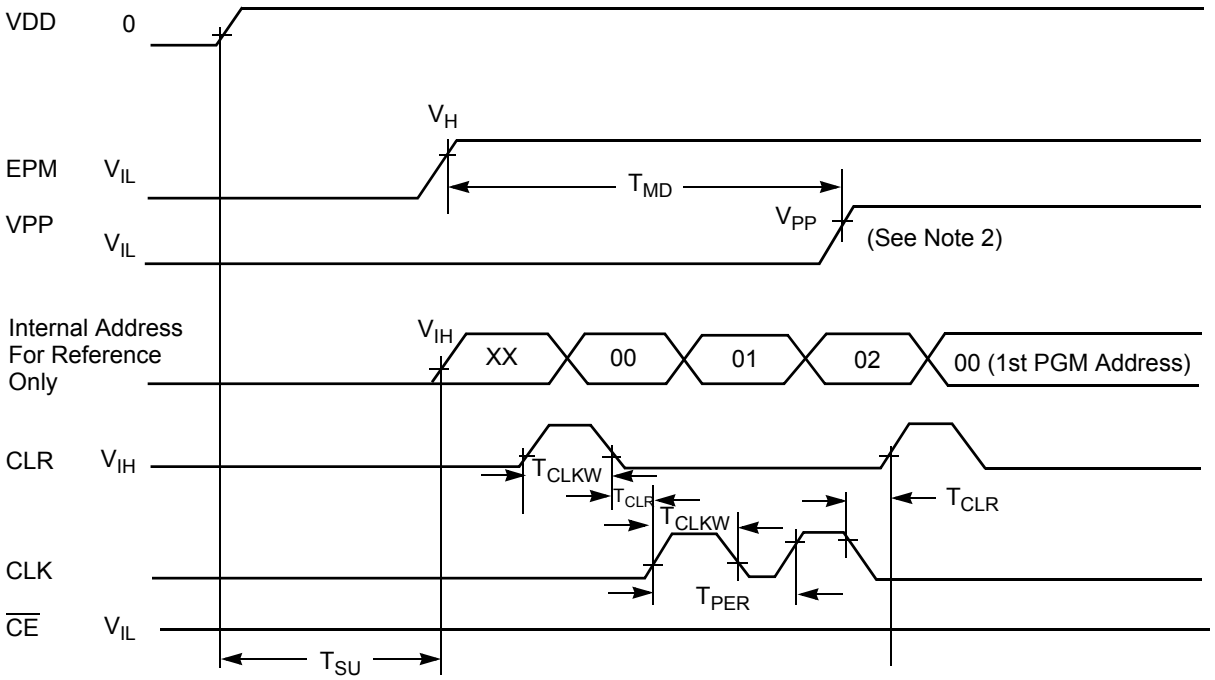


Figure 7. Changing Modes Waveforms

Table 8. Changing Modes Waveform Timing

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{SU}	Setup Time	1			us

Notes:
1. Exit all modes by setting EPM and VPP below V_H.
2. There is no restriction on the rise and fall times of EPM and VPP between V_H and V_{IL}, except to ensure that overshoot does not exceed the maximum or minimum VPP and EPM voltages.
3. Timing for CLR and CLK are the same as for Figure 8.



Note:

1. Program/Read mode is the default mode (addr=0) which occurs automatically when EPM is kept below V_H.
2. Different modes can be entered by raising VPP after a set number of CLK pulses. The this example, VPP was raised after two pulses which placed the EPROM in mode 2.

Figure 8. Normal EPROM Power-Up Waveforms

Table 9. Normal EPROM Power-Up Waveform Timing

Symbol	Parameter	Minimum	Maximum	Units
T_{SU}	VDD High to EPM	20	n/a	ms
T_{CLKW}	CLK/CLR Pulse Width	125	n/a	ns
T_{PER}	CLK Period	250	n/a	ns
T_{MD}	EPM High to VPP High	1	[see Note 2]	µs
T_{CLR}	Clear Pulse Spacing to Clock Pulse	250	n/a	ns

Note: All pins must be powered down before or concurrently with V_{DD} power down. All pins must be at ground potential or floating after V_{DD} is removed.

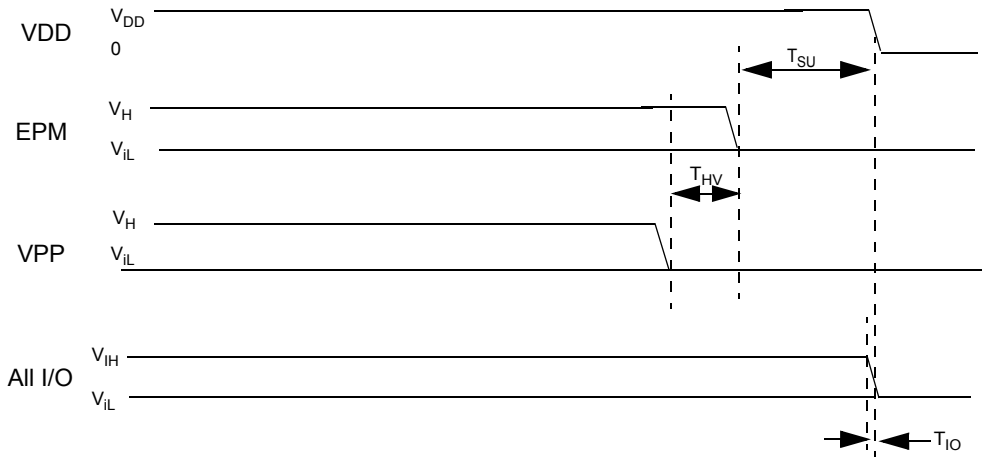


Figure 9. Power Down Timing Waveforms

Table 10. Power Down Waveform Timing

Symbol	Parameter	Minimum	Typical	Maximum	Units
T_{HV}	HV pins edges	0			us
T_{VDD}	HV pins low to V_{DD}=0	1			us
T_{IO}	I/O pins low to V_{DD}=0	0			us

Table 11. Device Pin Levels in EPROM Modes

Modes	Device Pins USER Mode - Upper EPROM Mode - Lower							Port 2 Config Data	Mode Addr A3–0	Notes
	P33 VPP	P32 EPM	XT1 $\overline{CE}$	P31 $\overline{OE}$	P30 $\overline{PGM}$	EPROM ADDR	VDD VDD			
EPROM Read	X	V_H	V_{IL}	V_{IL}	V_{IH}	Addr	V_{DD}	Out	00	1, 2
Program	V_{PP}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	Addr	V_V	In	00	1
Program Verify	V_{PP}	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Addr	V_V	Out	00	1
Program Options	V_{PP}	V_H	V_{IL}	V_{IH}	V_{IL}	0–1	V_V	In	03	1
Read Options	X	V_H	V_{IL}	V_{IL}	V_{IH}	0–1	V_{DD}	Out	03	1, 2

Note:
1. All modes are entered by first setting EPM above V_H. The address counter clears with CLR and then increments to the appropriate address. VPP is raised above V_H to latch the mode, and the address counter ise reset to zero before continuing. All address values are hexadecimal.
2. X = V_{IL} or V_{IH} after latching mode at V_H.

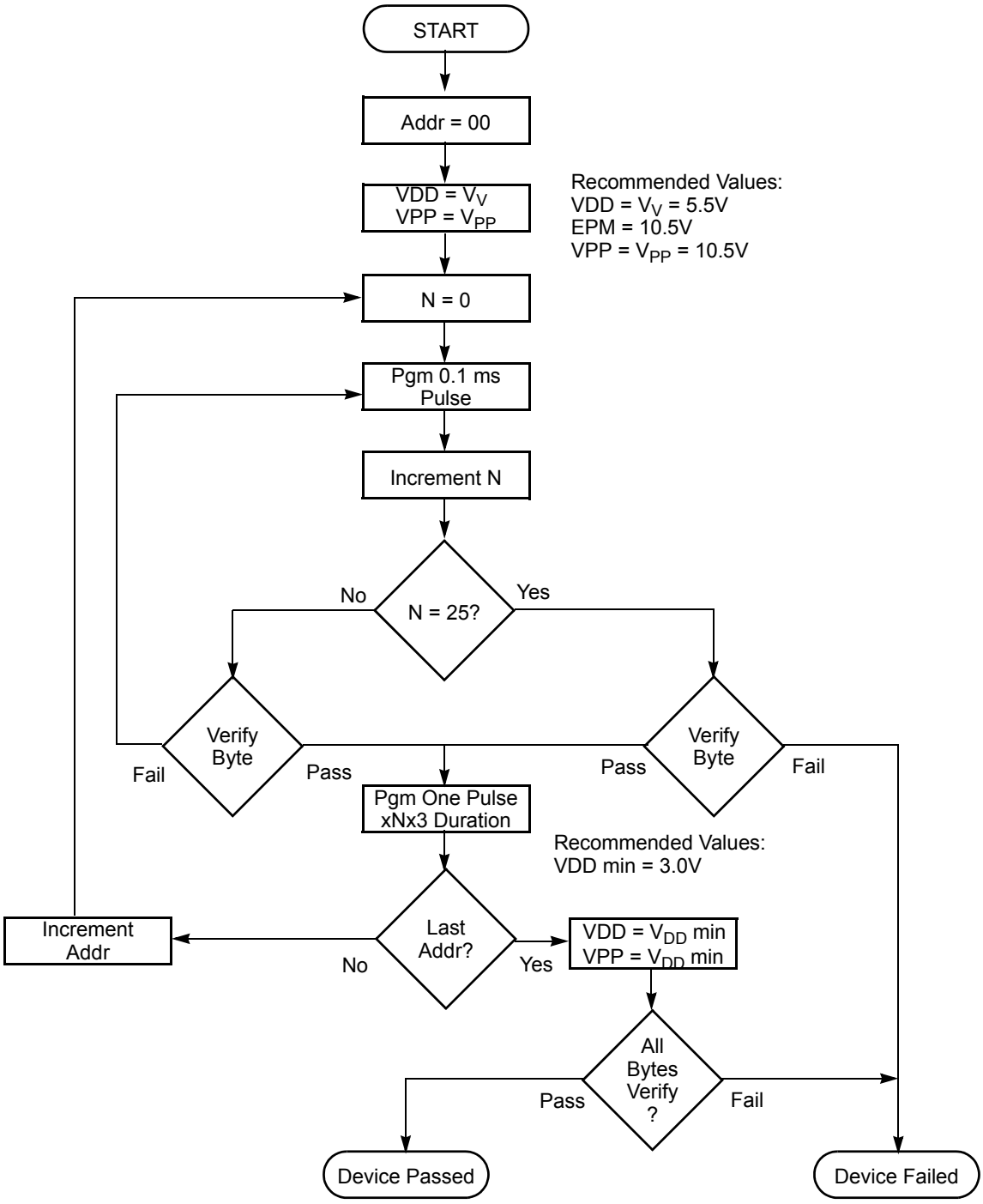


Figure 10. OTP Programming Flowchart

Summary: ZLP32300 versus Z86D73

Table 12. Summary of EPROM Differences Between ZLP32300 and Z86D73

	ZLP32300	Z86D73	Notes
FAB	UMC	ZiLOG	
V_{DD} for programming (nom)	5.5V	4.5V	1
V_{PP} (nom)	10.5V	12.75V	1
I_{DD}, maximum for 4 pages	10 mA		
I_{PP}, maximum for 4 pages	2mA	40mA	
I_{IL}, maximum	150 µA	110µA	
T_{PPW} (Program Pulse Width), minimum	0.1ms	1ms	
Timing Parameters (added for clarity)			
T_{AS}, T_{POR}	No	Yes	
T_{DH}, T_{CS}, T_{DV}, T_{DIT}, T_{DOT}, T_{CLR}, T_{HV}, T_{VDD}, T_{IO}	Yes	No	
Pinout			
44-Pin, 68-Pin	No	Yes	
20-Pin	Yes	No	
Option bits			
XTAL feedback disable, P00-P03 level (mouse mode Vt adjust), XTAL/RC, VBO bandgap	No	Yes	
ROM protect, Size 1, Size 0, 28-Pinout, 20-Pinout	Yes	No	
PGM pin assignment	P07	P02	2

Notes:
1. For ZLP32300, programming current flows through V_{DD}. For Z86D73, programming current flows through VPP.
2. The Z86D73 EPROM mode/PGM pin (P02) is not available on the new 20-pin configurations. It is relocated to P07. This change affects existing program adapter boards.

Ordering Information

Device	Part Number	Description	Part Number	Description
Crimzon™ ZLP32300	ZLP32300H4832	48-pin SSOP 32K OTP	ZLP32300H4808	48-pin SSOP 8K OTP
	ZLP32300P4032	40-pin PDIP 32K OTP	ZLP32300P4008	40-pin PDIP 8K OTP
	ZLP32300H2832	28-pin SSOP 32K OTP	ZLP32300H2808	28-pin SSOP 8K OTP
	ZLP32300P2832	28-pin PDIP 32K OTP	ZLP32300P2808	28-pin PDIP 8K OTP
	ZLP32300S2832	28-pin SOIC 32K OTP	ZLP32300S2808	28-pin SOIC 8K OTP
	ZLP32300H2032	20-pin SSOP 32K OTP	ZLP32300H2008	20-pin SSOP 8K OTP
	ZLP32300P2032	20-pin PDIP 32K OTP	ZLP32300P2008	20-pin PDIP 8K OTP
	ZLP32300S2032	20-pin SOIC 32K OTP	ZLP32300S2008	20-pin SOIC 8K OTP
	ZLP32300H4816	48-pin SSOP 16K OTP	ZLP32300H4804	48-pin SSOP 4K OTP
	ZLP32300P4016	40-pin PDIP 16K OTP	ZLP32300P4004	40-pin PDIP 4K OTP
	ZLP32300H2816	28-pin SSOP 16K OTP	ZLP32300H2804	28-pin SSOP 4K OTP
	ZLP32300P2816	28-pin PDIP 16K OTP	ZLP32300P2804	28-pin PDIP 4K OTP
	ZLP32300S2816	28-pin SOIC 16K OTP	ZLP32300S2804	28-pin SOIC 4K OTP
	ZLP32300H2016	20-pin SSOP 16K OTP	ZLP32300H2004	20-pin SSOP 4K OTP
	ZLP32300P2016	20-pin PDIP 16K OTP	ZLP32300S2004	20-pin SOIC 4K OTP
	ZLP32300S2016	20-pin SOIC 16K OTP	ZLP32300P2004	20-pin PDIP 4K OTP
	ZLP32300100KIT	Development Kit	Emulator	ZLP323ICE00ZEM

Note: Contact www.zilog.com for the die form.