UNITRODE

UCC1888
UCC2888
UCC3888

Off-line Power Supply Controller

FEATURES

- Transformerless Off-line Power Supply
- Wide 100VDC to 400VDC Allowable Input Range
- Fixed 5VDC or Adjustable Low Voltage Output
- Output Sinks 200mA, Sources 150mA Into a MOSFET Gate
- Uses Low Cost SMD Inductors
- Short Circuit Protected
- Optional Isolation Capability

DESCRIPTION

The UCC3888 controller is optimized for use as an off-line, low power, low voltage, regulated bias supply. The unique circuit topology utilized in this device can be visualized as two cascaded flyback converters, each operating in the discontinuous mode, both driven from a single external power switch. The significant benefit of this approach is the ability to achieve voltage conversion ratios as high as 400V to 2.7V with no transformer and low internal losses.

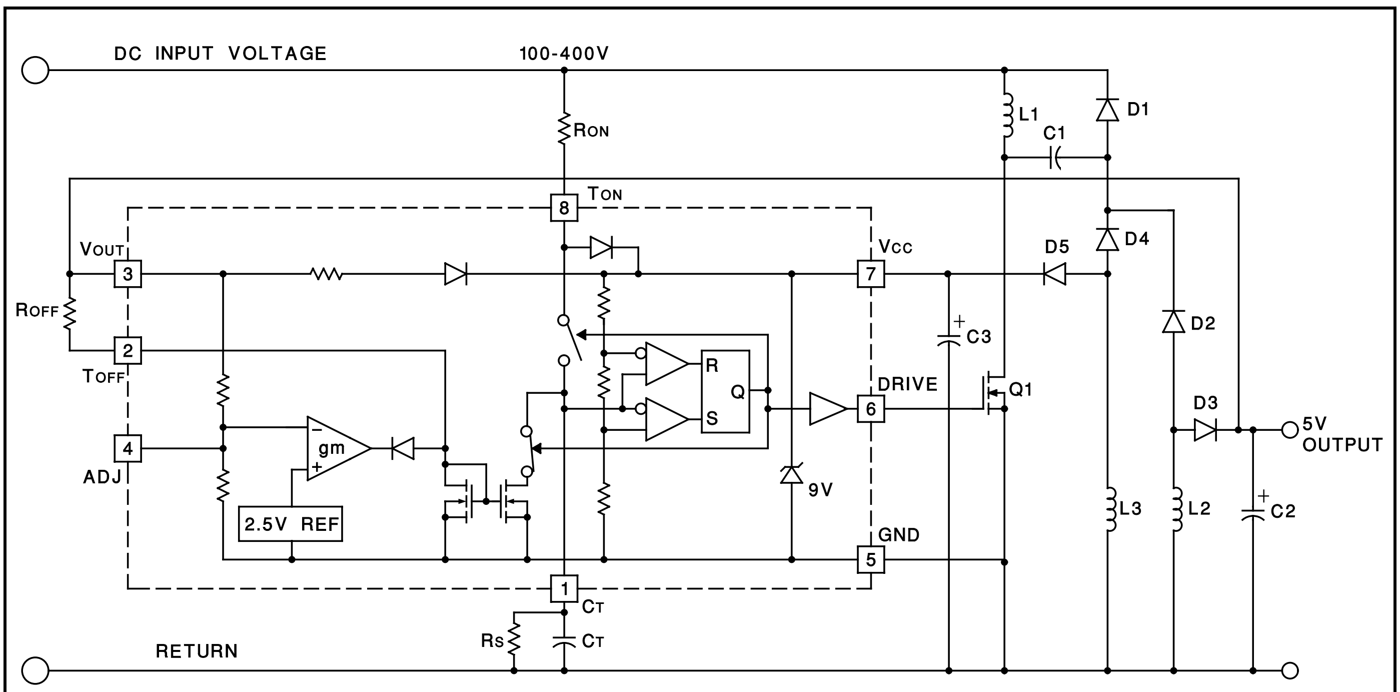
The control algorithm utilized by the UCC3888 sets the switch on time inversely proportional to the input line voltage and sets the switch off time inversely proportional to the output voltage. This action is automatically controlled by an internal feedback loop and reference. The cascaded configuration allows a voltage conversion from 400V to 2.7V to be achieved with a switch duty cycle of 7.6%. This topology also offers inherent short circuit protection since as the output voltage falls to zero, the switch off time approaches infinity.

The output voltage is set internally to 5V. It can be programmed for other output voltages with two external resistors. An isolated version can be achieved with this topology as described further in Unitrode Application Note U-149.

OPERATION

With reference to the application diagram below, when input voltage is first applied, the current through R_{ON} into T_{ON} is directed to V_{CC} where it charges the external capacitor, C3, connected to V_{CC}. As voltage builds on V_{CC}, an internal undervoltage lockout holds the circuit off and the output at DRIVE low until V_{CC} reaches 8.4V. At this time, DRIVE goes high turning on the power switch, Q1, and redirecting the current into T_{ON} to the timing capacitor, C_T. C_T charges to a fixed threshold with a current $I_{CHG}=0.8 \bullet (V_{IN} - 4.5V)/R_{ON}$. Since DRIVE will only be high for as long as C_T charges, the power switch on time will be inversely proportional to line voltage. This provides a constant (line voltage) • (switch on time) product.

TYPICAL APPLICATION



Note: This device incorporates patented technology used under license from Lambda Electronics, Inc. UDG-96013

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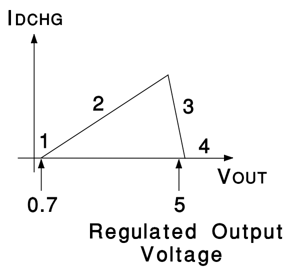
OPERATION (cont.)

At the end of the on time, Q1 is turned off and the current through R_{ON} is again diverted to V_{CC}. Thus the current through R_{ON}, which charges C_T during the on time, contributes to supplying power to the chip during the off time.

The power switch off time is controlled by the discharge of C_T which, in turn, is programmed by the regulated output voltage. The relationship between C_T discharge current, I_{DCHG}, and output voltage is illustrated as follows:



Region 1. When V_{OUT} = 0, the off time is infinite. This feature provides inherent short circuit protection. However, to ensure output voltage startup when the output is not a short, a high value resistor, R_S, is placed in parallel with C_T to establish a minimum switching frequency.

Region 2. As V_{OUT} rises above approximately 0.7V to its regulated value, I_{DCHG} is defined by R_{OFF}, and is equal to:

$$I_{DCHG} = (V_{OUT} - 0.7V) / R_{OFF}$$

As V_{OUT} increases, I_{DCHG} increases reducing off time. The operating frequency increases and V_{OUT} rises quickly to its regulated value.

Region 3. In this region, a transconductance amplifier reduces I_{DCHG} in order to maintain a regulated V_{OUT}.

Region 4. If V_{OUT} should rise above its regulation range, I_{DCHG} falls to zero and the circuit returns to the minimum frequency established by R_S and C_T.

The range of switching frequencies is established by R_{ON}, R_{OFF}, R_S, and C_T as follows:

$$\text{Frequency} = 1/(T_{ON} + T_{OFF})$$

$$T_{ON} = R_{ON} \bullet C_T \bullet 4.6\,V/(V_{IN} - 4.5V)$$

$$T_{OFF}\,(\max) = 1.4 \bullet R_S \bullet C_T$$

Regions 1 and 4

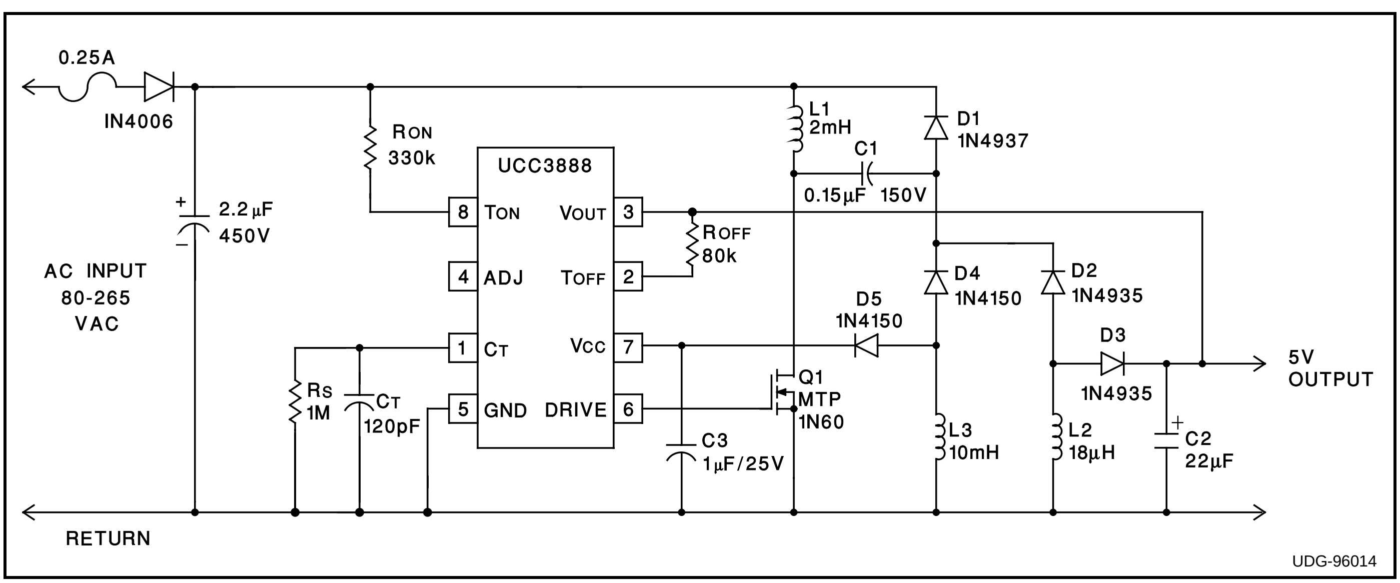
$$T_{OFF} = R_{OFF} \bullet C_T \bullet 3.7V/(V_{OUT} - 0.7V)$$

Region 2, excluding the effects of R_S which have a minimal impact on T_{OFF}.

The above equations assume that V_{CC} equals 9V. The voltage at T_{ON} increases from approximately 2.5V to 6.5V while C_T is charging. To take this into account, V_{IN} is adjusted by 4.5V in the calculation of T_{ON}. The voltage at T_{OFF} is approximately 0.7V.

DESIGN EXAMPLE

The UCC3888 regulates a 5 volt, 1 Watt nonisolated DC output from AC inputs between 80 and 265 volts. In this example, the IC is programmed to deliver a maximum on time gate drive pulse width of 2.2 microseconds which occurs at 80 VAC. The corresponding switching frequency is approximately 100kHz at low line, and overall efficiency is approximately 50%. Additional design information is available in Unitrode Application Note U-149.



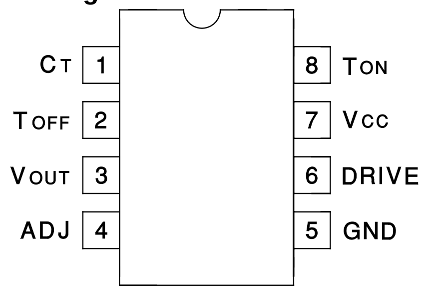
ABSOLUTE MAXIMUM RATINGS

I_{CC} 8mA
Current into T_{ON} Pin 1.5mA
Voltage on V_{OUT} Pin 20V
Current into T_{OFF} Pin 250µA
Storage Temperature . . . . -65°C to +150°C

Note: Unless otherwise indicated, voltages are referenced to ground and currents are positive into, negative out of, the specified terminals.

CONNECTION DIAGRAM

DIL-8, SOIC-8 (Top View)
N or J, D Package



ELECTRICAL CHARACTERISTICS

Unless otherwise stated, these specifications hold for T_A = 0°C to 70°C for the UCC3888, -40°C to +85°C for the UCC2888, and -55°C to +125°C for the UCC1888. No load at DRIVE pin (C_{LOAD}=0).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
General					
V_{CC} Zener Voltage	I_{CC} < 1.5mA	8.6	9.0	9.3	V
Startup Current	V_{OUT} = 0		150	250	µA
Operating Current I(V_{CC})	V_{CC} = V_{CC}(zener) – 100mV, F = 150kHz		1.2	2.5	mA
Under-Voltage-Lockout					
Start Threshold	V_{OUT} = 0	8.0	8.4	8.8	V
Minimum Operating Voltage after Start	V_{OUT} = 0	6.0	6.3	6.6	V
Hysteresis	V_{OUT} = 0	1.8			V
Oscillator					
Amplitude	V_{CC} = 9V	3.5	3.7	3.9	V
C_T to DRIVE high Propagation Delay	Overdrive = 0.2V		100	200	ns
C_T to DRIVE low Propagation Delay	Overdrive = 0.2V		50	100	ns
Driver					
VOL	I = 20mA, V_{CC} = 9V		0.15	0.4	V
	I = 100mA, V_{CC} = 9V		0.7	1.8	V
VOH	I = –20mA, V_{CC} = 9V	8.5	8.8		V
	I = –100mA, V_{CC} = 9V	6.1	7.8		V
Rise Time	C_{LOAD} = 1nF		35	70	ns
Fall Time	C_{LOAD} = 1nF		30	60	ns
Line Voltage Detection					
Charge Coefficient: I_{CHG} / I(T_{ON})	VCT = 3V, DRIVE = High, I(T_{ON}) = 1mA	0.73	0.79	0.85	
Minimum Line Voltage for Fault	R_{ON} = 330k	60	80	100	V
Minimum Current I(T_{ON}) for Fault	R_{ON} = 330k		220		µA
On Time During Fault	C_T = 150pF, V_{LINE} = Min – 1V		2		µs
Oscillator Restart Delay after Fault			0.5		ms
V_{OUT} Error Amp					
V_{OUT} Regulated 5V (ADJ Open)	V_{CC} = 9V, I_{DCHG} = I(T_{OFF})/2	4.5	5.0	5.5	V
Discharge Ratio: I_{DCHG} / I(T_{OFF})	I(T_{OFF}) = 50µA	0.93	1.00	1.07	
Voltage at T_{OFF}	I(T_{OFF}) = 50µA	0.6	0.95	1.3	V
Regulation gm (Note 1)	Max I_{DCHG} = 50µA		2.4		mA/V
	Max I_{DCHG} = 125µA	1.9	4.1	7.0	mA/V

Note 1: gm is defined as $\frac{\Delta I_{DCHG}}{\Delta V_{OUT}}$ *for the values of* V_{OUT} *when* V_{OUT} *is in regulation. The two points used to calculate gm are for* I_{DCHG} *at 65% and 35% of its maximum value.*

PIN DESCRIPTIONS

ADJ: The ADJ pin is used to provide a 5V regulated supply without additional external components. Other output voltages can be obtained by connecting a resistor divider between VOUT, ADJ and GND. Use the formula

$$V_{OUT} = 2.5V \bullet \frac{R1 + R2}{R2}$$

where R1 is connected between VOUT and ADJ, and R2 is connected between ADJ and GND. R1 || R2 should be less than 1kΩ to minimize the effect of the temperature coefficient of the internal 30k resistors which also connect to VOUT, ADJ, and GND. See Block Diagram.

CT (timing capacitor): The signal voltage at CT has a peak-to-peak swing of 3.7V for 9V VCC. As the voltage at CT crosses the oscillator upper threshold, DRIVE goes low. As the voltage on CT crosses the oscillator lower threshold, DRIVE goes high.

DRIVE: This output is a CMOS stage capable of sinking 200mA peak and sourcing 150mA peak. The output voltage swing is 0 to VCC.

GND (chip ground): All voltages are measured with respect to GND.

TOFF (regulated output control): TOFF sets the discharge current of the timing capacitor through an external resistor connected between VOUT and TOFF.

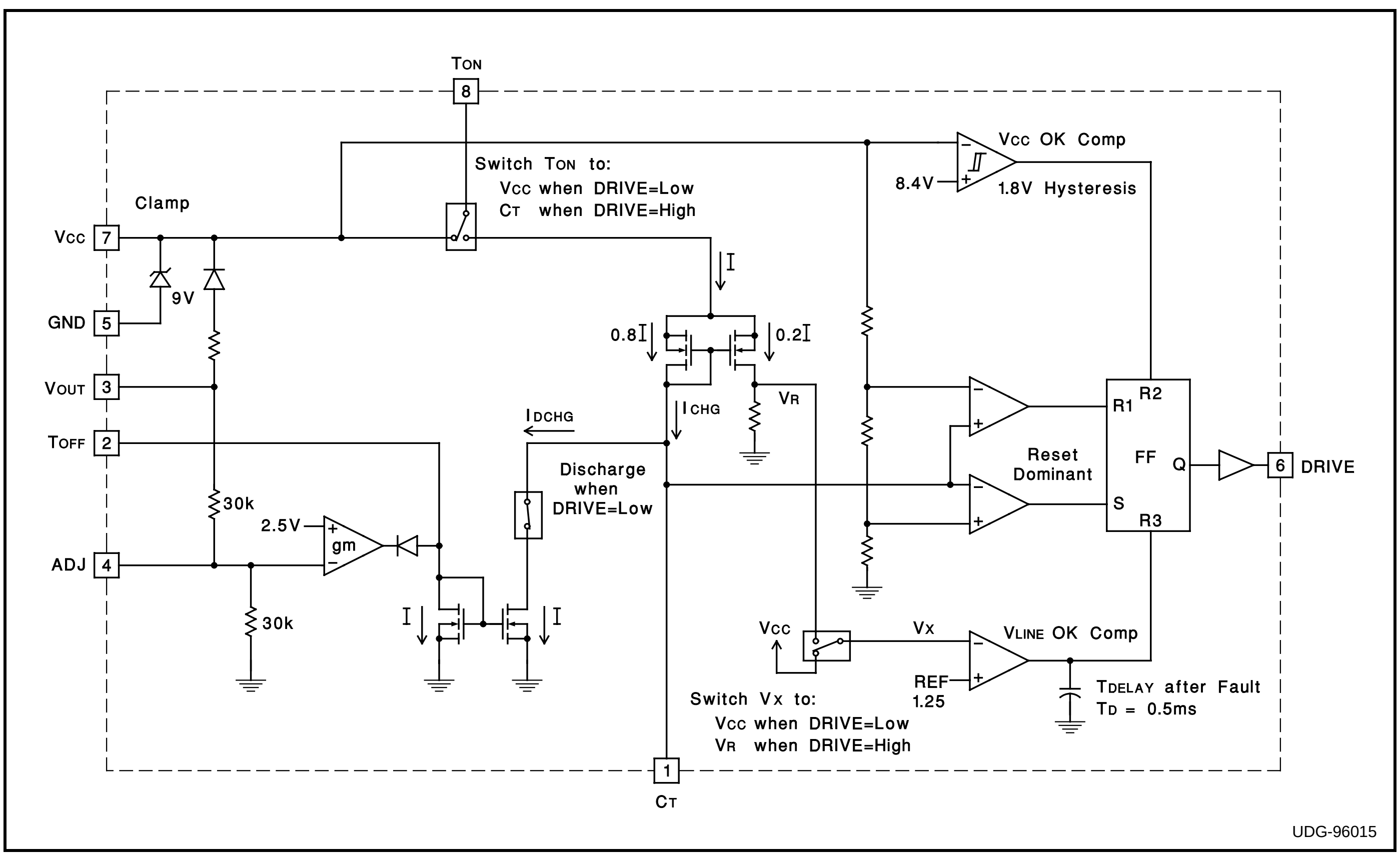
TON (line voltage control): TON serves three functions. When CT is discharging (off time), the current through TON is routed to VCC. When CT is charging (on time), the current through TON is split 80% to set the CT charge time and 20% to sense minimum line voltage which occurs for a TON current of 220µA. For a minimum line voltage of 80V, RON is 330kΩ.

The CT voltage slightly affects the value of the charge current during the on time. During this time, the voltage at the TON pin increases from 2.5V to 6.5V.

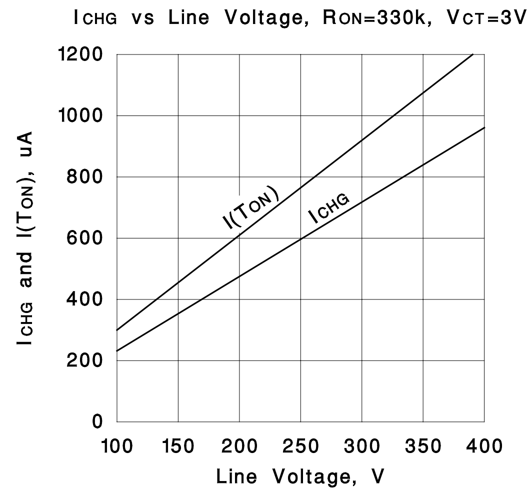
VCC (chip supply voltage): The supply voltage of the device at pin VCC is internally clamped at 9V. The device needs an external supply, from a source such as the rectified AC line or derived from the switching circuit. Precautions must be taken to ensure that total ICC does not exceed 8mA.

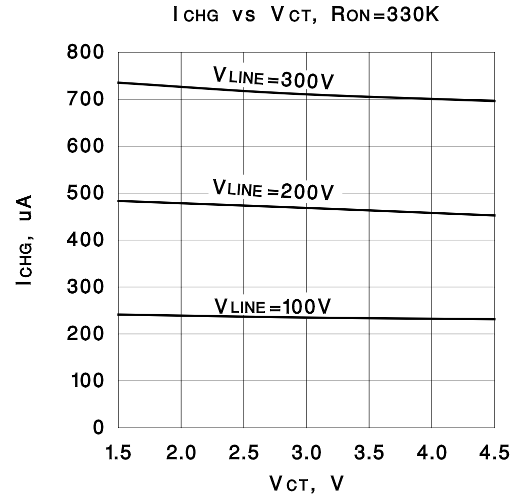
VOUT (regulated output): The VOUT pin is directly connected to the power supply output voltage. When VOUT is greater than VCC, VOUT bootstraps VCC.

BLOCK DIAGRAM



TYPICAL CHARACTERISTICS CURVES





UNITRODE CORPORATION
7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

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