

N-Ch 30V Fast Switching MOSFETs
General Description

The US3008 is the highest performance trench N-ch MOSFETs with extreme high cell density, which provide excellent R_{DS(on)} and gate charge for most of the small power switching and load switch applications.

The US3008 meet the RoHS and Green Product requirement with full function reliability approved.

Features

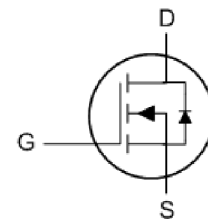
- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent C_{dv/dt} effect decline
- Green Device Available

Product Summary

BV _{DSS}	R _{DS(on)}	ID
30V	33mΩ	4.6A

Applications

- High Frequency Point-of-Load Synchronous Small power switching for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- Load Switch

SOT23 Pin Configuration

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V _{DS}	Drain-Source Voltage	30	V
V _{GS}	Gate-Source Voltage	±20	V
I _D @T _A =25°C	Continuous Drain Current, V _{GS} @ 10V ¹	4.6	A
I _D @T _A =70°C	Continuous Drain Current, V _{GS} @ 10V ¹	3.7	A
I _{DM}	Pulsed Drain Current ²	18.4	A
P _D @T _A =25°C	Total Power Dissipation ³	1	W
T _{STG}	Storage Temperature Range	-55 to 150	°C
T _J	Operating Junction Temperature Range	-55 to 150	°C

Thermal Data

Symbol	Parameter	Typ.	Max.	Unit
R _{θJA}	Thermal Resistance Junction-ambient ¹	---	125	°C/W
R _{θJC}	Thermal Resistance Junction-Case ¹	---	80	°C/W

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Electrical Characteristics ($T_J=25\text{ }^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	30	---	---	V
$\Delta BV_{DSS}/\Delta T_J$	BVDSS Temperature Coefficient	Reference to 25°C , $I_D=1\text{mA}$	---	0.023	---	V/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain-Source On-Resistance ²	$V_{GS}=10V, I_D=4A$	---	27	33	m Ω
		$V_{GS}=4.5V, I_D=3A$	---	36	50	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=250\mu A$	1.0	1.5	2.5	V
$\Delta V_{GS(th)}$	$V_{GS(th)}$ Temperature Coefficient		---	-4.2	---	mV/ $^\circ\text{C}$
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=24V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	1	μA
		$V_{DS}=24V, V_{GS}=0V, T_J=55^\circ\text{C}$	---	---	5	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
g_{fs}	Forward Transconductance	$V_{DS}=5V, I_D=4A$	---	7	---	S
R_g	Gate Resistance	$V_{DS}=0V, V_{GS}=0V, f=1\text{MHz}$	---	2.3	4.6	Ω
Q_g	Total Gate Charge (4.5V)	$V_{DS}=15V, V_{GS}=4.5V, I_D=4A$	---	4.9	6.9	nC
Q_{gs}	Gate-Source Charge		---	1.6	2.2	
Q_{gd}	Gate-Drain Charge		---	2.0	2.8	
$T_{d(on)}$	Turn-On Delay Time	$V_{DD}=15V, V_{GS}=10V, R_G=3.3\Omega$ $I_D=4A$	---	2	4	ns
T_r	Rise Time		---	34.4	62	
$T_{d(off)}$	Turn-Off Delay Time		---	13.2	26	
T_f	Fall Time		---	4.8	9.6	
C_{iss}	Input Capacitance	$V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	---	416	582	pF
C_{oss}	Output Capacitance		---	62	87	
C_{rss}	Reverse Transfer Capacitance		---	51	71	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current ^{1,4}	$V_G=V_D=0V$, Force Current	---	---	4.6	A
I_{SM}	Pulsed Source Current ^{2,4}		---	---	18.4	A
V_{SD}	Diode Forward Voltage ²	$V_{GS}=0V, I_S=1A, T_J=25^\circ\text{C}$	---	---	1.2	V
t_{rr}	Reverse Recovery Time	$I_F=4A, dI/dt=100A/\mu s, T_J=25^\circ\text{C}$	---	8.7	---	nS
Q_{rr}	Reverse Recovery Charge		---	2.3	---	nC

Note :

- 1.The data tested by surface mounted on a 1 inch² FR-4 board with 2OZ copper.
- 2.The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$
- 3.The power dissipation is limited by 150°C junction temperature
- 4.The data is theoretically the same as I_D and I_{DM} , in real applications , should be limited by total power dissipation.

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Typical Characteristics

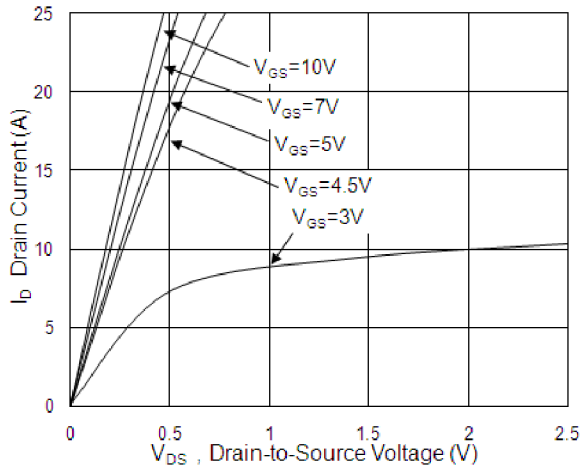


Fig.1 Typical Output Characteristics

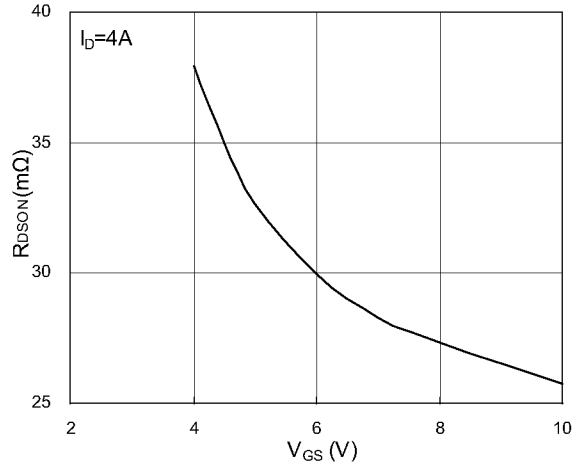


Fig.2 On-Resistance vs. Gate-Source

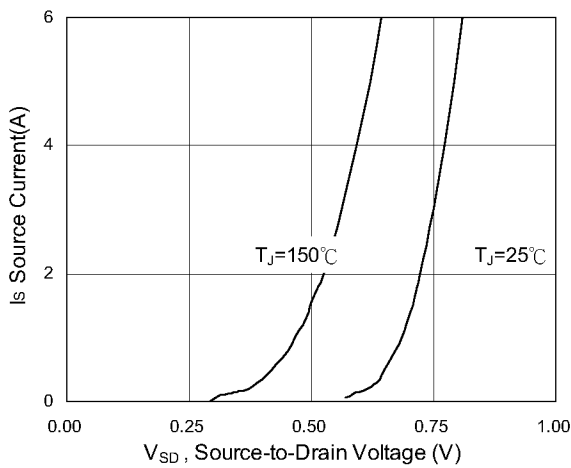


Fig.3 Forward Characteristics Of Reverse

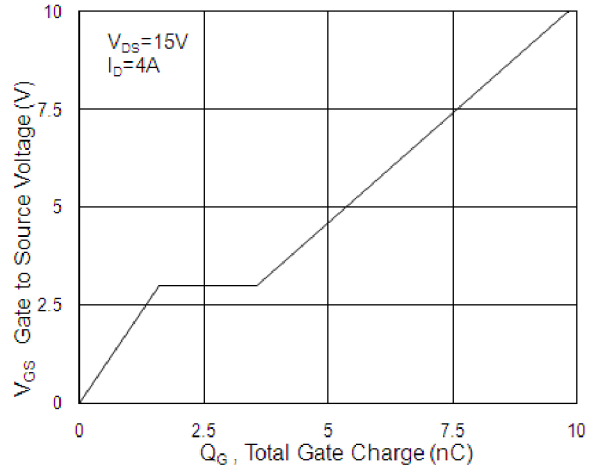


Fig.4 Gate-Charge Characteristics

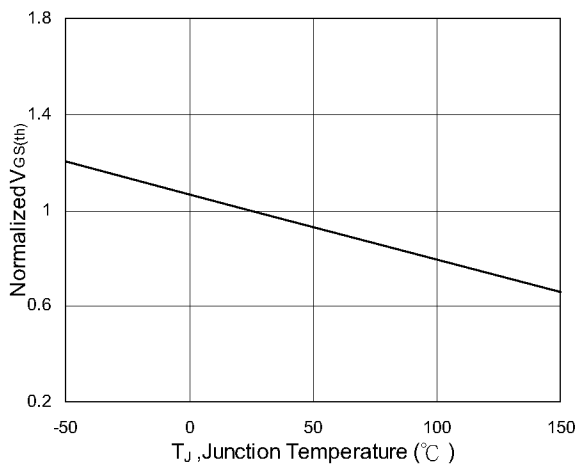


Fig.5 Normalized $V_{GS(th)}$ vs. T_J

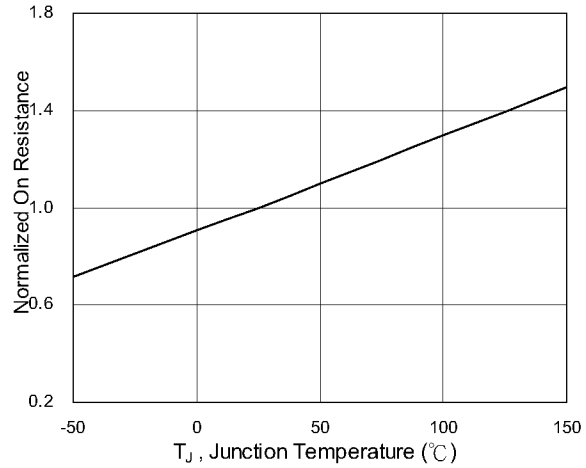


Fig.6 Normalized $R_{DS(on)}$ vs. T_J

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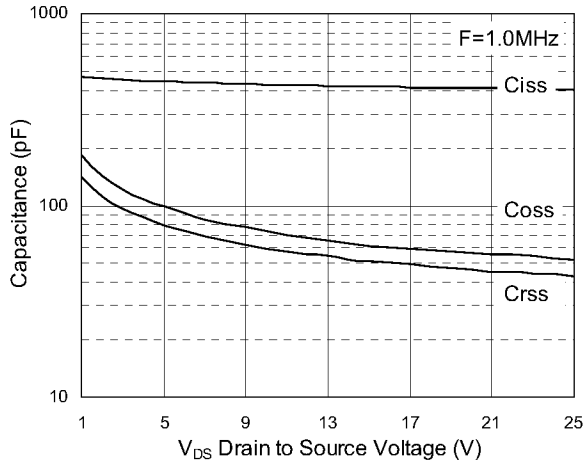


Fig.7 Capacitance

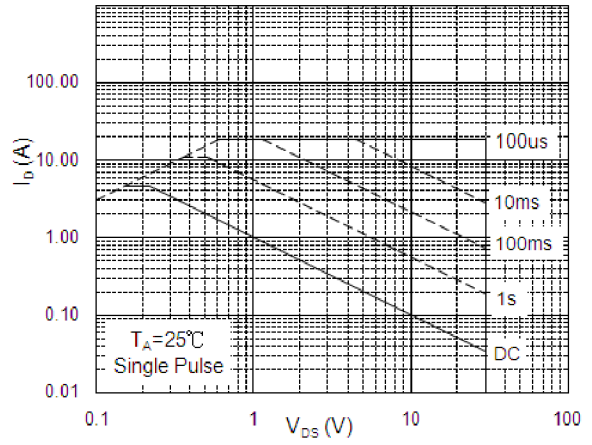


Fig.8 Safe Operating Area

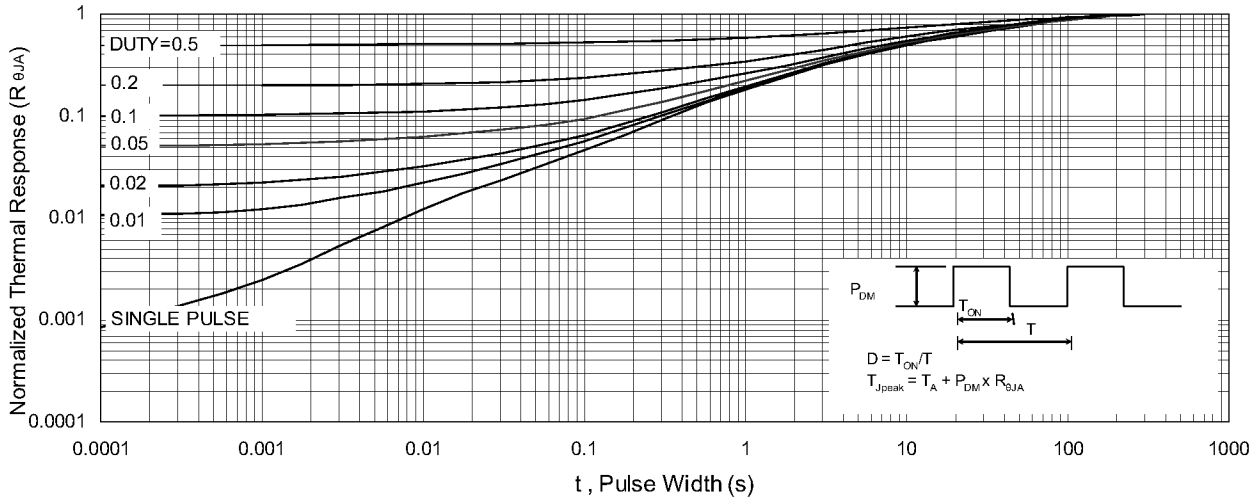


Fig.9 Normalized Maximum Transient Thermal Impedance

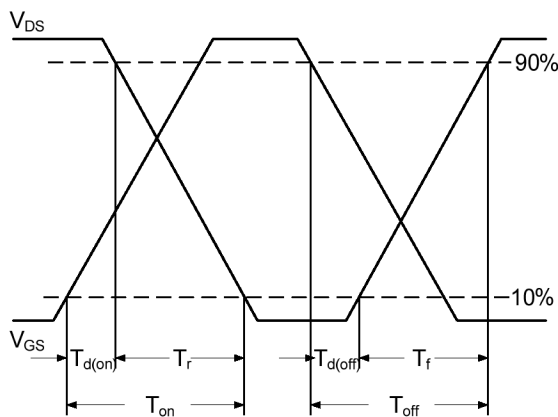


Fig.10 Switching Time Waveform

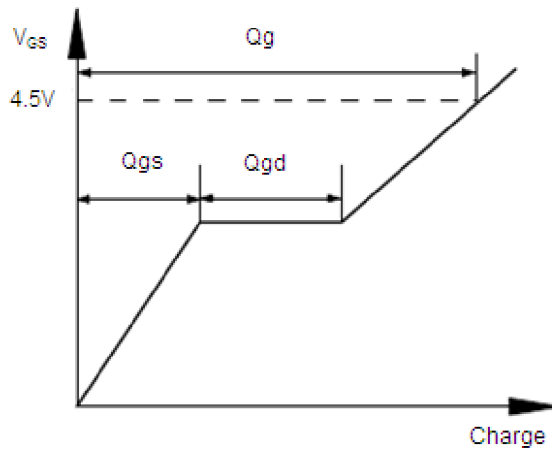


Fig.11 Gate Charge Waveform