Using the UCC25230EVM-754

User's Guide

Literature Number: SLUU670
November 2011

1.5-W Forward-Flyback DC-to-DC Converter for 48-V Telecom Biasing Supply

1 Introduction

This EVM is to help evaluate the UCC25230 PWM device in a forward-flyback or flyback DC-to-DC converter topology for a 48-V telecom biasing supply. The targeted application is telecom module design with nominal 48-V input. The EVM is a dual-output converter. Each channel is nominal 12 V and 65 mA for a total output power of 1.5 W. The design is made on a small footprint and low profile, the effective circuit area for the bias portion is 0.6 in x 0.5 in x 0.15 in (L x W x H). The UCC25230 is a highly integrated PWM controller operating as an isolated forward flyback. It has integrated high-side and low-side power switches and a control circuit with all key converter functions included.

2 Description

The EVM is a 1.5-W forward-flyback DC-to-DC converter that accepts an input range of 36 V to 72 V DC and converts it to two regulated output voltages, nominally 12 V and maximum 65-mA load current for each channel. The two outputs are 1500-V level isolated from each other, with one channel on the primary side and the other on the secondary side.

2.1 Typical Applications

- Biasing Power to Power on the Main Controller (whether on the primary or the secondary side of the isolation barrier)
- 48-V Telecom
- Server Systems
- Datacom
- DSP’s, ASIC’s, and FPGA’s

2.2 Features

- Start Up Directly from Telecom Input Voltage 36 V to 72 V DC
- Two Regulated 12-V Outputs, 65-mA Maximum Load Current
- Telecom Isolation from Primary-to-Secondary 1500 V
- Small Footprint and Low Profile Design
- Output Voltage Regulation (from no load to full load, and from low line to high line)
- Input Voltage Status Signal, (manually or automatically set up)
- Device Evaluation Test Points
- All Surface Mount Components and Industry Leading-Edge Small Footprint

3 Electrical Performance Specifications

Table 1. UCC25230EVM-754 Electrical Performance Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Characteristics					
Voltage range		36	48	72	V
Maximum input current	V_{IN} = 36 V and IOUT1 = IOUT2 = 65 mA		70		mA
No load input current			8.5		
Output Characteristics					
Output voltage, VOUT1	IOUT1 = 0 mA, IOUT2 = 65 mA	11.5	11.8	12.5	V
	IOUT1 = 65 mA, IOUT2 = 0 mA	11.5	11.8	12.5	
Output voltage, VOUT2	IOUT1 = 0 mA, IOUT2 = 100 mA	9.5	10.0	11.0	
	IOUT1 = 100 mA, IOUT2 = 0 mA	9.5	12.0	12.5	
Output load current, IOUT2 or IOUT2				65	mA
Output-1 voltage regulation (regulated output)	Line regulation: input voltage = 36 V to 72 V IOUT1 = IOUT2 = 100 mA			10	mV
	Load regulation: input voltage = 48 V IOUT1 = 0 mA to 100 mA IOUT2 = 100 mA			10	
Output-2 voltage regulation (cross-regulated output)	Line regulation: input voltage = 36V to 72V IOUT1 = IOU2 = 65 mA			0.75	V
	Load regulation: input voltage = 48 V IOUT1 = 65 mA IOUT2 = 0 mA to 65 mA			-1.35	
Output voltage ripple Output-1 and -2	At IOUT1 = IOUT2 = 65 mA		45	60	mVpp
Systems Characteristics					
Switching frequency			380		kHz
Peak efficiency	V_{IN} = 36 V, IOUT1 = IOUT2 = 50 mA		81%		
Full load efficiency	V_{IN} = 48 V, IOUT1 = IOUT2 = 65 mA		80%		
Input status good (TP4)		4.2		5.2	V
Operating temperature	Natural convection			45	ºC

NOTE: Effective bias real-estate size, L x W x H = 0.6 in x 0.5 in x 0.15 in and a board size of L x W = 2.2 in x 1.4 in.

4 Schematic

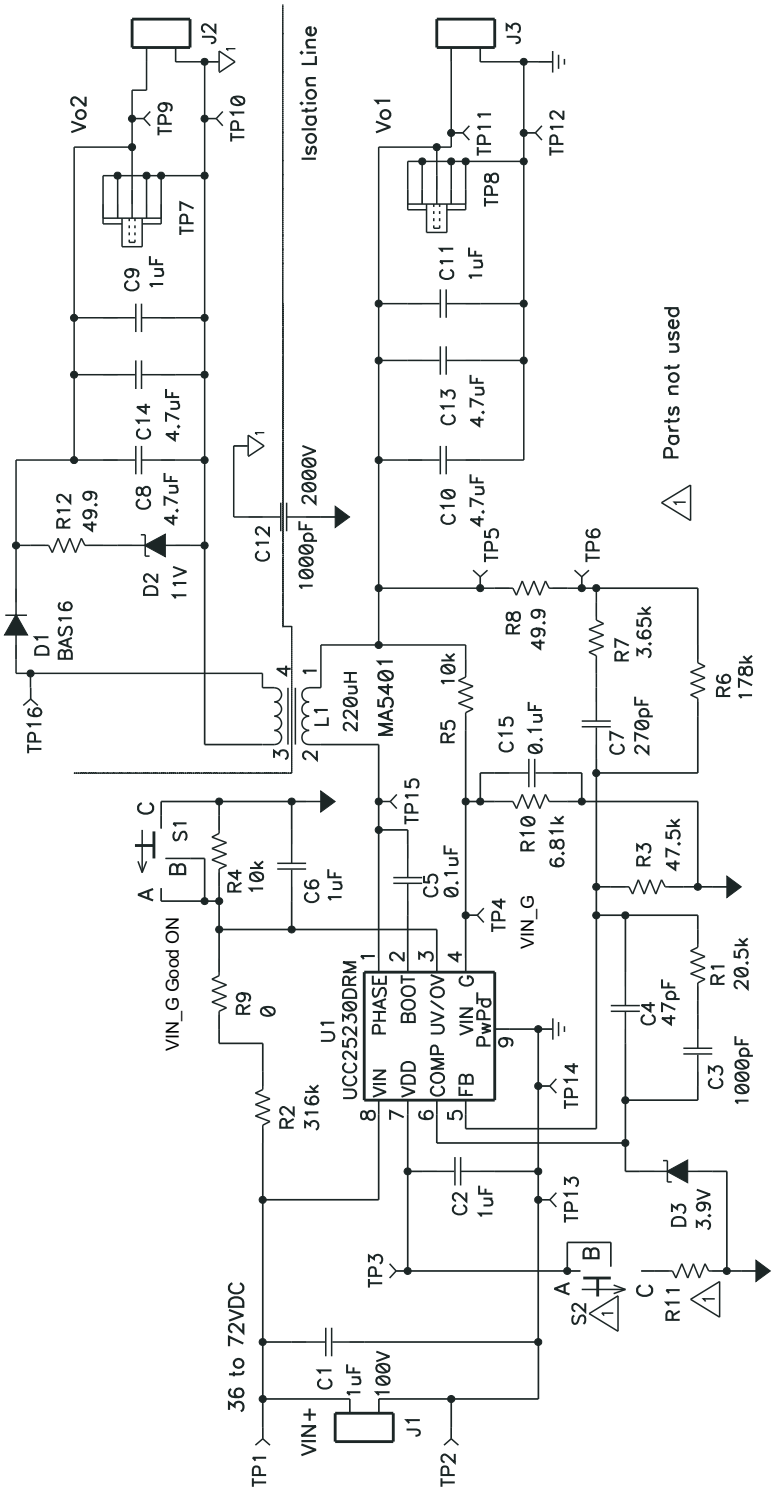

Figure 1. UCC25230EVM-754 Schematic

5 Test Setup

5.1 Test Equipment

Voltage Source: Vsc1, the input voltage shall be a variable DC source capable of supplying up to 72 V_{DC} at no less than 0.35 A_{DC}, and connected to J1 and Ams1 as shown in Figure 2.

Multimeters:

- **Ams1:** IIN, 0 mA_{DC} to 100 mA_{DC}, ammeter, four digits display.
- **Vms1:** VIN, 0-V to 75-V voltmeter, three and half digits display.
- **Vm1:** VOUT1, 0-V to 13-V voltmeter, three and half digits display.
- **Vm2:** VOUT2, 0-V to 13-V voltmeter, three and half digits display.

Output Load (Load-1 and Load-2): Electronic, 0 mA_{DC} to 200 mA_{DC} (2 units), For the output load on VOUT1 and VOUT2, a programmable electronic load capable of sinking not less than 100 mA_{DC} shall be used. The loads should have a current display, if not then an ammeter should be added in series with the load. Refer to the schematic shown in Figure 2.

Oscilloscope: A 20-MHz or equivalent analog or digital oscilloscope with Tektronix P6138 or equivalent oscilloscope probe. Set scope for AC coupling measurement with 20-MHz bandwidth limiting. Use 20-mV/div. vertical resolution, 5.0-µs/div. horizontal resolution for VOUT ripple voltage test. Set horizontal cursor to measure ripple voltage.

Recommended Wire Gauge: The minimum recommended wire size is AWG #26, with the total length of wire less than 8 feet (4 feet output, 4 feet return).

Ventilation FAN: A small fan capable of 200 LFM to 400 LFM is optional to reduce component temperatures, but it is not a requirement in the test at room temperature

5.2 Recommended Test Setup

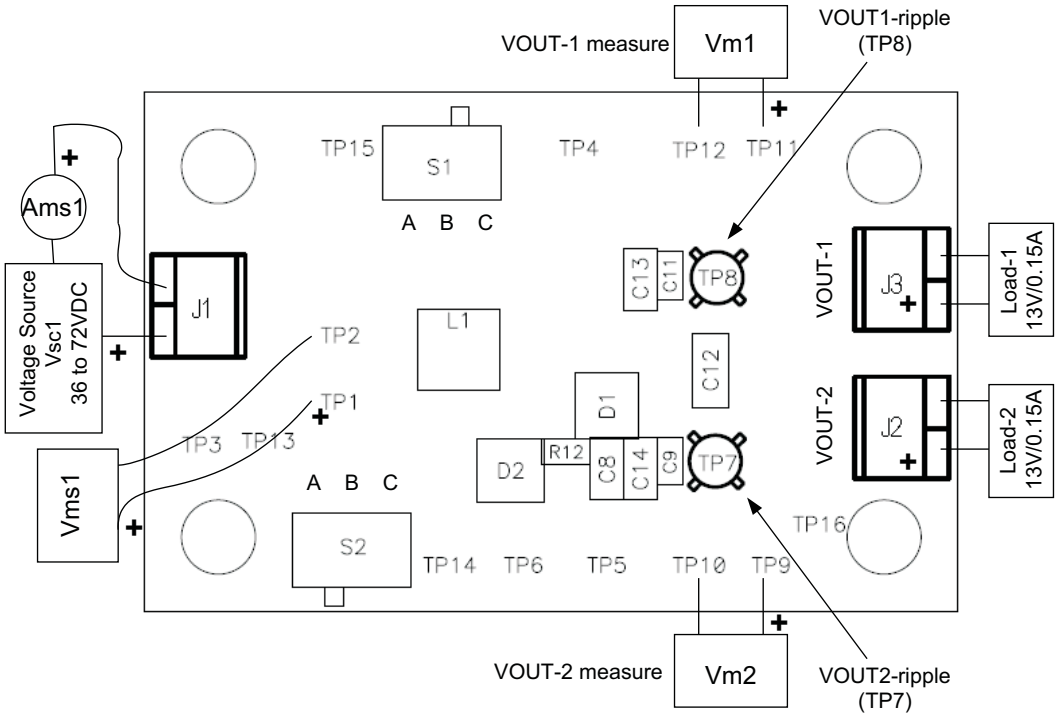

Figure 2. UCC25230EVM-754 Recommended Test Set Up

5.3 List of Test Points

Table 2. Test Points Functions

TEST POINTS	NAME	DESCRIPTION
TP1	Vin	Input voltage positive test point, for efficiency test
TP2	GND	Input voltage negative test point, for efficiency test
TP3	VDD	Device VDD on primary side
TP4	VIN_G	VIN_G good, when it is good, TP4 voltage is in 4.2 V to 5.2 V
TP5	Loop+	Feedback loop test point
TP6	Loop-	Feedback loop test point
TP7	Vo2_rpl	Output-2 voltage ripple test point
TP8	Vo1_rpl	Output-1 voltage ripple test point
TP9	Vo2+	Output-2 output terminal
TP10	Vo2-	Output-2 return terminal
TP11	Vo1+	Output-1 output terminal
TP12	Vo1-	Output-1 return terminal
TP13	GND	Primary-side ground
TP14	GND	Primary-side ground
TP15	Phase	Primary-side phase node
TP16	L1-2	Inductor coupled coil on the secondary side
J1	INPUT	Input voltage terminals
J2	VOUT-2	Output-2 load connection terminals
J3	VOUT-1	Output-1 load connection terminals
S1	VIN_G	Input voltage good manual switch
S2	VDD_short	VDD short circuit current measurement switch – not installed

6 Test Procedure

Set up the EVM based on Figure 2.

CAUTION

High voltage and high temperature present when the EVM is in operation!

6.1 Line/Load Regulation and Efficiency Measurement Procedure

1. Connect the ammeter Ams1 (0 mA to 100 mA range) between DC source and J1 as shown in Figure 2.
2. Prior to connecting the DC source, Vsc1, it is advisable to limit the source current to 0.35 A maximum. Make sure the DC source is initially set to 0 V and connected to J1 and Ams1 as shown in Figure 2.
3. Connect voltmeter, Vms1, on to the test points, TP1 (+) and TP2 (-) as shown in Figure 2.
4. Connect Load-1 to J3 as shown in Figure 2. Set Load-1 to constant current mode to sink 0 mA_{DC} before the input voltage on J1 is applied.
5. Connect voltmeter, Vm1 to test point TP11 (+) and TP12(-). Set Vm1 range 0 V to 13 V_{DC} as shown in Figure 2.
6. Connect Load-2 to J2 as shown in Figure 2. Set Load-2 to constant current mode to sink 0 mA_{DC} before the input voltage on J1 is applied.
7. Connect voltmeter, Vm2 to test point TP9 (+) and TP10(-). Set Vm2 range 0 V to 13 V_{DC} as shown in Figure 2.
8. Increase the DC source voltage from 0 V to 36.0 V_{DC}.
9. Set Load-1 to 65 mA ±0.1 mA.
10. Vary Load-2 to 0.0 mA to 65 mA.
11. Read Ams1, Vm1, and Vm2.
12. Set Load-1 to 0.0 mA.
13. Vary Load-1 to 0.0 mA to 65.0 mA
14. Read Ams1, Vm1, and Vm2.
15. Increase the DC source voltage to 72.0 V,
16. Repeat steps 9 to 14.
17. During above tests out ripple can be observed on TP8 for VOUT-1 and TP7 for VOUT-2.

6.2 Equipment Shutdown

1. Decrease Load-1 and Load-2 to 0 mA.
2. Decrease VIN from 72 V to 0 V.
3. Shut down V_{SC1}.
4. Shut down the loads.

7 Performance Data and Typical Characteristic Curves

Figure 3 through Figure 11 present typical performance curves for UCC25230EVM-754.

7.1 Efficiency

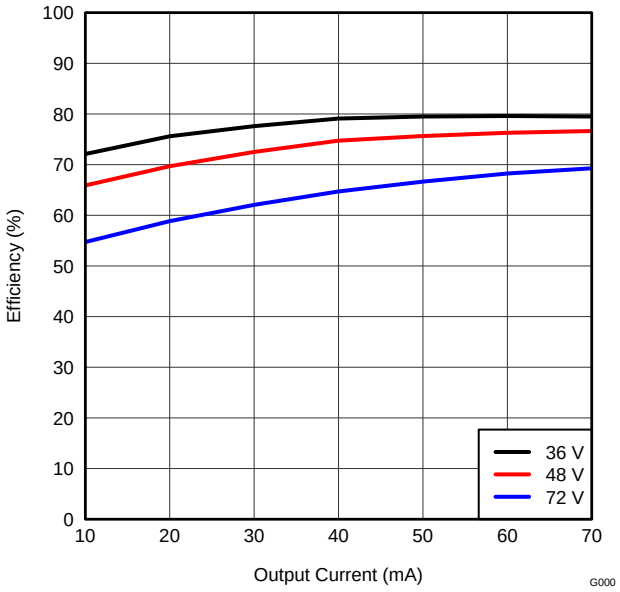

Figure 3.

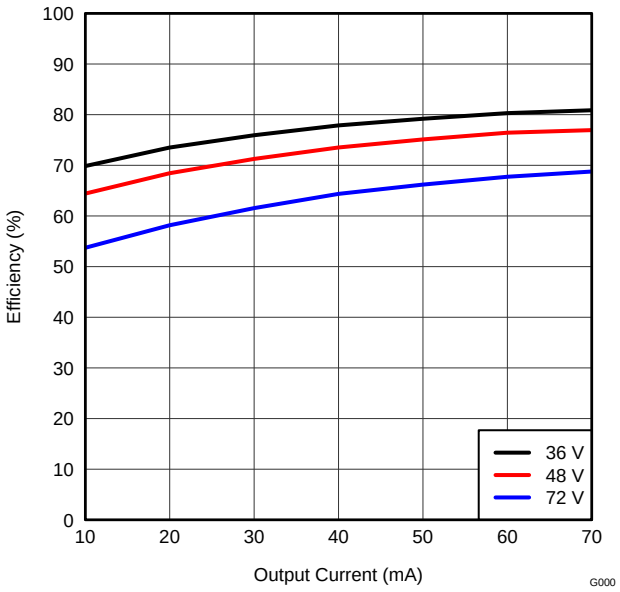

Figure 4.

7.2 Load Regulation

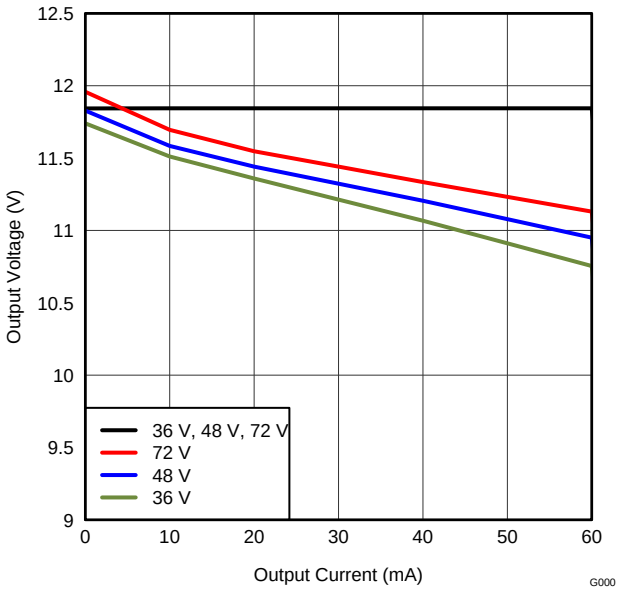

Figure 5.

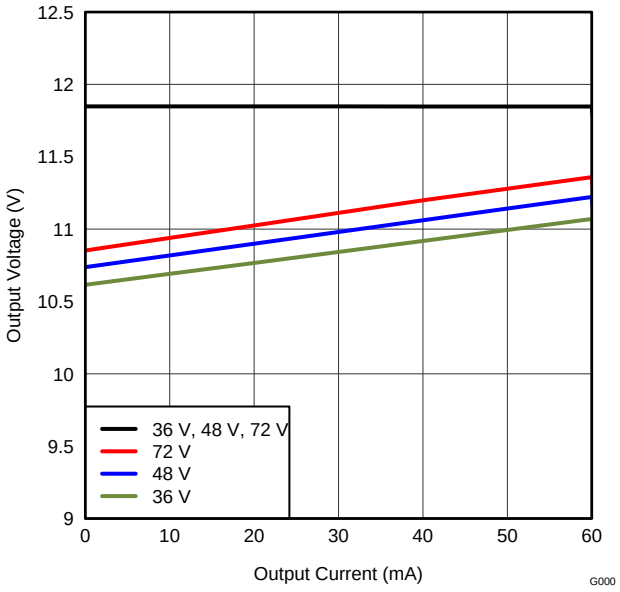

Figure 6.

7.3 Regulation at Corner Conditions

Table 3. UCC25230EVM-754 Regulation at Corners

V_{IN} (V)	I_{O1} (mA)	I_{O2} (mA)	V_{O1} (V)	V_{O2} (V)
36	0.0	0.0	11.85	11.50
		65.0		9.70
	65.0	0.0		12.10
		65.0		10.50
72	0.0	0.0		11.75
		65.0		10.25
	100.0	0.0		12.30
		65.0		11.10

7.4 Bode Plots

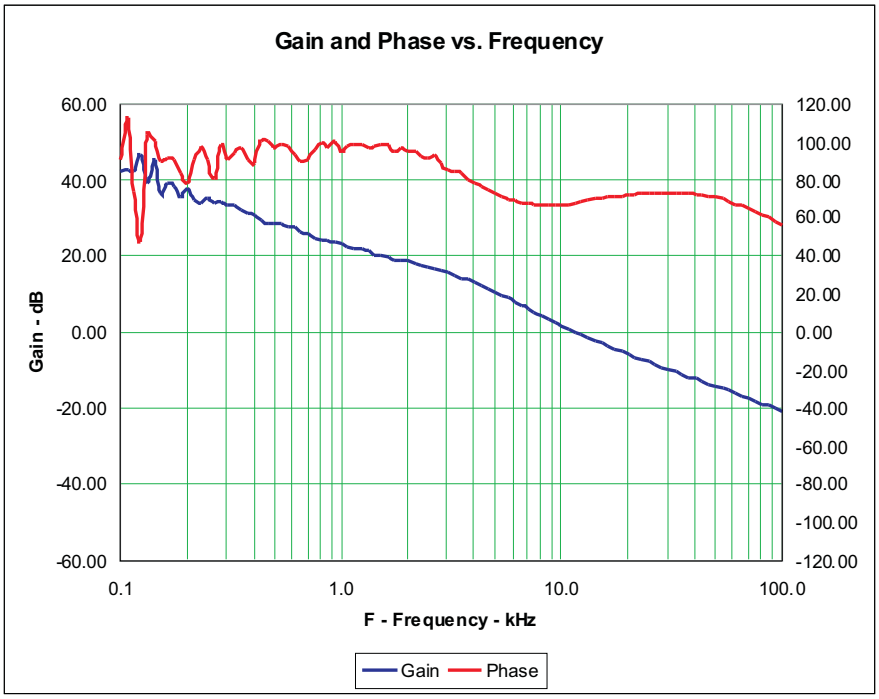

Figure 7. Bode Plots,
Test Points Used: TP5 and TP6,
(Vin = 48V, Io1 = 50mA, Io2 = 50mA)

7.5 Output Ripple

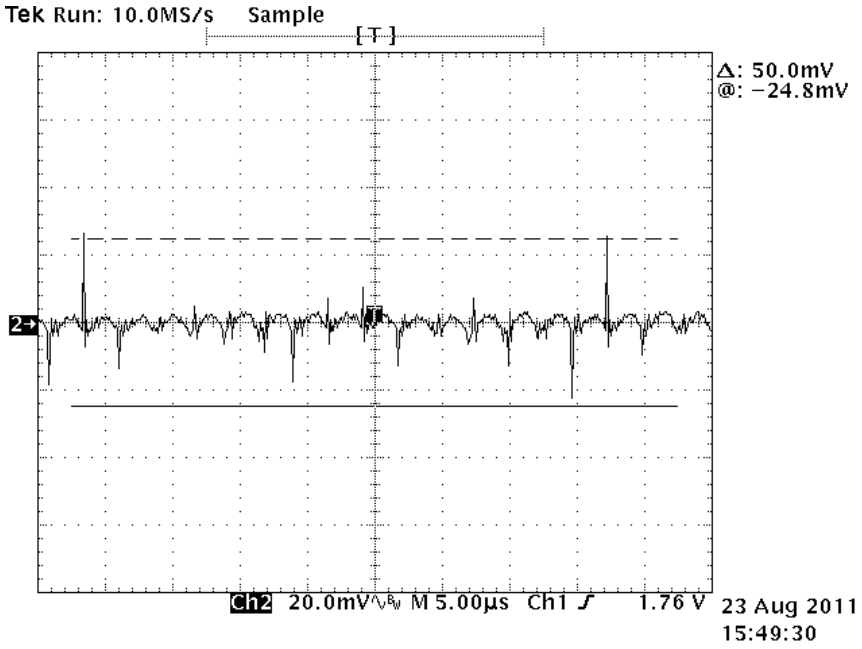

Figure 8. Output Ripple
(V_{IN} = 48 V, Io1 = Io2 = 50 mA from Vo1 (TP8) or Vo2 (TP7))

7.6 Phase-Node Voltage

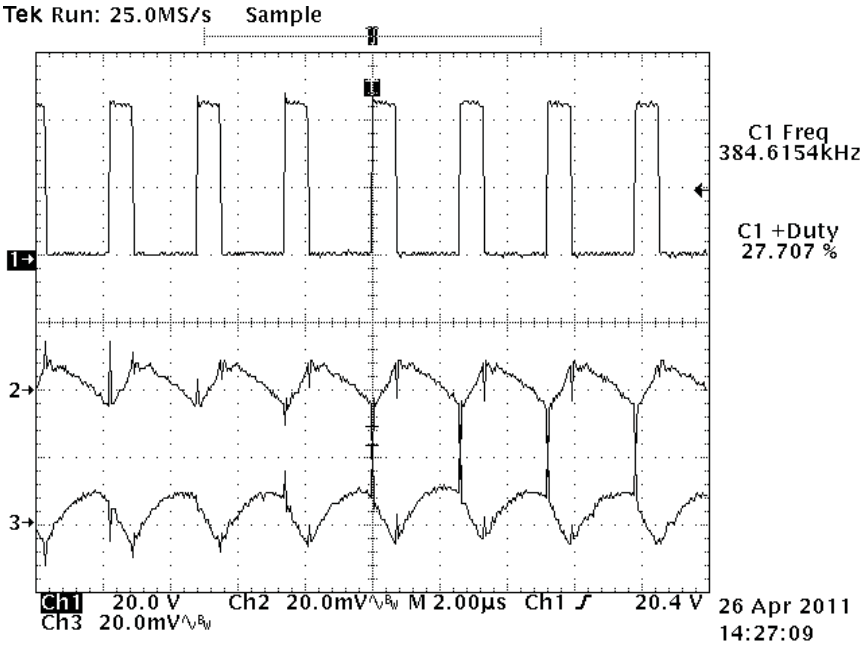

Figure 9. Switching-Node Waveform
(CH1 = Phase (TP15), Ch2 = Vo1 ripple, Ch3 = Vo2 ripple, V_{IN} = 48 V, Io1 = Io2 = 50 mA)

7.7 Turn-On Waveform

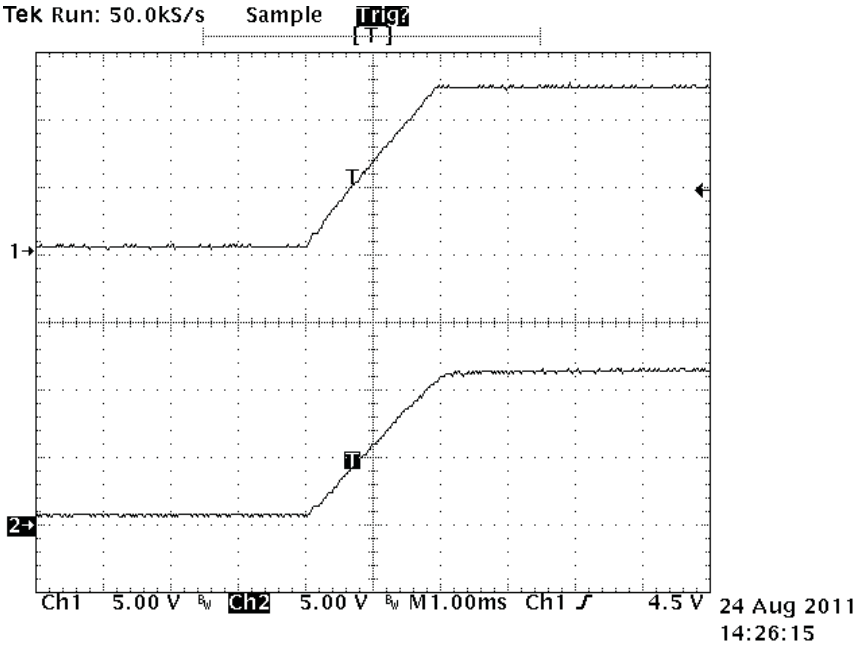

Figure 10. Enable Turn-On Waveform
(V_{IN} = 48 V, Io1 = Io2 = 50 mA, Ch1: Vo1 (TP8), Vo2 (TP7))

7.8 Turn-Off Waveform

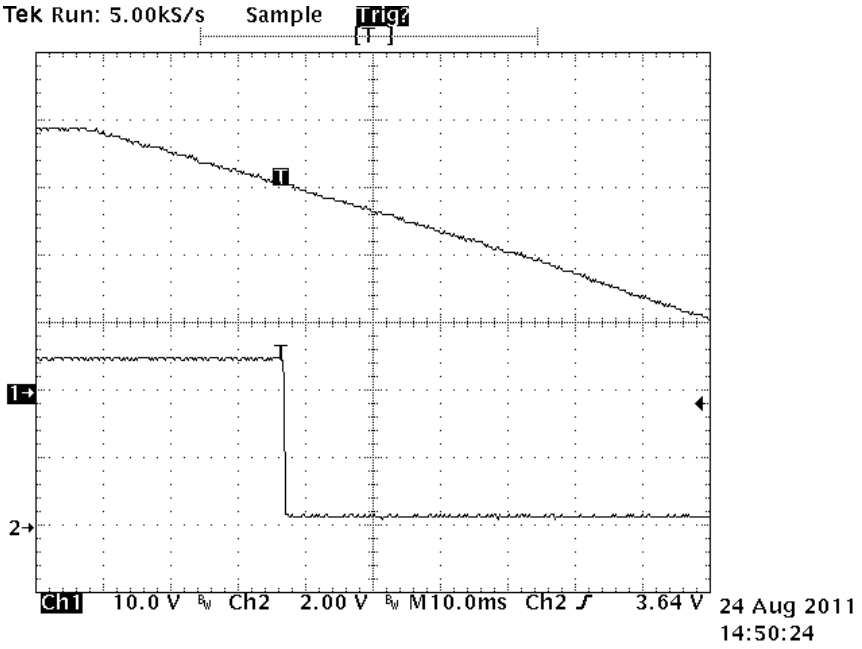

Figure 11. Enable Turn-Off Waveform
(Io1 = Io2 = 50 mA, Ch1: V_{IN} (TP1, 2), Ch2: VIN_G (TP4))

8 EVM Assembly Drawing and PCB layout

The following figures (Figure 12 through Figure 17) show the design of the UCC25230EVM-754 printed circuit board.

- **PCB dimensions:** L x W = 2.2 inch x 1.4 inch,
- **PCB material:** FR406 or compatible, four layers and 2-oz copper on each layer.

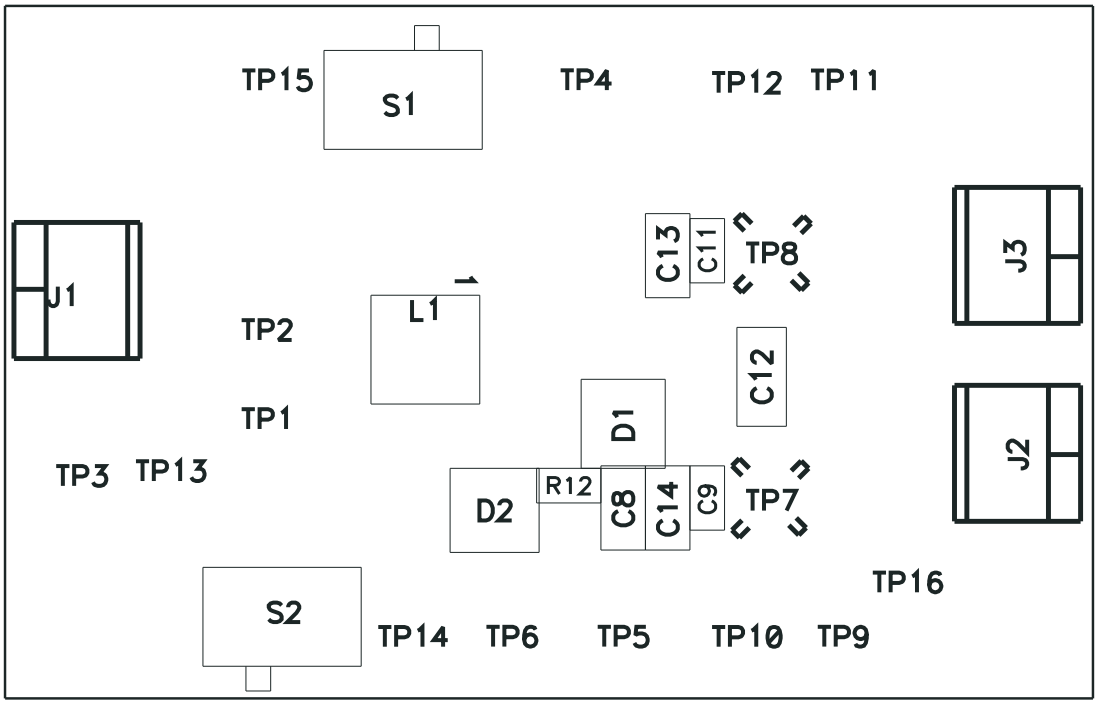

Figure 12. UCC25230EVM-754 Top Layer Assembly Drawing (top view)

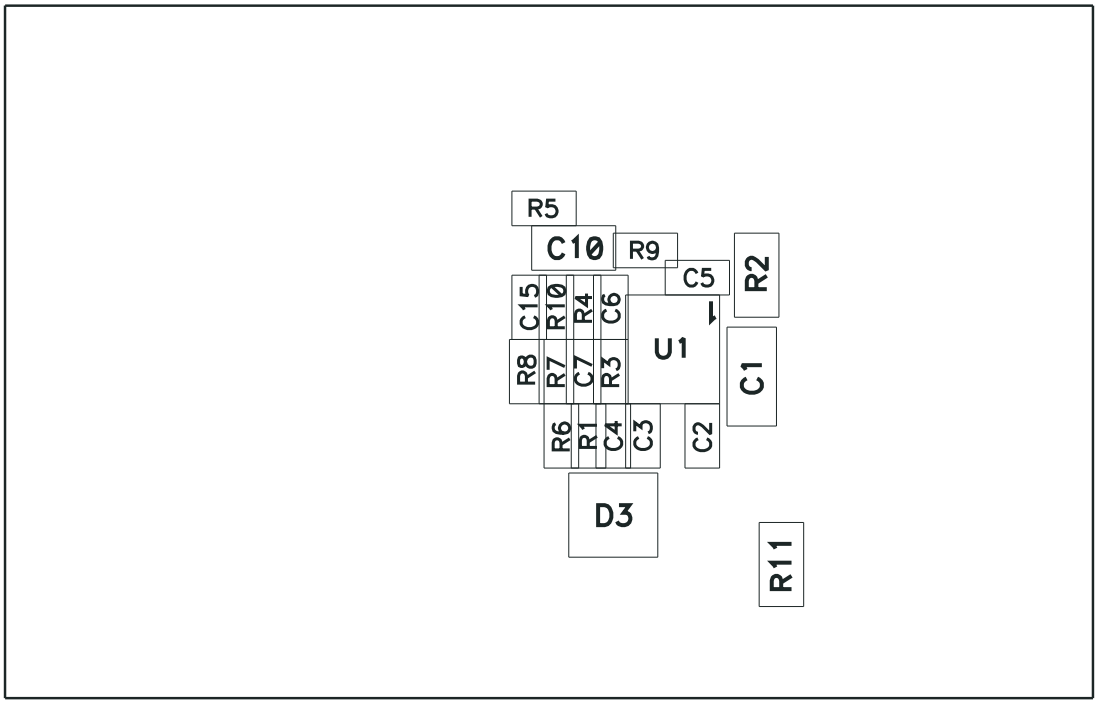

Figure 13. Bottom Assembly Drawing (bottom view)

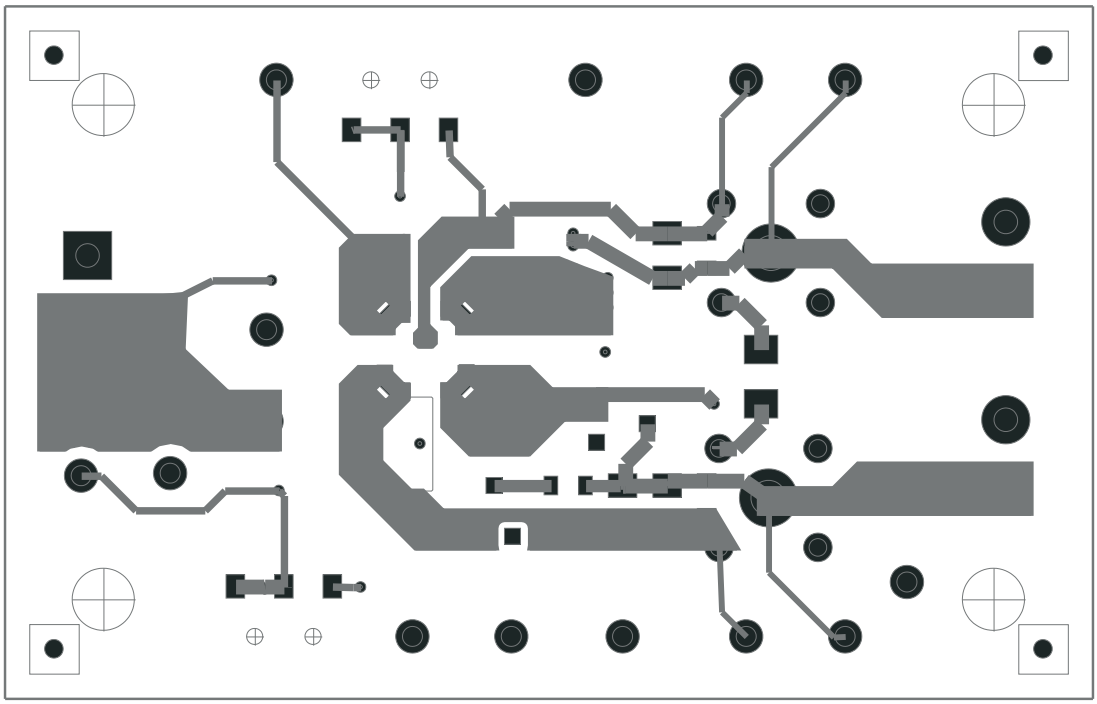

Figure 14. Top Copper (top View)

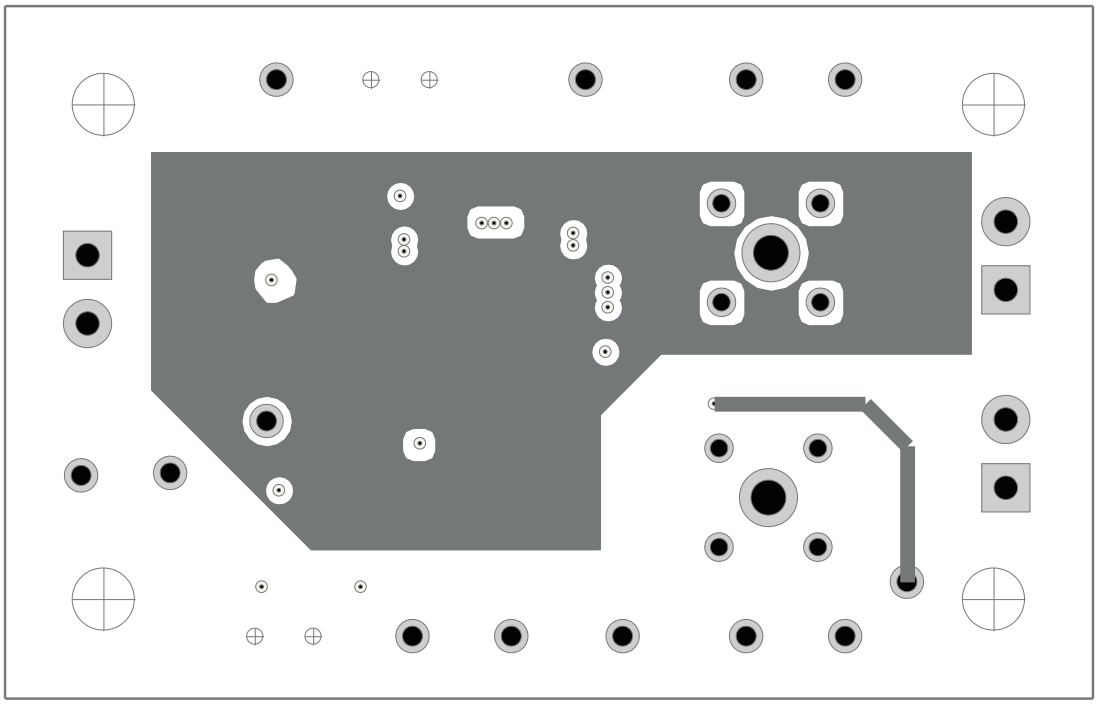

Figure 15. Internal Layer 1 (top view)

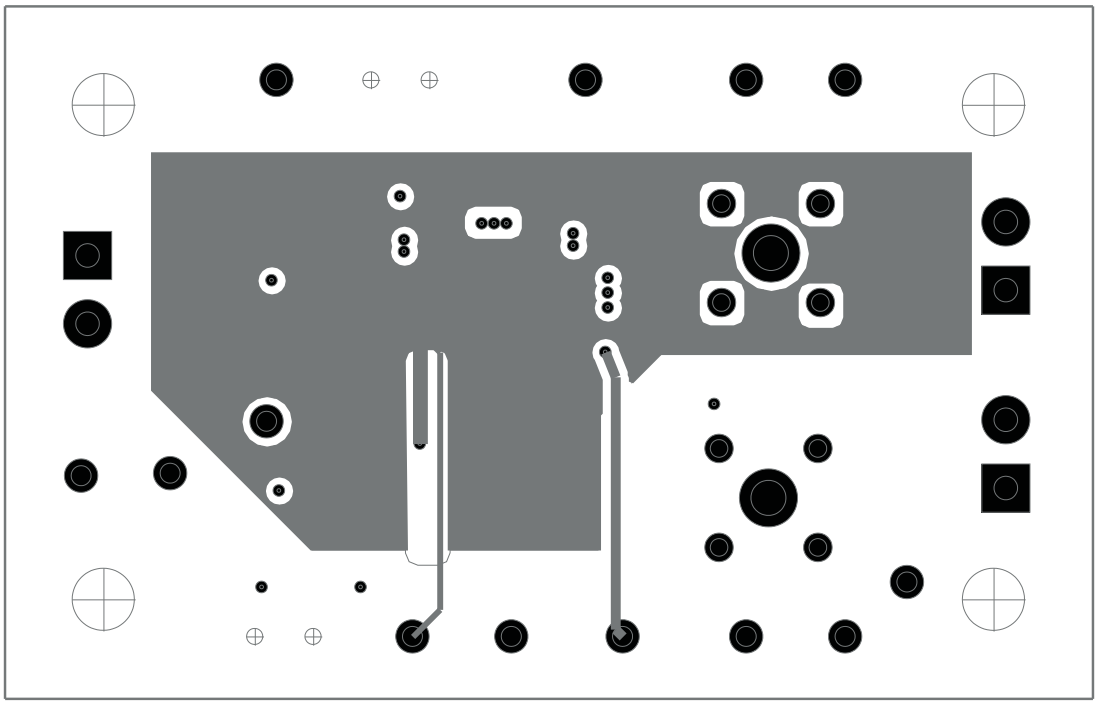

Figure 16. Internal Layer 2 (top view)

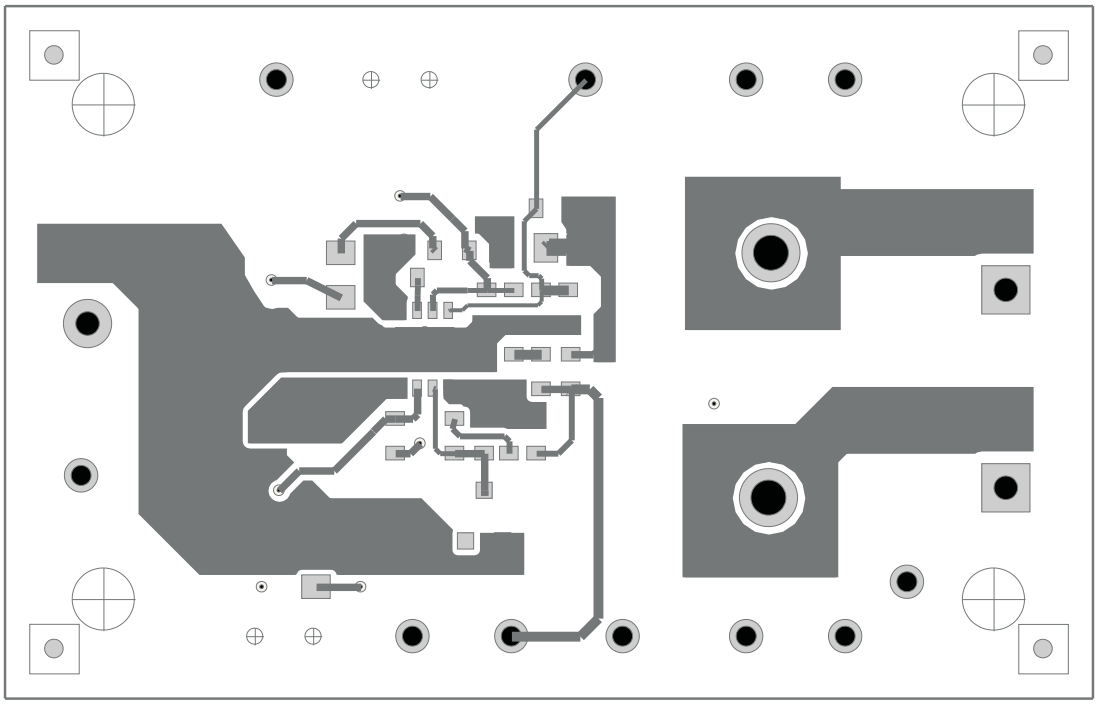

Figure 17. Bottom Copper (top view)

9 List of Materials

The EVM components list according to the schematic shown in Figure 1.

Table 4. UCC25230EVM-754 List of Materials

QTY	REF DES	DESCRIPTION	PART NUMBER	MFR
1	C1	Capacitor, ceramic, 100 V, X7R, 20%, 1 µF, 1206	std	std
1	C12	Capacitor, ceramic, 2000 V, X7R, 20%, 1000 pF, 1206	std	std
4	C2, C6, C9, C11	Capacitor, ceramic, 16 V, X7R, ±10%, 1 µF, 0603	std	std
1	C3	Capacitor, ceramic, 50 V, NP0, ±10%, 1000 pF, 0603	std	std
1	C4	Capacitor, ceramic, 50 V, X7R, ±10%, 47 pF, 0603	std	std
2	C5, C15	Capacitor, ceramic, 16 V, X7R, ±10%, 0.1 µF, 0603	std	std
1	C7	Capacitor, ceramic, 50 V, NP0, ±10%, 270 pF, 0603	std	std
4	C8, C10, C13, C14	Capacitor, ceramic, 16 V, X5R, ±10%, 4.7 µF, 0805	std	std
1	D1	Diode, switching, 200 mA, 85 V, 350 mW, SOT23	BAS16	Fairchild
1	D2	Diode, Zener, 11 V, 20 mA, 225 mW, 5%, SOT23	BZX84C11LT1G	Onsemi
1	D3	Diode, Zener, 3.9 V, 20 mA, 225 mW, 5%, SOT23	BZX84C3V9LT1G	Onsemi
3	J1, J2, J3	Terminal block, 2 pin, 6 A, 3.5 mm, 0.27 inch x 0.25 inch	OSTTE020161	OST
1	L1	Inductor, SMT, 0.35 A, 3.3 Ω, 220 µH, 0.19 inch x 0.19 inch	MA5401-AE	Coilcraft
1	R1	Resistor, chip, 1/16 W, 1%, 20.5 kΩ, 0603	std	std
1	R10	Resistor, chip, 1/16 W, 1%, 6.81 kΩ, 0603	std	std
0	R11	Resistor, chip, 1/10 W, 1%, open, 0805	std	std
1	R2	Resistor, chip, 1/8 W, 1%, 316 kΩ, 0805	std	std
1	R3	Resistor, chip, 1/16 W, 1%, 47.5 kΩ, 0603	std	std
2	R4, R5	Resistor, chip, 1/16 W, 1%, 10 kΩ, 0603	std	std
1	R6	Resistor, chip, 1/16 W, 1%, 178 kΩ, 0603	std	std
1	R7	Resistor, chip, 1/16 W, 1%, 3.65 kΩ, 0603	std	std
2	R8, R12	Resistor, chip, 1/16 W, 1%, 49.9 Ω, 0603	std	std
1	R9	Resistor, chip, 1/16 W, 1%, 0 Ω, 0603	std	std
1	S1	Switch, actuator SPDT, 0.18 inch x 0.28 inch	AYZ0102AGRLC	C & K
0	S2	Switch, actuator SPDT, open, 0.18 inch x 0.28 inch	AYZ0102AGRLC	C & K
1	U1	12-V to 100-V input, 0.25-A output switching converter, VSON	UCC25230DRM	TI

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of 36 V to 72 V and the output voltage range of 8.5 V to 12.5 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 60° C. The EVM is designed to operate properly with certain components above 60° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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