ASPEN Express™ Device
Multi-PHY *CellBus*® Access Device
TXC-05806

DATA SHEET
PRODUCT PREVIEW

PRODUCT PREVIEW

FEATURES

- 622 Mbit/s bi-directional throughput
- UTOPIA Level 1/2 interface (8/16-bit) with support for 64/124 ports at 50 MHz
- OAM Fault Management per ITU-T I.610
- UPC/NPC policing on ingress compliant with TM4.1
- Early Packet Discard (EPD) and Partial Packet Discard (PPD) in inlet and outlet direction
- Dual *CellBus* interfaces for load sharing or redundancy
- Inlet-side address translation and routing header insertion
- Outlet-side VPC or VCC header translation
- 512k cell shared SDRAM buffer memory
- Support for spatial multicast for 512 sessions
- Support for over-reservation of GFR, UBR, and VBR traffic
- Minimum Cell Rate (MCR) guarantees for egress queues
- *CellBus* traffic monitor mode
- Cell insertion and extraction via microprocessor interface port
- Microprocessor control port, selectable for Intel, Motorola 360 or Motorola MPC 860 interfaces
- Test Access Port for IEEE 1149.1 boundary scan
- +3.3 V and +1.8 V power supplies
- 456-lead Plastic Ball Grid Array (PBGA) package, 27 mm x 27 mm

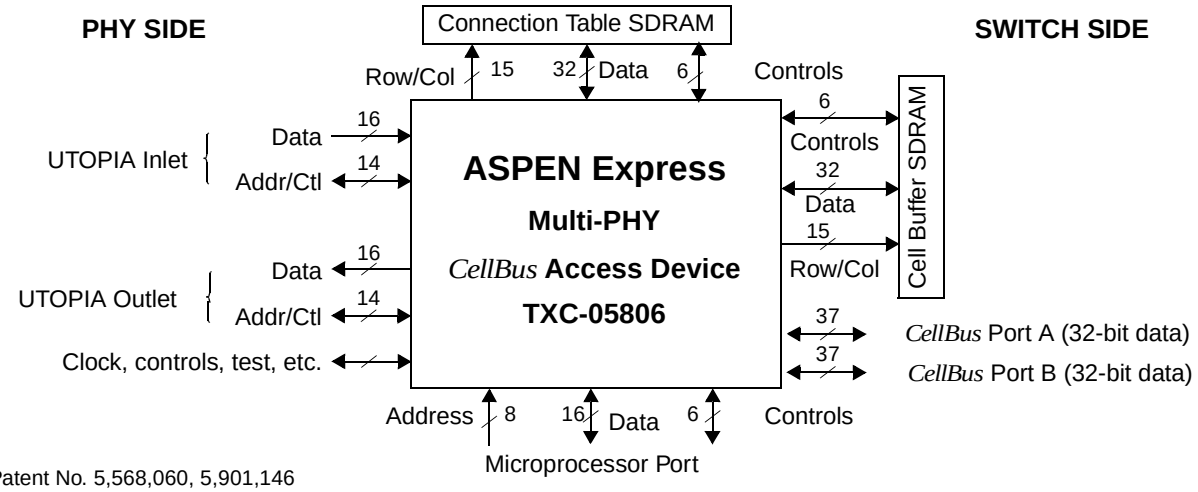
DESCRIPTION

The ASPEN® Express device is a single-chip solution for implementing cost-effective ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT®-3, CUBIT-*Pro*, CUBIT-622, or ASPEN devices, all interconnected by a 37-line common bus, the *CellBus*. The ASPEN Express provides enhanced traffic management to the *CellBus* family of ATM switching devices. ASPEN Express supports unicast and multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing, policing and inlet/outlet cell queuing. The ASPEN Express offers dual *CellBus* interfaces to support load sharing or redundancy.

The ASPEN Express is designed to interface directly with UTOPIA Level 1/2, 8/16-bit compliant devices, such as the PHAST-3P (TXC-06203) and the PHAST-12E (TXC-06212) at up to 50 MHz. On the switch side, the ASPEN Express interfaces directly with *CellBus* devices such as the CUBIT-*Pro* (TXC-05802B), CUBIT-3 (TXC-05804), CUBIT-622 (TXC-05805) and ASPEN (TXC-05810).

APPLICATIONS

- ATM Access Multiplexers
- DSLAM Applications
- Remote Access Equipment
- ATM LAN Switch
- Frame Relay Switch



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PRODUCT PREVIEW

TABLE OF CONTENTS

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PRODUCT PREVIEW

LIST OF FIGURES

PRODUCT PREVIEW

BLOCK DIAGRAM

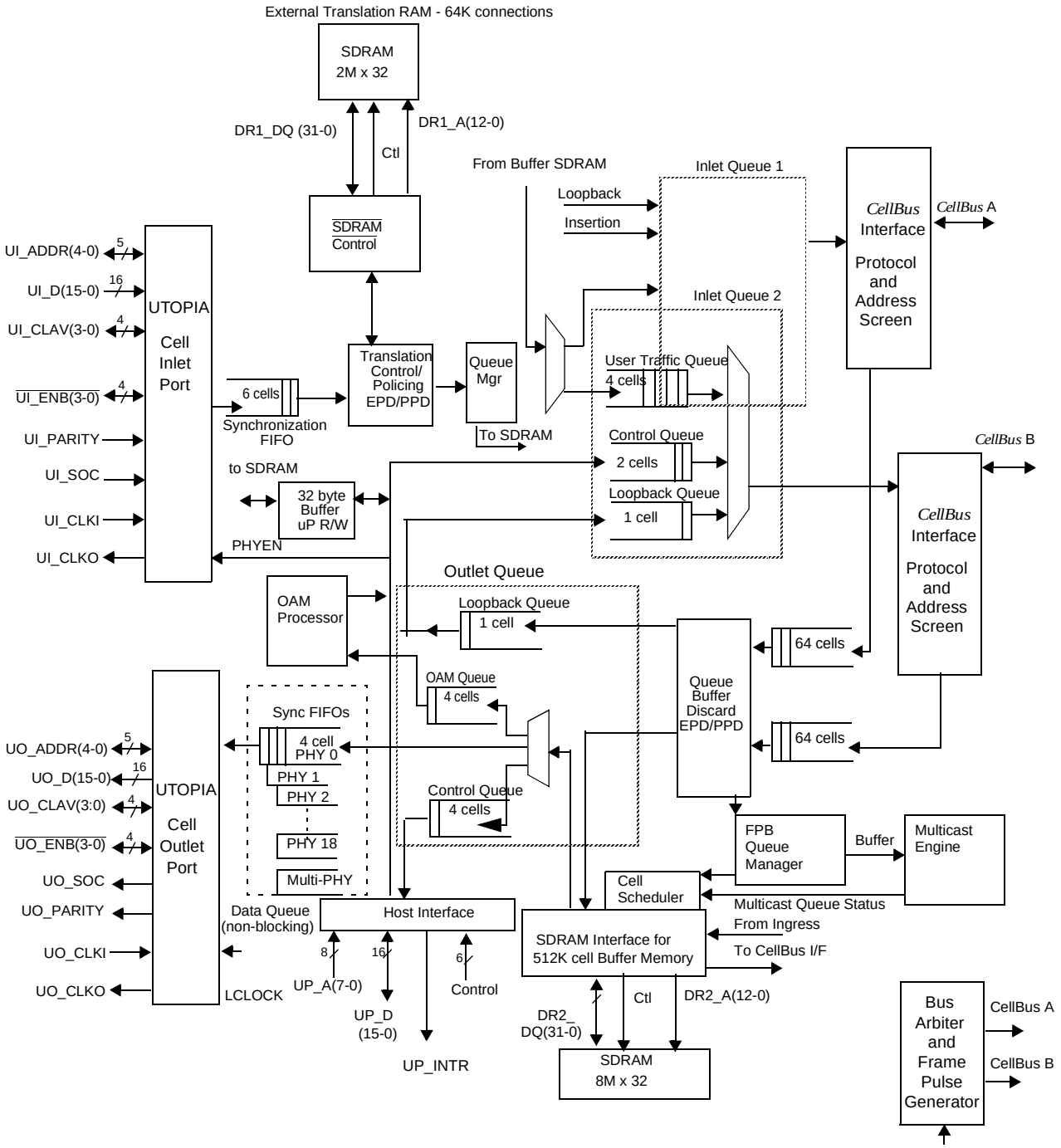


Figure 1. ASPEN Express (TXC-05806) Block Diagram

BLOCK DIAGRAM DESCRIPTION

Cell Inlet to *CellBus*

On the cell inlet side of the ASPEN Express is circuitry associated with accepting cells from the line and passing them to the *CellBus* with an appropriate header. The Cell Inlet Port block is selectable to be compatible with either the ATM Forum UTOPIA (Universal Test and Operations Physical Interface for ATM) Level 1 or 2 interface. Incoming cells may be translated using the ASPEN Express. Translation and routing header tables to support this function are contained in an external SDRAM (up to 64k connections). There is support for VPI, or VPI/VCI address translation. Lookup is supported for up to 600 VPIs within the full 4096 VPI range. Each port can be configured independently for 2 consecutive ranges of VPIs. Different PHYs can use overlapping ranges of VPI. Each VPI is then configured to support 2 ranges of VCI. The total number of VCIs supported cannot exceed 64k. Different VPIs can use overlapping ranges of VCI.

Each VCI can be configured for UPC. Full TM4.1 support for policing is provided utilizing two 32-bit GCRA engines implementing the Virtual Scheduling Algorithm with a 20 ns resolution clock.

Ingress and egress queues share a 512K cell buffer in SDRAM and utilize a decoupling FIFO for each *CellBus*. The ingress queuing consists of 8 priority queues for each CellBus. Queue limits are enforced for each queue via dynamic buffer allocation.

When the ASPEN Express has a cell pending in one of its ingress queues, it makes a *CellBus* access request, and upon receiving a grant will send the cell to the *CellBus* in standard *CellBus* format. In addition to data cells, the ASPEN Express can also send Control cells from the local microprocessor to the bus. Diagnostic loopback cells received from the CellBus may be looped back to the CellBus to a designated *CellBus* device/queue. Both the Control cells and the Loopback cells have inlet queues consisting of FIFOs with a depth of two cells and one cell, respectively.

Local switching is supported so that cells received from the Utopia can be directly queued to egress queues and routed back to another (or the same) Utopia address.

A count is kept for total numbers of invalid cells received. An invalid cell is one in which the VPI or VCI is out of range of the configured lookup table. Registers hold Port, VPI and VCI of the last invalid cell received. Misrouted cells are defined as connections whose active bit has not been set; a count is kept for all misrouted cells. Per VC statistics include cell count, non-conforming cells for GCRA1 and non-conforming cells for GCRA2 as well as buffer discard counts for each connection and each queue.

Early Packet Discard (EPD) and Partial Packet Discard (PPD) are ATM cell discard techniques which maximize the transmission of whole packets (goodput) for AAL5 adapted packet traffic. These techniques minimize transmission of partial packets since these represent wasted bandwidth; any cells dropped from a packet require the retransmission of the entire packet by the network. Both EPD and PPD are supported (per VCC) for ingress and egress. The ingress connection table will hold the packet discard state for ingress connections (VCCs). A separate packet discard state machine will keep track of packet discard states for each VCC in the connection table. If a cell is discarded (either due to UPC/NPC or queue full) and packet discard is enabled, the connection drops all remaining cells of the packet. A separate EPD queue threshold triggers EPD for all new packets received while the queue threshold exceeds this level.

Segment or end-end OAM cells for selected VCCs (F5) or VPCs (F4) may be selectively routed to the OAM processor. The OAM processor handles all OAM FM functions per ITU-T I.610 including AIS, RDI, Continuity Check and Loopback. All loopback cells can be routed to the host processor. Management flows are identified by assigning them to the host extraction queue; all management cells are extracted to the host.

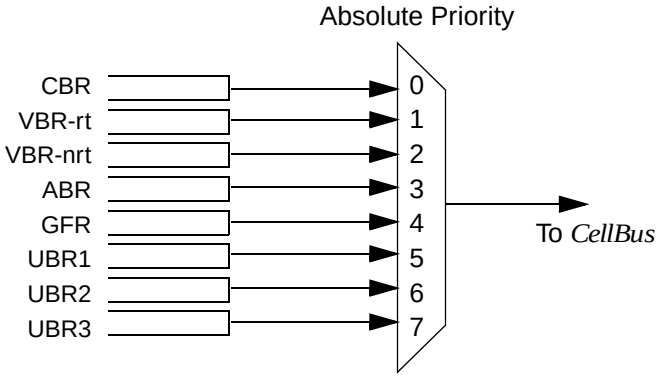


Figure 2. ASPEN Express Ingress External Queueing Structure per *CellBus*

CellBus to Cell Outlet

On the cell outlet side, cells received from the *CellBus* are screened for their *CellBus* address and, if they are identified for this device, are routed into a FIFO structure in the Outlet Queue block. The *CellBus* address is set by Unit Address leads $\overline{UA(4\text{-}0)}$ or configured by the host. Cells arriving from the *CellBus* are tagged as unicast or multicast in the CellBus Routing Header (CBRH). If tagged as a multicast cell, the Tandem Routing Header (TRH) will contain a multicast session ID. There are up to 511 different multicast sessions shared by all devices on both *CellBuses.* Each ASPEN Express may be programmed to accept cells associated with these multicast sessions in the Multicast Session Table (MST). Each entry in the MST contains a list of destination ports for that device to which a cell will be forwarded (max. all 64 ports). If all entries in the MST for a given session are '0', then all cells for this session are not accepted by the screen. Control cells are routed to a separate queue in external memory and are sent to the host processor. *CellBus* loopback cells arriving from the bus are routed to a 1-cell outlet loopback queue and then looped back to the *CellBus* with a new *CellBus* routing header/Tandem Routing Header.

All multicast cells are queued in 1 of 3 priority queues per port - VBR, GFR or UBR. These multicast queues are given higher priority than their unicast equivalents as shown in Figure 3. The multicast engine replicates the buffer pointer to these queues and does not waste buffer space replicating the cell. Each multicast session may be configured to translate each leaf to a unique cell header for spatial multicast.

All cells are stored in the shared 512k cell buffer SDRAM and queued in one of 8 service categories associated with the destination port. Multicast cells share 3 service class priority queues (VBR, GFR and UBR) per port. Each multicast queue has a higher priority than its corresponding unicast queue. Available buffer space is decreased by 8 cells for each multicast cell stored but it is only stored once regardless of the number of replications specified. Therefore, appropriate consideration must be given to provisioning unicast and multicast queues.

The ASPEN Express supports queue over-reservation to accommodate traffic burstiness inherent in video and internet traffic. Using this technique, the sum of all queue limits in a service category may exceed the buffer allocation for the entire class. Cells may be discarded if either the individual queue limit is exceeded or the service category buffer limit is exceeded.

At the cell outlet, cells may optionally be translated for either VPC or VCC header translation. Provisions are made for insertion of an Explicit Forward Congestion Indication (EFCI) bit when queues exceed a configurable dynamic threshold. Statistics are kept for discarded cells (per queue, per VC, and per service category) and received cells are counted per VC.

Unicast cells from the *CellBus* are identified by a 16-bit connection ID (CID) contained in the TRH which is unique for each connection. Both VPI and VCI are translated for a VCC. All VCCs within a VPC share a common connection ID. If header translation is configured, only the VPI will be translated (for a VPC) and the VCI passed through. Multicast cells are identified either by the multicast session contained in the TRH or in the CBRH. The device can be configured for either method of multicast identification in order to allow backward compatibility with older *CellBus* devices in existing ASPEN and/or CUBIT systems. All leaves of a multicast session may be uniquely translated for VPI/VCI.

Control cells may be extracted to the host or the OAM processor by assigning the appropriate QID (0x213) for cell extraction to the connection via the connection table.

Additionally, if enabled the ASPEN Express may be placed in a *CellBus* monitoring mode. In this mode, the ASPEN Express accepts all traffic coming in from the *CellBus* regardless of the *CellBus* ID specified in the CBRH. The cells are enqueued based on *CellBus* ID, *CellBus* IDs 0-15 are enqueued in service class 0 queues for ports 0-15, *CellBus* IDs 16-31 are enqueued in service class 0 queues for ports 16-31. Additionally, all broadcast and multicast traffic are sent to queue 0 port 32.

In support of APS applications, the *CellBus* ID may be configured differently for receive and transmit directions so that 2 devices may have the same *CellBus* receive addresses but different *CellBus* transmit addresses. When this mode is set (UA_FLIP = 1), the *CellBus* receive ID is set to both $\overline{UA(4\text{-}1)}$ = 0 and $\overline{UA(4\text{-}1)}$ = 1. The *CellBus* transmit address remains = UA.

In support of 32 user mode, the *CellBus* ID may be configured to use 2 IDs for transmit so that it can utilize both phases of the 32 user *CellBus* frame and achieve full bandwidth support in 32 user mode. In this case a second *CellBus* transmit address = UA + 16 is used.

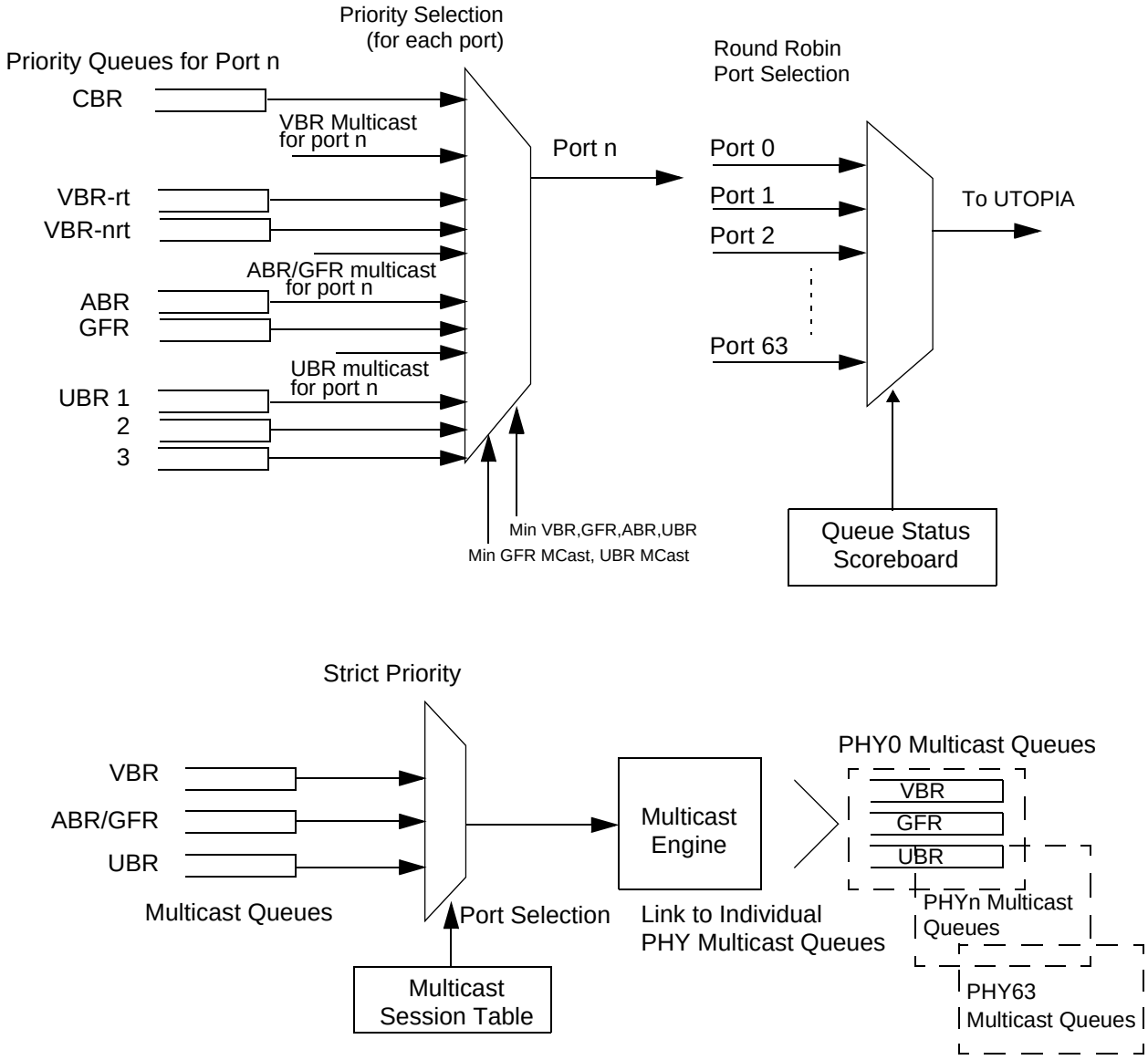


Figure 3. ASPEN Express Egress External Queuing Structure

Starvation Prevention

A starvation prevention mechanism exists for VBR-nrt, ABR, GFR and all UBR egress queues including GFR multicast and UBR multicast. The mechanism guarantees that each queue will receive at least as much bandwidth as is specified for that service category. In addition to unicast queues, GFR and UBR multicast each have their own specified MCR rates. Each queue not meeting its specified minimum cell rate is serviced at a constant inter-cell time interval. If all minimum rates specified add up to 100% of the available bandwidth then the effect is a weighted priority scheduling of the queues instead of the default strict priority. The mechanism is work conserving so that if any queue does not utilize its minimum rate, that bandwidth is available to other queues in strict priority.

Dynamic Buffer Allocation

All (ingress and egress) queues share a common 512k cell buffer. Each service category queue for ingress may specify an Early Discard Threshold (EDT) and a Discard Threshold (DT). The parameter specified for EDT is DTexp which is the square root of the reciprocal of the share of free cell buffers available. For example, if DTexp = 4 then EDT = 1/16 x number of free cell buffers. All cells entering a queue whose EDT threshold is exceeded are subject to discard if they are CLP1 cells and the connection is configured as CLP significant or EPD discard if the connection is configured as AAL5 and the cell represents the beginning of a packet. The Discard Threshold = EDT + BuffMin where BuffMin is a constant parameter representing a minimum buffer reservation for that queue. Figure 4 shows a graphic representation of the dynamic thresholds as a function of available buffer space. Cells entering the queue when the DT is exceeded are subject to discard unless the connection is configured as AAL5 and the cell represents the end of packet.

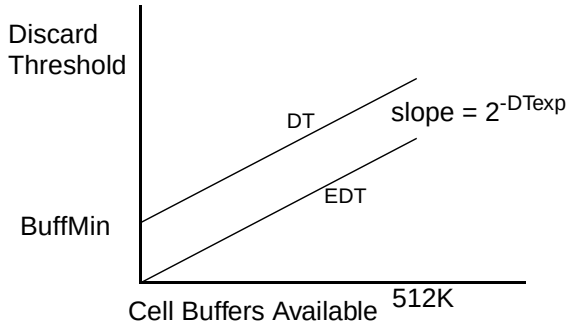


Figure 4. Graphic Representation of DT and EDT thresholds vs. Free Cell Buffers Available

Egress queues utilize the same discard thresholds for each service category. The discard thresholds apply to queues for all ports of that service category. Port modifier parameters may be specified to increase or decrease the discard thresholds for all queues of that port relative to their service category discard thresholds. A second set of discard thresholds are also available for the sum of all queues for each service category. This is a constant discard threshold (SCDT) and an early discard threshold (SCEDT). If a cell enters a service category queue while the SCEDT is exceeded then that cell will be subject to CLP1 discard and EPD just as if its own queue EDT was exceeded. Likewise, if a cell enters a service category queue while the SCDT is exceeded for that service category, then the cell will be discarded unless it is the end of packet for an AAL5 designated flow.

PRODUCT PREVIEW

DEVICE INTERFACES

Microprocessor Interface

A 16-bit microprocessor data bus supports either Intel or Motorola processor interfaces. All communication to and from the chip is done via an internal mailbox. A gateway processor accesses the mailbox and processes messages from the host. All configuration and management may be done through this interface. A host driver is available providing a high level API to the host to manage the chip.

UTOPIA Interface

The ASPEN Express's UTOPIA 2 port constitutes the main interface for the cell traffic between the ASPEN Express and other devices. The ATM Forum compatible Level 2 interface can address up to 64 physical devices in ATM layer emulation (master) mode by incorporating 4 CLAV/ENB signals thereby allowing each polling cycle to address 4 devices but only 1 is selected for a given transfer. ASPEN Express supports both master and slave modes of operation.

VCC/VPC cross-connect: Connections may be switched directly from 1 UTOPIA port to another.

The possible UTOPIA configurations in cell mode are shown in Figures 5, 6, 7 and 8.

Note: All physical layer devices must be initialized prior to configuring and enabling the UTOPIA interface on ASPEN, to ensure proper signaling startup.

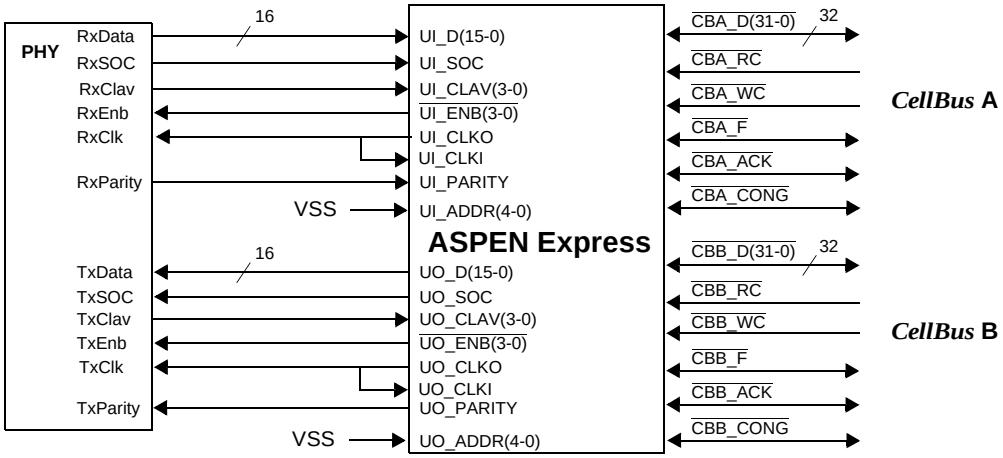


Figure 5. ASPEN Express Device in ATM Layer, Single-PHY Mode Configuration

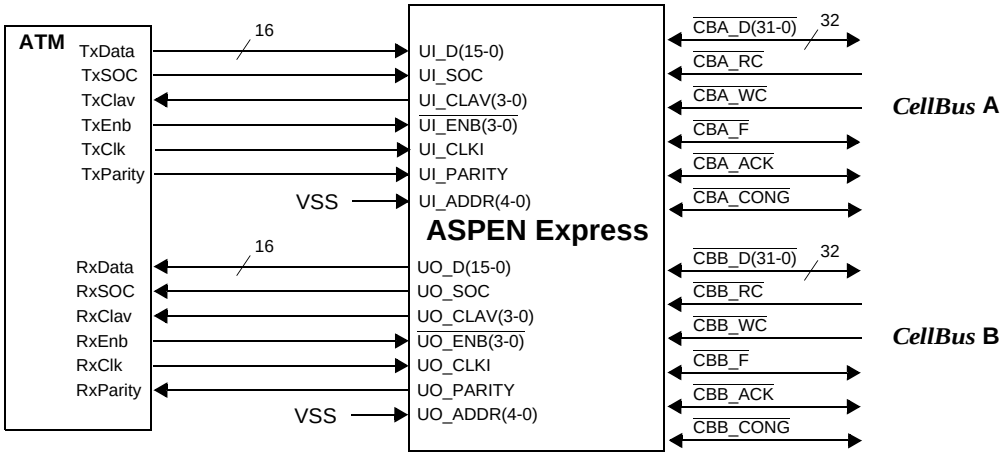


Figure 6. ASPEN Express Device in PHY Layer, Single-PHY Mode Configuration

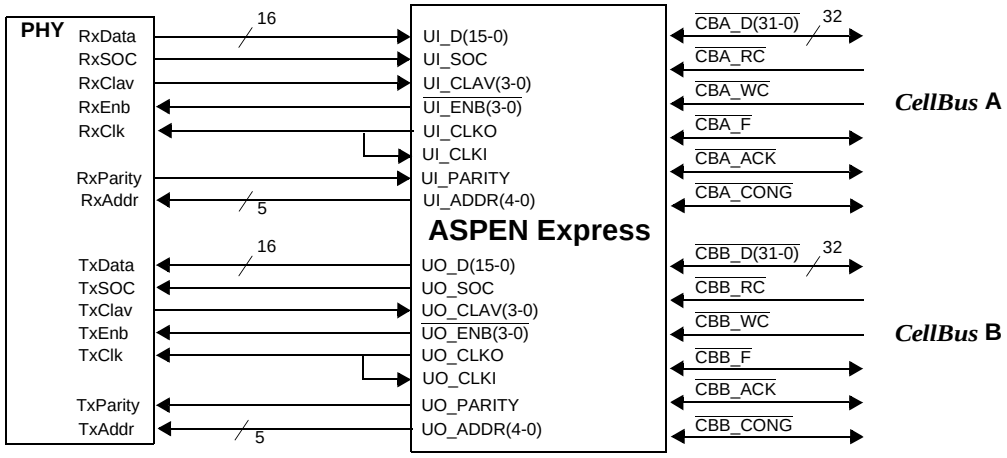


Figure 7. ASPEN Express Device in ATM Layer, Multi-PHY Mode Configuration

PRODUCT PREVIEW

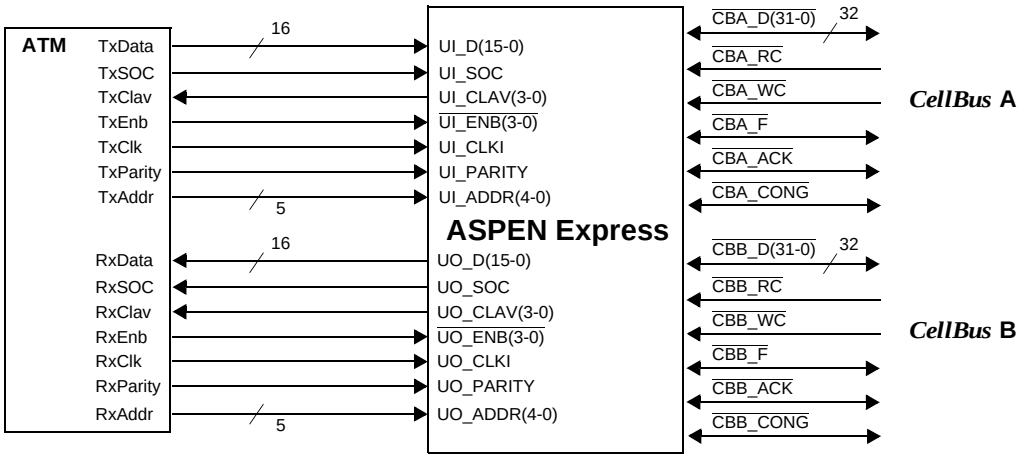


Figure 8. ASPEN Express Device in PHY Layer, Multi-PHY Mode Configuration

Dual Latency 124 port Operation:

For dual latency DSL devices, the Aspen Express will support 124 ports in a special mode called Dual Latency. In this mode, each pair of dual latency ports shares the lookup space for that port so that VPI/VCI combinations cannot be duplicated for both the low and high latency ports. Likewise, these 2 ports share the 11 egress queues (8 unicast and 3 multicast) so that the low latency channel (real time) uses the CBR, VBR-rt and VBR multicast queues. All other queues are dedicated to the high latency (data) channel. The dual latency channel pairs are mapped as follows:

Table 1. Dual Latency Channel Mapping

Utopia Address	CLAV/ENB Pair	Low Latency Ports	High Latency Ports
0 - 30	1	0 - 15	16 - 30
0 - 30	2	31 - 46	47 - 61
0 - 30	3	62 - 77	78 - 92
0 - 30	4	93 - 108	109 - 123

where each Low Latency and High Latency port are paired together respectively (i.e. channel 0 and 16 are paired together in the same DSL subscriber as are 108 and 123).

Dual *CellBus* Interface

The *CellBus* is a 37-lead GTLP shared bus with 32 bits of data. It can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Access to the bus is controlled by a bus controller which resides in each *CellBus* device. Up to 32 *CellBus* devices may be connected on a single bus and 1 of them must be selected as the bus controller by setting its $\overline{\text{ENARBA}}$ or $\overline{\text{ENARBB}}$ lead low. Three different priorities may be requested by each device to the arbiter for access to the bus. The Aspen Express has two *CellBus* interfaces which may be used for either load sharing or redundancy.

CellBus bridging capability is provided which allows traffic to be switched from one *CellBus* to the other on a per connection basis. This allows scalability of port density and bandwidth by using multiple Aspen Express devices; one *CellBus* of each device is connected together as a local *CellBus* which allows switching between the devices. The other *CellBus* for each device is then used to connect to selected line cards in the system which are only serviced by that *CellBus.*

Connection Table Memory Interface

An external local memory is required by the ASPEN Express for policing statistics and address translation. The ASPEN Express integrates a complete memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a 100 MHz SDRAM. No external timing or control logic is required. The CT RAM memory controller directly addresses up to 8 Mbytes (64Mb, 128Mb or 256Mb SDRAMs may be used). The Connection Table memory controller is configured to use either (two) 16-bit memories or (one) 32-bit memory (see Figure 9).

Cell Buffer Memory Interface

An external local memory is required by the ASPEN Express for cell queuing. The ASPEN Express integrates a complete SDRAM memory controller to support this local memory. The on-chip memory controller provides a glueless interface to a 32-bit 100 MHz SDRAM. No external timing or control logic is required. The SDRAM memory controller directly addresses up to 8 Mbytes of external memory to enable a maximum shared buffer size of 524,288 cells. The Cell Buffer memory controller is configured to use either (two) 16-bit memories or (one) 32-bit memory (64Mb, 128Mb or 256Mb SDRAMS may be used, see Figure 9).

Boundary Scan (Test Access) Port

The test interface includes a five-lead Test Access Port (TAP) as the boundary scan port that conforms to the IEEE 1149.1 standard. This standard provides external boundary scan functions to read and write the external input/output leads from the TAP for board and component test.

PRODUCT PREVIEW

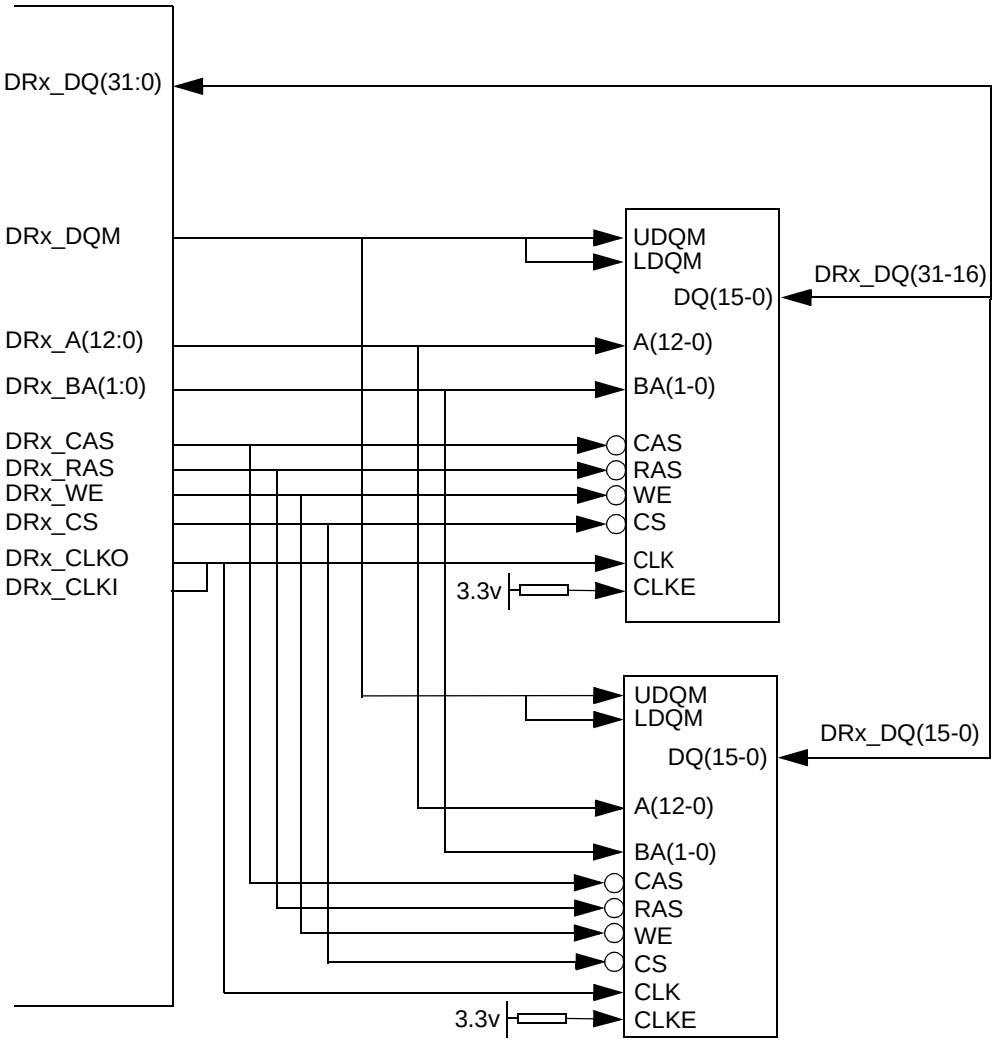


Figure 9. ASPEN Express SDRAM Configuration

OPERATION

INTRODUCTION TO *CellBus* ARCHITECTURE

This section provides an introduction to *CellBus* bus architecture and operation. Additional technical information is provided in Appendix A and B of a TranSwitch Technical Manual, document number TXC-05802-TM1, entitled "*CellBus* Bus Technical Manual and CUBIT-*Pro* Applications", which is available as a CUBIT-*Pro* document from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

CellBus Operation

The ASPEN Express is a versatile CMOS VLSI device for implementing ATM switching and traffic management functions. Various ATM cell switching or multiplexing structures can be formed by interconnection of a number of ASPEN Express devices (or other TranSwitch *CellBus* compatible devices) over a 37-line parallel bus with 32 data bits, the *CellBus*. Since the interconnect structure is a bus, communication between any of the devices on the bus is possible. Each cell placed onto either *CellBus* by an ASPEN Express device can be routed either to one single *CellBus* device port (unicast addressing), or to multiple *CellBus* device ports (multicast or broadcast addressing). Depending upon the needs of an application, up to 32 *CellBus* devices may be interconnected on either *CellBus*. With a *CellBus* frequency of 40 MHz, the raw bandwidth of each *CellBus* exceeds 1 Gbit/s.

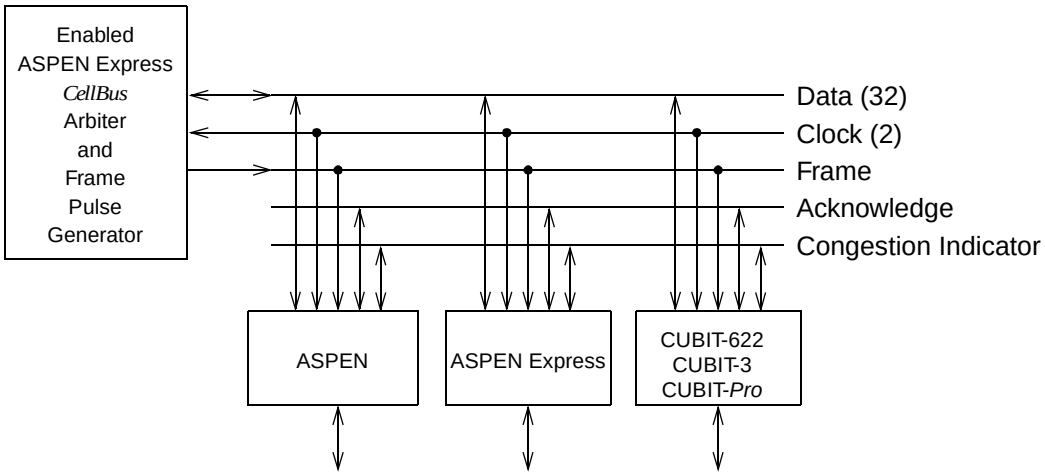


Figure 10. *CellBus* **Structure**

The *CellBus*, shown in Figure 10, is a shared bus, and can be implemented either on a single circuit card, or in a backplane configuration among multiple circuit cards. Since multiple ASPEN Express devices share the same bus, bus access contention must be resolved. This access contention is resolved by use of a central arbitration function. ASPEN Express devices will request bus access, and the central bus Arbiter will grant access back, in response. The circuitry for this bus Arbiter and frame pulse generator is included inside the ASPEN Express device. Any one ASPEN Express on a given bus in a system may be enabled to perform the bus arbitration and frame pulse generation functions for the arbitrated bus.

PRODUCT PREVIEW

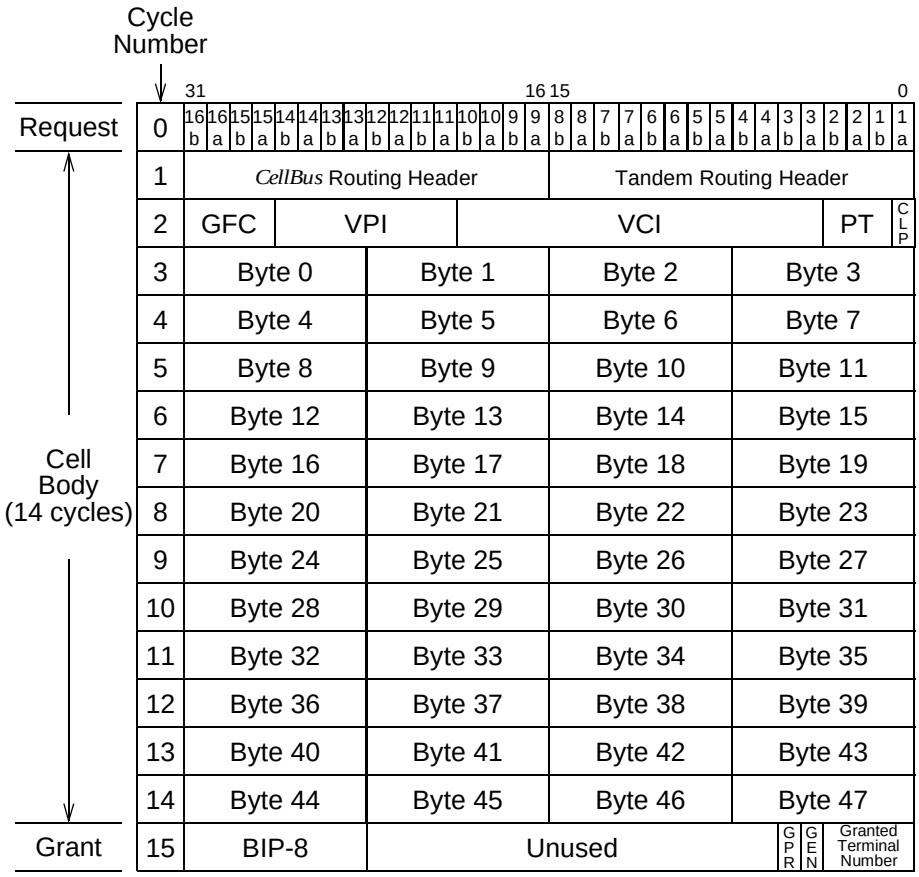


Figure 11. *CellBus* Frame Format

The *CellBus* has a framed format that is 16 clock cycles long and 32 bits wide, as illustrated in Figure 11. The first cycle of each frame is the Request cycle (Cycle 0), during which those ASPEN Express devices (or other *CellBus* devices) which have a cell to send to the *CellBus* each make an access request by asserting one or two assigned bits on the *CellBus*. The $\overline{\text{CBA\_F}}$/$\overline{\text{CBB\_F}}$, $\overline{\text{CBA\_ACK}}$/$\overline{\text{CBB\_ACK}}$, and $\overline{\text{CBA\_CONG}}$/$\overline{\text{CBB\_CONG}}$ signals are asserted during a Request cycle. The *CellBus* ID assigned to each ASPEN Express by Unit Address leads $\overline{\text{UA(4-0)}}$ uniquely specifies which two bits it may assert during the *CellBus* Request cycle time. *CellBus* IDs 0-15 are used for 16-user systems and IDs 0-31 are used for 32-user systems (see Figure 12). For example, when leads $\overline{\text{UA(4-0)}}$ are all high, the *CellBus* ID is 0 and bits 1a and 1b are selected. By asserting one of its assigned bits, or the other, or both, access requests of three different priorities may be made (controlled via bits P1, P0 in memory address 00AH). A central *CellBus* Arbiter accepts these access requests, executes an arbitration algorithm (highest priority served first, round-robin within each priority), and issues a *CellBus* access grant during the final cycle of the frame, the Grant cycle (Cycle 15). Each grant issued by the *CellBus* Arbiter is for one *CellBus* device to send one cell to the *CellBus*. Whichever *CellBus* device is issued a grant during a Grant cycle will transmit its cell during the 14 Cell Body clock cycles of the next bus frame, and will also drive an 8-bit cell parity check (BIP-8) during the Grant cycle of that *CellBus* frame. Each cell sent can be of unicast, multicast, or broadcast type. ASPEN Express devices will accept single-address cells routed to an address defined by its address straps $\overline{\text{UA(4-0)}}$ as well as all broadcast cells, and multicast cells whose multicast session IDs are configured appropriately. Thus, cells may be sent from any one ASPEN Express to any one ASPEN Express (or other *CellBus* device) or to multiple destinations.

The ASPEN Express can be operated in either 16-user or 32-user mode, selectable via the U32 lead, as shown in Figure 12. For the 16-user mode, all *CellBus* frames have an associated frame pulse CBA_F/CBB_F. However, in 32-user mode the frame is duplicated, so that an odd and even frame are provided. The distinction between these two frames is given by the location of the Request cycle relative to the frame pulse. The Request cycle in the even frame coincides with the frame pulse, whereas in the odd frame the pulse is not present. In the even frame ASPEN Express devices with *CellBus* address 0 -15 (lower 16 users) request access to the *CellBus*, and in the odd frame ASPEN Express devices 16-31 (upper 16 users) request access to the *CellBus*. The full *CellBus* bandwidth is available to be shared among all the users on the *CellBus* in either 16 or 32-user mode.

An additional feature available in the ASPEN Express is a software configuration bit called DualTX_A and DualTX_B. These controls allow each *CellBus* to assume 2 *CellBus* addresses for transmit - one in the range of 0-15 and the other in the range of 16-31 so that the device can utilize the entire bandwidth of the *CellBus* in a 32-user configuration.

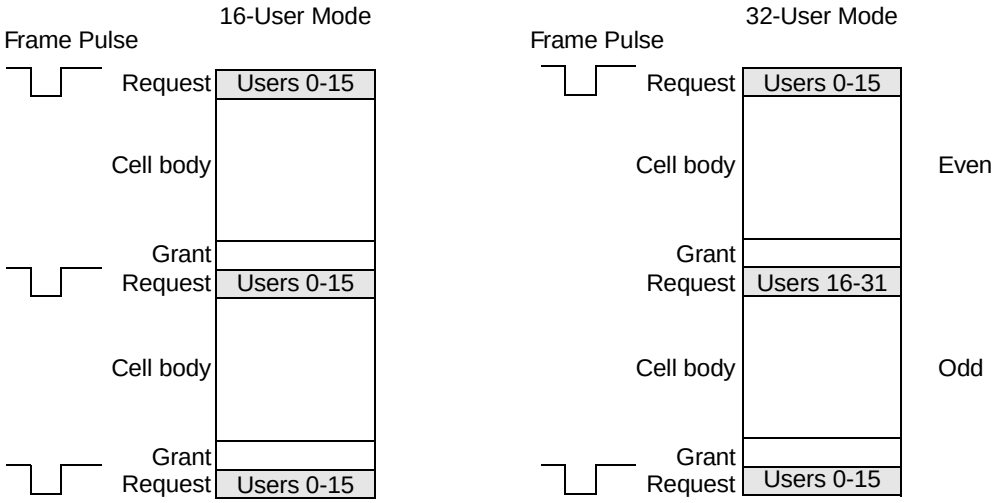


Figure 12. *CellBus* **16/32-User Modes - Frame Formats**

To detect *CellBus* errors, a BIP-8 (Bit Interleave Parity byte) is calculated over the 54-byte data field that extends from the first Tandem Routing Header byte in Cycle 1 through the final payload data byte, Byte 47 in Cycle 14. The BIP-8 is generated by the transmitting ASPEN Express using the following algorithm: The first byte of the Tandem Routing Header is exclusive-or gated with an all-ones byte, creating a starting seed value. This seed value is then exclusive-or gated with the second byte of the Tandem Routing Header. The result is then exclusive-or gated with the next byte in the cell. This process is repeated with every successive byte in the cell, through Byte 47 of the payload, and the final result is transmitted as the BIP-8 byte in cycle 15. The receiving Aspen Express performs the same process and compares the generated BIP-8 with the received BIP-8. If no errors are detected the receiving ASPEN Express drives CBA_ACK/CBB_ACK low, acknowledging receipt of a cell. The *CellBus* Routing Header has its own CRC-4 field and is not included in the BIP-8 calculation. A cell with a BIP-8 or CRC-4 error is discarded.

The only signals required to operate the *CellBus* which are not sourced by a ASPEN Express device are two transfer clocks per *CellBus*: write clocks CBA_WC, CBB_WC and read clocks CBA_RC, CBB_RC. These clock signals are of the same frequency, but may be slightly phase-offset to accommodate different backplanes and devices. The frame pulse used to define the bus frame cycle is sent out by one of the ASPEN Express devices, the arbitration function is also performed by the same ASPEN Express device. Each Aspen Express device contains the circuitry for both the bus Arbiter and the Frame Pulse Generator. Only one ASPEN Express per *CellBus* will have this circuitry enabled, by setting the ENARBA/ENARBB leads on the device to the active low level.

CellBus Cell Routing

The *CellBus* architecture allows several types of cell routing from any one inlet port to the outlet ports of the ASPEN Express devices on the *CellBus*:

- Point-to-Point Routing: In Unicast or Single Address cell routing a cell coming into an inlet port is transferred to a single outlet port of a specific *CellBus* device. The ASPEN Express can also address a cell to itself, effectively implementing both the inlet and outlet ports.
- Point-to-Multipoint (Multicast): In multicast routing the cell arriving at the inlet port is sent to the subset of outlet ports that belong to the specific multicast session in each *CellBus* device on the *CellBus*.
- Point-to-Multipoint (Broadcast): A cell coming into the inlet port is routed to all of the outlet ports of all the *CellBus* devices on the *CellBus*.

For each of the routing methods the cells can be sent to different output queues according to whether the cell is used as a data cell or as control/loopback cell. Furthermore, data cells can be selected to go to one of four different data outlet queues per UTOPIA 2 outlet port: CBR queue, VBR-rt queue, VBR-nrt queue, and UBR/GFR queue.

The encoding rules for the two-byte *CellBus* Routing Header in Bits 31-16 of Cycle 1 are summarized in Figure 13.

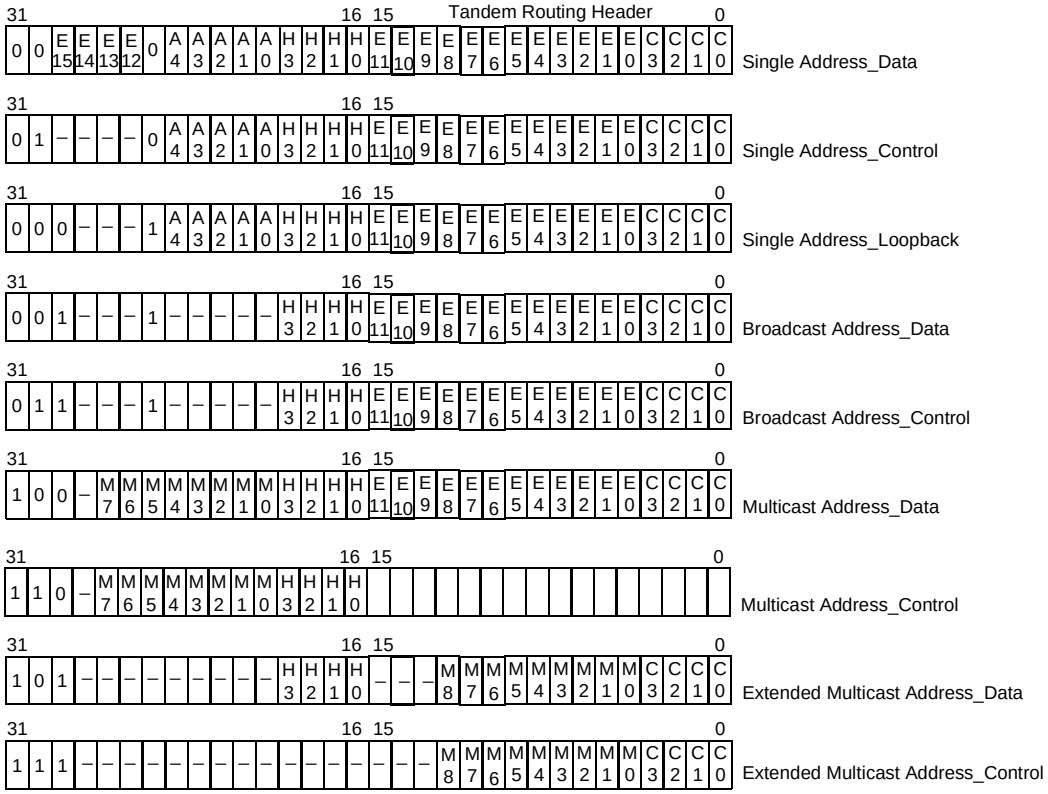


Figure 13. *CellBus* **Routing Header Formats**

CellBus Routing Header Format

The *CellBus* Routing Header contains the following fields, as shown in Figure 13:

A: ASPEN Express single address field (5 bits, for 32 addresses). A0 is the LSB. For example, A(4-0)=00000 is the address value for the ASPEN Express whose five device identity straps $\overline{UA(4\text{-}0)}$ are all tied high (HHHHH).

M: Multicast number field (9 bits, for 512 multicast sessions). M0 is the LSB.

H: CRC-4 field. This 4-bit field H(3-0) provides *CellBus* Routing Header error protection across the *CellBus* in both directions. It is calculated over the 12-bit word (X11-X0) in bits 31-20 of the Routing Header using the following logic, where ⊕ represents logical exclusive-or:

$H3 = (\overline{X7} \oplus \overline{X9} \oplus \overline{X3} \oplus \overline{X10} \oplus \overline{X8} \oplus \overline{X5} \oplus \overline{X2})$

$H2 = (X6 \oplus X8 \oplus X2 \oplus X9 \oplus X7 \oplus X4 \oplus X1)$

$H1 = (\overline{X5} \oplus \overline{X7} \oplus \overline{X1} \oplus \overline{X8} \oplus \overline{X6} \oplus \overline{X3} \oplus \overline{X0})$

$H0 = (X8 \oplus X10 \oplus X4 \oplus X11 \oplus X9 \oplus X6 \oplus X3 \oplus X0)$

For cells arriving from the *CellBus*, the ASPEN Express automatically calculates the corresponding CRC-4 and sets to 1 the status bit CRCF (bit 7 in register 008H) if it is not the same as that in bits H(3-0) of the received Routing Header. This status bit may be enabled to cause an interrupt signal to the microprocessor by setting to 1 the enable bit INTEN7 (bit 7 in register 009H). The CRC-4 is automatically calculated and inserted by the ASPEN Express into cells sent to the *CellBus*.

Tandem Routing Header Format

In ASPEN Express applications, the Tandem Routing Header bits 11-0 (Extended Queue field) are used for queue and priority selection and include cyclical redundancy protection (C3-C0).

E: Extended Queue field E(15-0). E(5-0) indicate connection I.D., and C(3-0) is the CRC-4.

CellBus Status Signals and Monitoring

The ASPEN Express provides the capability to monitor the activity on the *CellBus*. The essential signals that determine whether the *CellBus* is active (in the absence of any cell traffic) are the clock signals and the frame pulse.

The *CellBus* clocks (read and write) are generated externally to the ASPEN Express. If either of these clocks fails, the entire *CellBus* will cease operation. The ASPEN Express provides the capability to detect the absence of clock signal for more than the equivalent of 32 processor clock (PCLK) cycles. The failure detection is performed independently for the *CellBus* Read Clocks $\overline{CBA\_RC}$, $\overline{CBB\_RC}$ and the *CellBus* Write Clocks ($\overline{CBA\_WC}$, $\overline{CBB\_WC}$).

Either event can be used to generate a microprocessor interrupt provided that the corresponding bit in the interrupt enable register is set.

The second monitoring function concerns the detection of loss of frame (CBLOF). The detection mechanism looks for two consecutive missing *CellBus* frame pulses $\overline{CBA\_F}$/$\overline{CBB\_F}$ in 32-user mode (U32 = Low), and four consecutive missing *CellBus* frame pulses in 16-user mode. The *CellBus* Read Clock must be present to detect Loss of Frame Pulse. CBLOF will generate an interrupt to the microprocessor if the corresponding interrupt enable bit is 1 (register 006H, bit 2: INTENA2).

Apart from the detection of loss of *CellBus* Read and Write clocks, the device has a recovery mechanism that re-synchronizes the device to the *CellBus* frame pulse as soon as the *CellBus* clocks are restored and stabilized to resume normal operation.

THE *CellBus* INTERFACE

Thirty-seven lines comprise the *CellBus* interface, as shown in Figures 1 and 10. There are thirty-two data lines, with Frame, Acknowledge, and Congestion Indicator lines, all sourced by a ASPEN Express device, and two Clock lines sourced by external drivers. Additional technical information for implementing a *CellBus* Bus with circuit cards plugged into backplane connectors is provided in a document entitled "TranSwitch *CellBus* Bus Reference Design Guideline for CUBIT-*Pro* Applications", Revision 0.5 dated February 19, 1999, which is available as a CUBIT-*Pro* document from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

Operation with Internal GTL+ Transceivers

Gunning Transceiver Logic (GTL+) transceivers for *CellBus* Data, Frame, Acknowledge, and Congestion Indicator lines are contained internally in the ASPEN Express, along with two clock line GTL+ receivers. Each of the drivers has a typical current sink capability of 45 mA and is capable of driving a bus on a card or on a backplane directly. Each of the GTL+ lines is to be pulled up at each of its ends by a 50 ohm (± 5%) resistor (metal film or carbon composition) to a +1.5 V low-impedance supply. Each end of each line should have a filtering capacitor connected from the +1.5 V supply to ground, as shown in Figure 14.

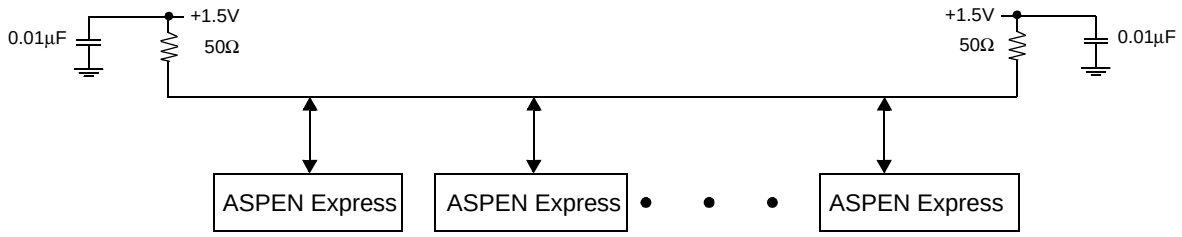


Figure 14. External Circuit Requirements for GTL+ Transceivers

In the ASPEN Express lead configuration, all of the leads involved with the *CellBus* interface are aligned along one side of the package (between lead rows AB and W). This side of the package must be aligned toward the board connector, or toward the *CellBus*, with as little board trace length as possible between the leads and the connector or *CellBus*, to maximize operating speed.

Clock Source

Two GTL+ clock signals must be driven to the *CellBus* from an external source. These are the write clocks, $\overline{\text{CBA\_WC}}$, $\overline{\text{CBB\_WC}}$, and the read clocks, $\overline{\text{CBA\_RC}}$, $\overline{\text{CBB\_RC}}$. A phase relationship keeping the write clock between 0.5 and 4 nanoseconds behind the read clock is needed to ensure proper synchronous *CellBus* operation. When the clock driver is driven from the center of the backplane (i.e., no greater than half a backplane length from any card) a minimum phase distance of 1.0 ns or more must be maintained. When the driver is at one of the ends, a more conservative 2-4 ns minimum is required. In any *CellBus* implementation, on the backplane and on each card, care must be taken to ensure that these two lines are routed together. The capacitive and inductive loadings of the two lines should be as nearly equal as possible, to maintain performance. At the drive point, a delay line should be used to maintain a stable delay, and the read and write clock drivers must be units of the same integrated circuit package. All of these precautions will ensure the most stable clocks and permit the highest possible operating speed.

CellBus Bus Arbiter Selection

One copy of the *CellBus* Bus Arbiter circuitry is included inside each ASPEN Express device. Enabling of the Arbiter on a particular ASPEN Express is done by connecting the $\overline{\text{ENARBA}}$, $\overline{\text{ENARBB}}$ leads of that device to ground (V_{SS}). Only one Arbiter may be enabled at a time. It is the responsibility of the overall system control to decide which ASPEN Express will have its Arbiter enabled, and to enable it. Failure of an Arbiter can be

detected by using the NOGRT indications. If multiple ASPEN Express devices are indicating NOGRT failures, an Arbiter failure is indicated. It is again the responsibility of system control to enable another *CellBus* Arbiter. Upon switching from one Arbiter to another, the receiving devices on the *CellBus* will automatically re-align to the new frame position within one *CellBus* frame.

MULTICAST SESSION MEMORY

A multicast address data cell is sent to all ASPEN Express devices, and each ASPEN Express will check the multicast session (max 512) and lookup in its Multicast Session Table (MST) if this device should participate in the multicast session. Each of the 512 multicast session addresses has a 64-bit list of destination ports to which a cell can be forwarded (max. all 64 ports). For each bit that is set to 1 in the list corresponding to the received multicast address, the cell is forwarded to the port corresponding to that bit. Each ASPEN Express device can be configured to accept any or all of the 512 possible multicast sessions and send them to any or all of the possible 64 destination ports by setting the bit in the corresponding location in the table. The multicast process adopted is a pointer replication process as opposed to a cell duplication process. Pointers to a given multicast cell are added to their appropriate destination queues without replicating the cell. All Broadcast Traffic uses Multicast Session 0.

If any port becomes disabled, the active bit corresponding to that port should be reset and then disable the UTOPIA port by resetting to zero the corresponding PHYEN bit in registers A01H to A08H. Resetting the active bit will prevent the cell from being replicated to the queue for that port.

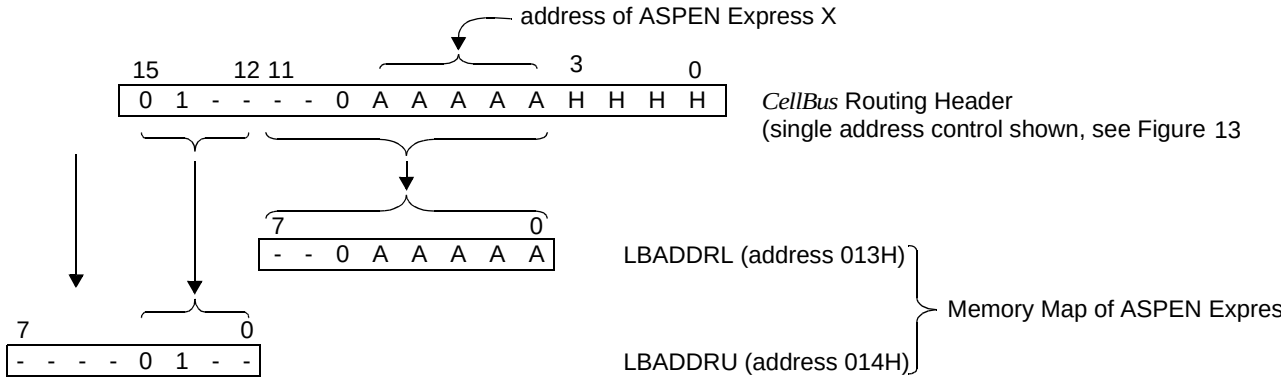
Note: In order to update the leaves associated with a particular multicast session, eight consecutive memory addresses must be written, starting with the address corresponding to Ports 7-0 (i.e., starting with 200H for session number 0, through 11F8H for session number 511).

Multicast control cells have their own multicast session table for up to 31 sessions. Multicast control cells are only accepted by *CellBus* devices (depending on the state of the control multicast session table) and not replicated to multiple ports. These cells are sent to the Control Receive Queue for extraction to the host processor. The multicast session table memory contains 1 bit for each session.

LOOPBACK CELL TRANSMIT, RECEIVE, AND RELAY

The loopback function is provided for diagnostic purposes. It may be used on-line (ONLINE = 1), or off-line (ONLINE = 0). A loopback path for a cell from ASPEN Express X to ASPEN Express Y and back to ASPEN Express X can be set up by loading the LBADDR registers in addresses 013H and 014H of ASPEN Express Y with the single address control *CellBus* Routing Header of ASPEN Express X, as shown in Figure 15. The microprocessor then writes a cell with a single address loopback Routing Header for ASPEN Express Y into the control transmit buffer (Addresses 0A0H-0D7H) of ASPEN Express X and causes the cell to be sent. When ASPEN Express Y receives the cell it will use the contents of LBADDR to form a new Routing Header for the cell and send it back to ASPEN Express X. ASPEN Express X will receive the cell and place it in the control receive buffer where it can be examined by the microprocessor.

The above description assumes that the loopback cell originates in the control transmit buffer of ASPEN Express X, but it could also be received from the inlet port. Any of the six Routing Header formats shown in Figure 13 could actually be loaded in the LBADDRL/U registers of ASPEN Express Y instead of the single address control *CellBus* Routing Header of ASPEN Express X, with a corresponding change in the final destination of the loopback cell.



Note: - indicates don't care state

Figure 15. Loading the Loopback Registers

All aspects of system operation are the responsibility of the control system implemented for use of the ASPEN Express devices. Care must be taken to ensure that no more than one ASPEN Express is trying to set up a loopback into the same ASPEN Express, or mis-routing will ensue.

BOUNDARY SCAN

The IEEE 1149.1 Standard defines the requirements of a boundary scan architecture that has been specified by the IEEE Joint Test Action Group (JTAG). Boundary scan is a specialized scan architecture that provides absorbability and controllability for the interface leads of the device. The Test Access Port block, which implements the boundary scan functions, consists of a Test Access Port (TAP) controller, instruction and data registers, and a boundary scan register path bordering the input and output leads, as illustrated in Figure 16. The boundary scan test bus interface consists of four input signals (i.e., the Test Clock (TCK), Test Mode Select (TMS), Test Data Input (TDI) and Test Reset ($\overline{TRS}$) input signals) and a Test Data Output (TDO) output signal. A brief description of boundary scan operation is provided below; further information is available in the IEEE Standard document.

The TAP controller receives external control information via a Test Clock (TCK) signal, a Test Mode Select (TMS) signal, and a Test Reset ($\overline{TRS}$) signal, and it sends control signals to the internal scan paths. The scan path architecture consists of a 16-bit serial instruction register and two or more serial data registers. The instruction and data registers are connected in parallel between the serial Test Data Input (TDI) and Test Data Output (TDO) signals. The Test Data Input (TDI) signal is routed to both the instruction and data registers and is used to transfer serial data into a register during a scan operation. The Test Data Output (TDO) is selected to send data from either register during a scan operation. The timing of the boundary scan signals is shown in Figure 43.

When boundary scan testing is not being performed, the boundary scan register is transparent, allowing the input and output signals at the device leads to pass to and from the device's internal logic. During boundary scan testing, the boundary scan register disables the normal flow of input and output signals to allow the device to be controlled and observed via scan operations. Data is read out from internal test registers LSB first.

Boundary Scan Support

The following boundary scan test instructions are supported

- EXTEST
- SAMPLE/PRELOAD
- BYPASS
- IDCODE
- HIGHZ
- CLAMP

EXTEST Test Instruction:

One of the required boundary scan tests is the external boundary test (EXTEST) instruction. When this instruction is shifted in, the device is forced into an off-line test mode. While in this test mode, the test bus can shift data through the boundary scan registers to control the external input and output leads.

SAMPLE/PRELOAD Test Instruction:

When the SAMPLE/PRELOAD instruction is shifted in, the device remains fully operational. While in this test mode, input data, and data destined for device outputs, can be captured and shifted out for inspection. The data is captured in response to control signals sent to the TAP controller.

BYPASS Test Instruction:

When the BYPASS instruction is shifted in, the device remains fully operational. While in this test mode, a scan operation will transfer serial data from the TDI input, through an internal scan cell, to the TDO lead. The purpose of this instruction is to abbreviate the scan path through the circuits that are not being tested to only a single clock delay.

IDCODE Instruction

When the IDCODE instruction is shifted in, the device remains fully operational. The purpose of this instruction is to output the device ID code register on the TDO lead.

HIGHZ Instruction

The HIGHZ instruction is used to place all outputs in an inactive drive state (high impedance). In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring the risk of damage to the component.

CLAMP Instruction

The CLAMP instruction allows the state of the signals driven from the component leads to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. The signals driven from the component leads will not switch while the CLAMP instruction is selected.

BSDL File

A Boundary Scan Description Language (BSDL) file for the ASPEN Express device will be made available for download from the Products page of the TranSwitch Internet Web site at www.transwitch.com.

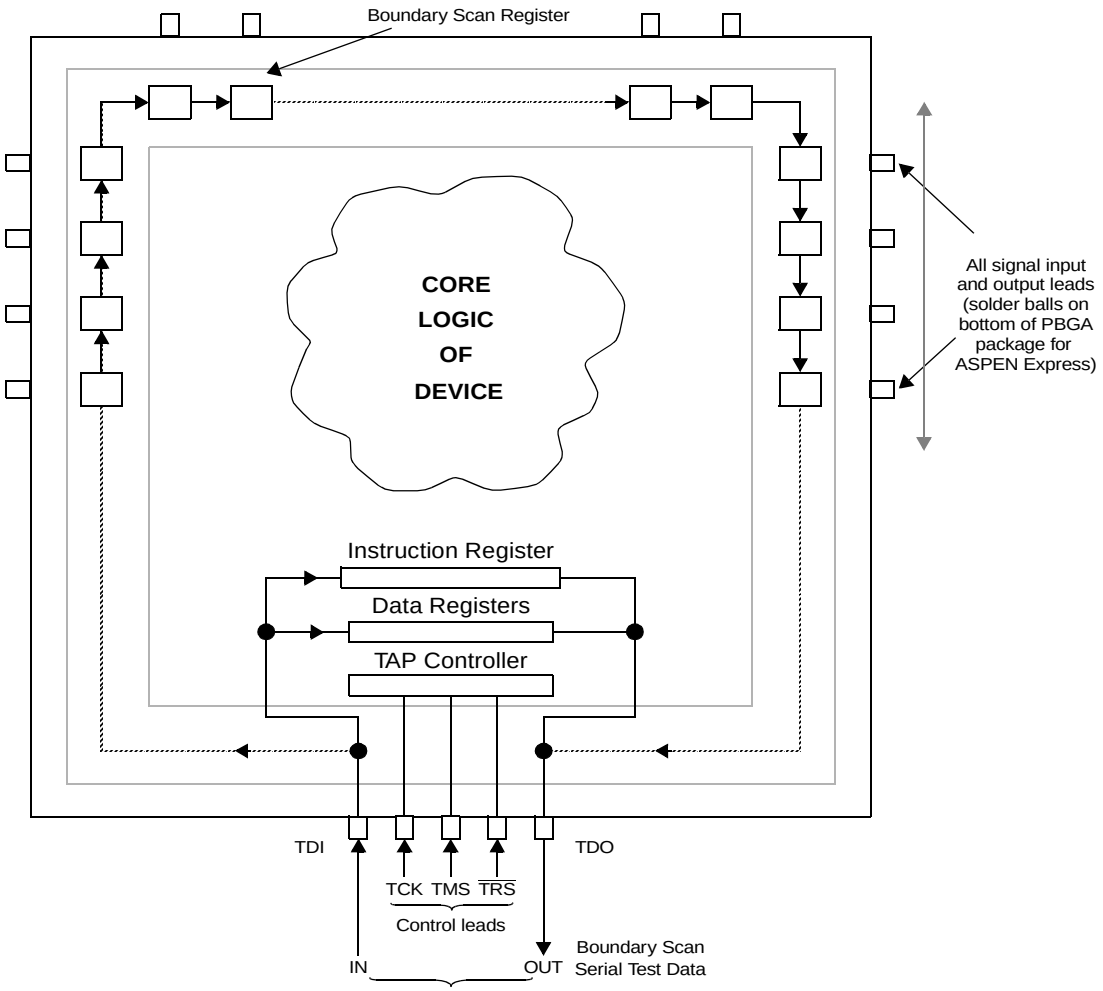


Figure 16. Boundary Scan Top-Level Block Diagram

PRODUCT PREVIEW

LEAD DESCRIPTIONS

POWER SUPPLY, GROUND LEADS

Symbol	Lead No.	Name/Function
VDD18	C3, C24, D4, D23, E7, E11, E17, E20, F5, F22, G5, G22, K5, K22, L5, L22, T5, T22, U5, U22, Y5, Y22, AA5, AA22, AB8, AB9, AB12, AB13, AB18, AB19	**V_{DD18}:** +1.8 volt ±5% CMOS core supply voltage.
VDD33	H5, H22, J5, J22, M5, N5, P22, R22, V5, V22, W5, W22, AB6, AB7, AB10, AB11, AB16, AB17, AB20, AB21	**V_{DD33}:** +3.3 volt ±5% CMOS input/output pad supply voltage.
Note: VDD18 and VDD33 Power Up Sequence Because of the multi-power ESD structure used for CMOS I/O cells, there is a parasitic forward diode path from core power rail (V_{DD18}) to I/O power rail (V_{DD33}). So, if V_{DD18} is powered up earlier than V_{DD33}, there will be current flowing through the parasitic diode that may trigger latch-up. To avoid this problem, users can take either one of the approaches below: **(1) Power Up VDD33 First** Turning on V_{DD33} first prevents the parasitic diode turning on. For example, power up V_{DD33} first and then V_{DD18}. Note that TXC does not recommend to power up V_{DD33} much earlier than V_{DD18} for reliability reasons. That is because the un-powered V_{DD18} may result in short circuit current (crowbar current) on the CMOS IO cell's post-driver for unknown state. Bus conflict may also occur when only V_{DD33} is powered on. The maximum interval that V_{DD18} must be powered up after V_{DD33} depends on the slew rate of power ramp-up in customer's application. **(2) Place a Schottky Diode Between VDD18 and VDD33** If we can ensure that the parasitic diode does not turn on, we can even power up lower voltage first. This can be done by inserting an external diode between V_{DD18} and V_{DD33} on the board. By connecting the Schottky diode with anode to lower voltage rail (V_{DD18}) and cathode to higher voltage rail (V_{DD33}), we can force the latter to ramp up with the former with the voltage drop (Schottky diode Vt=150mV~200mV) less than the threshold voltage of the parasitic diode (parasitic diode Vt=500mV~600mV). This prevent from turning on the parasitic diode between power rails, hence avoiding latch up. The external diode will be turned off when V_{DD33} is powered up to its normal voltage. This approach requires an additional device on system board, which could be a cost concern.		
VSS	A1, A26, E6, E8, E9, E10, E12, E13, E14, E15, E16, E18, E19, E21, K23, K24, K25, J24, L11, L12, L13, L14, L15, L16, M2, M11, M12, M13, M14, M15, M16, M22, N2, N4, N11, N12, N13, N14, N15, N16, N22, P5, P11, P12, P13, P14, P15, P16, R5, R11, R12, R13, R14, R15, R16, T11, T12, T13, T14, T15, T16, W4, AB14, AB15, AC4, AC23, AD3, AD24, AF1, AF26	**V_{SS}:** Ground, 0 volt reference.

Symbol	Lead No.	Name/Function
VDDBOOT_A	B6	**VDDBOOT_A:** +1.8V, ± 5%, supply voltage, which must be present for the *CellBus* A disable function to work. VDDBOOT_A is a diode isolated supply that is powered up before VDD18, VDD33 during hot insertion applications.
VDDBOOT_B	D17	**VDDBOOT_B:** +1.8V, ± 5%, supply voltage, which must be present for the *CellBus* B disable function to work. VDDBOOT_B is a diode isolated supply that is powered up before VDD18, VDD33 during hot insertion applications.
PLL_AVDD	AC22	**PLL Analog VDD:** Filtered 1.8 volts +/- 5% input for PLL block.
PLL_AVSS	AD23	**PLL Analog VSS:** Separate 0 volt reference input for PLL block.
PLL_DVDD	AE24	**PLL Digital VDD:** 1.8 volts +/- 5% input for PLL block.
PLL_DVSS	AF25	**PLL Digital VSS:** Input for PLL block.

* Note: I = Input; O = Output; T = Tristate

NO CONNECT AND SPARE LEADS

Symbol	Lead No.	I/O	Type	Name/Function
NC	A13, A14, B1, B2, B13, B14, B25, C26, D24, E23, AB5, AB22, AE2, AE25, AF2	--		**No Connect:** NC leads are not to be connected, not even to another NC lead, but must be left floating. Connection of NC leads may impair performance or cause damage to the device. Some NC leads may be assigned functions in future upgrades of the device. Backwards compatibility of the upgraded device in existing applications may rely upon these leads having been left floating.
XGNT	E4	I/O (T)	LVTTLpd/ CMOS 8mA	**SPARE 1:** Tie to V_{SS}.
XTDEN	AC26	I/O (T)	LVTTLpu/ CMOS 8mA	**SPARE 3:** Tie to V_{DD33}.

PRODUCT PREVIEW

UTOPIA INLET INTERFACE

Symbol**	Lead No.	I/O	Type*	Name/Function
UI_ADDR(4-0)	AC14, AF15, AD14, AE14, AF14	I/O (T)	LVTTL /CMOS 16mA	**UTOPIA Inlet Multi-PHY Address:** UTOPIA mode - Used for polling each port to determine the availability of cell space in PHY mode, and availability of a cell for transfer in ATM mode (Rx bus). Input in PHY emulation mode, output in ATM emulation mode (Tx bus).
UI_CLAV(3-0)	AE16, AF16, AD15, AE15	I/O (T)	LVTTL/ CMOS 16mA	**UTOPIA Inlet Cell/Packet Available:** Input in ATM mode, output in PHY mode. Active high signal indicating that space is available to receive a cell (PHY mode) or that a cell is available to be sent by the PHY device (ATM mode).
UI_CLKI	AF12	I	LVTTL	**UTOPIA Inlet Clock Input:** UTOPIA interface input clock. Inlet signals are used for Rx bus in ATM emulation and Tx bus in PHY emulation.
UI_CLKO	AF13	O (T)	CMOS 16mA	**UTOPIA Inlet Clock Output:** UTOPIA interface output clock. Outlet signals are used for Tx bus in ATM emulation and Rx bus in PHY emulation mode.
UI_D(15-0)	AF10, AE10, AC11, AD10, AF9, AE9, AD13, AC13, AE12, AD12, AF11, AE11, AC12, AD11, AF8, AC10	I	LVTTL	**UTOPIA Inlet Data:** Input data bus.
$\overline{\text{UI\_ENB(3-0)}}$	AE17, AF17, AD16, AC15	I/O (T)	LVTTL/ CMOS 16mA	**UTOPIA Inlet Enable:** Input in PHY mode, output in ATM mode. Active low read enable signal for cell transfer in ATM mode. Active low write enable in PHY mode.
UI_SOC	AE13	I	LVTTL	**UTOPIA InletStart of Cell:** **UTOPIA mode** - Start of Cell indicator.
UI_PARITY	AF18	I	LVTTL	**UTOPIA Inlet Parity:** Parity over UI_D(15-0), 8 or 16 bits are considered depending on the configuration.

* See Input, Output and Input/Output Parameters section for Type definitions.

** Signals which are active when low or upon their falling edges are shown as negated (overlined).

PRODUCT PREVIEW

UTOPIA OUTLET INTERFACE

Symbol	Lead No.	I/O	Type	Name/Function
UO_ADDR(4-0)	AF19, AE18, AF24, AD17, AC16	I/O (T)	LVTTL/ CMOS 16mA	**UTOPIA Outlet Multi-PHY Address:** Used for polling each port to determine the availability of a cell in PHY mode, and availability of a cell space for transfer in ATM mode. Input in PHY emulation mode (on Tx bus), output in ATM emulation mode.(on Tx bus).
UO_CLAV(3-0)	AC18, AE19, AD18, AC17	I/O (T)	LVTTL/ CMOS 16mA	**UTOPIA Outlet Cell Available:** Input in ATM mode, output in PHY mode. Active high signal indicating a cell space is available in the external PHY device to receive a cell when in ATM mode. In PHY mode it indicates that a cell is available to be sent to the ATM device.
UO_CLKI	AF20	I	LVTTL	**UTOPIA Outlet Clock Input:** UTOPIA interface input clock
UO_CLKO	AF21	O (T)	CMOS 16mA	**UTOPIA Outlet Clock Output:** UTOPIA interface output clock
UO_D(15-0)	AC24, AD22, AE22, AF23, AD21, Y23, AA24, AB25, AA23, AB24, AC25, AD26, AD25, AB23, AF22, AE21	O (T)	CMOS 16mA	**UTOPIA Outlet Data:** Output data bus. This is the Transmit bus in ATM emulation mode or the Rx bus in PHY emulation mode.
$\overline{\text{UO\_ENB(3-0)}}$	AC19, AD20, AE20, AD19	I/O (T)	LVTTL/ CMOS 16mA	**UTOPIA Outlet Enable:** Input in PHY mode, output in ATM mode. Active low read enable signal for cell output. One clav/enable pair for every 16 PHYs.
UO_SOC	AC20	O (T)	CMOS 16mA	**UTOPIA Outlet Start of Cell:** Start of Cell indicator.
UO_PARITY	AB26	O (T)	CMOS 16mA	**UTOPIA Outlet Parity: Odd** Parity over UI_D(15-0), 8 or 16 bits are considered depending on mode configured.
UO_STBY1	AC3	I/O	LVTTLpd /CMOS 8mA	**UTOPIA Outlet Standby:** Setting this lead high will tri-state the UTOPIA output bus and halt transmission.

PRODUCT PREVIEW

CellBus BUS PORT A

Symbol	Lead No.	I/O	Type	Name/Function
$\overline{\text{CBA\_ACK}}$	A10	I/O (T)	GTL+	***CellBus* A Acknowledge:** Active low acknowledge for each cell received on *CellBus* A.
$\overline{\text{CBA\_CONG}}$	C13	I/O (T)	GTL+	***CellBus* A Congestion:** Active low congestion indicator set by receiving device for *CellBus* A
$\overline{\text{CBA\_D(31-24)}}$	A3, C4, D7, C5, D5, A4, E5, B7	I/O (T)	GTL+	***CellBus* A Data:** Active low 32-bit parallel data input/output bus for *CellBus* A.
$\overline{\text{CBA\_D(23-16)}}$	D8, B3, D9, A6, A5, B4, C9, C6	I/O (T)	GTL+	
$\overline{\text{CBA\_D(15-8)}}$	D6, B9, A8, C7, B10, C10, D10, C8	I/O (T)	GTL+	
$\overline{\text{CBA\_D(7-0)}}$	D12, C11, D11, A9, D13, C12, B11, B12	I/O (T)	GTL+	
$\overline{\text{CBA\_F}}$	A11	I/O (T)	GTL+	***CellBus* A Frame Pulse:** Active low pulse that occurs once for every 16 or 32 *CellBus* A clock cycles, corresponding to selection of 16-user or 32-user modes. See U32 lead
$\overline{\text{CBA\_RC}}$	A2	I	GTL+	***CellBus* A Read Clock:** Used to clock in data from A bus. Falling edge used for data transfer. (The max operational frequency of the *CellBus* clock on the backplane is dependent on the *CellBus* backplane characteristics.)
$\overline{\text{CBA\_WC}}$	B5	I	GTL+	***CellBus* A Write Clock:** Used to drive data on the A bus. Falling edge used for data transfer. (The max operational frequency of the *CellBus* clock on the backplane is dependent on the *CellBus* backplane characteristics.)
$\overline{\text{CBA\_DISABLE}}$	A12	I	CMOS1.8	***CellBus* A Disable:** Active low. Force all *CellBus* A outputs of the device to tri-state ("off"), independent of the V_{DD18} and V_{DD33} power supplies. However, VDDBOOT_A input must be present. (CBA_DISABLE and VDDBOOT_A signals are part of the ASPEN Express hot-insertion capability.)

Symbol	Lead No.	I/O	Type	Name/Function
CBA_VREF	B8	I	Reference Voltage	**CBA_VREF:** Reference voltage for GTL+ receivers on *CellBus* A. CBA_VREF is 2/3 V_{tt} +/– 2%, where Vtt is the backplane termination voltage (nominally Vtt = +1.5V). (This signal is not part of the *CellBus* backplane.)
CBA_REXT	A7	I	External Resistor	***CellBus* A External Resistor:** CBA_REXT is to be connected to VSS via an external 1.0k ohm +/- 1% resistor, and is used for GTL+ temperature compensation. This signal is not part of the *CellBus* A backplane.

***CellBus* PORT B**

Symbol	Lead No.	I/O	Type	Name/Function
$\overline{\text{CBB\_ACK}}$	A24	I/O (T)	GTL+	***CellBus* B Acknowledge:** Active low acknowledge for each cell received on *CellBus* B.
$\overline{\text{CBB\_CONG}}$	B24	I/O (T)	GTL+	***CellBus* B Congestion:** Active low congestion indicator set by receiving device for *CellBus* B.
$\overline{\text{CBB\_D(31-24)}}$	C14, A15, B15, B16, D15, A17, A16, C16	I/O (T)	GTL+	***CellBus* B Data:** Active low 32-bit parallel data input/output bus for *CellBus* B.
$\overline{\text{CBB\_D(23-16)}}$	B17, C17, D16, B18, A18, A19, B19, C18	I/O (T)	GTL+	
$\overline{\text{CBB\_D(15-8)}}$	D19, C19, B20, C20, D20, C21, A21, B21	I/O (T)	GTL+	
$\overline{\text{CBB\_D(7-0)}}$	B23, D22, A22, B22, C23, D21, A23, E22	I/O (T)	GTL+	
$\overline{\text{CBB\_F}}$	C22	I/O (T)	GTL+	***CellBus* B Frame Pulse:** Active low pulse that occurs once for every 16 or 32 *CellBus* B clock cycles, corresponding to selection of 16-user or 32-user modes. See U32 lead.

PRODUCT PREVIEW

PRODUCT PREVIEW

Symbol	Lead No.	I/O	Type	Name/Function
$\overline{\text{CBB\_RC}}$	C15	I	GTL+	***CellBus* B Read Clock:** Used to clock in data from B bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 50 MHz. (The max operational frequency of the *CellBus* clock on the backplane is dependent on the *CellBus* backplane characteristics.)
$\overline{\text{CBB\_WC}}$	D14	I	GTL+	***CellBus* B Write Clock:** Used to drive data on the B bus. Falling edge used for data transfer. The maximum frequency of the read and write clocks is 50 MHz. (The max operational frequency of the *CellBus* clock on the backplane is dependent on the *CellBus* backplane characteristics.)
$\overline{\text{CBB\_DISABLE}}$	A25	I	CMOS1.8	***CellBus* B Disable:** Active low. Force all *CellBus* B outputs of the device to tri-state ("off"), independent of the V_{DD18} and V_{DD33} power supplies. However, VDDBOOT_B input must be present. (CBB_DISABLE and VDDBOOT_B signals are part of the ASPEN Express hot-insertion capability.)
CBB_VREF	D18	I	Reference Voltage	**CBB_VREF:** Reference voltage for GTL+ receivers on *CellBus* B. CBB_VREF is 2/3 V_{tt} +/– 2%, where V_{tt} is the backplane termination voltage (nominally Vtt = +1.5V). (This signal is not part of the *CellBus* backplane.)
CBB_REXT	A20	I	External Resistor	***CellBus* B External Resistor:** CBB_REXT is to be connected to VSS via an external 1.0k ohm +/- 1% resistor, and is used for GTL+ temperature compensation. This signal is not part of the *CellBus* B backplane.

EXTERNAL CONTROL SDRAM INTERFACE

Symbol	Lead No.	I/O	Type	Name/Function
DR1_DQ(31-24)	F2, H3, H2, J2, L4, M4, R2, P2	I/O (T)	LVTTL/ CMOS 8mA	**Control SDRAM Data:** Bidirectional 32-bit data bus used for reading input and writing output data from/to the external SDRAM.
DR1_DQ(23-16)	Y2, M3, L3, J1, K4, G1, H4, G4			
DR1_DQ(15-8)	E1, F1, J4, H1, K2, L2, W3, P1			
DR1_DQ(7-0)	N3, L1, K1, K3, J3, G2, G3, E2			
DR1_A(12-0)	R4, T3, U2, T4, V1, V2, W1, W2, Y1, V4, V3, U4, U3	O (T)	CMOS 8mA	**Control SDRAM Address:** 13-bit row/col address output bus used to select external SDRAM address for read or write access.
DR1_BA(1-0)	U1, T2	O (T)	CMOS 8mA	**Control SDRAM Bank Address:** 2-bit address used to select SDRAM bank.
$\overline{\text{DR1\_CAS}}$	R1	O (T)	CMOS 8mA	**Cell Buffer SDRAM Column Address Strobe:** Active low.
DR1_CLKO	N1	O (T)	CMOS 12mA	**Control SDRAM Clock Output:** Clock output for external Control SDRAM interface.
DR1_CLKI	M1	I	LVTTL	**Control SDRAM Clock Input:** Clock input for external SDRAM interface read. This clock input must be directly connected to clock output DR1_CLKO.
$\overline{\text{DR1\_CS}}$	T1	O (T)	CMOS 8 mA	**Control SDRAM Chip Select:** Active low. Chip select output for external SDRAM interface
DR1_DQM	P3	O (T)	CMOS 8mA	**Control SDRAM DQ Mask:** Active high. DR2. Controls the data output buffers in read mode. In write mode it masks the data from being written to the memory array.
$\overline{\text{DR1\_RAS}}$	R3	O (T)	CMOS 8mA	**Control SDRAM Row Address Strobe:** Active low.
$\overline{\text{DR1\_WE}}$	P4	O (T)	CMOS 8mA	**Control SDRAM Write Enable:** Active low.

PRODUCT PREVIEW

EXTERNAL CELL BUFFER SDRAM INTERFACE

Symbol	Lead No.	I/O	Type	Name/Function
DR2_DQ(31-24)	E25, F25, G25, H25, L23, M23, M26, N26	I/O (T)	LVTTL/ CMOS 8mA	**Cell Buffer SDRAM Data:** Bidirectional 32-bit data bus used for reading input and writing output Cell Buffer data from/to the external SDRAM.
DR2_DQ(23-16)	N24, M24, L24, J25, J23, F26, E26, D26			
DR2_DQ(15-8)	F23, G23, H23, G26, C25, L25, M25, N25			
DR2_DQ(7-0)	N23, L26, K26, D25, H24, G24, F24, E24			
DR2_A(12-0)	R25, T26, T24, T25, U26, U25, U24, U23, W25, W26, V25, V26, T23	O (T)	CMOS 8mA	**Cell Buffer SDRAM Address:** 13-bit row/col address output bus used to select external SDRAM address for read or write access.
DR2_BA(1-0)	R23, R24	O (T)	CMOS 8mA	**Cell Buffer SDRAM Bank Address:** 2-bit address used to select SDRAM bank.
$\overline{\text{DR2\_CAS}}$	P24	O (T)	CMOS 8mA	**Cell Buffer SDRAM Column Address Strobe:** Active low.
DR2_CLKO	J26	O (T)	CMOS 12mA	**Cell Buffer SDRAM Clock Output:** Clock output for external CELL Buffer SDRAM interface.
DR2_CLKI	H26	I	LVTTL	**Cell Buffer SDRAM Clock Input:** Clock input for external Cell Buffer SDRAM interface read. This clock input must be directly connected to clock output DR2_CLKO.
$\overline{\text{DR2\_CS}}$	R26	O (T)	CMOS 8mA	**Cell Buffer SDRAM Chip Select:** Active low. Chip select output for external SDRAM interface
DR2_DQM	P25	O (T)	CMOS 8mA	**Cell Buffer SDRAM DQ Mask:** Active high. Controls the data output buffers in read mode. In write mode it masks the data from being written to the memory array.
$\overline{\text{DR2\_RAS}}$	P23	O (T)	CMOS 8mA	**Cell Buffer SDRAM Row Address Strobe:** Active low.
$\overline{\text{DR2\_WE}}$	P26	O (T)	CMOS 8mA	**Cell Buffer SDRAM Write Enable:** Active low.

PRODUCT PREVIEW

MICROPROCESSOR PORT

Symbol	Lead No.	I/O	Type	Name/Function
UP_A(7-0)	AB3 AC1, AA4, AA3, AB2, Y4, AB1, AA2	I	LVTTL	**Microprocessor Address:** 8-bit address lines from microprocessor. UP_A0 is LSB.
UP_D(15-8)	AC7, AD6, AE5, AF4, AC6, AD5, AF3, AE4	I/O (T)	LVTTL/ CMOS 8mA	**Microprocessor Data:** Bidirectional 16-bit data lines used for transferring data to and from microprocessor. UP_D0 is LSB. Bit 15 is the MSB.
UP_D(7-0)	AC5, AD4, AE3, AE1 AB4, AD2, AD1, AC2			
UP_INTR	AE8	O (T)	CMOS 8mA	**Microprocessor Interrupt:** Active high for Intel, active low for Motorola and MPC860 modes.
UP_MODE_(1-0)	AC8, AE6	I	LVTTL	**Microprocessor Mode:** 00=Intel, 01=Motorola, 10=MPC860, 11=reserved
UP_CLK	AF5	I	LVTTL	**Microprocessor Chip Clock:** Clock output from MPC860. Tie to '0' for other modes.
UP_RDWR	AD7	I	LVTTL	**Microprocessor Read/Write:** Indicate the direction of data transfer. In MPC860 or Motorola Modes, UPRDWR = 1, Read UPRDWR = 0, Write. In Intel Mode, is an Active Low read command.
UP_ACK	AF7	O (T)	CMOS 8mA	**Microprocessor Acknowledge:** Indicates normal completion of the bus transfer. 1) In MPC860 mode, active low, corresponds to TA. This output requires an external pull-up resistor. Note: Device asserts this high before tri-stating to improve acknowledge timing. 2) In Motorola mode, active low, corresponds to DTACK. This output requires an external pull-up resistor. 3) In Intel Mode, active high, corresponds to RDY. This output requires an external pull-down resistor.
$\overline{\text{UP\_SEL}}$	AE7	I	LVTTL	**Microprocessor Chip Select:** Chip select lead for Microprocessor interface.
$\overline{\text{UP\_WR}}$	AC9	I	LVTTL	**Microprocessor Write:** Active low. Only valid in Intel Mode. Must be 1 in Motorola and MPC860 Modes.
$\overline{\text{UP\_RST}}$	AF6	I	LVTTL	**Microprocessor Reset:** Active low. Reset from micro.

Symbol	Lead No.	I/O	Type	Name/Function
$\overline{\text{UP\_TS}}$	AD8	I	LVTTL	**Microprocessor Transfer Start:** Only used in MPC860 Mode. Asserted by CPU to indicate the start of a bus cycle that transfer data to/from slave device. Connected to MPC860 TS signal. The transfer start (signal $\overline{\text{UP\_TS}}$) indicates the beginning of a transaction on the bus addressing a slave device. $\overline{\text{UP\_TS}}$ is asserted only for the first cycle of the transaction and is negated in the successive clock cycles until the end of the transaction. An external pull-up resistor should be connected to $\overline{\text{UP\_TS}}$.

CONTROL STRAPS

Symbol	Lead No.	I/O	Type	Name/Function
DEVHIZ	AA25	I	LVTTLpd	**Device High Impedance:** Active high to set all outputs (except TDO) to high-impedance. Tie to V_{SS}.
$\overline{\text{ENARBA}}$	D3	I	LVTTLpd	**Enable Arbiter *CellBus* A:** Active low signal to enable local *CellBus* Arbiter and Frame Pulse Generator in this device for *CellBus* A.
$\overline{\text{ENARBB}}$	B26	I	LVTTLpd	**Enable Arbiter *CellBus* B:** Active low signal to enable local *CellBus* Arbiter and Frame Pulse Generator for *CellBus* B.
UA_Flip	F3	I	LVTTLpd	**Unit Address Flip:** 0 = the *CellBus* receive address is the inversion of $\overline{\text{UA}}$, 1 = the receive address is the inversion of $\overline{\text{UA(4-1)}}$ and the LSB is not used.
$\overline{\text{UA(4-0)}}$	C2, C1, D2, E3, F4	I	LVTTLpd	**Unit Address *CellBus*:** Five active low device identity straps, used to identify this *CellBus* device in a system containing up to 32 devices (binary numbers from 0 to 31, $\overline{\text{UA4}}$ is MSB). This address is latched on powerup for both *CellBuses* but may be changed by a host command.
U32	D1	I	LVTTLpd	**User 32 *CellBus*:** Control strap for setting maximum number of ASPEN Express's that can be connected to a *CellBus*. 0 = 16 users, 1 = 32 users

Symbol	Lead No.	I/O	Type	Name/Function
ICSA	AA1	I	LVTTLpu	**Internal Clock Select:** Set to agree with external PLL reference clock frequency as follows:
ICSB	Y3	I	LVTTLpu	

PLLREF	ICSA	ICSB	Mult
50 MHz	1	1	2
33 1/3 MHz	1	0	3
33 1/3 MHz	0	1	3
25MHz	0	0	4

RESET AND TEST LEADS (INCLUDING TEST ACCESS PORT FOR BOUNDARY SCAN)

Symbol	Lead No.	I/O	Type	Name/Function
TDO	Y24	O (T)	CMOS 8 mA	**Test Data Output:** Boundary scan output for data and test instructions from internal test registers.
$\overline{TRS}$	V23	I	LVTTLpu	**Test Mode Reset:** A 1 microsecond (minimum) low on this lead resets the boundary scan; recommended for use after power-up initialization as well.
TMS	Y26	I	LVTTLpu	**Test Mode Select:** Boundary scan test mode select.
TDI	W24	I	LVTTLpu	**Test Data Input:** Boundary scan input for data and test instructions.
TCK	Y25	I	LVTTLpu	**Test Clock:** Boundary scan clock. Input signals are clocked in on its rising edge.
$\overline{RST}$	AA26	I	LVTLLpu	**Hardware Reset:** An active low pulse with minimum width of 300 ns which must be applied after power-up to reset all registers, counters, and FIFOs. The reset is asynchronous going into the reset state, but requires all external clocks to be active and stable during the reset state.
TSTMODE	V24	I	LVTTLpd	**Test Mode:** Active high to enable device test. Tie to V_{SS}.
SCAN	W23	I	LVTTLpd	**SCAN Test:** Active high to enable device internal scan test. Tie to V_{SS}.
PLLBYP	AC21	I	LVTTLpd	**Processor Clock Bypass:** Used to bypass internal PLL during production testing when PL_BYP = 1. Must be tied to V_{SS} for customer applications.
PLLREF	AE23	I	LVTTL	**Processor Clock:** PLL clock reference having 45% min/55% max duty cycle. Internally, speed is multiplied in a PLL to generate the system clock. PLLREF Frequency can be either 25 MHz, 33.33 MHz, or 50 MHz. See ICSA/ICSB leads.

PRODUCT PREVIEW

Symbol	Lead No.	I/O	Type	Name/Function
IDDTEST	AE26	I	LVTTLpd	**IDD Test:** Active high to enable device internal idd test. Tie to V_{SS}.
LCLK	AD9	I	LVTTL	**Local UTOPIA Clock:** This is a clock that can be selected for UTOPIA interfaces when in ATM emulation mode. The maximum clock frequency is 50 MHz 45% min/55% max duty cycle.

ABSOLUTE MAXIMUM RATINGS AND ENVIRONMENTAL LIMITATIONS

Parameter	Symbol	Min	Max	Unit	Conditions
Supply voltage (CMOS I/O)	V_{DD33}	-0.3	+3.9	V	Note 1, 4
Supply voltage (Core)	V_{DD18}	-0.3	+2.1	V	Note 1, 4
DC input voltage	V_{IN}	-0.5	5.5	V	Note 1, 4
Storage temperature range	T_S	-55	150	^oC	Note 1
Ambient operating temperature	T_A	-40	85	^oC	0 ft/min linear airflow
Moisture Exposure Level	ME	5		Level	per EIA/JEDEC JESD22-A112-A
Relative Humidity, during assembly	RH	30	60	%	Note 2
Relative Humidity, in-circuit	RH	0	100	%	non-condensing
ESD Classification	ESD	Absolute value 2000		V	Note 3
Latch-up	LU				Meets JEDEC STD-78

Notes:

1. Operating conditions outside the min-max ranges specified may cause permanent device failure. Exposure to conditions near the min or max limits for extended periods may impair device reliability.
2. Pre-assembly storage in non-drypack conditions is not recommended. Please refer to the instructions on the "CAUTION" label on the drypack bag in which devices are supplied.
3. Test method for ESD per MIL-STD-883D, method 3015.7.
4. Device core is 1.8V only.

THERMAL CHARACTERISTICS

Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal resistance - junction to ambient		20		$^oC/W$	0 ft/min linear airflow

POWER REQUIREMENTS

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD33}	3.15	3.3	3.45	V	
I_{DD33}		230		mA	See Notes 1,2 and 3
P_{DD33}		759		mW	See Notes 1,2 and 3
V_{DD18}	1.71	1.8	1.89	V	
I_{DD18}		400		mA	See Notes 1,2 and 3
P_{DD18}		720		mW	See Notes 1,2 and 3
$V_{DDBOOT\ A,\ B}$	1.71	1.8	1.89	V	See Notes 1 and 2
$I_{DDBOOT\ A,\ B}$		0.10		mA	See Notes 1 and 2
Total Power		1479		mW	See Notes 1 and 2

Notes:

1. Typical values estimated with nominal voltages at 25° C
2. All I_{DD} and P_{DD} values are dependent upon V_{DD}.
3. Conditions: UTOPIA = 50 MHz, *CellBus* = 40 MHz, internal system clock = 100 MHz.

INPUT, OUTPUT AND INPUT/OUTPUT PARAMETERS

Input Parameters For CMOS1.8

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	1.26			V	$1.71 \leq V_{DD18} \leq 1.89$ $1.71 \leq$ VddbootA,B ≤ 1.89
V_{IL}			0.36	V	$1.71 \leq V_{DD18} \leq 1.89$ $1.71 \leq$ VddbootA,B ≤ 1.89
Input leakage current	-10		10	µA	$V_{IN} = V_{DD18}$ or V_{SS}
Input capacitance		5		pF	

Input Parameters For LVTTL

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$ or V_{SS}
Input capacitance		5		pF	

Input Parameters For LVTTLpu (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{IN} = V_{DD33}$
Input capacitance		5		pF	

Input Parameters For LVTTLpd (internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	28		85	µA	$V_{IN} = V_{DD33}$
Input leakage current	-10		10	µA	$V_{IN} = V_{SS}$
Input capacitance		5		pF	

Output Parameters For CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -8 mA
V_{OL}			0.4	V	I_{OL} = 8 mA
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	
Leakage Tristate	-10		10	µA	

Output Parameters For CMOS 12mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -12 mA
V_{OL}		0.2	0.4	V	I_{OL} = 12 mA
I_{OL}			12.0	mA	
I_{OH}			-12.0	mA	
Leakage Tristate	-10		10	µA	

Output Parameters For CMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{OH}	2.4			V	I_{OH} = -16 mA
V_{OL}		0.2	0.4	V	I_{OL} = 16 mA
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	
Leakage Tristate	-10		10	µA	

Input/Output Parameters For GTL+

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	V_{REF}+0.05			V	
V_{IL}			V_{REF}-0.05	V	
Input leakage current	-10		10	µA	
GTL+ lead capacitance		5		pF	
V_{OL}			0.5	V	I_{OL} = 50 mA
V_{OL}			0.3	V	I_{OL} = 36 mA
I_{OL}			50	mA	Loaded with 21 Ω to +1.5 V

PRODUCT PREVIEW

Input/Output Parameters For LVTTL/CMOS 8mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14; I_{OH = -8 mA}$
V_{OL}			0.4	V	$V_{DD33}= 3.14; I_{OL = 8 mA}$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

Input/Output Parameters For LVTTLpu/CMOS 8mA (internal pull-up resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	-90		-25	µA	$V_{IN} = V_{SS}$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14; I_{OH = -8 mA}$
V_{OL}			0.4	V	$V_{DD33}= 3.14; I_{OL = 8 mA}$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

Input/Output Parameters For LVTTLpd/CMOS 8mA (internal pull-down resistor)

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input current	28		85	µA	$V_{IN} = V_{DD33}$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14; I_{OH = -8 mA}$
V_{OL}			0.4	V	$V_{DD33}= 3.14; I_{OL = 8 mA}$
I_{OL}			8.0	mA	
I_{OH}			-8.0	mA	

Input/Output Parameters For LVTTL/CMOS 12mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14; I_{OH = -12 mA}$
V_{OL}			0.4	V	$V_{DD33}= 3.14; I_{OL = 12 mA}$
I_{OL}			12.0	mA	
I_{OH}			-12.0	mA	

Input/Output Parameters For LVTTL/CMOS 16mA

Parameter	Min	Typ	Max	Unit	Test Conditions
V_{IH}	2.0			V	$3.14 \leq V_{DD33} \leq 3.46$
V_{IL}			0.8	V	$3.14 \leq V_{DD33} \leq 3.46$
Input leakage current	-10		10	µA	$V_{DD33} = 3.46$
Input capacitance		5		pF	
V_{OH}	2.4			V	$V_{DD33}= 3.14; I_{OH = -16 mA}$
V_{OL}			0.4	V	$V_{DD33}= 3.14; I_{OL = 16 mA}$
I_{OL}			16.0	mA	
I_{OH}			-16.0	mA	

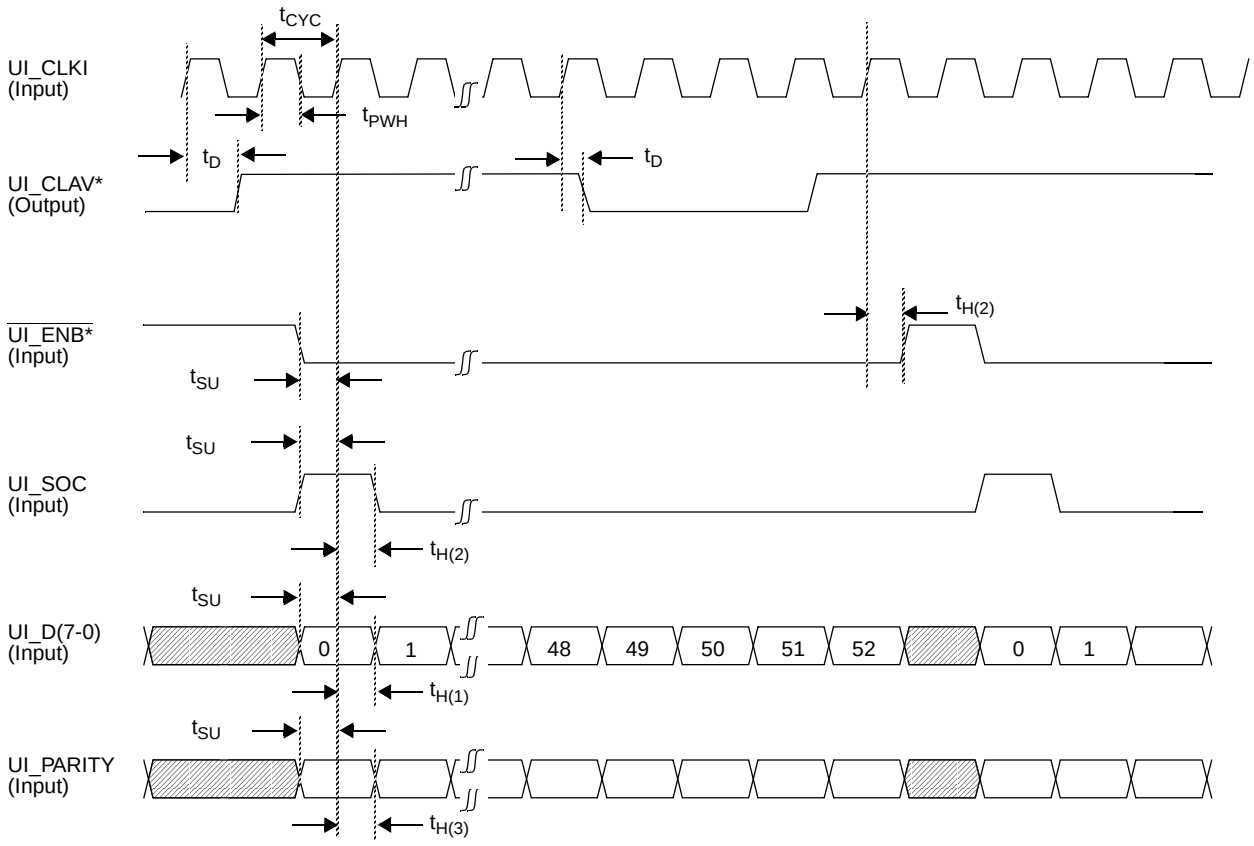
PRODUCT PREVIEW

PRODUCT PREVIEW

TIMING CHARACTERISTICS

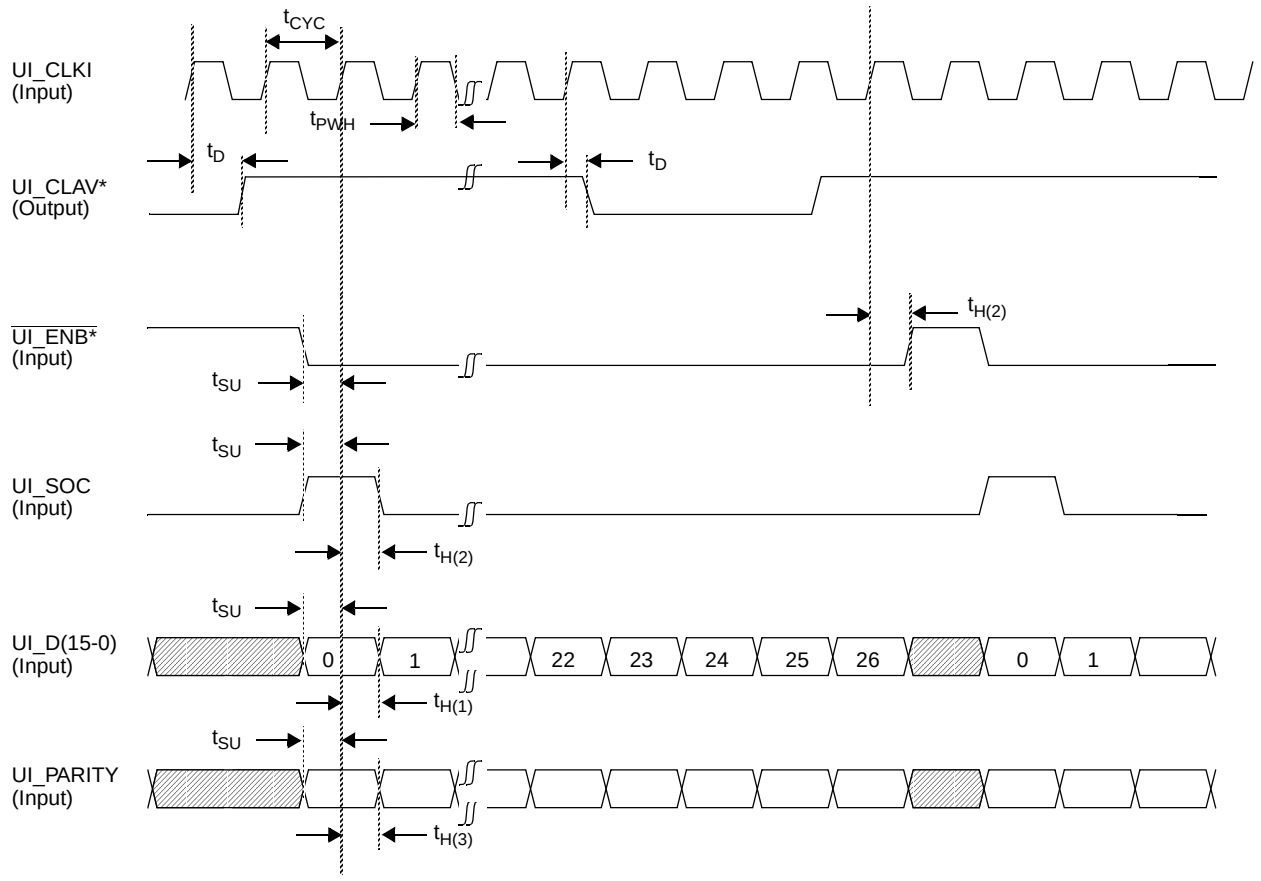
Detailed timing diagrams for the ASPEN Express device are provided in Figures 17 through 43, with values for the timing intervals given in tables below the waveform drawings. All output times are measured with a maximum 25 pF load capacitance, unless noted otherwise. Timing parameters are measured at voltage levels of $(V_{IH}+V_{IL})/2$ and $(V_{OH}+V_{OL})/2$, for input and output signals, respectively.

Figure 17. Timing of Receive Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(7-0), UI_SOC, $\overline{\text{UI\_ENB*}}$ setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(7-0) hold time after UI_CLKI↑	$t_{H(1)}$	1.0			ns
UI_SOC, $\overline{\text{UI\_ENB*}}$ hold time after UI_CLKI↑	$t_{H(2)}$	1.0			ns
UI_CLAV* delay from UI_CLKI↑	t_D	2.0		10.0	ns
UI_SOC, UI_PARITY hold time after UI_CLK↑	$t_{H(3)}$	2.0			ns

Figure 18. Timing of Receive Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 16-bit)

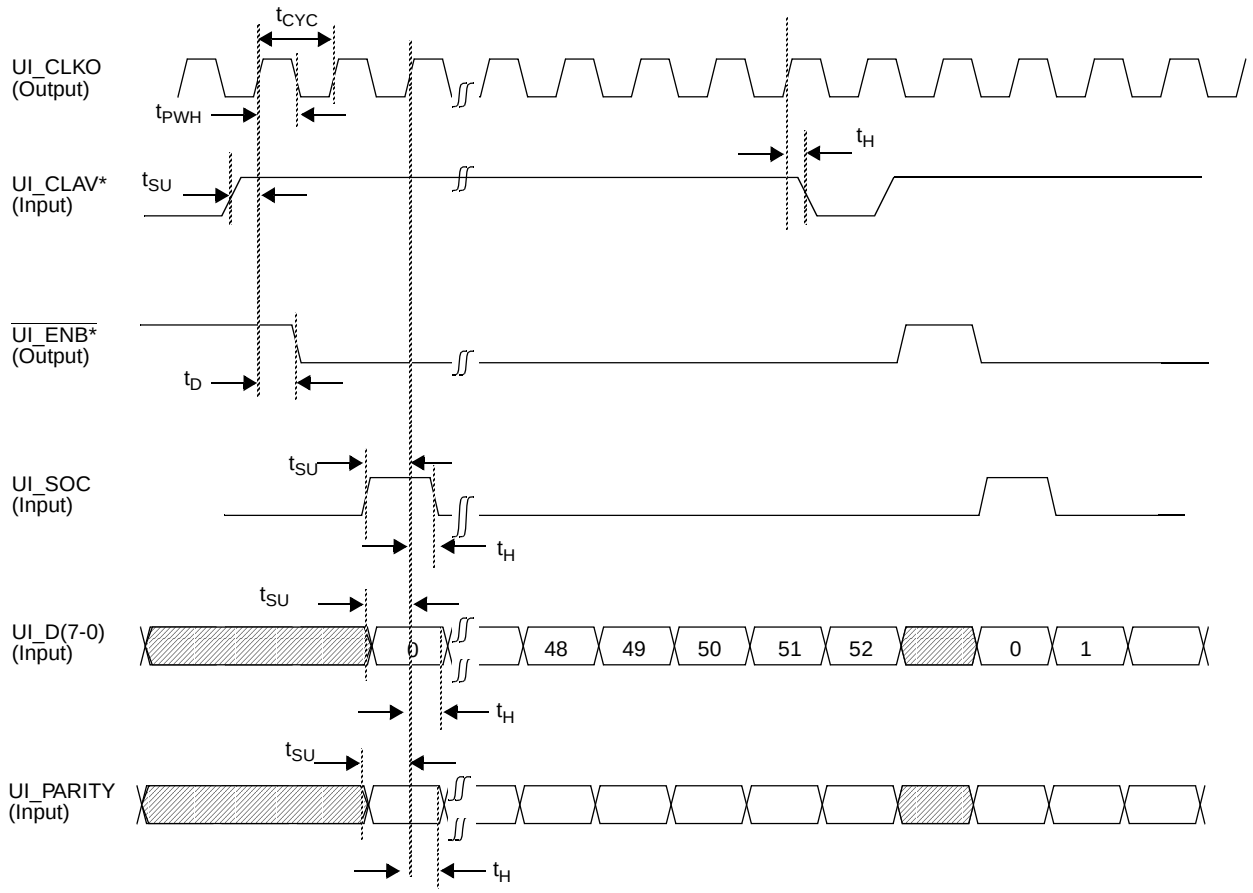


Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(15-0), UI_SOC, $\overline{\text{UI\_ENB*}}$ setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(15-0) hold time after UI_CLKI↑	$t_{H(1)}$	1.0			ns
UI_SOC, $\overline{\text{UI\_ENB*}}$ hold time after UI_CLKI↑	$t_{H(2)}$	1.0			ns
UI_CLAV* delay from UI_CLKI↑	t_D	2.0		10.0	ns
UI_SOC, UI_PARITY hold time after UI_CLK↑	$t_{H(3)}$	2.0			ns

PRODUCT PREVIEW

PRODUCT PREVIEW

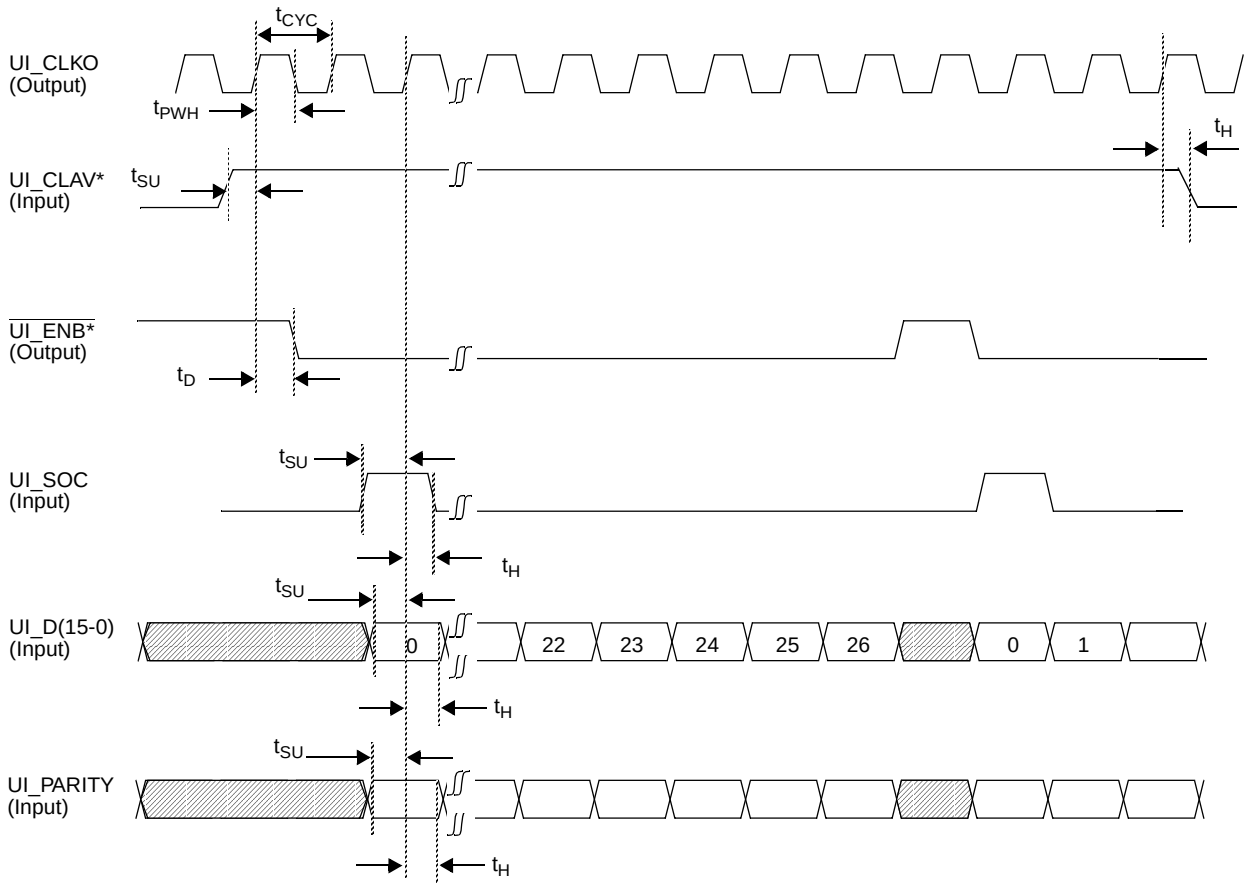
Figure 19. Timing of Receive Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKO clock period	t_{CYC}	20			ns
UI_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D (7-0), UI_SOC, UI_CLAV* setup time to UI_CLKO↑	t_{SU}	4.0			ns
UI_D (7-0), UI_SOC, UI_CLAV*, UI_PARITY hold time after UI_CLKO↑	t_H	1.0			ns
$\overline{\text{UI\_ENB*}}$ delay from UI_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for Ingress and Egress UTOPIA interfaces.

Figure 20. Timing of Receive Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 16-bit)



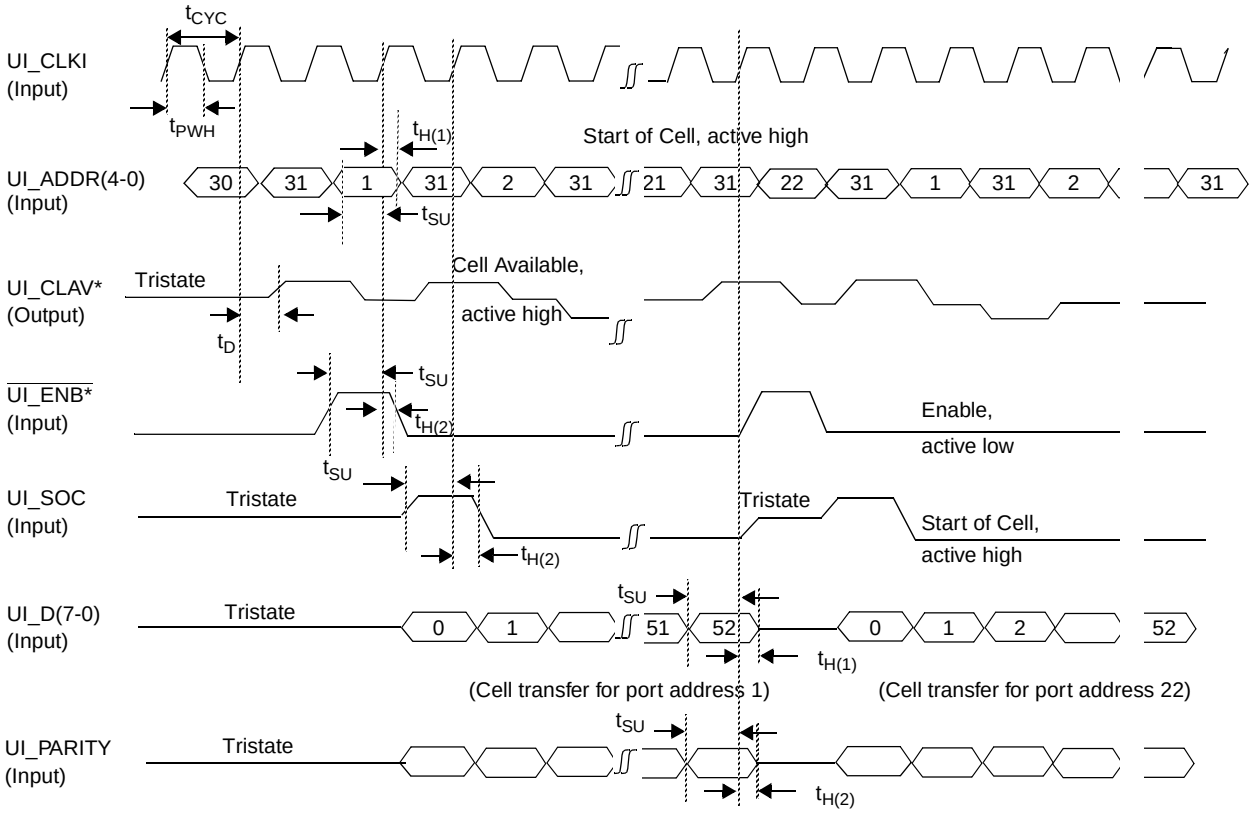
Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKO clock period	t_{CYC}	20			ns
UI_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(15-0), UI_SOC, UI_CLAV* setup time to UI_CLKO↑	t_{SU}	4.0			ns
UI_D(15-0), UI_SOC, UI_CLAV*, UI_PARITY hold time after UI_CLKO↑	t_H	1.0			ns
$\overline{\text{UI\_ENB*}}$ delay from UI_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: LCLK is selected by software, LCLK is used for Ingress and Egress UTOPIA interfaces.

PRODUCT PREVIEW

PRODUCT PREVIEW

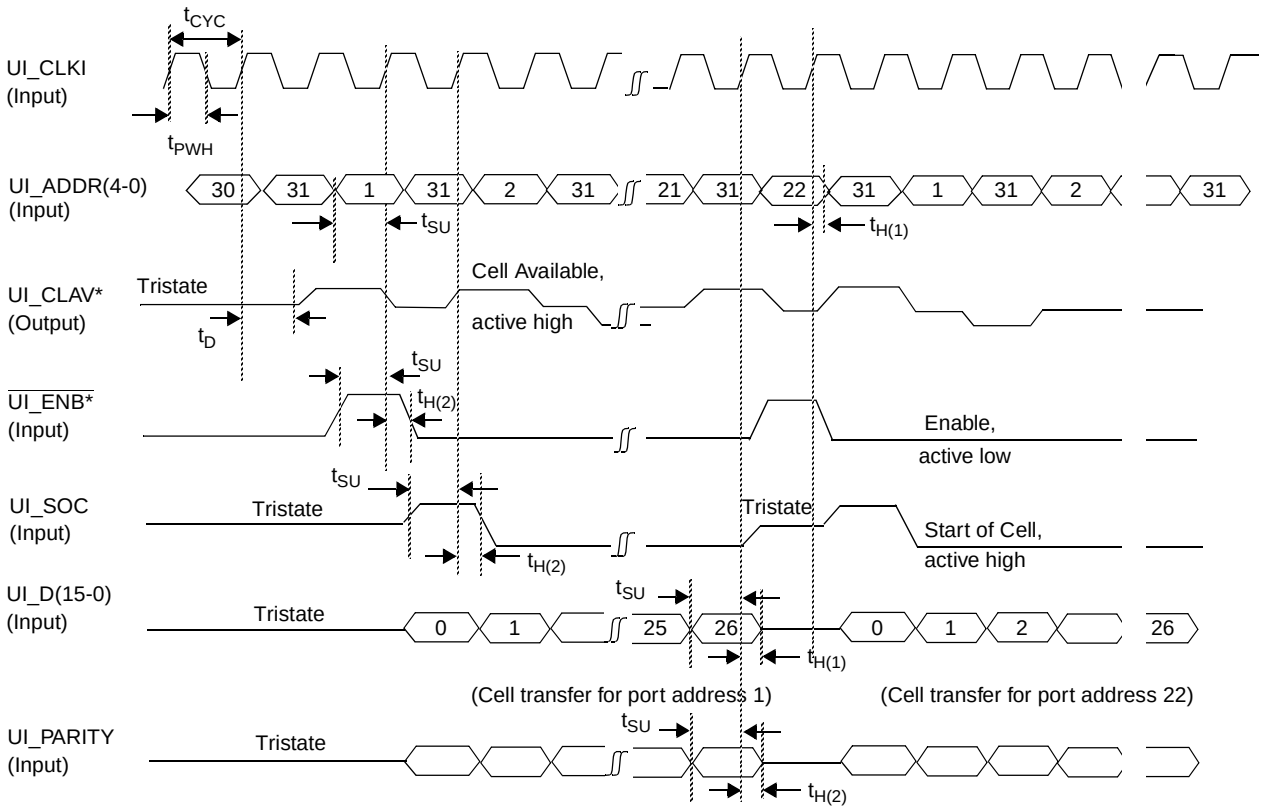
Figure 21. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(7-0), UI_SOC, UI_ADDR(4-0), UI_ENB* setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(7-0), UI_ADDR(4-0) hold time after UI_CLKI↑	$t_{H(1)}$	1.0			ns
UI_SOC, UI_ENB*, UI_PARITY hold time after UI_CLKI↑	$t_{H(2)}$	1.0			ns
UI_CLAV* delay from UI_CLKI↑	t_D	2.0		10.0	ns

Note: LCLK is selected by software, LCLK is used for Ingress and Egress UTOPIA interfaces.

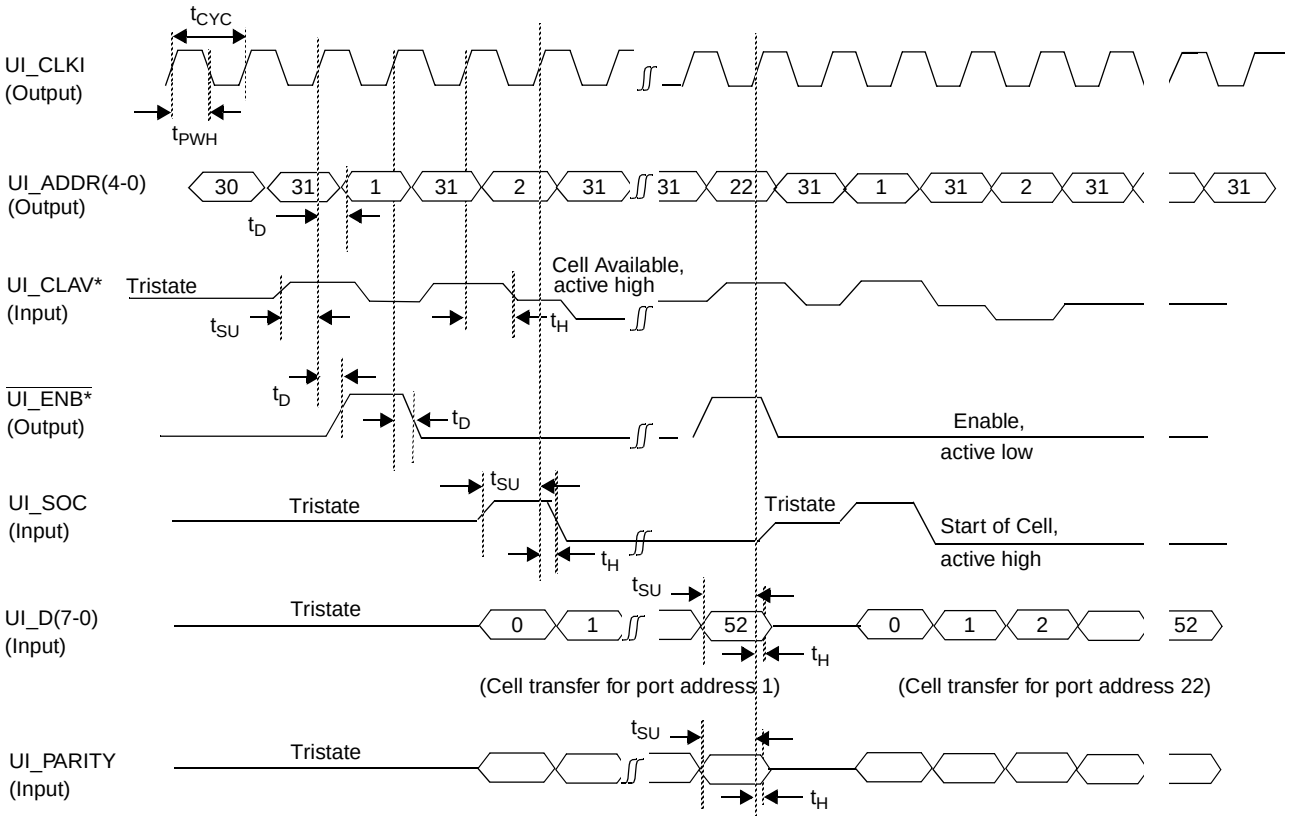
Figure 22. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(15-0), UI_SOC, UI_ADDR(4-0), UI_ENB* setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(15-0), UI_ADDR(4-0) hold time after UI_CLKI↑	$t_{H(1)}$	1.0			ns
UI_SOC, UI_ENB*, UI_PARITY hold time after UI_CLKI↑	$t_{H(2)}$	1.0			ns
UI_CLAV* delay from UI_CLKI↑	t_D	2.0		10.0	ns

PRODUCT PREVIEW

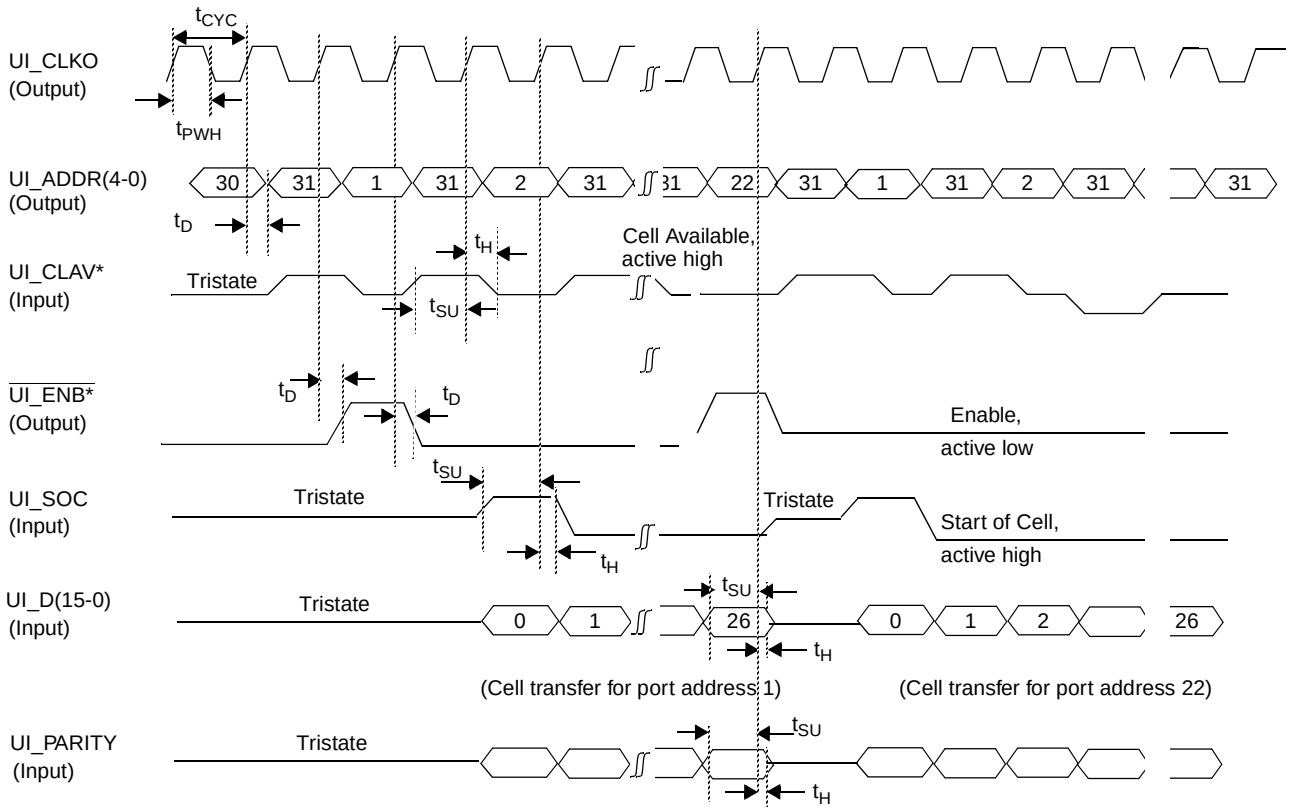
Figure 23. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(7-0), UI_SOC, UI_CLAV* setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(7-0), UI_SOC, UI_CLAV*, UI_PARITY hold time after UI_CLKI↑	t_H	1.0			ns
UI_ADDR(4-0), $\overline{\text{UI\_ENB*}}$ delay from UI_CLKI↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

Figure 24. Timing of Receive Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)

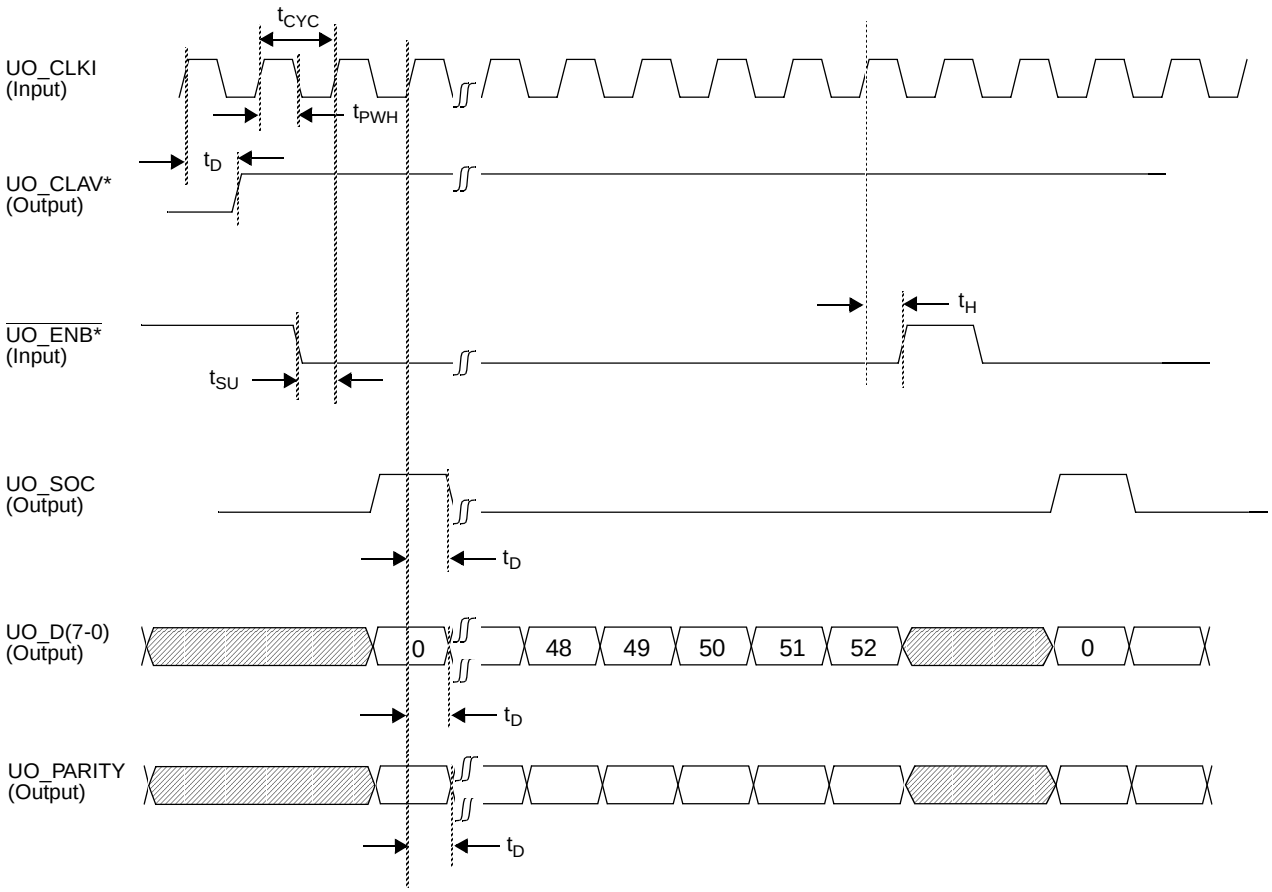


Parameter	Symbol	Min	Typ	Max	Unit
UI_CLKI clock period	t_{CYC}	20			ns
UI_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
UI_D(15-0), UI_SOC, UI_CLAV* setup time to UI_CLKI↑	t_{SU}	4.0			ns
UI_D(15-0), UI_SOC, UI_CLAV*, UI_PARITY hold time after UI_CLKI↑	t_H	1.0			ns
UI_ADDR(4-0), $\overline{\text{UI\_ENB*}}$ delay from UI_CLKI↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

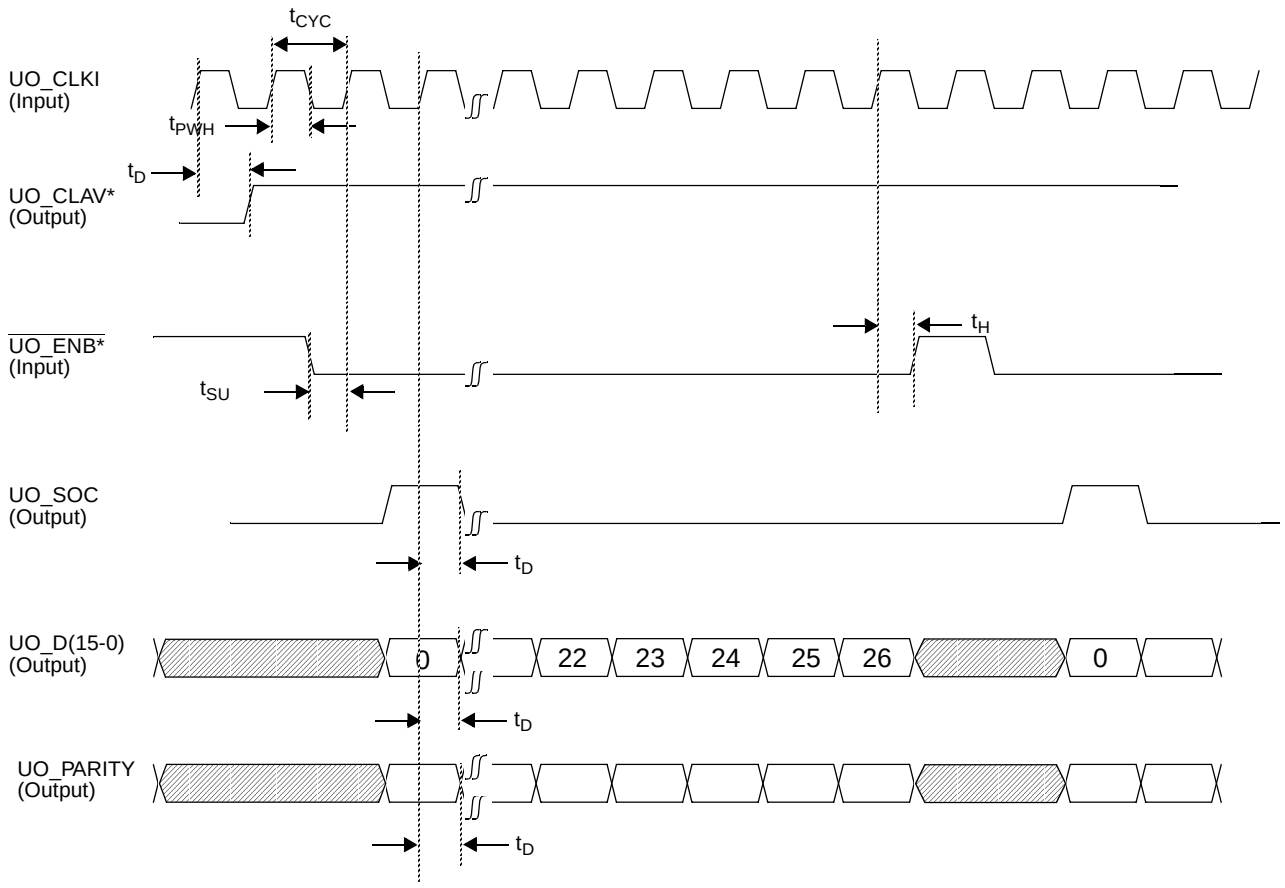
PRODUCT PREVIEW

Figure 25. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKI clock period	t_{CYC}	20			ns
UO_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{UO\_ENB*}}$ setup time to UO_CLKI↑	t_{SU}	4.0			ns
$\overline{\text{UO\_ENB*}}$ hold time after UO_CLKI↑	t_H	1.0			ns
UO_D(7-0), UO_SOC, UO_CLAV*, UO_PARITY delay from UO_CLKI↑	t_D	2.0		10.0	ns

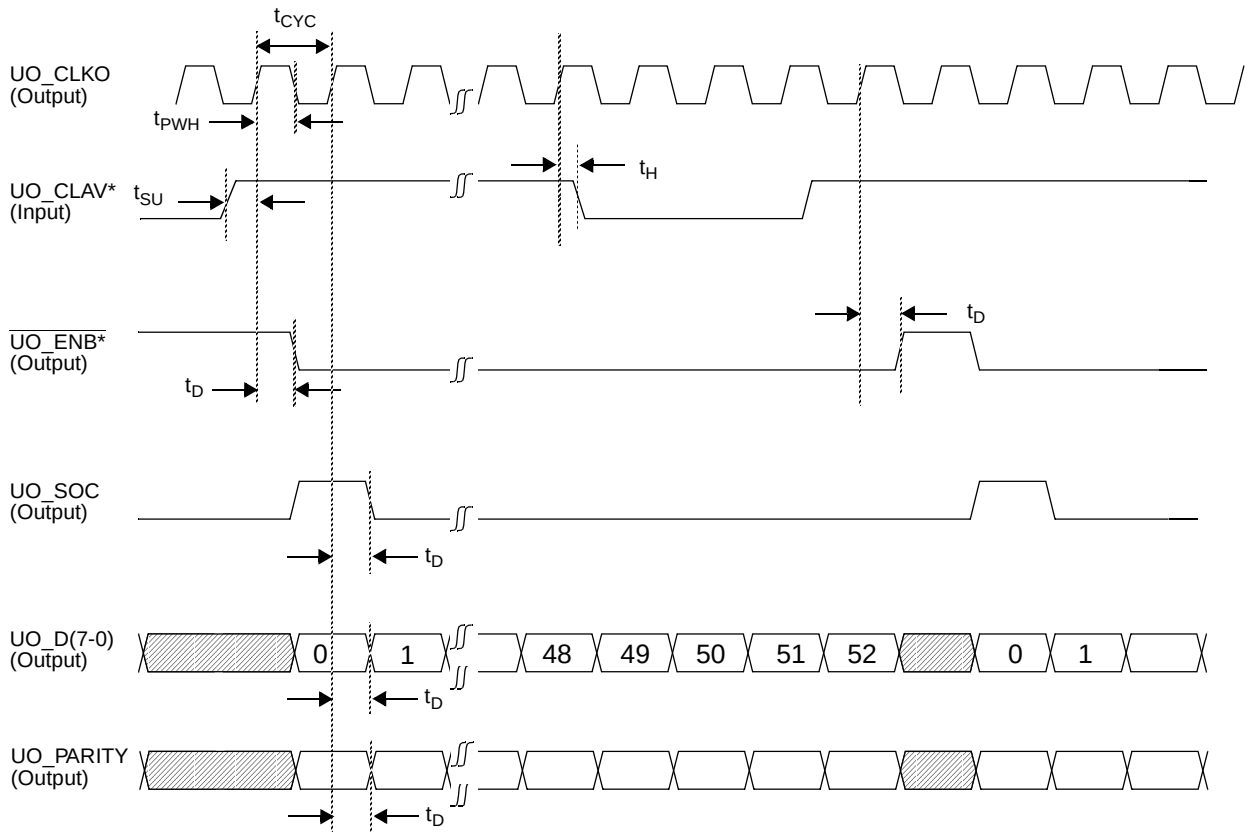
Figure 26. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (PHY Layer Emulation, 16-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKI clock period	t_{CYC}	20			ns
UO_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{UO\_ENB*}}$ setup time to UO_CLKI↑	t_{SU}	4.0			ns
$\overline{\text{UO\_ENB*}}$ hold time after UO_CLKI↑	t_H	1.0			ns
UO_DUO_D(15-0), UO_SOC, UO_CLAV*, UO_PARITY delay from UO_CLKI↑	t_D	2.0		10.0	ns

PRODUCT PREVIEW

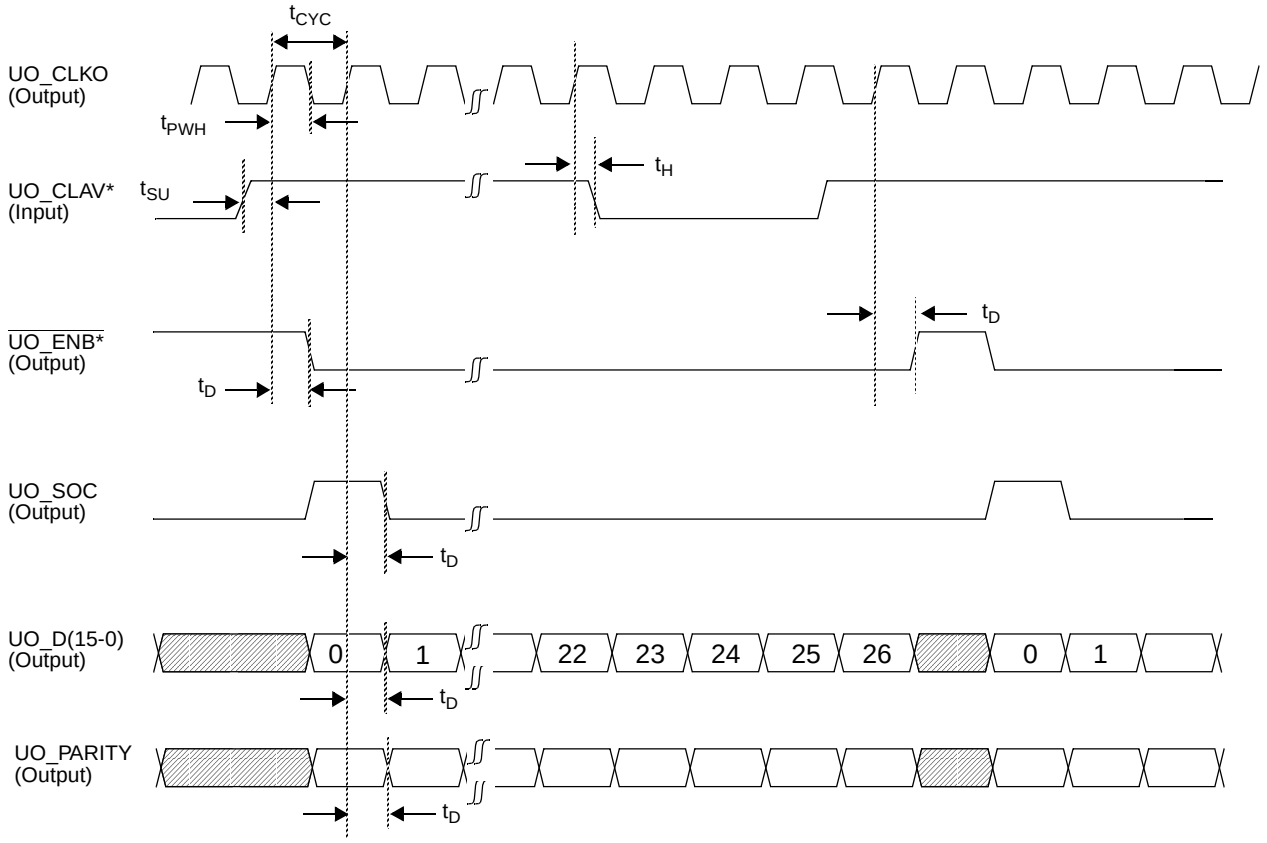
Figure 27. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKO clock period	t_{CYC}	20			ns
UO_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UO_CLAV* setup time to UO_CLKO↑	t_{SU}	4.0			ns
UO_CLAV* hold time after UO_CLKO↑	t_H	1.0			ns
UO_D(7-0), UO_SOC, $\overline{\text{UO\_ENB*}}$, UO_PARITY delay from UO_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

Figure 28. Timing of Transmit Interface for UTOPIA Mode, Single-PHY (ATM Layer Emulation, 16-bit)

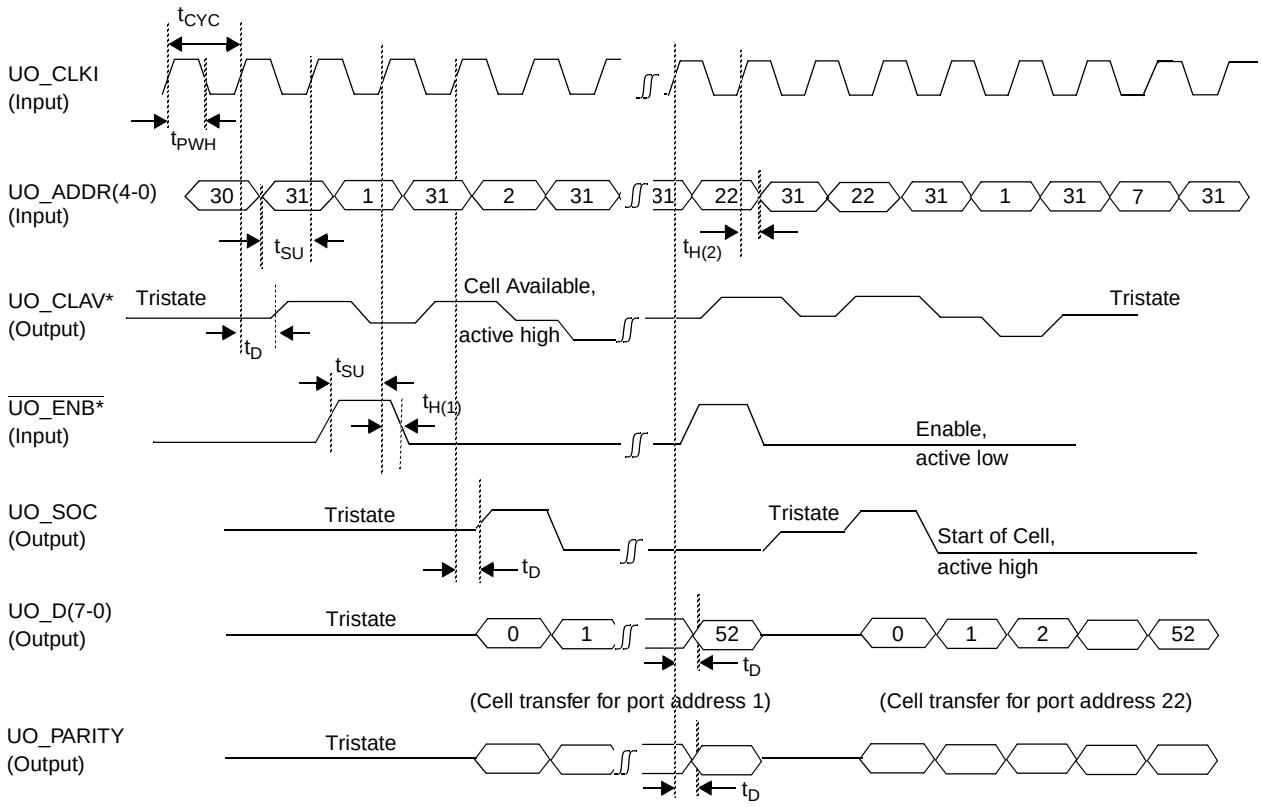


Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKO clock period	t_{CYC}	20			ns
UO_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UO_CLAV* setup time to UO_CLKO↑	t_{SU}	4.0			ns
UO_CLAV* hold time after UO_CLKO↑	t_H	1.0			ns
UO_D(15-0), UO_SOC, $\overline{\text{UO\_ENB*}}$, UO_PARITY delay from UO_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

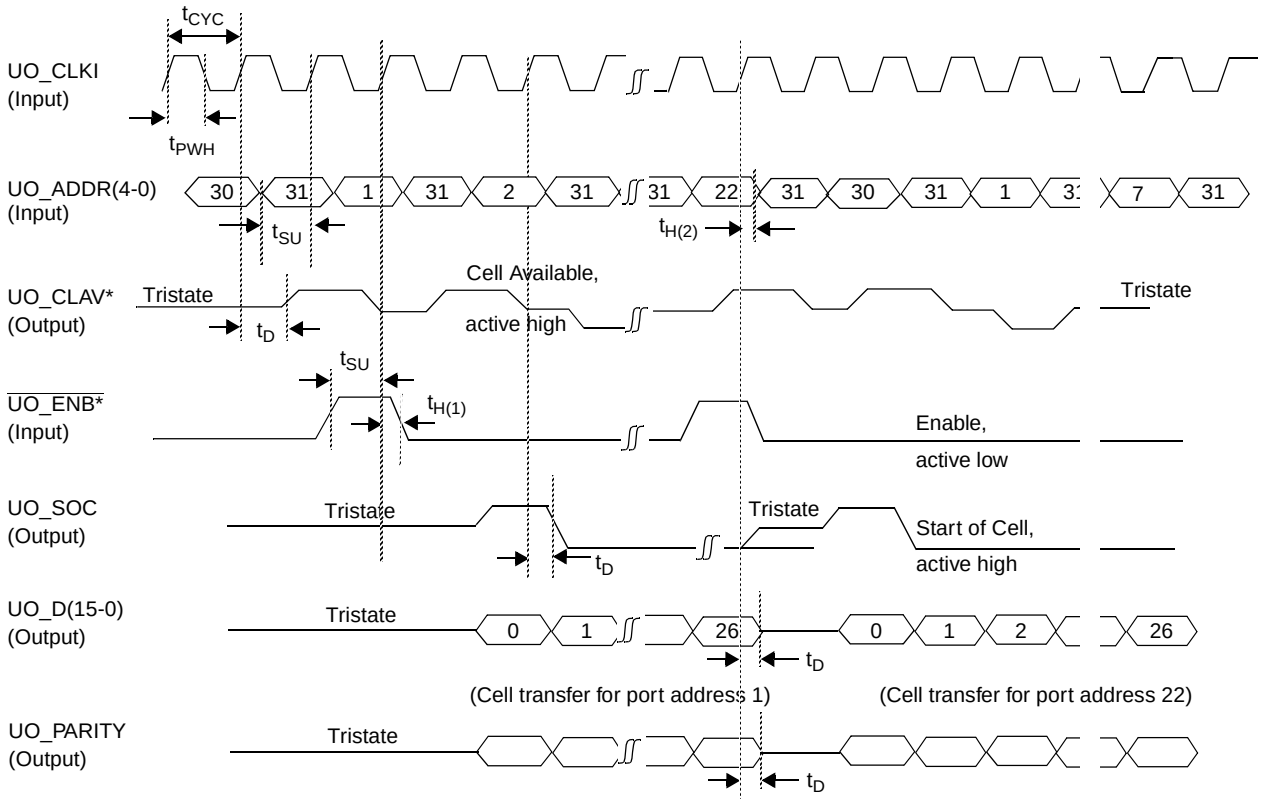
PRODUCT PREVIEW

Figure 29. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKI clock period	t_{CYC}	20			ns
UO_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{UO\_ENB*}}$, UO_ADDR(4-0) setup time to UO_CLKI↑	t_{SU}	4.0			ns
$\overline{\text{UO\_ENB*}}$ hold time after UO_CLKI↑	$t_{H(1)}$	1.0			ns
UO_ADDR(4-0) hold time after UO_CLKI↑	$t_{H(2)}$	1.0			ns
UO_D(7-0), UO_SOC, UO_CLAV*, UO_PARITY delay from UO_CLKI↑	t_D	2.0		10.0	ns

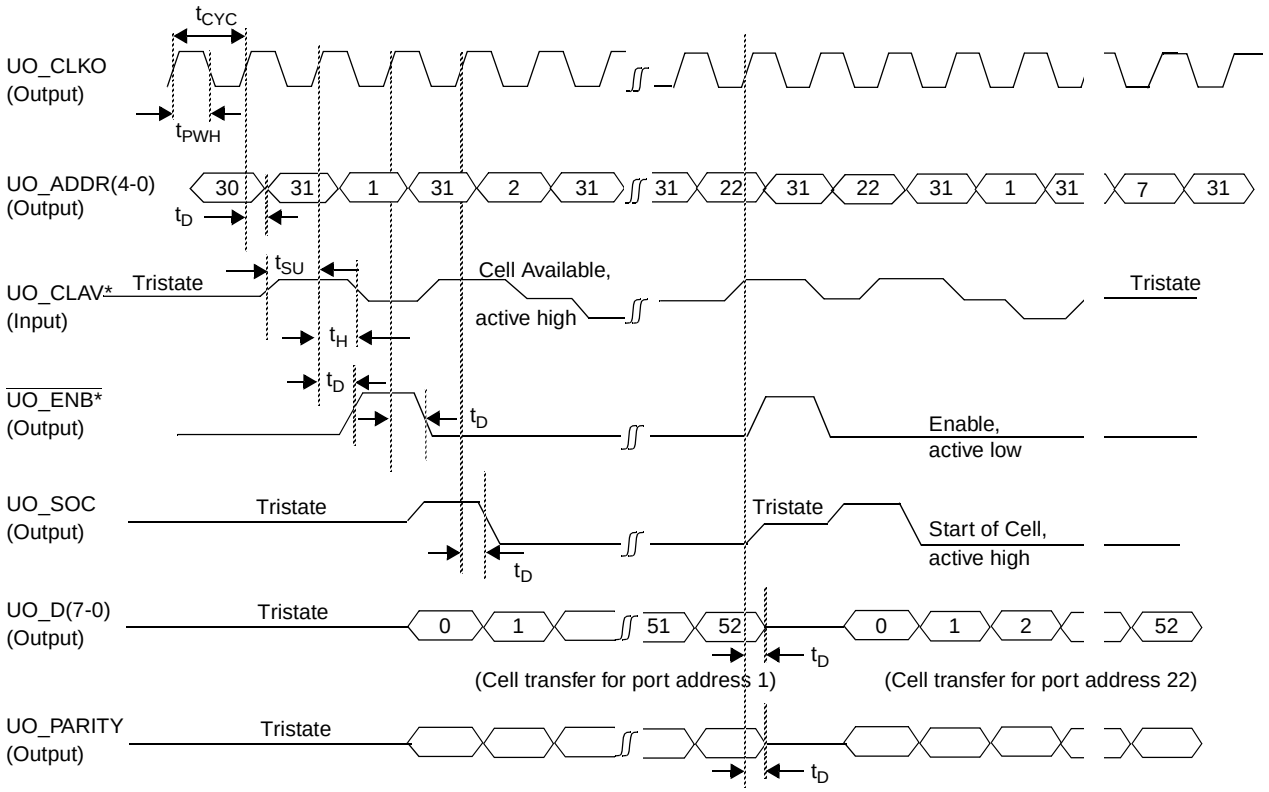
Figure 30. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (PHY Layer Emulation, 16-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKI clock period	t_{CYC}	20			ns
UO_CLKI duty cycle, t_{PWH}/t_{CYC}		40		60	%
$\overline{\text{UO\_ENB*}}$, UO_ADDR(4-0) setup time to UO_CLKI↑	t_{SU}	4.0			ns
$\overline{\text{UO\_ENB*}}$ hold time after UO_CLKI↑	$t_{H(1)}$	1.0			ns
UO_ADDR(4-0) hold time after UO_CLKI↑	$t_{H(2)}$	1.0			ns
UO_D(15-0), UO_SOC, UO_CLAV*, UO_PARITY delay from UO_CLKI↑	t_D	2.0		10.0	ns

PRODUCT PREVIEW

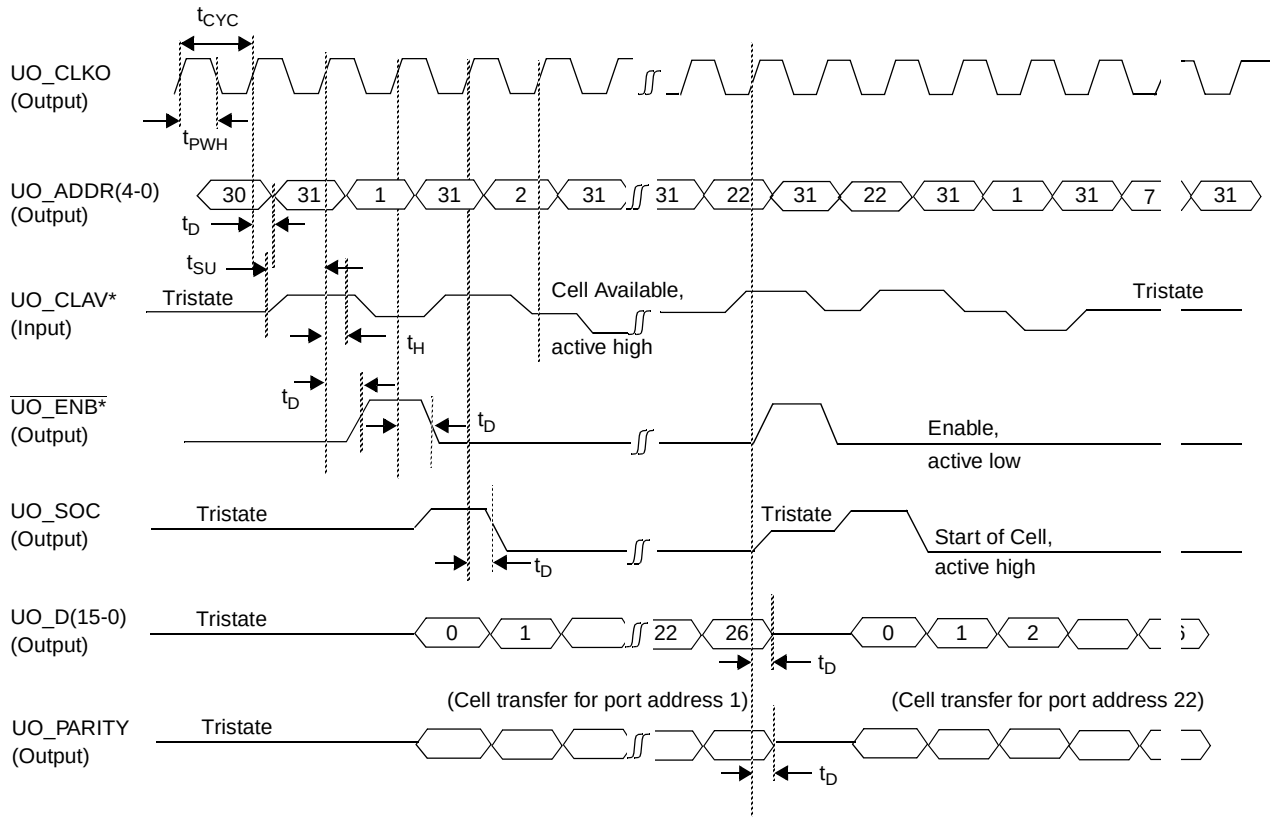
Figure 31. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 8-bit)



Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKO clock period	t_{CYC}	20			ns
UO_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UO_CLAV* setup time to UO_CLKO↑	t_{SU}	4.0			ns
UO_CLAV* hold time after UO_CLKO↑	t_H	1.0			ns
UO_D(7-0), UO_SOC, UO_ADDR(4-0), UO_ENB*, UO_PARITY delay from UO_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

Figure 32. Timing of Transmit Interface for UTOPIA Mode, Multi-PHY (ATM Layer Emulation, 16-bit)

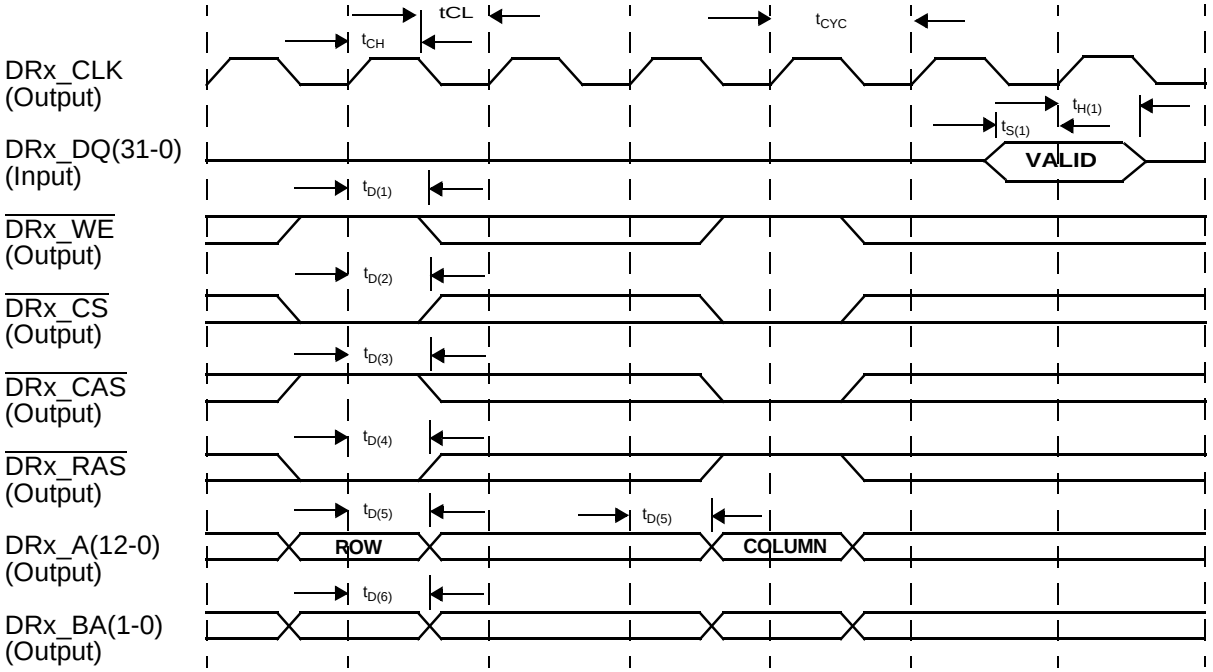


Parameter	Symbol	Min	Typ	Max	Unit
UO_CLKO clock period	t_{CYC}	20			ns
UO_CLKO duty cycle, t_{PWH}/t_{CYC}		40		60	%
UO_CLAV* setup time to UO_CLKO↑	t_{SU}	4.0			ns
UO_CLAV* hold time after UO_CLKO↑	t_H	1.0			ns
UO_D(15-0), UO_SOC, UO_ADDR(4-0), UO_ENB*, UO_PARITY delay from UO_CLKO↑	t_D	2.0		10.0	ns
LCLK duty cycle (See Note)		45		55	%

Note: When CLK_SEL = 0, LCLK is used for UTOPIA interfaces.

PRODUCT PREVIEW

Figure 33. SDRAM Read Timing

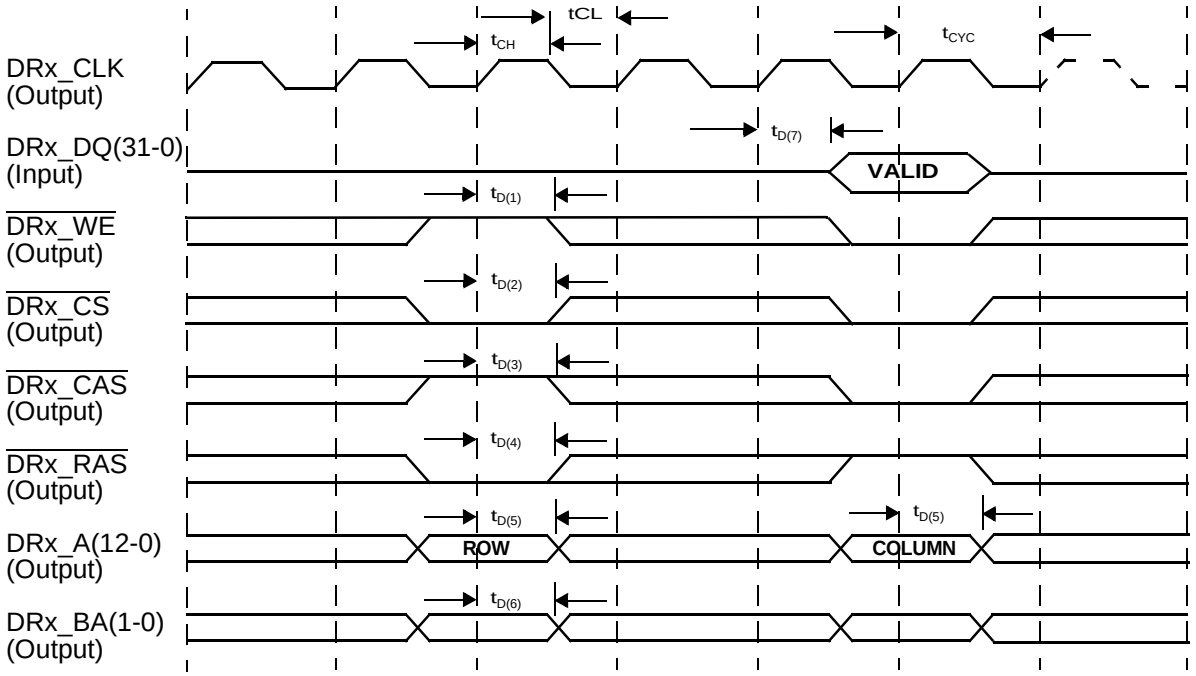


Parameter	Symbol	Min	Typ	Max	Unit
Clock Period	t_{CYC}	9.0			ns
Clock High Width	t_{CH}	3.0			ns
Clock Low Width	t_{CL}	3.0			ns
$\overline{\text{DRx\_WE}}$ delay after DRx_CLK↑	$t_{D(1)}$	1.2		5.0	ns
$\overline{\text{DRx\_CS}}$ delay after DRx_CLK↑	$t_{D(2)}$	1.2		5.0	ns
$\overline{\text{DRx\_CAS}}$ delay after DRx_CLK↑	$t_{D(3)}$	1.2		5.0	ns
$\overline{\text{DRx\_RAS}}$ delay after DRx_CLK↑	$t_{D(4)}$	1.2		5.0	ns
DRx_A(12-0) delay after DRx_CLK↑	$t_{D(5)}$	1.2		5.0	ns
DRx_BA(1-0) delay after DRx_CLK↑	$t_{D(6)}$	1.2		5.0	ns
DRx_DQ(31-0) setup before DRx_CLK↑	$t_{S(1)}$	1.5			ns
DRx_DQ(31-0) hold after DRx_CLK↑	$t_{H(1)}$	0.5			ns

Notes:

1. DRx above means either DR1_ or DR2_
2. DRx_CLK is assumed to have 22 ohm series terminating resistor connected to a compound capacitive load of 30 pF.

Figure 34. SDRAM Write Timing



Parameter	Symbol	Min	Typ	Max	Unit
Clock Period	t_{CYC}	9.0			ns
Clock High Width	t_{CH}	3.0			ns
Clock Low Width	t_{CL}	3.0			ns
$\overline{\text{DRx\_WE}}$ delay after DRx_CLK↑	$t_{D(1)}$	1.2		5.0	ns
$\overline{\text{DRx\_CS}}$ delay after DRx_CLK↑	$t_{D(2)}$	1.2		5.0	ns
$\overline{\text{DRx\_CAS}}$ delay after DRx_CLK↑	$t_{D(3)}$	1.2		5.0	ns
$\overline{\text{DRx\_RAS}}$ delay after DRx_CLK↑	$t_{D(4)}$	1.2		5.0	ns
DRx_A(12-0) delay after DRx_CLK↑	$t_{D(5)}$	1.2		5.0	ns
DRx_BA(1-0) delay after DRx_CLK↑	$t_{D(6)}$	1.2		5.0	ns
DRx_DQ(31-0) delay after DRx_CLK↑	$t_{D(7)}$	1.2		5.0	ns

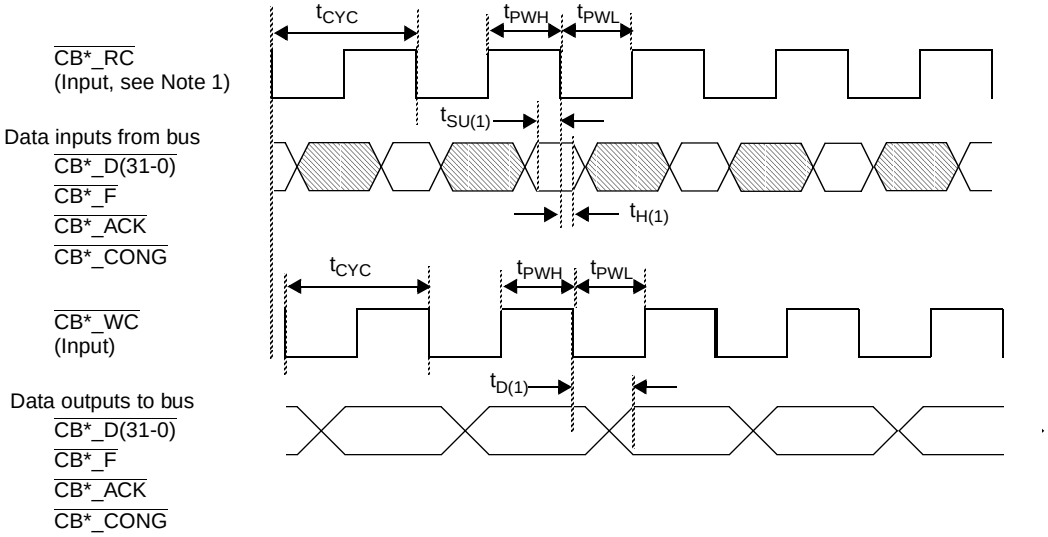
Notes:

1. DRx above means either DR1_ or DR2_
2. DRx_CLK is assumed to have 22 ohm series terminating resistor connected to a compound capacitive load of 30 pF.

PRODUCT PREVIEW

PRODUCT PREVIEW

Figure 35. Timing of Signals for *CellBus* Interfaces



Parameter	Symbol	Min	Typ	Max	Unit
$\overline{\text{CB*\_RC}}$, $\overline{\text{CB*\_WC}}$ cycle time	t_{CYC}	see Note 3			ns
$\overline{\text{CB*\_RC}}$, $\overline{\text{CB*\_WC}}$ duty cycle	t_{PWH}/t_{CYC}	40		60	%
CellBus inputs setup time before $\overline{\text{CB*\_RC}}\downarrow$	$t_{SU(1)}$	1.0			ns
CellBus inputs hold time after $\overline{\text{CB*\_RC}}\downarrow$	$t_{H(1)}$	2.0			ns
CellBus outputs delay after $\overline{\text{CB*\_WC}}\downarrow$	$t_{D(1)}$	See Note 2		See Note 2	ns

Notes:

1. The timing shown applies to the signals of both *CellBus* A and *CellBus* B, where * = A or B.
2. The ASPEN Express device *CellBus* write clock to *CellBus* data out time delay $t_{D(1)}$ has two components, internal delay and GTL+ driver delay. The internal delay consists of the delay from the $\overline{\text{CB*\_WC}}$ input, through the GTL+ receiver, internal ASPEN Express device circuitry and into the (internal) input lead of the GTL+ driver. This internal delay is dependent solely on temperature, voltage and process variation and has minimum and maximum values of 2.0 ns and 7.0 ns, respectively. The GTL+ driver delay includes the effects of the (internal) GTL+ driver and all external loading, from the chip bond wire inductance onwards. For the purposes of specification, a test load is used which consists of a 10.7 nH bond wire inductance from the VLSI device output pad to the package output lead, and a 50 ohm resistor to +1.5 volts with a 1.0 pF capacitor to ground from the package output lead. The total value of $t_{D(1)}$ is increased to the following minimum and maximum values (shown below) when using this load.
3. The Maximum operational frequency of the *CellBus* clock on the backplane is dependent on the *CellBus* backplane characteristics.

$t_{D(1)}$ Minimum Delay (ns) Internal + GTL+ = Total Pad	*CellBus* Output Signal Transition	$t_{D(1)}$ Maximum Delay (ns) Internal + GTL+ = Total Pad
2.0 + 0.5 = 2.5	Z to Low	7.0 + 2.0 = 9.0
2.0 + 3.0 = 5.0	Low to Z	7.0 + 4.2 = 11.2

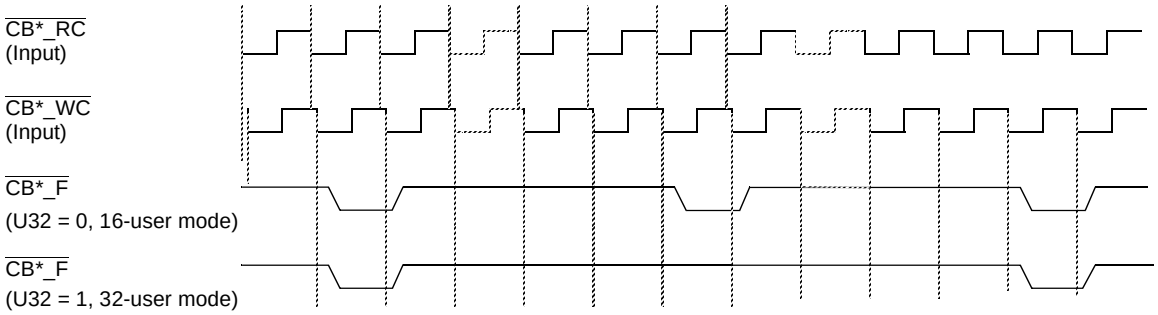
These output delay values by themselves may be inadequate to complete a system design. TranSwitch strongly recommends that all *CellBus* applications should be analyzed by high speed backplane and simulation specialists, using such tools as HSpice® analog circuit simulation.

These simulations can model timing from one ASPEN Express device, through various levels of system interconnect, to another ASPEN Express device, and include the effects of the device package, printed circuit board, connectors and backplane. The results of these simulations, when added to the internal delay, will provide the actual value of $t_{D(1)}$ for a given system. TranSwitch is able to support simulations by providing up-to-date models of the GTL+ transceiver used within the ASPEN Express device.

Please contact the TranSwitch Applications Engineering Department for additional information, a list of proven high speed simulation consultants, and support.

HSpice is a registered trademark of Meta-Software, Inc.

Figure 36. Timing of *CellBus* Frame Position

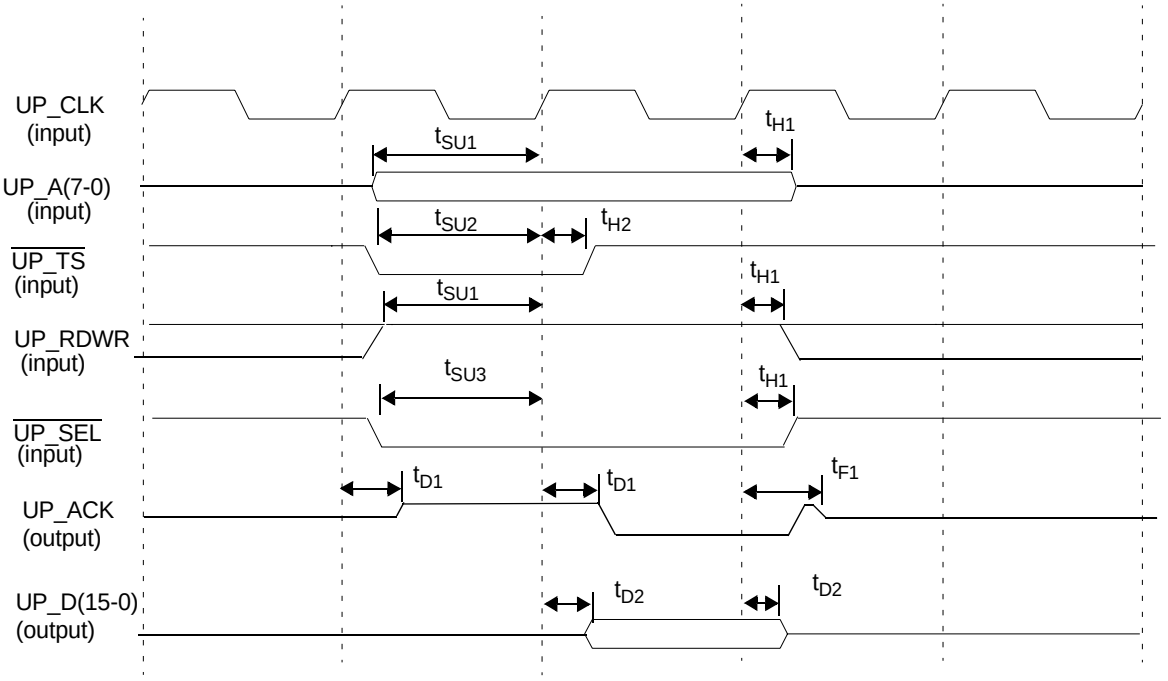


Note: The timing shown applies to the signals of both *CellBus* A and *CellBus* B, where * = A or B.

PRODUCT PREVIEW

MICROPROCESSOR INTERFACE TIMING

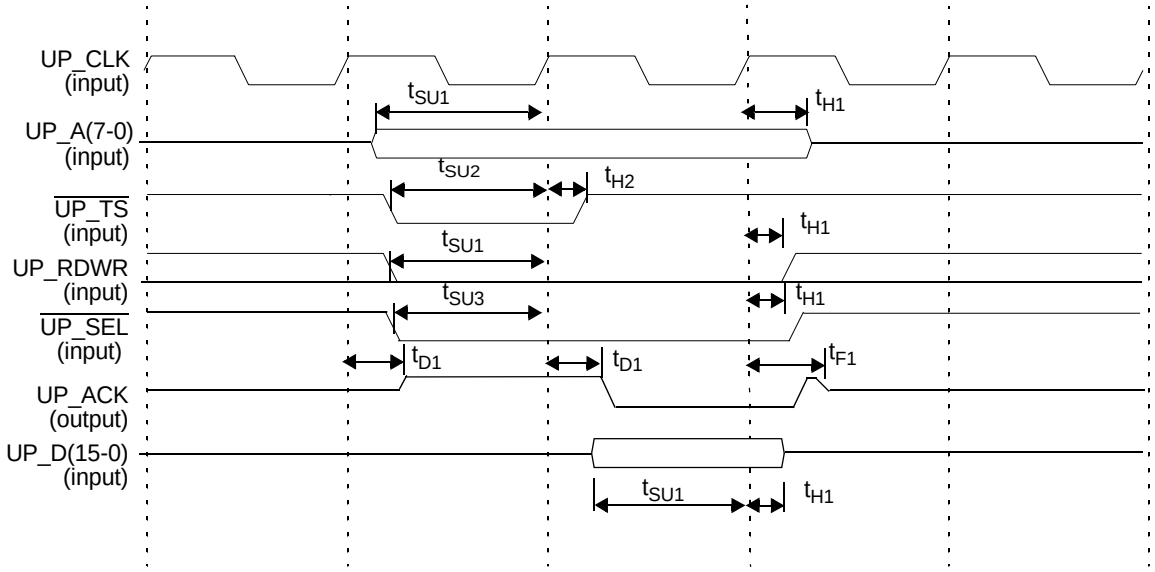
Figure 37. MPC860 Single Read Cycle Timing, UPMODE=10



Parameter	Symbol	Min	Typ	Max	Unit
UP_CLK period	t_{CYC}	20.0			ns
UP_A(7-0), UP_RDWR, UP_D(15-0) setup to UP_CLK ↑	t_{SU1}	3.0			ns
UP_A(7-0), UP_RDWR, $\overline{\text{UP\_SEL}}$ hold from UP_CLK↑	t_{H1}	2.0			ns
$\overline{\text{UP\_TS}}$ setup time to UP_CLK ↑	t_{SU2}	3.0			ns
$\overline{\text{UP\_TS}}$ hold time from UP_CLK ↑	t_{H2}	2.0			ns
$\overline{\text{UP\_SEL}}$ setup to UP_CLK ↑	t_{SU3}	3.0			ns
UP_ACK delay from UP_CLK ↑	t_{D1}	2.0		9.0	ns
UP_ACK float delay from UP_CLK ↑	t_{F1}	2.0		15.0	ns
UP_D(15-0) delay from UP_CLK ↑	t_{D2}	2.0		10.0	ns

Note:UP_ACK requires a pull-up resistor to V_{DD33} for proper operation.

Figure 38. MPC860 Single Write Cycle Timing, UPMODE=10



Note: UP_ACK requires a pull-up resistor to V_{DD33} for proper operation.

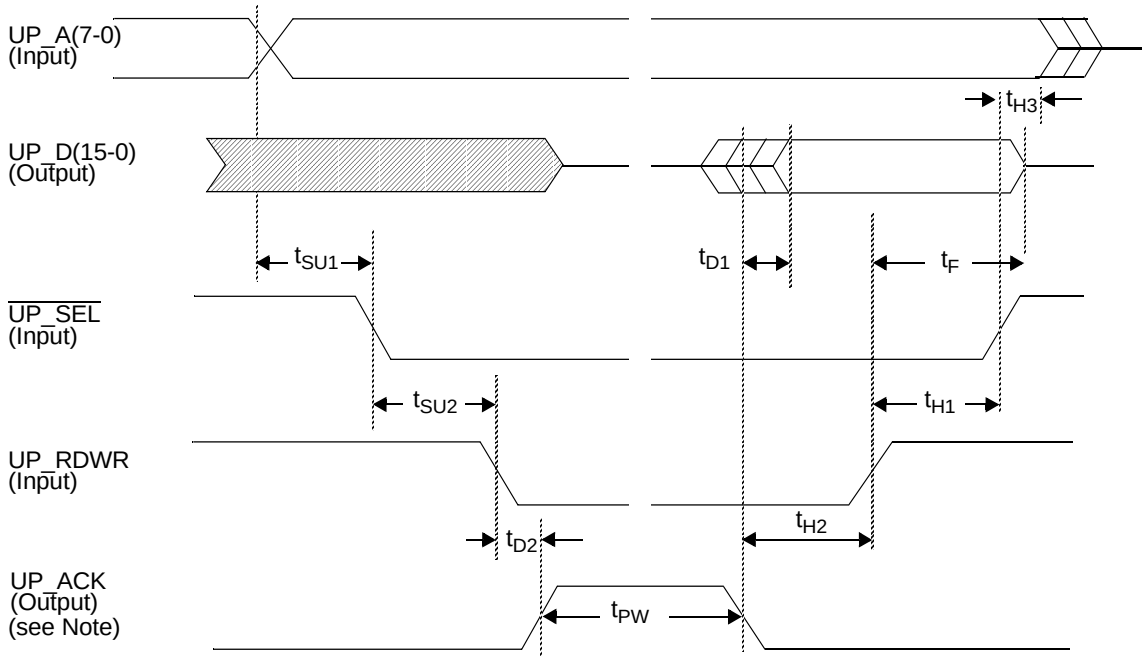
Parameter	Symbol	Min	Typ	Max	Unit
UP_CLK period	t_{CYC}	20.0			ns
UP_A(7-0), UP_RDWR, UP_D(15-00 setup to UP_CLK ↑	t_{SU1}	3.0			ns
UP_A(7-0), UP_D(15-0), UP_RDWR, $\overline{\text{UP\_SEL}}$ hold from UP_CLK ↑	t_{H1}	2.0			ns
$\overline{\text{UP\_TS}}$ setup time to UP_CLK ↑	t_{SU2}	3.0			ns
$\overline{\text{UP\_TS}}$ hold time from UP_CLK ↑	t_{H2}	2.0			ns
$\overline{\text{UP\_SEL}}$ setup to UP_CLK ↑	t_{SU3}	3.0			ns
UP_ACK delay from UP_CLK ↑	t_{D1}	2.0		9.0	ns
UP_ACK float delay from UP_CLK ↑	t_{F1}	2.0		15.0	ns

Figure 39 and Figure 40 (on following pages) show the timing relationship of UPB internal and external signals for read/write timing in Intel Mode. ReadRequest, ReadReady, and ReadRequestMade are internal signals within the Intel/Motorola Subblock.

PRODUCT PREVIEW

PRODUCT PREVIEW

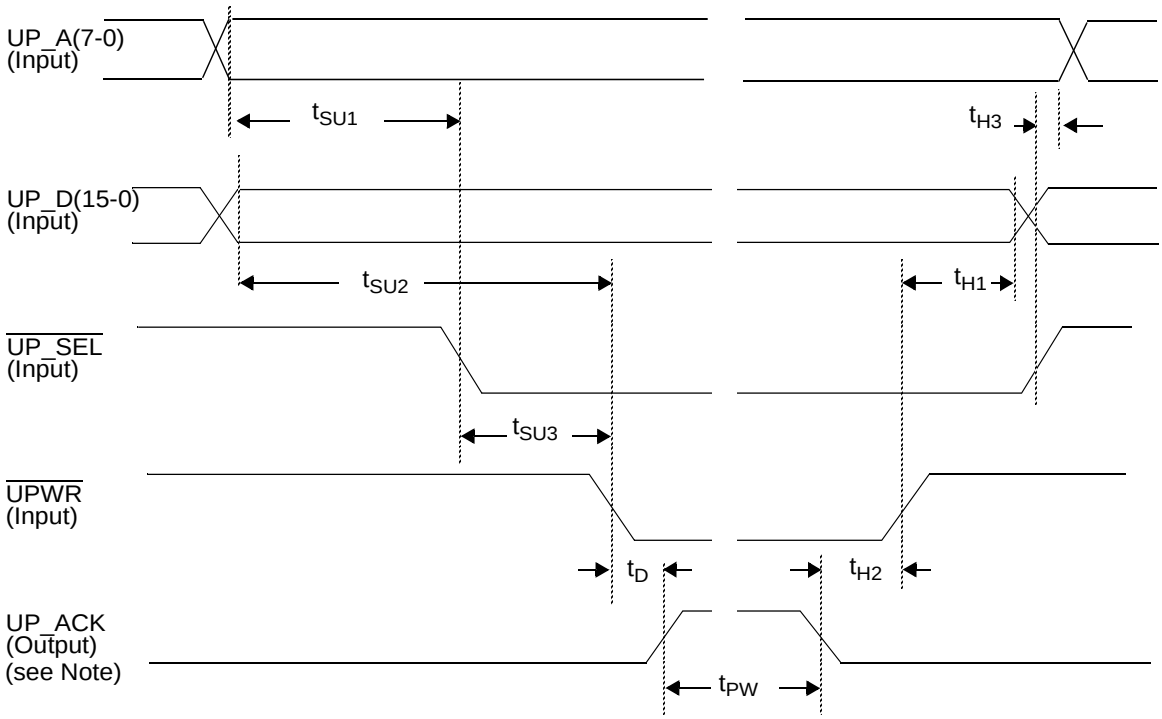
Figure 39. Intel Mode Read Cycle, UPMODE=00



Note: UP_ACK requires a pull-down resistor to V_{SS} for proper operation.

Parameter	Symbol	Min	Typ	Max	Unit
UP_A(7-0) setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU1}	0.0			ns
UP_A(7-0) hold time after $\overline{\text{UP\_SEL}}\uparrow$	t_{H3}	0.0			ns
UP_D(15-0) valid delay after UP_ACK$\uparrow$	t_{D1}	-10		0	ns
UP_D(15-0) float time to tri-state after UP_RDWR$\uparrow$	t_F	2.0		10.5	ns
$\overline{\text{UP\_SEL}}$ setup time to UP_RDWR$\downarrow$	t_{SU2}	1.0			ns
$\overline{\text{UP\_SEL}}$ hold time after UP_RDWR$\uparrow$	t_{H1}	1.5			ns
UP_RDWR hold time after UP_ACK$\uparrow$	t_{H2}	0.0			ns
UP_ACK delay after UP_RDWR$\downarrow$	t_{D2}	0.0		12	ns
UP_ACK pulse width	t_{PW}	0.0			ns

Figure 40. Intel Mode Write Cycle, UPMODE=00



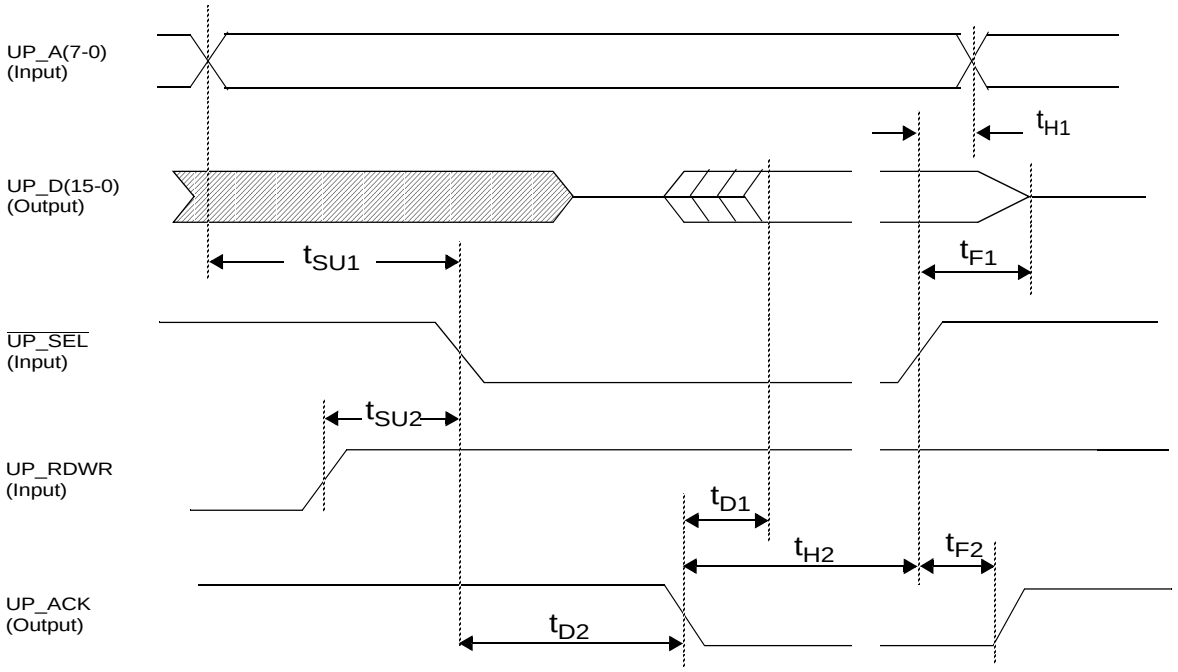
Note: UP_ACK requires a pull-down resistor to V_{SS} for proper operation.

Parameter	Symbol	Min	Typ	Max	Unit
UP_A(7-0) setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU1}	0.0			ns
UP_A(7-0) hold time to $\overline{\text{UP\_SEL}}\uparrow$	t_{H3}	0.0			ns
UPWR hold after UP_ACK↑	t_{H2}	0.0			ns
UP_D(15-0) valid setup time to $\overline{\text{UPWR}}\downarrow$	t_{SU2}	0.0			ns
UP_D(15-0) hold time after $\overline{\text{UPWR}}\uparrow$	t_{H1}	5.0			ns
$\overline{\text{UP\_SEL}}$ setup time to $\overline{\text{UPWR}}\downarrow$	t_{SU3}	0.6			ns
UP_ACK delay after $\overline{\text{UPWR}}\downarrow$	t_D	0.0		10	ns
UP_ACK pulse width	t_{PW}	0.0			ns

PRODUCT PREVIEW

PRODUCT PREVIEW

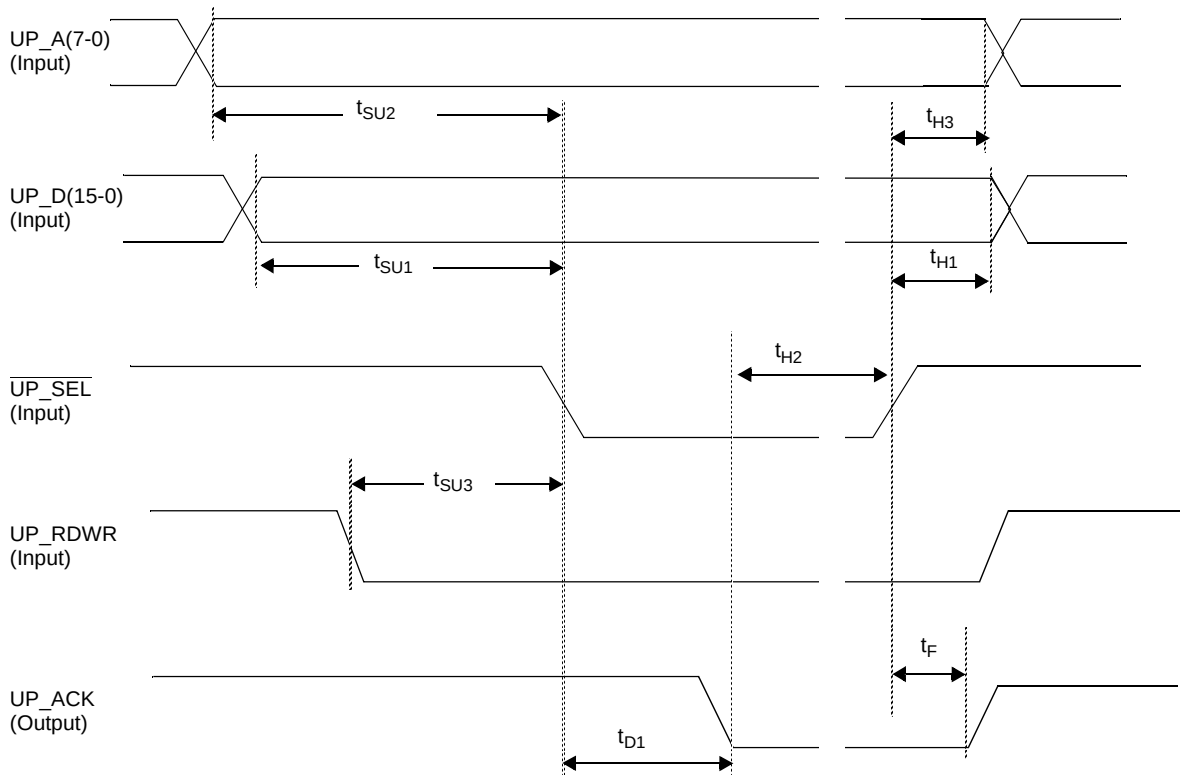
Figure 41. Motorola Mode Read Cycle, UPMODE=01



Note: UP_ACK requires a pull-up resistor to V_{DD33} for proper operation.

Parameter	Symbol	Min	Typ	Max	Unit
UP_A(7-0) valid setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU1}	0.0			ns
UP_A(7-0) valid hold time from $\overline{\text{UP\_SEL}}\uparrow$	t_{H1}	0.0			ns
UP_D(15-0) float time after $\overline{\text{UP\_SEL}}\uparrow$	t_{F1}	2.0		7.0	ns
UP_D(15-0) valid output delay after UP_ACK$\downarrow$	t_{D1}			0.0	ns
$\overline{\text{UP\_SEL}}$ hold time after UP_ACK$\downarrow$	t_{H2}	5.0			ns
UP_RDWR setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU2}	0.0			ns
UP_ACK$\downarrow$ delay time from $\overline{\text{UP\_SEL}}\downarrow$	t_{D2}	40			ns
UP_ACK float time after $\overline{\text{UP\_SEL}}\uparrow$	t_{F2}	2.0		12	ns

Figure 42. Motorola Mode Write Cycle, UPMODE=01



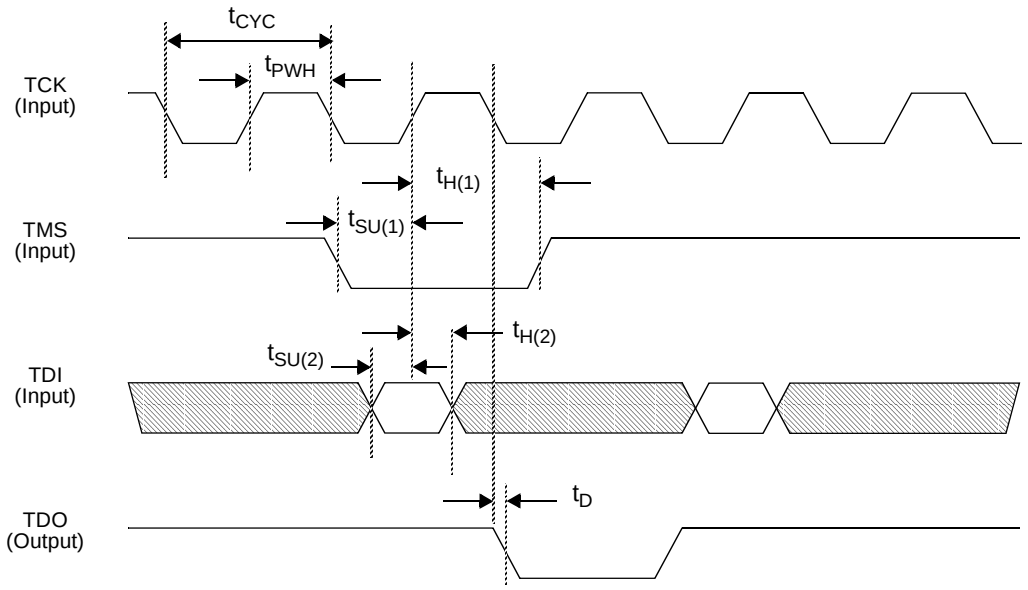
Parameter	Symbol	Min	Typ	Max	Unit
UP_A(7-0) valid setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU2}	0.0			ns
UP_A(7-0) valid hold time from $\overline{\text{UP\_SEL}}\uparrow$	t_{H3}	0.0			ns
UP_D(15-0) valid setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU1}	0.0			ns
UP_D(15-0) hold time after $\overline{\text{UP\_SEL}}\uparrow$	t_{H1}	0.0			ns
$\overline{\text{UP\_SEL}}$ hold time after UP_ACK$\downarrow$	t_{H2}	0.0			ns
UP_RDWR$\downarrow$ setup time to $\overline{\text{UP\_SEL}}\downarrow$	t_{SU3}	0.0			ns
UP_ACK$\downarrow$ delay after $\overline{\text{UP\_SEL}}\downarrow$	t_{D1}	40			ns
UP_ACK float time after $\overline{\text{UP\_SEL}}\uparrow$	t_F	1.0		10	ns

Note: UP_ACK requires a pull-up resistor to V_{DD33} for proper operation.

PRODUCT PREVIEW

PRODUCT PREVIEW

Figure 43. Boundary Scan Timing Diagram



Parameter	Symbol	Min	Max	Unit
TCK clock cycle time	t_{CYC}	50		ns
TCK clock duty cycle	t_{PWH}/t_{CYC}	40	60	%
TMS setup time before TCK↑	$t_{SU(1)}$	4.0		ns
TMS hold time after TCK↑	$t_{H(1)}$	0.0		ns
TDI setup time before TCK↑	$t_{SU(2)}$	4.0		ns
TDI hold time after TCK↑	$t_{H(2)}$	0.0		ns
TDO delay after TCK↓	t_D		12.0	ns

MEMORY MAP

Host Address (hex)	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	RW	MBOX_WRFIFO_DW_BOM															
01		Reserved															
02	RW	MBOX_WRFIFO_DW_COM															
03		Reserved															
04	RW	MBOX_WRFIFO_DW_EOM															
05-0B		Reserved															
0C	RO	MBOX_RDFIFO_DR															
0D-13		Reserved															
14	RW	Reserved										WRFIFO_Wr_Status			WRFIFO_Rd_Status		
15	RW	Reserved									Write_FIFO_Msg_Cnt						
16	RW	Reserved									Write_ FIFO_ Thresh	Write_ FIFO_ Above_ _Full	Write_ FIFO_ Empty	Reserved			
17	RW	Reserved									Write_FIFO_Fullness						
18-1B		Reserved															
1C	RW	Reserved										RDFIFO_Wr_Status			RDFIFO_Rd_Status		
1D	RW	Reserved									Read_FIFO_Msg_Cnt						
1E	RW	Reserved									Read_ FIFO_Ab ove_ Thresh	Read_ FIFO _Full	Read_ FIFO_ Empty	Reserved			
1F	RW	Reserved									Read_FIFO_Fullness						
20-23		Reserved															
24	RW	Reserved									Write_FIFO_Thresh						
25-27		Reserved															
28	RW	Reserved									Read_FIFO_Thresh						
29-2B		Reserved															

PRODUCT PREVIEW

Host Address (hex)	Mode	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
2C	RW	Reserved											Write_FIFO_Error_IMask	Write_FIFO_NotEmpty_IMask	Write_FIFO_Thresh_IMask	Write_FIFO_Empty_IMask	Write_FIFO_Full_IMask
All Odd 2D-4D		**Reserved**															
2E	RW	Reserved											Read_FIFO_Error_IMask	Read_FIFO_NotEmpty_IMask	Read_FIFO_Thresh_IMask	Read_FIFO_Empty_IMask	Read_FIFO_Full_IMask
30	RW	Reserved												Write_FIFO_Error_Status			
32	RW	Reserved												Read_FIFO_Error_Status			
34	RW	Reserved						Write_FIFO_Error_Count									
36	RW	Reserved						Read_FIFO_Error_Count									
38	RW	DEVICE_RST															
3A	RO	MFG_ID															
3C	RO	DEVICE_ID															
3E	RO	Reserved						Version						Mask			
40	RW	GPA_LS															
42	RW	GPA_MS															
44	RW	GPB_LS															
46	RW	GPB_MS															
48	RW	GPC_LS															
4A	RW	GPC_MS															
4C	RW	GPD_LS															
4E	RW	GPD_MS															
50	RW	Watchdog_Enable															
52	RW	Watchdog_Activate_Change															

MEMORY MAP DESCRIPTIONS

Host Address	Mode	Bit	Symbol	Value After Reset	Description
00	RW	15-0	MBOX_ WRFIFO_ DW_BOM	0x0000	A write to this register puts 16 bits into Write FIFO and marks it as the first word of a message (BOM).
02	RW	15-0	MBOX_ WRFIFO_ DW_COM	0x0000	A write to this register puts 16 bits into Write FIFO and marks it as continuation of message (COM).
04	RW	15-0	MBOX_ WRFIFO_ DW_EOM	0x0000	A write to this register puts 16 bits into Write FIFO, marking it as an end of message (EOM).
0C	RO	15-0	MBOX_ RDFIFO_DR	0x0000	A read from this register reads 16 bits from Read FIFO. Do not read from this register if Read FIFO is empty.
14	RO	15-6	MBOX_ WRFIFO_ STATUS0	0x0000	Reserved
		5-3		000	**WRFIFO_Wr_Status** = Status of last word written to Write FIFO. 000 = No message. 001 = Beginning of message (BOM). 010 = Continuation of message (COM). 100 = End of message, 2 bytes valid (EOM).
		2-0		000	**WRFIFO_Rd_Status** = Status of last word read from Write FIFO. 000 = No message. 001 = Beginning of message (BOM). 010 = Continuation of message (COM). 110 = End of message, 4 bytes valid (EOM).
15	RO	15-8	MBOX_ WRFIFO_ STATUS1	0x00	Reserved
		7-0		0x00	Write_FIFO_Msg_Cnt = Number of complete messages in Write FIFO

PRODUCT PREVIEW

PRODUCT PREVIEW

Host Address	Mode	Bit	Symbol	Value After Reset	Description
16	RO	15-7	MBOX_ WRFIFO_ STATUS2	0x000	Reserved
		6		0	Write_FIFO_Above_Thresh = 1 if Write_FIFO_Fullness > Write_FIFO_Thresh
		5		0	Write_FIFO_Full = 1 if Write FIFO full, 0 otherwise
		4		1	Write_FIFO_Empty = 1 if Write FIFOempty, 0 otherwise
		3-0		0000	Reserved
17	RO	15-8	MBOX_ WRFIFO_ STATUS3	0x00	Reserved
		7-0		0x00	Write_FIFO_Fullness = Number of bytes in Write FIFO
1C	RO	15-6	MBOX_ RDFIFO_ STATUS0	0x000	Reserved
		5-3		000	**RDFIFO _Wr_Status** = Status of last word written to Read FIFO by device. 000 = No message. 001 = Beginning of message (BOM). 010 = Continuation of message (COM). 110 = End of message, 4 bytes valid (EOM).
		2-0		000	**RDFIFO _Rd_Status** = Status of last word read from Read FIFO by device. 000 = No message. 001 = Beginning of message (BOM). 010 = Continuation of message (COM). 100 = End of message, 2 bytes valid (EOM).
1D	RO	15-8	MBOX_ RDFIFO_ STATUS1	0x00	Reserved
		7-0		0x00	Read_FIFO_Msg_Cnt = Number of complete messages in Read FIFO
1E	RO	15-7	MBOX_ RDFIFO_ STATUS2	0x000	Reserved
		6		0	Read_FIFO_Above_Thresh = 1 if Read_FIFO_Fullness > Read_FIFO_Thresh
		5		0	Read_FIFO_Full = 1 if Read FIFOfull, 0 otherwise
		4		1	Read_FIFO_Empty = 1 if Read FIFOempty, 0 otherwise
		3-0		0000	Reserved

Host Address	Mode	Bit	Symbol	Value After Reset	Description
1F	RO	15-8	MBOX_ RDFIFO_ STATUS3	0x00	Reserved
		7-0		0x00	Read_FIFO_Fullness = Number of bytes in Read FIFO
24	RW	15-8	MBOX_ WRFIFO_ THRESH0	0x00	Reserved
		7-0		0x10	Write_FIFO_Thresh = Threshold at which the Write_FIFO_Thresh bit will be set.
28	RW	15-8	MBOX_ RDFIFO_ THRESH0	0x00	Reserved
		7-0		0x10	Read_FIFO_Thresh = Threshold at which the Read_FIFO_Thresh bit will be set
2C	RW	15-5	MBOX_ WRFIFO_ INTMASK	0x0000	Reserved
		4		0	Write_FIFO_Error_IMask = Generate Host Processor interface interrupt when Write_FIFO_Error_Status /= 0000
		3		0	Write_FIFO_NotEmpty_IMask = Generate microprocessor interface interrupt when Write_FIFO_Empty = 0
		2		0	Write_FIFO_Thresh_IMask = Generate Xtensa interrupt when Write_FIFO_Thresh = 1
		1		0	Write_FIFO_Empty_IMask = Generate Xtensa interrupt when Write_FIFO_Empty=1
		0		0	Write_FIFO_Full_IMask = Generate Xtensa interrupt when Write_FIFO_Full = 1
2E	RW	15-5	MBOX_ RDFIFO_ INTMASK	0x0000	Reserved
		4		0	Read_FIFO_Error_IMask = Generate Host Processor interface interrupt when Read_FIFO_Error_Status /= 0000
		3		0	Read_FIFO_NotEmpty_IMask = Generate Host Processor interface interrupt when Read_FIFO_Empty = 0
		2		0	Read_FIFO_Thresh_IMask = Generate Xtensa interrupt when Read_FIFO_Thresh = 1
		1		0	Read_FIFO_Empty_IMask = Generate Xtensa interrupt when Read_FIFO_Empty=1
		0		0	Read_FIFO_Full_IMask = Generate Xtensa interrupt when Read_FIFO_Full = 1

PRODUCT PREVIEW

PRODUCT PREVIEW

Host Address	Mode	Bit	Symbol	Value After Reset	Description
30	RO	15-4	MBOX_ WRFIFO_ ERRSTATUS	0x0000	Reserved
		3-0		0000	Write_FIFO_Error_Status - Nature of last error to occur in Write FIFO 0000 = NoError 0001 = WriteOnFull 0010 = ReadOnEmpty 0011 = MissingBOM 0100 = MissingEOM
32	RO	15-4	MBOX_ RDFIFO_ ERRSTATUS	0x0000	Reserved
		3-0		0000	Read_FIFO_Error_Status - Nature of last error to occur in Read FIFO 0000 = NoError 0001 = WriteOnFull 0010 = ReadOnEmpty 0011 = MissingBOM 0100 = MissingEOM
34	RW	15-8	MBOX_ WRFIFO_ ERR_CNT	0x00	Reserved
		7-0		0x00	Write_FIFO_Error_Count - Number of errors that have occurred in Write FIFO. This register is not cleared upon read. It can only be cleared from the device side.
36	RW	15-8	MBOX_ RDFIFO_ ERR_CNT	0x00	Reserved
		7-0		0x00	Read_FIFO_Error_Count - Number of errors that have occurred in Read FIFO. This register is not cleared upon read. It can only be cleared from the device side.
38	RW	15-0	DEVICE _RST	0x0000	Device Reset. Writing 0x9339 to this register will assert software reset output (SWRST_N(1)='0' resets entire chip (including processor) except for DCB1). Writing 0x5771 to this register will assert software reset output (SWRST_N(0)='0' resets entire chip (including processor)) Writing any other values will deassert software reset outputs (SWRST_N="11")
3A	RO	15-0	MFG_ID	0x00D7	Manufacturer ID
3C	RO	15-0	DEVICE ID	0x16AE	Device ID - P/N = 05806 in binary

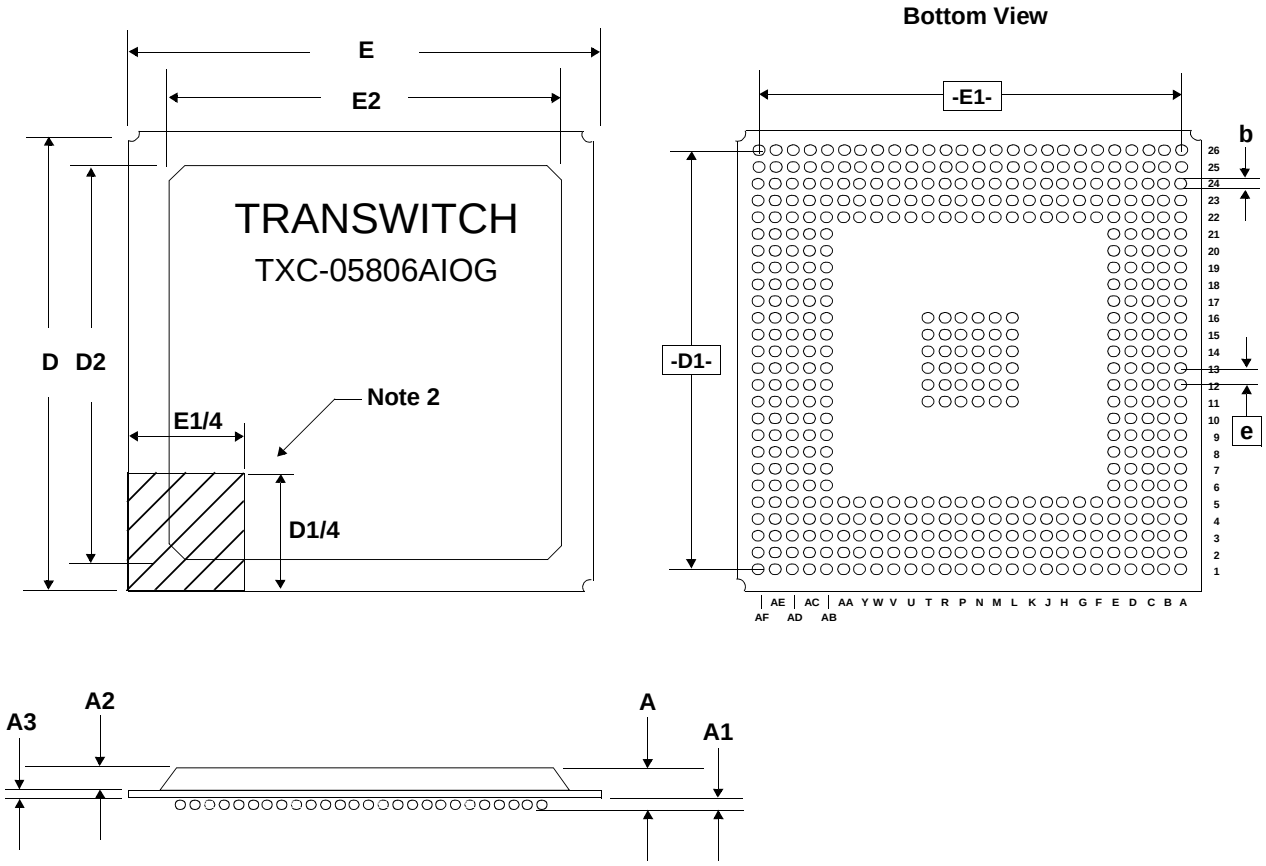
Host Address	Mode	Bit	Symbol	Value After Reset	Description
3E	RO	15-8	VERSION_ MASK	0x00	Reserved
		7-4		0000	Version Number
		3-0		0000	Mask Number
40	RW	15-0	GP_A_LS	0x0000	Scratch Register A.
42	RW	15-0	GP_A_MS	0x0000	Scratch Register A.
44	RW	15-0	GP_B_LS	0x0000	Scratch Register B.
46	RW	15-0	GP_B_MS	0x0000	Scratch Register B.
48	RW	15-0	GP_C_LS	0x0000	Scratch Register C.
4A	RW	15-0	GP_C_MS	0x0000	Scratch Register C.
4C	RW	15-0	GP_D_LS	0x0000	Scratch Register D.
4E	RW	15-0	GP_D_MS	0x0000	Scratch Register D.
50	RW	15-1	Watchdog_ Enable	0x0000	Reserved
		0		0	Bit 0: '1' Watchdog Timer Enabled '0' Watchdog Timer Disabled Value written is loaded into a Watchdog_Timer_Enable_Temp register.
52	RW	15-0	Watchdog_ Activate_ Change	0x0000	Writing the code 0x56A1 to Watchdog_Activate_Change register activates the values held in temp Watchdog_Timer_Enable_Temp register. Writing any other value has no effect. Read from Watchdog_Activate_Change returns 0x0000

* All addresses in memory map description tables are hexadecimal. Reserved and "Don't Care" addresses are not listed.

PRODUCT PREVIEW

PACKAGE INFORMATION

The ASPEN Express device is available in a 456-lead plastic ball grid array (PBGA) suitable for surface mounting, as shown in Figure 44.



Notes:

1. All dimensions are in millimeters. Values shown are for reference only.
2. Identification of the solder ball A1 corner is contained within this shaded zone. Package corner may not be a 90° angle.

Dimension (Note 1)	Min	Max
A (Nom)	2.23	
A1	0.40	0.60
A2 (Nom)	1.12	1.22
A3 (Nom)	0.56	
b (Ref.)	0.63	
D	27.00	
D1 (Nom)	25.00	
D2	23.95	24.70
E	27.00	
E1 (Nom)	25.00	
E2	23.95	24.70
e (Ref.)	1.00	

Figure 44. ASPEN Express TXC-05806 456-Lead Plastic Ball Grid Array Package

ORDERING INFORMATION

Part Number: TXC-05806AIOG 456-lead Plastic Ball Grid Array Package (PBGA)

RELATED PRODUCTS

TXC-05802B, CUBIT-*Pro* VLSI Device (*CellBus* Bus Switch). Implements cost effective ATM multiplexing and switching systems, based on the 32-bit *CellBus* architecture. A single-chip solution, the CUBIT-*Pro* has the ability to send and also receive cells for control purposes over the same *CellBus*. *CellBus* technology works at aggregate rates of up to 1 gigabit per second and provides header translation, multiplexing, concentration and switching functions for a wide variety of small-to-medium size ATM systems.

TXC-05804, CUBIT-3 VLSI Device (*CellBus* Bus Switch). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. Such systems are constructed from a number of CUBIT-3 devices, all interconnected by a 37-line common bus, the *CellBus.* CUBIT-3 supports unicast, broadcast and spatial multicast transfers, and has all necessary functions for implementing a switch: cell address translation, cell routing and outlet cell queuing. This device interfaces with CUBIT-*Pro* devices.

TXC-05805, CUBIT-622 VLSI Device (Multi-PHY *CellBus* Access Device). A single-chip solution for implementing low-cost ATM multiplexing and switching systems, based on the *CellBus* architecture. The CUBIT-622 device is an enhanced version of the CUBIT-3 (TXC-05804) device. The two major enhancements include a throughput increase to 622 Mbit/s and a port density increase to 64 ports. The rate decoupling FIFO has been increased from 4 to 32 cells on ingress to accommodate the higher bandwidth interface.

TXC-05810, ASPEN VLSI Device (*CellBus* Access Processor). ASPEN supports *CellBus* operation in both Cell and Packet modes via two independent *CellBus* ports. These may be configured to support redundant system operation or alternatively, to provide greater system throughput. Line interface is via UTOPIA 1 or 2 for ATM cells or UTOPIA 2P for variable length packets. Buffering of data traffic and control information, such as connection tables is stored in an external synchronous SRAM.

TXC-06203, PHAST-3P VLSI Device (STM-1/STS-3c SDH/SONET Overhead Terminator with CDB/PPP UTOPIA Interface). This is an STM-1/STS-3c section, line and path overhead termination device that provides CDB or PPP (HDLC) processing using an 8-bit or 16-bit UTOPIA single-PHY or multi-PHY interface for downstream access. A bit-serial or byte-parallel line interface is provided.

TXC-06212, PHAST-12E VLSI Device (Programmable, High-Performance ATM/PPP/TDM SONET/SDH Overhead Terminator for Level 12 with Enhanced Features). This PHAST-12E VLSI device provides programmable, high performance ATM/Packet/Transmission for Level 12 applications with enhanced features.

REFERENCE DOCUMENTS

- TranSwitch Corporation TXC-05806-AN2 Application Note 541 for the ASPEN Express Multi-PHY *CellBus* Access VLSI Device, entitled "Logical Multicast for ASPEN Express".
- The ATM Forum: UTOPIA Specification Level 2, Version 1.0, June 1995
- The ATM Forum: Traffic Management Specification, Version 4.1, March 1999
- ITU-T Recommendation I.610 - “B-ISDN Operation and Maintenance Principles and Functions”, February 1999

APPLICATION EXAMPLE

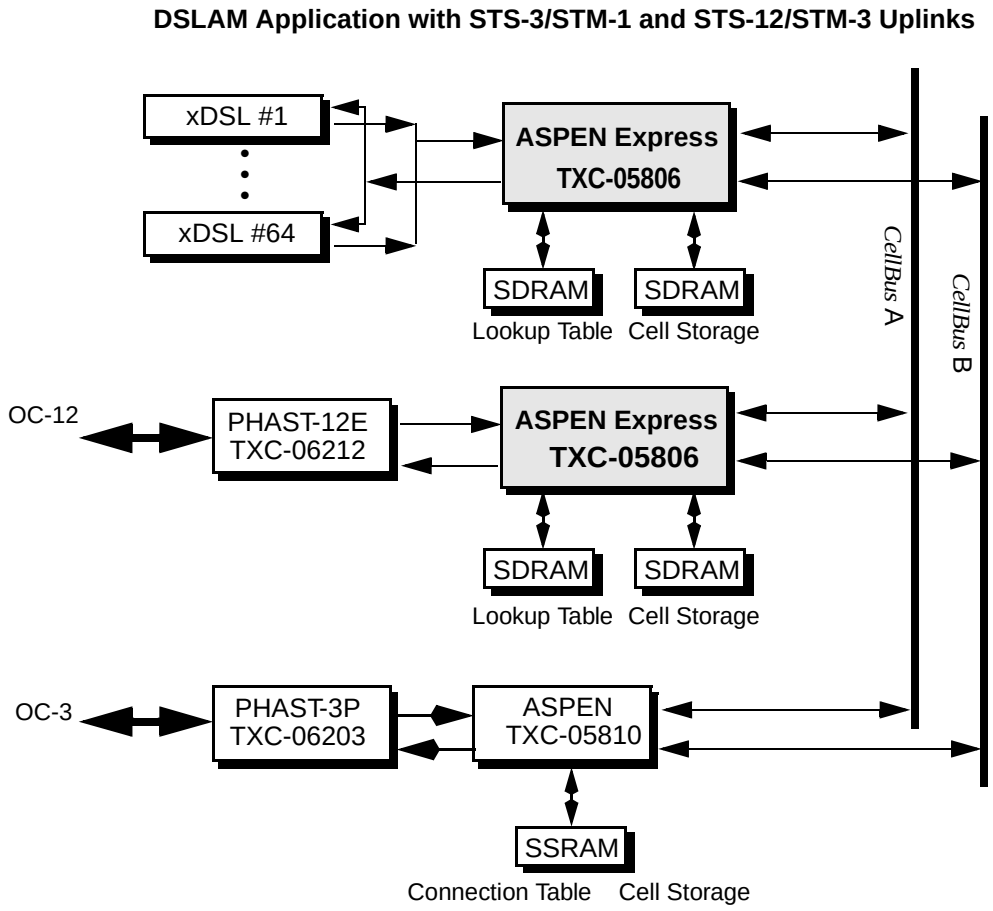


Figure 45. ASPEN Express TXC-05806 and Related Product Applications

PRODUCT PREVIEW

PRODUCT PREVIEW

STANDARDS DOCUMENTATION SOURCES

Telecommunication technical standards and reference documentation may be obtained from the following organizations:

ANSI (U.S.A.):

American National Standards Institute
25 West 43rd Street
New York, New York 10036
Tel: (212) 642-4900
Fax: (212) 398-0023
Web: www.ansi.org

The ATM Forum (U.S.A., Europe, Asia):

404 Balboa Street
San Francisco, CA 94118
Tel: (415) 561-6275
Fax: (415) 561-6120
Web: www.atmforum.com

ATM Forum Europe Office

Kingsland House - 5th Floor
361-373 City Road
London EC1 1PQ, England
Tel: 20 7837 7882
Fax: 20 7417 7500

ATM Forum Asia-Pacific Office

Hamamatsucho Suzuki Building 3F
1-2-11, Hamamatsucho, Minato-ku
Tokyo 105-0013, Japan
Tel: 3 3438 3694
Fax: 3 3438 3698

Bellcore (See Telcordia)

CCITT (See ITU-T)

EIA (U.S.A.):

Electronic Industries Association
Global Engineering Documents
15 Inverness Way East
Englewood, CO 80112
Tel: (800) 854-7179 (within U.S.A.)
Tel: (303) 397-7956 (outside U.S.A.)
Fax: (303) 397-2740
Web: www.global.ihs.com

ETSI (Europe):

European Telecommunications Standards Institute
650 route des Lucioles
06921 Sophia-Antipolis Cedex, France
Tel: 4 92 94 42 00
Fax: 4 93 65 47 16
Web: www.etsi.org

GO-MVIP (U.S.A.):

The Global Organization for Multi-Vendor Integration Protocol (GO-MVIP)
3220 N Street NW, Suite 360
Washington, DC 20007

Tel: (800) 669-6857 (within U.S.A.)
Tel: (903) 769-3717 (outside U.S.A.)
Fax: (903) 769-3818
Web: www.mvip.org

ITU-T (International):

Publication Services of International Telecommunication Union
Telecommunication Standardization Sector
Place des Nations, CH 1211
Geneve 20, Switzerland

Tel: 22 730 5852
Fax: 22 730 5853
Web: www.itu.int

MIL-STD (U.S.A.):

DODSSP Standardization Documents Ordering Desk
Building 4 / Section D
700 Robbins Avenue
Philadelphia, PA 19111-5094

Tel: (215) 697-2179
Fax: (215) 697-1462
Web: www.dodssp.daps.mil

PCI SIG (U.S.A.):

PCI Special Interest Group
5440 SW Westgate Dr., #217
Portland, OR 97221

Tel: (800) 433-5177 (within U.S.A.)
Tel: (503) 291-2569 (outside U.S.A.)
Fax: (503) 297-1090
Web: www.pcisig.com

Telcordia (U.S.A.):

Telcordia Technologies, Inc.
Attention - Customer Service
8 Corporate Place Rm 3A184
Piscataway, NJ 08854-4157

Tel: (800) 521-2673 (within U.S.A.)
Tel: (732) 699-2000 (outside U.S.A.)
Fax: (732) 336-2559
Web: www.telcordia.com

TTC (Japan):

TTC Standard Publishing Group of the Telecommunication Technology Committee
Hamamatsu-cho Suzuki Building
1-2-11, Hamamatsu-cho, Minato-ku
Tokyo 105-0013, Japan

Tel: 3 3432 1551
Fax: 3 3432 1553
Web: www.ttc.or.jp

- NOTES -

PRODUCT PREVIEW

PRODUCT PREVIEW information documents contain information on products in their formative or design phase of development. Features, characteristic data and other specifications are subject to change. Contact TranSwitch Applications Engineering for current information on this product.

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