i5140-N

SD/MMC Memory Card Controller Datasheet

Version 1.1

iCreate Technologies Corporation

2006/3/8

Data sheet marking

iCreate uses various markings in the data sheet to designate each document phase as it relates to the product development stage.

Marking	Description
Objective Specification	The objective specification contains data for new product development.
Advance Information	The information is on products in the design phase. Your designs should not be finalized with this information.
Preliminary	This is preliminary information on new products but not yet fully characterized. The specifications in these data sheets are subject to change in any manner without notice.
No Marking	Information contained in the data sheet is on products in full production.

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1. Introduction

1.1. General description

i5140 is a high performance flash memory controller for SD/MMC interface flash memory cards. This chip is based on iCreate 3rd-generation flash engine to achieve high data transfer rate. The enhanced designs include high performance CPU, multi-bank flash access, 8/16-bit flash interface, and Reed-Solomon based ECC capability. Voltage-Regulator, Power-on-reset and RC oscillator are integrated to reduce BOM cost and PCB area. Typical applications of i5140 are SD, miniSD, MMC and RS-MMC memory card.

1.2. Features

- Compliant to SD1.1, MMC4.1 standards
- 1/4/8-bit host data transfer
- SD/MMC Clock frequency 0 ~ 52 MHz
- Integrated power-on-reset and RC oscillator
- On-the-fly ECC (4 Byte per 528 Byte)
- Wear-leveling mechanism
- Support large block NAND type flash
- Support small block NAND type flash
- Support AG-AND type flash
- 4 flash chips enable
- Auto-suspend to conserve energy

1.3. Block diagram

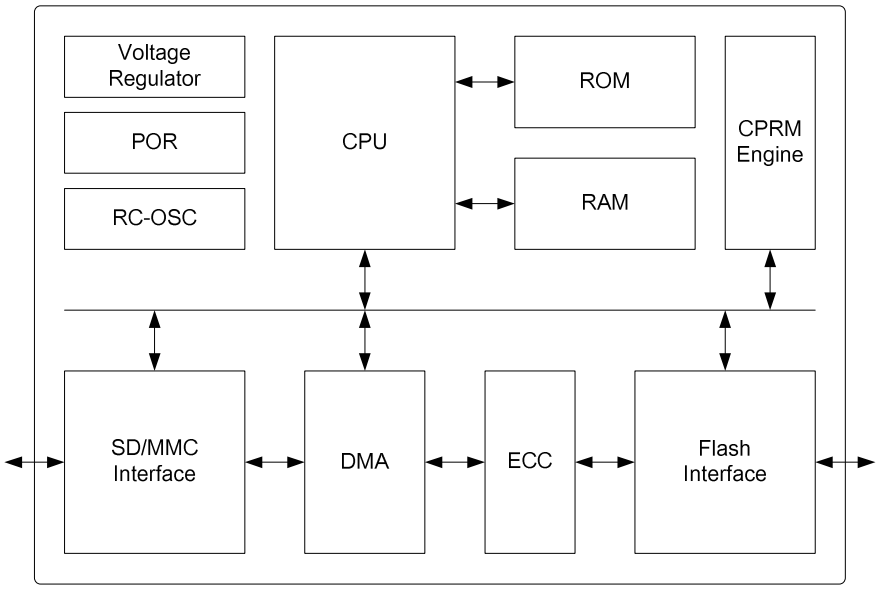


Figure 1. Block diagram

2. Pin Diagram and Description

2.1. Pin Diagram

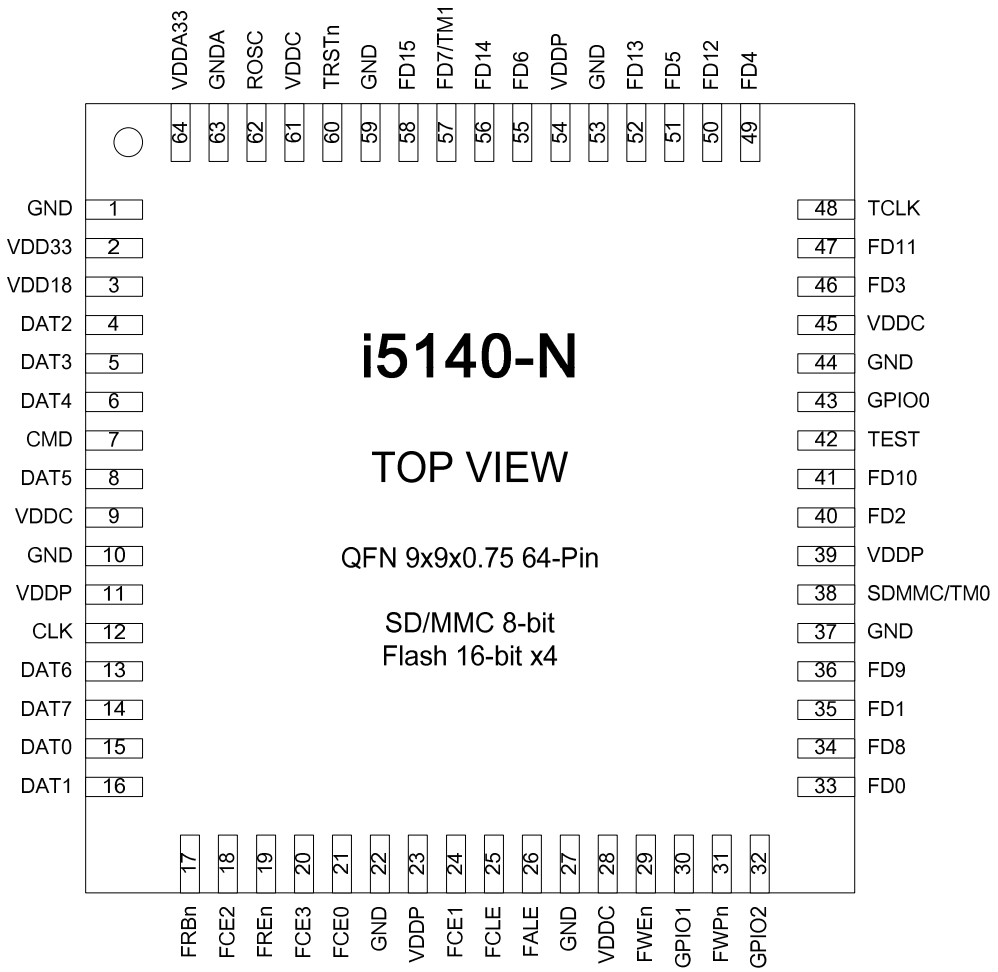


Figure 2. Pin Diagram

2.2. Pin Description

Pin Name	Type*1	Description
VDD33	Power	Internal regulator 3.3V input pin.
VDD18	Power	Internal regulator 1.8V output pin.
VDDC	Power	1.8V power supply for core.
VDDP	Power	3.3V power supply for I/O.
GND	Power	Power supply ground.
VDDA33	Power	3.3V power supply for analog block.
GNDA	Power	Power supply ground for analog block.
ROSC	Analog	Connect 3.9K Ohm resister to VDD18 for internal 50MHz clock generator.
DAT0~7	IO/ST/PUC	SD/MMC Data Bus
CMD	IO/ST/PUC	SD/MMC Command/Response signal
CLK	I/ST	SD/MMC Clock input.
FCE0~7	IO/ST/PUC	Flash chip enable signal.
FRBn	IO/ST/PUC	Flash Ready/Busy signal
FCLE	IO/ST/PUC	Flash command latch enable
FALE	IO/ST/PUC	Flash address latch enable.
FREn	IO/ST/PUC	Flash read enable.
FWEn	IO/ST/PUC	Flash write enable.
FWPn	IO/ST/PUC	Flash write protect.
FD0~FD15	IO/ST/PUC	Flash data bus.
SDMMC	I	SD/MMC Selection. MMC Mode when Tie-High and SD Mode when Tie-Low.
TEST	I/PD	Test mode enable. This pin must floating or tie-low when normal operation.
TCLK	I/ST	Clock for test mode.
TRSTn	I/PD	Reset for test mode.
GPIO0~2	IO/ST/PUC	General purpose I/O pin.

*1: I/O Type I: Input pin. IO: Bidirectional pin.ST: pin with S Trigger. Analog: Analog pin

PD: pin with pull-down resister. PUC: pin with controllable pull-up resister. Power: Power Pin

Table 1. Pin Description

3. Internal Regulator, Power-ON Reset and RC oscillator

3.1. Regulator

The internal voltage regulator input 3.3V and output 1.8V used for core power supply as shown in Figure 3.

3.2. Power-on-reset and brown-out-reset

The internal reset control unit has power-on-reset (POR). To use internal POR, only provide 3.3V to VDDA33 and GNDA connected to ground as shown in Figure 3.

3.3. RC oscillator

An integrated RC oscillator can be used to reduce BOM cost. ROSC must be connected to 1.8V through a resistor, as shown in Figure 3.

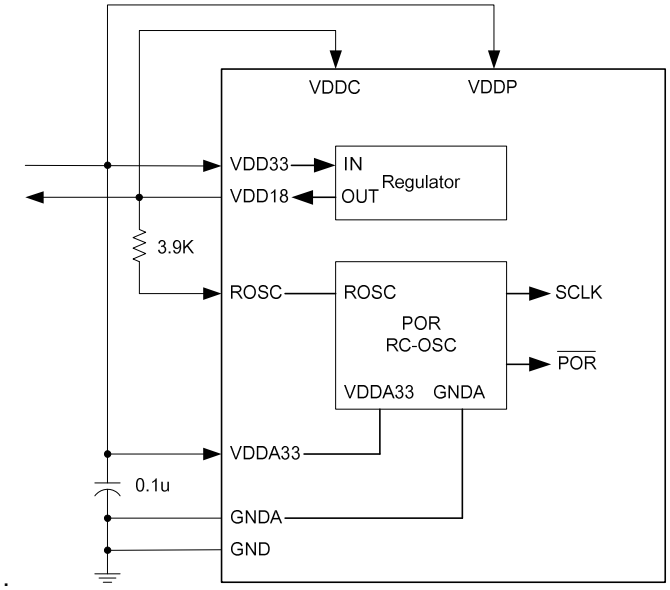


Figure 3. Pin connection to use internal Regulator, Power-ON Reset and Oscillator

4. Electrical specifications

4.1. Absolute maximum ratings

Symbol	Description	Value	Unit	Notes
V_{DD}	I/O Power Supply Voltage	- 0.3 to +3.6	V	VDDP, VDD33, VDD33A
V_{DDC}	Core Power Supply Voltage	- 0.3 to +1.98	V	VDDC
V_{IN}, V_{OUT}	All input/output voltages	- 0.3 to VDD + 0.3	V	
Tstg	Storage temperature range	- 45 to +85	℃	

Table 2. Absolute maximum ratings

4.2. Recommended operating conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	I/O Power Supply Voltage	2.7	3.3	3.6	V
V_{DDC}	Core Power Supply Voltage	1.62	1.8	1.98	V
T_{OPR}	Operating temperature	0		70	°C

Table 3. Recommended operation conditions

4.3. Power-on-reset characteristics

Symbol	Parameter	Typ.	Unit
V_T(POR)	Threshold voltage of power-on-reset	2.6	V

Table 4. Power-on-reset characteristics

4.4. Bus Operating Conditions

4.4.1. General

Parameter	Symbol	Min.	Max.	Unit	Remark
Peak voltage on all lines		-0.5	3.6	V	
All inputs					
Input Leakages Current		-10	10	μA	
All outputs					
Output Leakages Current		-10	10	μA	

Table 5. Bus Operating Conditions – General

4.4.2. Bus Signal Level

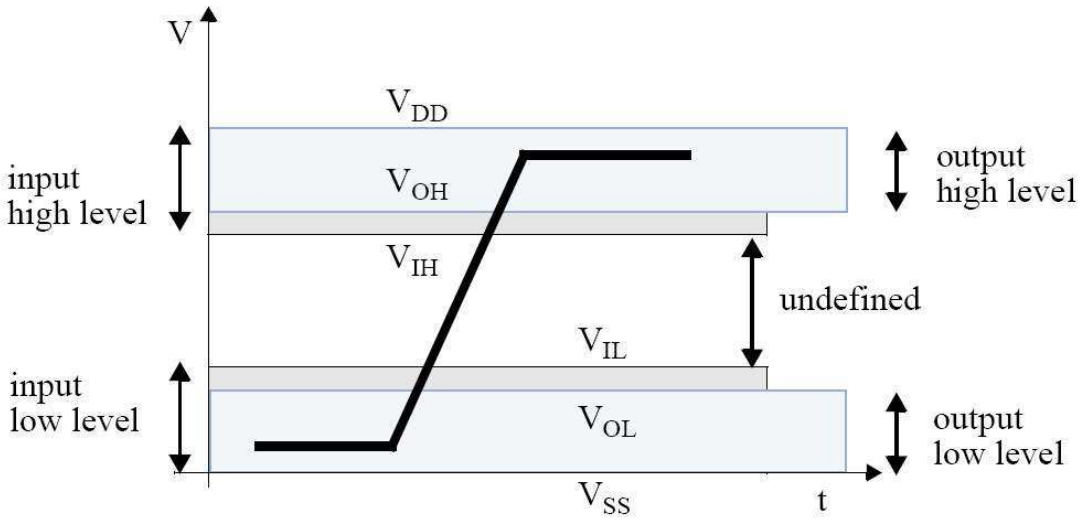


Figure 4. Bus Signal Level

4.5. SD Mode Bus Operating Conditions

4.5.1. Deault

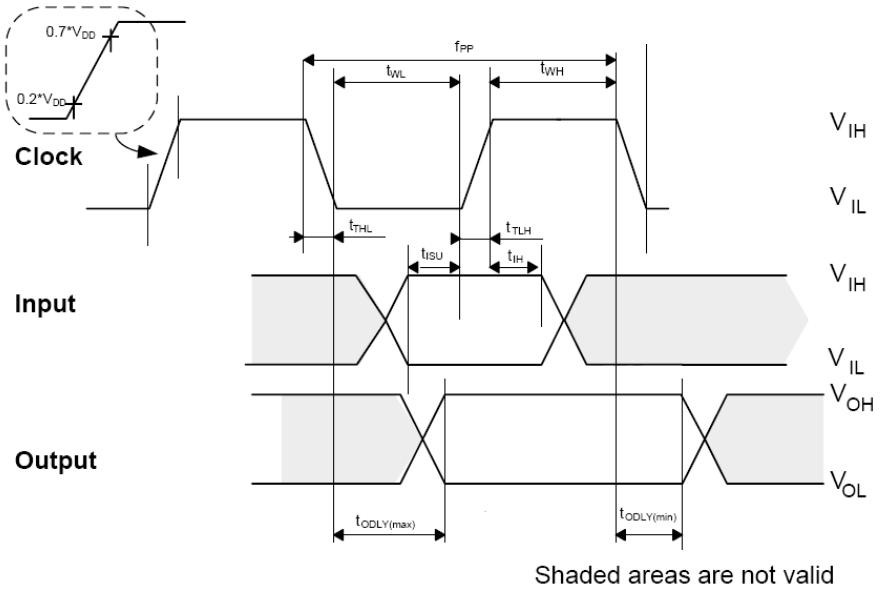


Figure 5. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (Default)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	25	MHz	$C_{CARD} \leq 10pF$ (1 card)
Clock frequency Identification Mode	f_{OD}	$0_{(1)}$/100	400	KHz	$C_{CARD} \leq 10pF$ (1 card)
Clock low time	t_{WL}	10		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock high time	t_{WH}	10		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock rise time	t_{TLH}		10	ns	$C_{CARD} \leq 10pF$ (1 card)
Clock fall time	t_{THL}		10	ns	$C_{CARD} \leq 10pF$ (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	$C_{CARD} \leq 10pF$ (1 card)
Input hold time	t_{IH}	5		ns	$C_{CARD} \leq 10pF$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	$C_L \leq 40pF$ (1 card)
Output Delay time during Identification Mode	t_{ODLY}	0	50	ns	$C_L \leq 40pF$ (1 card)

(1) 0 Hz means to stop the clock. The given minimum frequency range is for cases were continues clock is required.

Table 6. SD Mode: Bus Timing – Parameters Value (Default)

4.5.2. High Speed

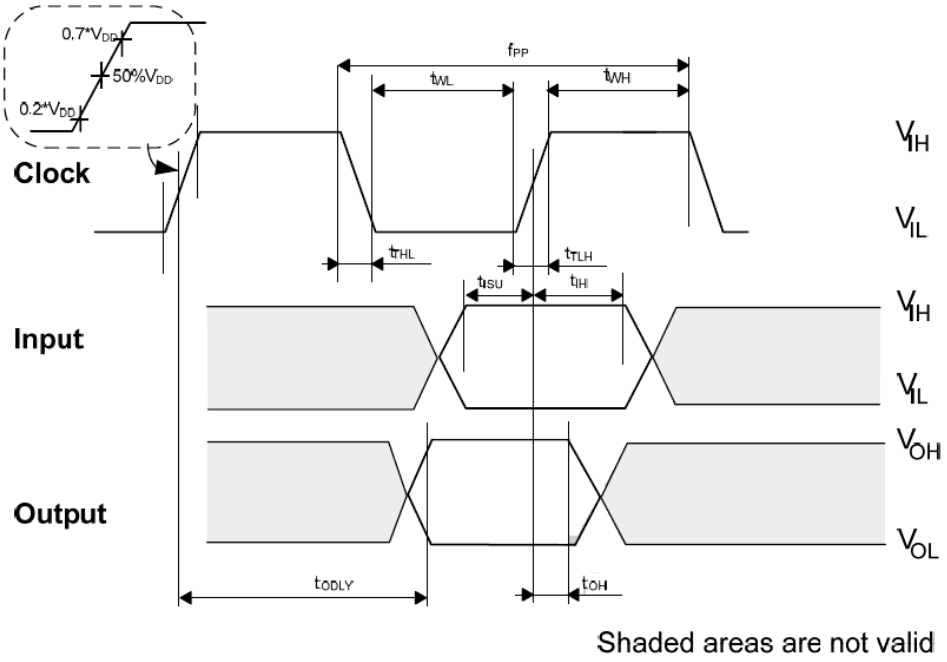


Figure 6. SD Mode: Timing Diagram Data Input/Output Referenced to Clock (High-Speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min(V_{IH}) and max (V_{IL}),					
Clock frequency Data Transfer Mode	f_{PP}	0	50	MHz	$C_{CARD} \leq 10pF$ (1 card)
Clock low time	t_{WL}	7		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock high time	t_{WH}	7		ns	$C_{CARD} \leq 10pF$ (1 card)
Clock rise time	t_{TLH}		3	ns	$C_{CARD} \leq 10pF$ (1 card)
Clock fall time	t_{THL}		3	ns	$C_{CARD} \leq 10pF$ (1 card)

Parameter	Symbol	Min.	Max.	Unit	Remark
Input CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	$C_{CARD} \leq 10pF$ (1 card)
Input hold time	t_{IH}	2		ns	$C_{CARD} \leq 10pF$ (1 card)
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	$C_L \leq 40pF$ (1 card)
Output Hold time	t_{OH}	2.5		ns	$C_L \geq 15pF$ (1 card)
Total System capacitance for each line	C_L		40	pF	1 card

(1) In order to satisfy severe timing, host shall drive only one card.

Table 7. SD Mode: Bus Timing – Parameters Values (High-Speed)

4.6. MMC Mode Bus Operating Conditions

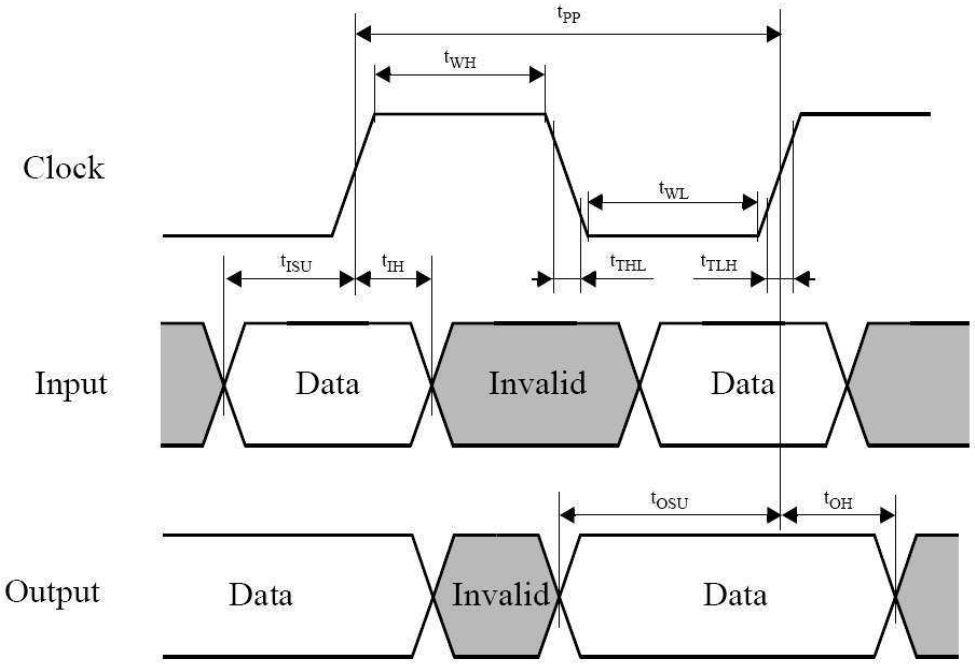


Figure 7. MMC Mode: Timing Diagram - Data Input/Output

4.6.1. Card Interface Timing

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)[2]	f_{PP}	0	26/52	MHz	C_L <= 30 pF Tolerance: +100KHz
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	Tolerance: +20KHz
Clock low time	t_{WL}	6.5		ns	C_L <= 30 pF
Clock rise time[3]	t_{TLH}		3	ns	C_L <= 30 pF
Clock fall time	t_{THL}		3	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	5		ns	C_L <= 30 pF
Output hold time	t_{OH}	5		ns	C_L <= 30 pF

Parameter	Symbol	Min	Max.	Unit	Remark
Signal rise time[4]	t_{rise}		3	ns	C_L <= 30 pF
Signal fall time	t_{fall}		3	ns	C_L <= 30 pF

Table 8. MMC Mode: High-Speed Card Interface Timing

1) All timing values are measured relative to 50% of voltage level
2) A MultiMediaCard shall support the full frequency range from 0-26Mhz, or 0-52MHz
3) Rise and fall times are measured from 10%-90% of voltage level
4) Rise and fall times are measured from 10%-90% of voltage level

Parameter	Symbol	Min	Max.	Unit	Remark
Clock CLK[1]					
Clock frequency Data Transfer Mode (PP)	f_{PP}	0	20	MHz	C_L <= 30 pF
Clock frequency Identification Mode (OD)	f_{OD}	0	400	kHz	
Clock low time	t_{WL}	10		ns	C_L <= 30 pF
Clock rise time[2]	t_{TLH}		10	ns	C_L <= 30 pF
Clock fall time	t_{THL}		10	ns	C_L <= 30 pF
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3		ns	C_L <= 30 pF
Input hold time	t_{IH}	3		ns	C_L <= 30 pF
Outputs CMD, DAT (referenced to CLK)					
Output set-up time	t_{OSU}	13.1		ns	C_L <= 30 pF
Output hold time	t_{OH}	9.7		ns	C_L <= 30 pF

1) All timing values are measured relative to 50% of voltage level
2) Clock rise and fall times are measured from VIL to VIH of voltage level

Table 9. MMC Mode: Backwards Compatible Card Interface Timing

4.7. Flash Interface Command Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCLH	FCLE hold time	10		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns

Table 10. Timing Parameters: Flash Interface Command Write

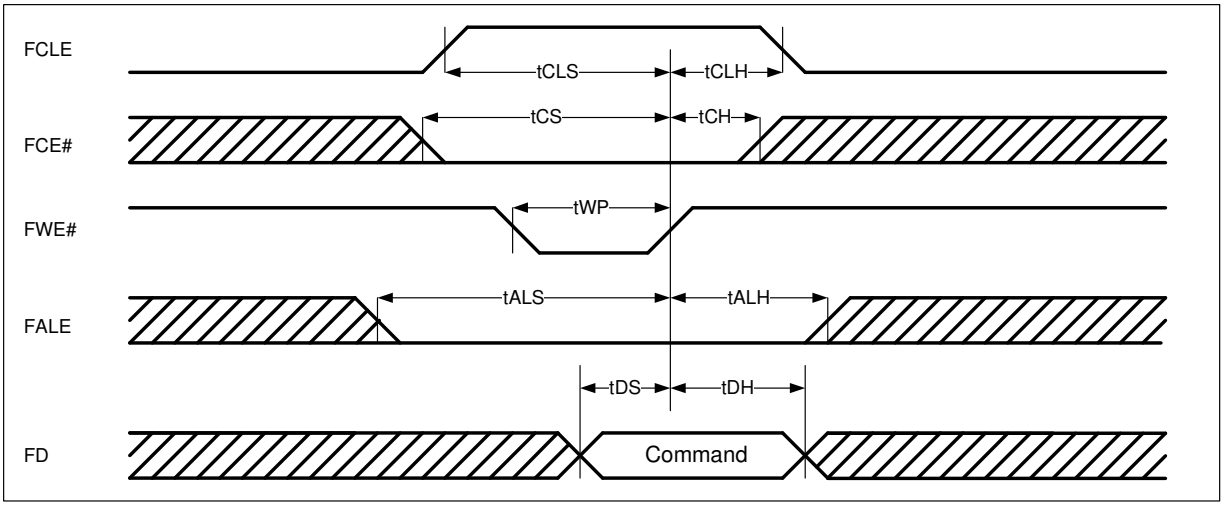


Figure 8. Timing Diagram: Flash Interface Command Write

4.8. Flash Interface Address Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLS	FCLE setup time	0		ns
tCS	FCE# setup time	0		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tWH	FWE# high hold time	15		ns
tALS	FALE setup time	0		ns
tALH	FALE hold time	10		ns
tDS	Data Setup time	20		ns
tDH	Data hold time	10		ns
tWC	Flash write cycle time	50		

Table 11. Timing Parameters: Flash Interface Address Write

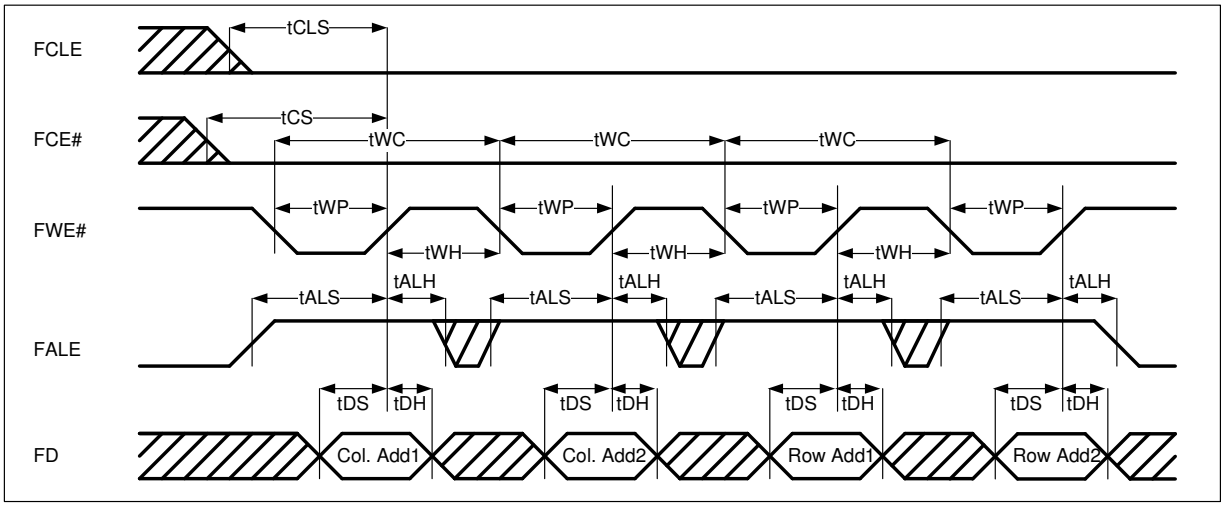


Figure 9. Timing Diagram: Flash Interface Address Write

4.9. Flash Interface Data Write AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLH	FCLE hold time	10		ns
tCH	FCE# hold time	10		ns
tWP	FWE# pulse width	25		ns
tWH	FWE# high hold time	15		ns
tALS	FALE setup time	0		ns
tDS	Data setup time	20		ns
tDH	Data hold time	10		ns
tWC	Flash write cycle time	50		ns

Table 12. Timing Parameters: Flash Interface Data Write

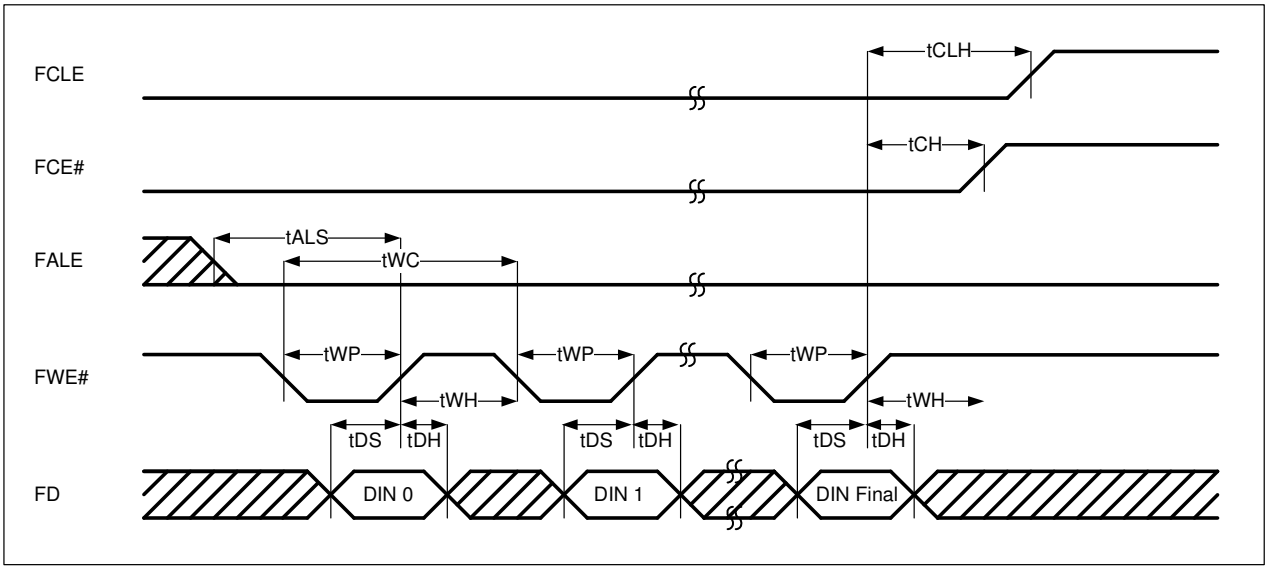


Figure 10. Timing Diagram: Flash Interface Data Write

4.10. Flash Interface Data Read AC characteristics

Symbol	Parameter	Min.	Max.	Unit
tCLR	FCLE to FRE# delay	10		ns
tAR	ALE to FRE# delay	10		ns
tRR	Ready to FRE# low	20		ns
tRC	Read cycle time	30		ns

Table 13. Timing Parameters: Flash Interface Data Read

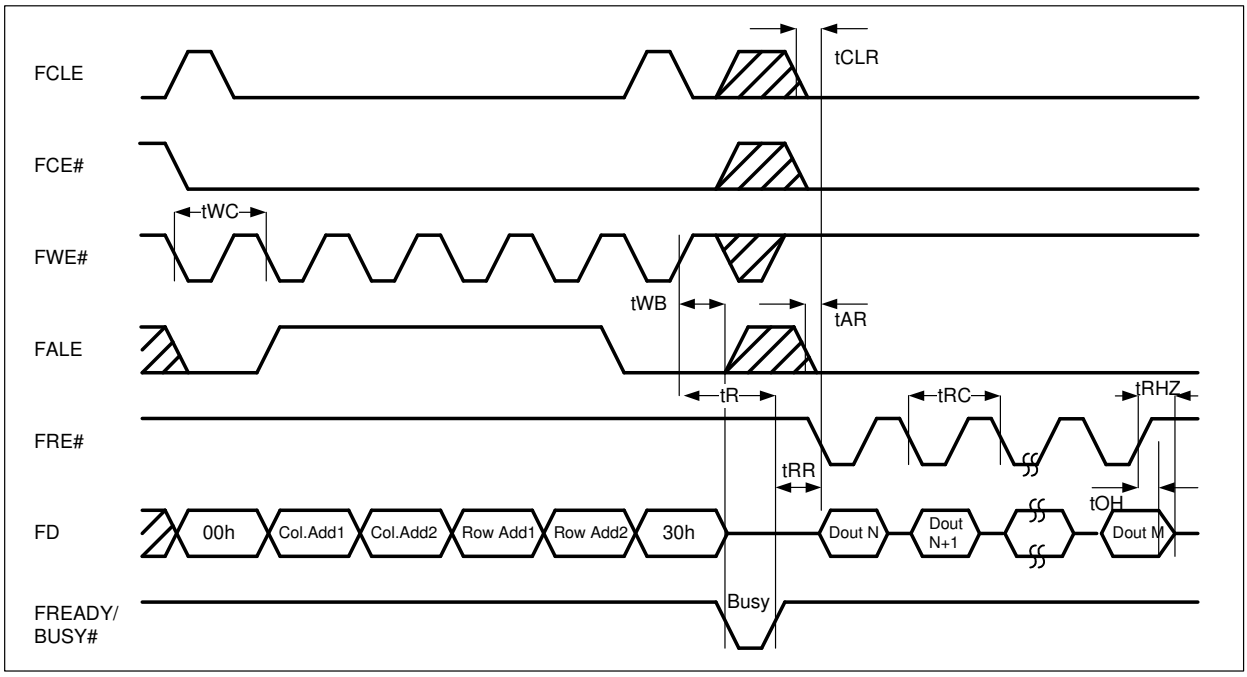


Figure 11. Timing Diagram: Flash Interface Data Read

5. Bond Pad Location

5.1. Bonding Diagram

Die-Size: 2388.5 um x 2337.8 um

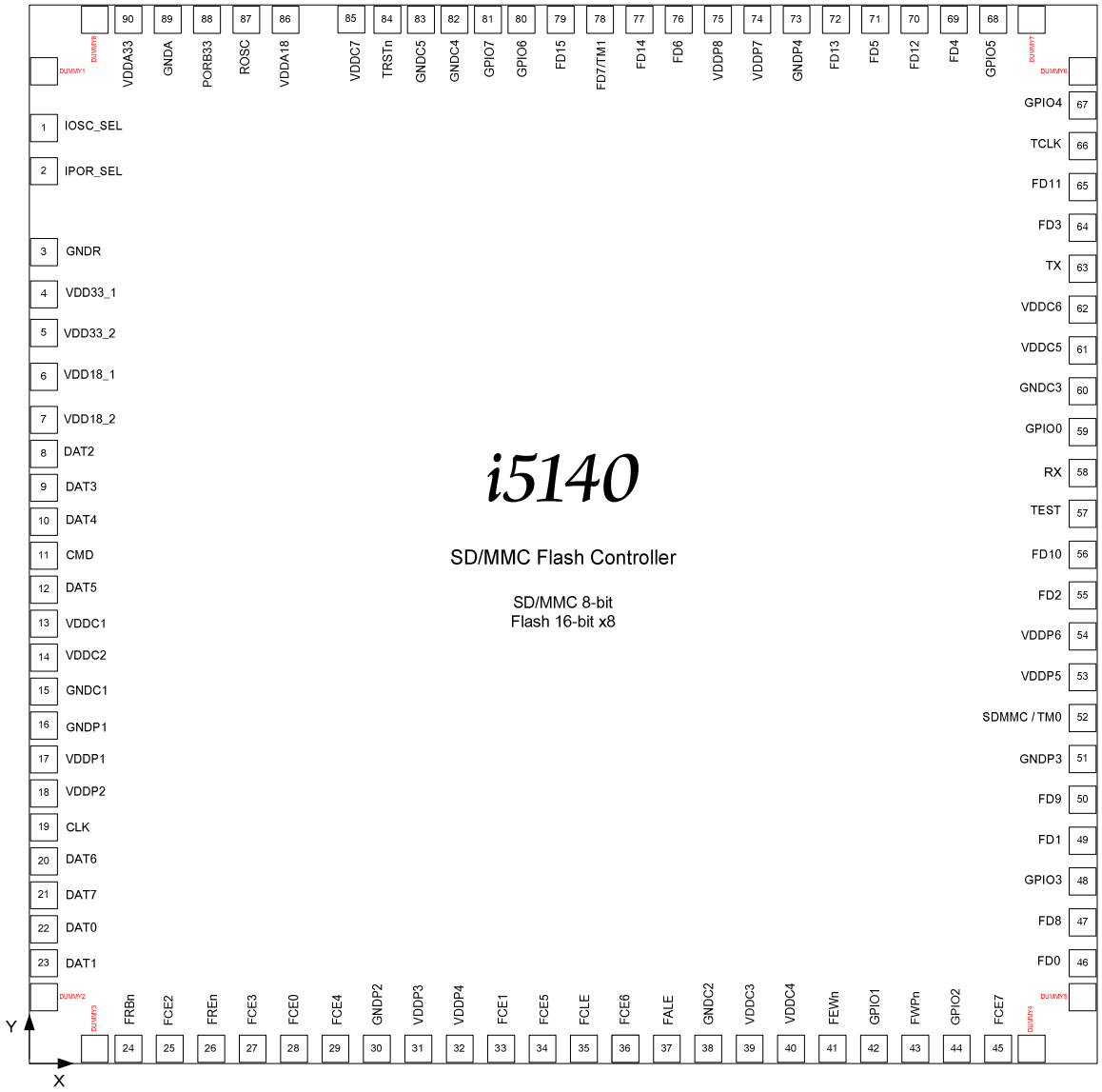


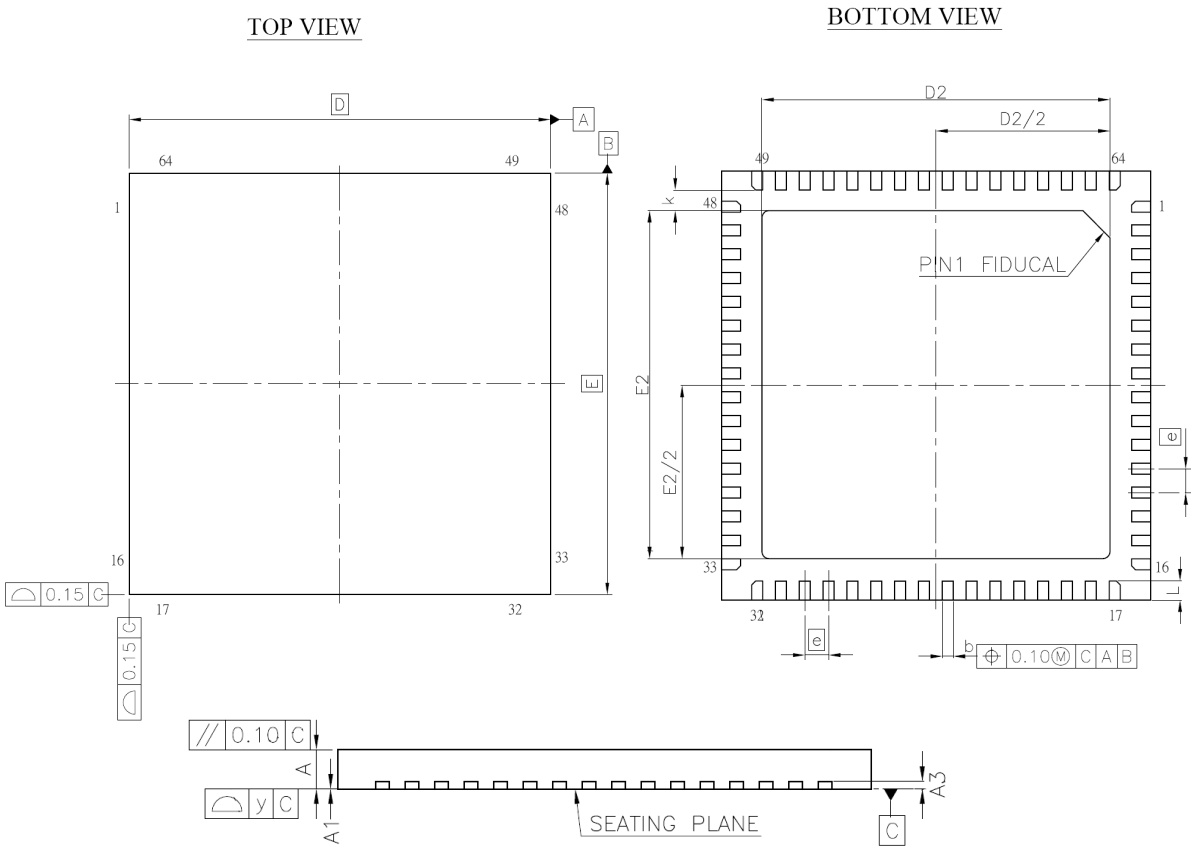
Figure 12. i5140 Die Bonding Diagram

5.2. Bond PAD Coordinate

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	IOSC_SEL	32.5	2065.935	31	VDDP	869.99	32.5	61	VDDC	2356	1574.95
2	IPOR_SEL	32.5	1970.88	32	VDDP	962.635	32.5	62	VDDC	2356	1665.18
3	GNDR	32.5	1791.9	33	FCE1	1055.275	32.5	63	TX	2356	1755.41
4	VDD33_1	32.5	1698.74	34	FCE5	1147.92	32.5	64	FD3	2356	1845.64
5	VDD33_2	32.5	1613.74	35	FCLE	1240.56	32.5	65	FD11	2356	1935.87
6	VDD18_1	32.5	1516.8	36	FCE6	1333.2	32.5	66	TCLK	2356	2026.1
7	VDD18_2	32.5	1421.5	37	FALE	1425.845	32.5	67	GPIO4	2356	2116.34
8	DAT2	32.5	1346.5	38	GNDC	1518.485	32.5	68	GPIO5	2155.88	2305.34
9	DAT3	32.5	1271.5	39	VDDC	1611.13	32.5	69	FD4	2067.945	2305.34
10	DAT4	32.5	1196.5	40	VDDC	1703.77	32.5	70	FD12	1980.02	2305.34
11	CMD	32.5	1121.5	41	FWEn	1796.41	32.5	71	FD5	1892.09	2305.34
12	DAT5	32.5	1046.5	42	GPIO1	1889.055	32.5	72	FD13	1804.165	2305.34
13	VDDC1	32.5	971.5	43	FWP	1981.695	32.5	73	GNDP	1716.24	2305.34
14	VDDC2	32.5	896.5	44	GPIO2	2074.34	32.5	74	VDDP	1628.315	2305.34
15	GNDC1	32.5	821.5	45	FCE7	2167	32.5	75	VDDP	1540.39	2305.34
16	GNDP1	32.5	746.5	46	FD0	2356	221.5	76	FD6	1452.46	2305.34
17	VDDP1	32.5	671.5	47	FD8	2356	311.73	77	FD14	1364.535	2305.34
18	VDDP2	32.5	596.5	48	GPIO3	2356	401.96	78	FD7	1276.61	2305.34
19	CLK	32.5	521.5	49	FD1	2356	492.19	79	FD15	1188.685	2305.34
20	DAT6	32.5	446.5	50	FD9	2356	582.42	80	GPIO6	1100.76	2305.34
21	DAT7	32.5	371.5	51	GNDP	2356	672.65	81	GPIO7	1025.76	2305.34
22	DAT0	32.5	296.5	52	TM0	2356	762.88	82	GNDC	950.76	2305.34
23	DAT1	32.5	221.5	53	VDDP	2356	853.11	83	GNDC	875.76	2305.34
24	FRBn	221.5	32.5	54	VDDP	2356	943.34	84	TRSTn	800.76	2305.34
25	FCE2	314.14	32.5	55	FD2	2356	1033.57	85	VDDC	725.76	2305.34
26	FREn	406.78	32.5	56	FD10	2356	1123.8	86	VDDA18	573.2	2305.34
27	FCE3	499.425	32.5	57	TEST	2356	1214.03	87	ROSC	485.275	2305.34
28	FCE0	592.065	32.5	58	RX	2356	1304.26	88	PORB33	397.35	2305.34
29	FCE4	684.71	32.5	59	GPIO0	2356	1394.49	89	GNDA	309.425	2305.34
30	GNDP	777.35	32.5	60	GNDC	2356	1484.72	90	VDDA33	221.5	2305.34

Table 14. i5140 Bond PAD Coordinate

6. Package Dimensions



SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.61	0.66	0.70	24.0	26.0	28.0
A1	0	0.02	0.05	0	0.79	1.97
A3	0.127 REF			5 REF		
b	0.18	0.25	0.30	7.1	9.8	11.8
D	9.00 BSC			354.3 BSC		
D2	7.20	7.30	7.40	283	287	291
E	9.00 BSC			354.3 BSC		
E2	7.20	7.30	7.40	283	287	291
e	0.50 BSC			19.7 BSC		
k	0.20			7.9		
L	0.30	0.40	0.50	11.8	15.7	19.7
y	0.08			3.15		

Figure 13. i5140-N Package Diagram