TEXAS INSTRUMENTS

TLV1562 EVM

User's Guide

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Mixed Signal Products

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Read This First

How to Use This Manual

This document contains the following chapters:

- Chapter 1 – EVM Overview
- Chapter 2 –Getting Started
- Chapter 3 – User Configurations
- Chapter 4 – Control Modes

Related Documentation From Texas Instruments

Data Sheets:

THS3001	Literature No. SLVS022H
SN74LVT245B	Literature No. SLOS217A
TLE2142CD	Literature No. SLOS183A
SN74AHCT74	Literature No. SCLS263I
SN74AHCT32	Literature No. SCLS248G
SN74AHCT00	Literature No. SCLS229F
SN74AHCT163	Literature No. SCLS337F
SN74AHCT374	Literature No. SCLS241H
SN74ABTH245B	Literature No. SCBS663D
SN74AHCT139	Literature No. SCLS267I
SN74AHC08	Literature No. SLCS236C
SN74ALVC08	Literature No. SCES101D
TPS7101	Literature No. SLVS092F
TPS76133	Literature No. SLVS178A
THS5651A	Literature No. SLAS260
THS5641A	Literature No. SLAS199A
THS5671A	Literature No. SLAS201
THS5661A	Literature No. SLAS247
TLV1562	Literature No. SLAS162
TLV5618A	Literature No. SLAS230E

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Chapter 1

EVM Overview

This chapter gives a general overview of the TLV1562 evaluation module (EVM), and provides a general description of the features and functions to consider in using this module properly.

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1.1 System Block Diagram

The TLV1562 EVM provides a practical platform for evaluating the following devices:

- TLV1562 10-bit resolution, 2 MSPS throughput, CMOS low-power, parallel output analog-to-digital converter.
- TLV5618A 12-bit resolution, 1.2 MSPS update rate, serial DAC
- THS5651 10-bit resolution, 100 MSPS update rate, parallel CommsDAC

The EVM supports the SOIC (DW) package style, but all devices are available in other packages — see the relevant data sheets SLAS162, SLAS156E, SLAS197A and Table 1–1.

Table 1–1. Package Styles Available

Device	D Package† Supported?	DW Package‡ Supported?	PW Package§ Supported?
TLV1562	No	Yes, 28 pins	Yes, 28 pins
TLV5618A	Yes, 8 pins	No	No
THS5651A	No	Yes, 28 pins	Yes, 28 pins

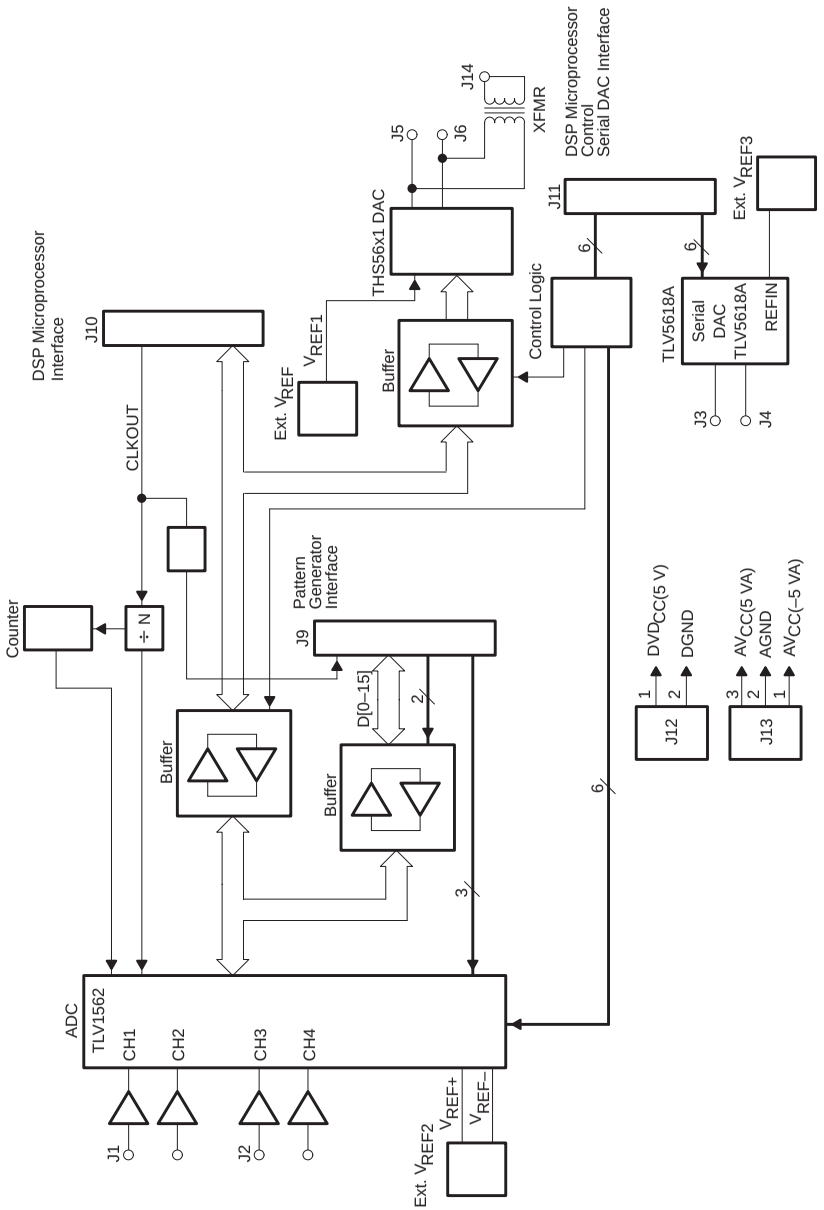
† The D package is a TSSOP device, with pins on a 0.65–mm pitch.

‡ The DW package is a small outline (SOIC) device, with pins on a 1.27–mm pitch.

§ The PW package is a TSSOP device, with pins on a 0.65–mm pitch.

Figure 1–1 shows the basic elements of the TLV1562 EVM. This comprises input buffers, control logic, a CommsDAC, a serial DAC, external Vrefs, and an RF transformer. This illustration provides a general overview of the EVM. It is not meant to replace the circuit diagram, but to give a brief indication of the features and functions available. It should be read in combination with the circuit diagram supplied and the device data sheet SLAA162.

Figure 1–1. Block Diagram



1.2 TLV1562 ADC System Outline

This printed wiring board (PWB) EVM supports the TLV1562 analog-to-digital converter and two different types of DACs.

- THS5641A, THS5651A, THS5661A, THS5671A
- TLV5618A

The THS56X1 family of DACs has parallel data input. The resolution and maximum sampling frequency is the main difference between these parts. The TLV5618A is a 12-bit resolution serial data device. General features of these DACs are given in Table 1–2.

Table 1–2. General ADC/DAC Features

Device	Resolution	Output Channels	Supports Vref_int/ Vref_Ext	Throughput VDD =3.3V	Throughput VDD= 5 V	Available Package	EVM Order Number
TLV1562	10-bit	D[0–9]	Vref_Ext only	1.6 MSPS	2 MSPS	DW/PW	TLV1562 with TLV5618A and THS56X1
TLV5618A	12-bit	1	Vref_Ext only	No	1.21 MSPS	D,P,JG,FK	TLV1562 with TLV5618A and THS56X1
THS5671A	14-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	TLV1562 with TLV5618A and THS56X1
THS5661A	12-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	TLV1562 with TLV5618A and THS56X1
THS5651A	10-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	TLV1562 with TLV5618A and THS56X1
THS5641A	8-bit	2	Yes	67 MSPS	100 MSPS	DW/PW	TLV1562 with TLV5618A and THS56X1

1.2.1 THS5671A/THS5661A/THS5651A/THS5641A CommsDAC

The low-power CMOS CommsDAC device integrates a 1.2-V bandgap reference, a current-source-array, a control amplifier, output current switches and input latches/logic for controlling the differential output current switches. The device has good linearity and excellent SFDR specification, symmetrical output ON/OFF switching, differential output, and can directly drive a 50-Ω load. The CommsDAC family consists of pin compatible 14-, 12-, 10-, and 8-bit DACs. All devices offer identical user interface and operate from an analog supply of 5 V and a digital supply of 3.3 V or 5 V. The THS56X1 full-scale current is adjustable from 2 mA to 20 mA. Power dissipation at 5 V is less than 175 mW and in sleep mode the standby power is about 25 mW. The THS56X1 is driven by the on-chip analog reference voltage or by an external reference voltage.

The THS56X1digital-to-analog converter (DAC) presented on the EVM can be used in loopback mode, where the ADC output is fed directly into the DAC. It can also be used as an independent device with either the DSP starter kit (DSK) interface or a suitable pattern generator (see TI's *THS56x1 EVM for the THS5641/51/61/71 8-Bit, 10-Bit, 12-Bit, and 14-Bit ADC* User's Guide, Literature number SLAU032 for more details).

1.2.2 TLV5618A Serial DAC

The TLV5618A is a dual output 12-bit serial data acquisition system with buffered reference inputs and analog outputs. Digital control of the device is over a 3-wire CMOS-compatible serial bus. The digital communication protocols include the SPI, QSPI and Microwire. This chip receives a 16-bit word for programming and producing the analog output. The device runs on a low voltage +5 V supply and a nominal 2.048 V external Vref. A power-on reset function is incorporated in the device to ensure consistent start-up conditions. The input data update rate is 1.21 MSPS and the device has a software power-down mode.

As normally designed, the ADC output data is stored in the DSP onboard memory so that they can be processed at a later time. This allows better throughput of data from both the ADC and the DACs. Consideration of how the application software handles the hardware interface between the DSP and DAC can play a major part in the data transfer process.

The serial DAC, for example, can be used to convert the data stored in memory to an analog signal. An oscilloscope is used to compared the serial DAC output and the ADC analog input.

1.2.3 TLV1562 Parallel ADC

Data sheet SLAS162 and application report SLAA040 detail how to use the TLV1562, together with the THS56X1 DAC and TLV5618A, to build a complete data acquisition system. The TLV1562 device has a number of unique features: software programmable power down, auto power down, Avdd supply range 2.7 V to 5.5 V, low power consumption, simultaneous sample and hold, programmable conversion modes, built-in multiplexer with 2 differential or 4 single-ended input channels, internal or external supplied device clock, binary or 2s complement output, and DSP/microprocessor parallel interface. The four conversion modes are: mono interrupt, dual interrupt, mono continuous, and dual continuous. The converter has a pair of differential high-impedance reference inputs that make it somewhat easy to do ratiometric conversion, input scaling, and isolation of the converter analog circuits from noise that may be present on the power supply lines.

The device has a ±5% maximum mid-scale error, full-scale error, and zero-scale error due to gain error in the sample and hold amplifier. However, the mid-scale error can be compensated for by performing a device calibration after powering up the part.

1.2.4 Control/Interface

1.2.4.1 C542 DSP Interface

The TLV1562 has a chip-select ($\overline{CS}$) pin, input clock (CLKIN), sample/conversion start signal ($\overline{CSTART}$), read signal input ($\overline{RD}$), write signal ($\overline{WR}$), and 10 parallel data I/O lines (D9:0).

The converter integrates the $\overline{CSTART}$ signal to carry out sampling and conversion timing without using the parallel data bus. The TMS320C542 has only one general-purpose output. As a result the $\overline{CSTART}$ signal is generated with address decoder logic.

The schematic diagram in Figure 1-2 shows the pin-to-pin connections between the TLV1562 EVM and the TMS320C542 DSKplus. It is relatively easy to test the four ADC modes of operation with the configuration in Figure 1-2.

Figure 1–2. TLV1562 to C54X DSP Interface

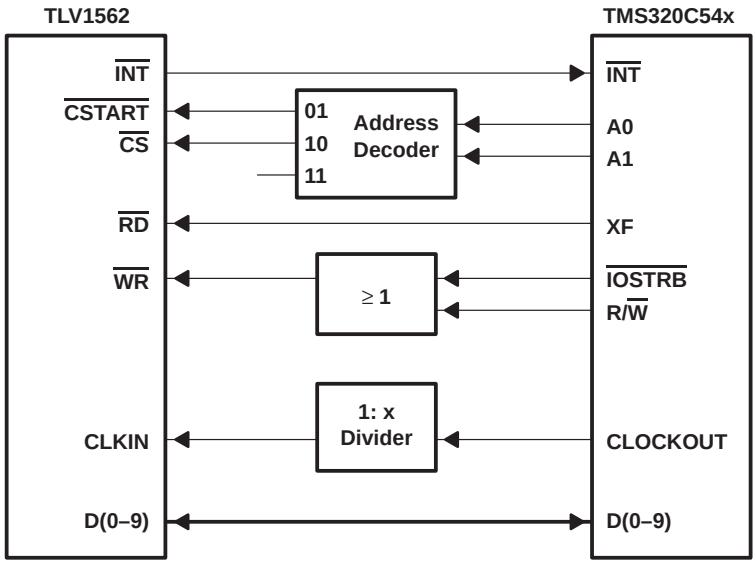
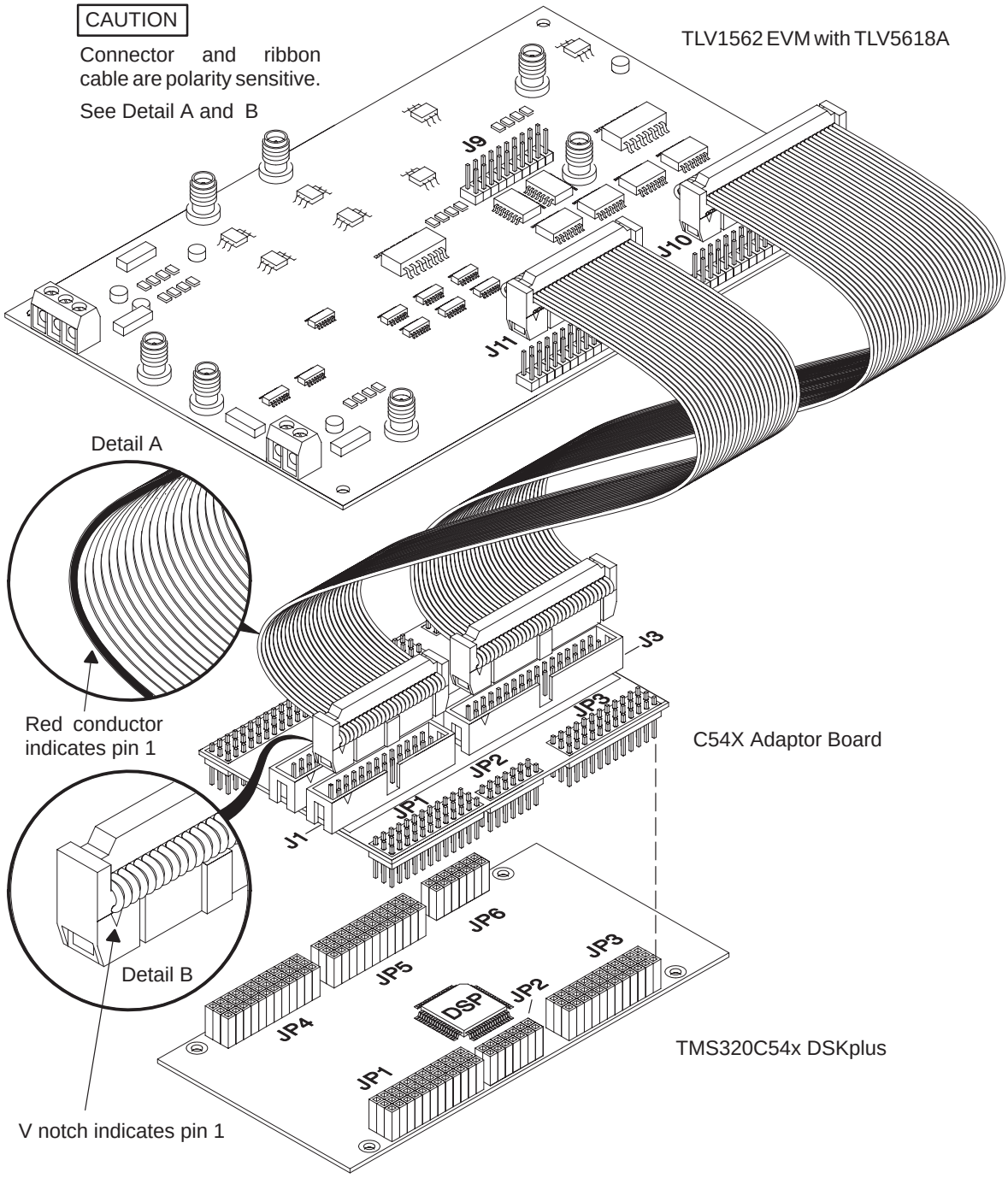


Figure 1–3. C542 DSKplus Organization



1.2.4.2 Logic Analyzer/Pattern Generator Interface

A separate interface connector (J9) interfaces a pattern generator to the EVM. The connector J9 interfaces directly to a HP16500C with HP16555D logic analyzer card and HP16522A pattern generator card. The HP16522A provides stimulus for the TLV1562 device.

1.2.4.3 Operational Amplifier Interface Circuit

The THS3001 is the basic circuit element of the op amp interface circuit used in this design. The device is a high-speed, current feedback operational amplifier suitable for driving a high capacitance load. Some of the other device features are: 6500-V/µs slew rate, –96 dBc distortion figure, 450 MHz bandwidth, 40 nS settling time, and ±5-V supply voltages.

The op amp interface circuit is used to buffer the analog input signal on its way to the TLV1562 input channel. Each amplifier provides unity gain and the amplifier noninverting input is connected to a dc voltage used to offset the input signal.

1.2.4.4 External Voltage Reference Circuits

A TL1431 precision shunt voltage regulator, a resistor network, and two THS3001 op amps, configured as unit gain noninverting buffer amplifiers provide the TLV1562 device reference voltages VREFP and VREFM. The TL1431 has 0.4% initial accuracy and a TC (temperature coefficient) of 30 ppm/°C, making the device a suitable voltage reference for a 10-bit ADC operating in a temperature controlled environment. Wide-range temperature operation requires a more precise voltage reference, such as, the VRE3025.

1.2.4.5 TLV5618A Serial DAC Interface

This device is a 12-bit serial input and output data converter with a digital interface that can be clocked at speeds up to 20 MHz. The analog output update rate is 1.21 MSPS and two outputs are available on an 8-pin package device. In this application the buffered SPI port of the DSP provides the DSP interface to the serial DAC.

1.2.4.6 THS56X1 Parallel DAC Interface

The 12-bit resolution THS5661A or 10-bit resolution THS5651A DAC, often used on the TLV1562 EVM board, can update its output at 100 MSPS. The two outputs can each supply up to 20mA of current. Sixteen data lines (D15:0), two address lines (A0, A1) and the $\overline{\text{IOSTROBE}}$ control line from the DSP are used to interface the DAC.

1.3 EVM Operating Modes

There are four modes of operation for the EVM:

- ❑ DSK/Microprocessor mode
- ❑ Serial DAC mode
- ❑ Parallel DAC mode
- ❑ Pattern generator mode

Each mode is discussed below.

1.3.1 C542 DSKplus/Microprocessor Mode

Running the application software causes the C542 DSP starter kit (DSK) to supply the sample clock, the EVM device-select control signals, and the ADC configuration data via the 16-bit data bus. The software stores the ADC output data words in onboard DSP memory.

On the EVM board, a divide by 4 circuit generates the ADC CLKIN signal using the CLKOUT signal coming from the DSP. Address lines A0 and A1 are used to create $\overline{CS}$, $\overline{CSTART}$ and the $\overline{PDAC}$ signals. Both $\overline{R/W}$ and $\overline{IOSTROBE}$ are used to generate the ADC $\overline{WR}$ control signal. The XF signal from the DSP directly drives $\overline{RD}$ pin. In Application Report SLAA040 an alternative implementation is described in Figure 2.

Jumpers W1, W2, W11, and W12 are used for selecting the ADC analog inputs. Jumpers W3, W4, W10, W23, W24, W25, W26, and W29 are used for configuring the ADC.

1.3.2 TLV5618A Serial DAC Mode

The DSP buffered SPI port provides the interface to the serial DAC. Under control of the application software routine, the DSP can be made to output previously stored ADC samples, through the SPI port, to the TLV5618A DAC. The serial DAC dual outputs are available at J3 and J4. When receiving data jumpers W14, W20, W21, and W22 are used to configure the DAC, a TPS71010 shunt regulator supplies the DAC 2.5V reference voltage.

1.3.2.1 McBSP Interface

The CLKS signal required for true McBSP interfacing could be provided through J8, fed from the output of a signal generator or a crystal oscillator.

The other McBSP implementation is as follows:

- ❑ Connect the signal coming from J8 to the CLKR input of the DSP.
- ❑ Connect the CLKX signal from the DSP to the SCLK pin of the DAC.

1.3.3 THS56X1 Parallel DAC Mode

In this application, data from the ADC can be fed to the parallel DAC and DSP or pattern generator at the same time — so called data loopback testing.

Single-ended analog output is derived from the THS56X1 CommsDAC differential output pair, IOUT1 and IOUT2, via a 1:1 RF transformer. The resistor network, which comprises R16, R49, and R50, reflects 50 Ω across the transformer output. The potentiometer, connected to the device BIASJ pin, is used to set the full-scale current. When 20 mA of current flows through the 50-Ω load resistor (connected to IOUT1 and IOUT2) the differential voltage measured across IOUT1 and IOUT2 terminals (J5 and J6) is 2Vp-p.

Jumpers W13, W15, W16, W25, and W26 are used to configure the DAC. W16 is used for setting the DAC operating modes. Mode 0 (W16, closed) supports binary input data word format. Mode 1 (W16, opened) sets the device to twos complement input configuration.

1.3.4 Pattern Generator Mode

Anyone working with hardware will know, probably from experience, that a pattern generator is a versatile piece of test equipment. It has the advantage of being immediately programmed to generate arbitrary waveforms and timings. The HP16500C with HP16555D logic analyzer card and HP16522A pattern generator card can be used to provide stimulus for the TLV1562 device. In practice, the pattern generator is programmed to output the required TLV1562 configuration data and control signals. The logic analyzer card is used to capture and store data coming from the ADC.

1.4 Power and Cabling Requirements

The EVM dc supply voltages are analog ±5 V and digital 5 V. These voltages should be supplied to the EVM through shielded twisted-pair wire for best performance. This type of power cabling minimizes any stray or transient pickup from the higher–frequency digital circuitry. A TPS76133 shunt regulator is used to generate 3.3-V from the digital 5 V (DVDCC). The 3.3 V is required when the ADC output buffers are SN74LVT245. If ribbon cables are used for interfacing to both J10 and J11, the crosstalk between adjacent conductors is minimized if shielded ribbon cables are used.

1.5 CommsDAC Output Configurations

The THS56X1 DAC output can be configured as single-ended outputs or as a differential output (see THS5661A, 12-bit, 100 MSPS, CommsDAC data sheet, SLAS200). The RF transformer is used to convert the differential pair IOUTA and IOUTB to single-ended output.

1.6 Printed-Circuit Assembly Options Available

To ensure the flexibility of the printed-circuit board (PCB), the TLV1562 EVM supports four possible commsDACs (THS56X1 devices) and a TLV5618A device. Table 1–3 shows the basic parameters of each digital-to-analog converter.

Table 1–3. Possible DACs

DAC Part No.	No. of Bits	Speed	EVM Order No.
TLV5618A	12	1.21 MSP	TLV1562 with TLV5618A
THS5671A	14	100 MSPS	TLV1562 with TLV5618A and THS5671A
THS5661A	12	100 MSPS	TLV1562 with TLV5618A and THS5661A
THS5651A	10	100 MSPS	TLV1562 with TLV5618A and THS5651A
THS5641A	8	100 MSPS	TLV1562 with TLV5618A and THS5641A

Ensure that the printed-circuit assembly (PCA) has the correct check mark on the silkscreen indicating the ADC.

Each PCA may have additional hardware to install, if appropriate.

Chapter 2

Getting Started

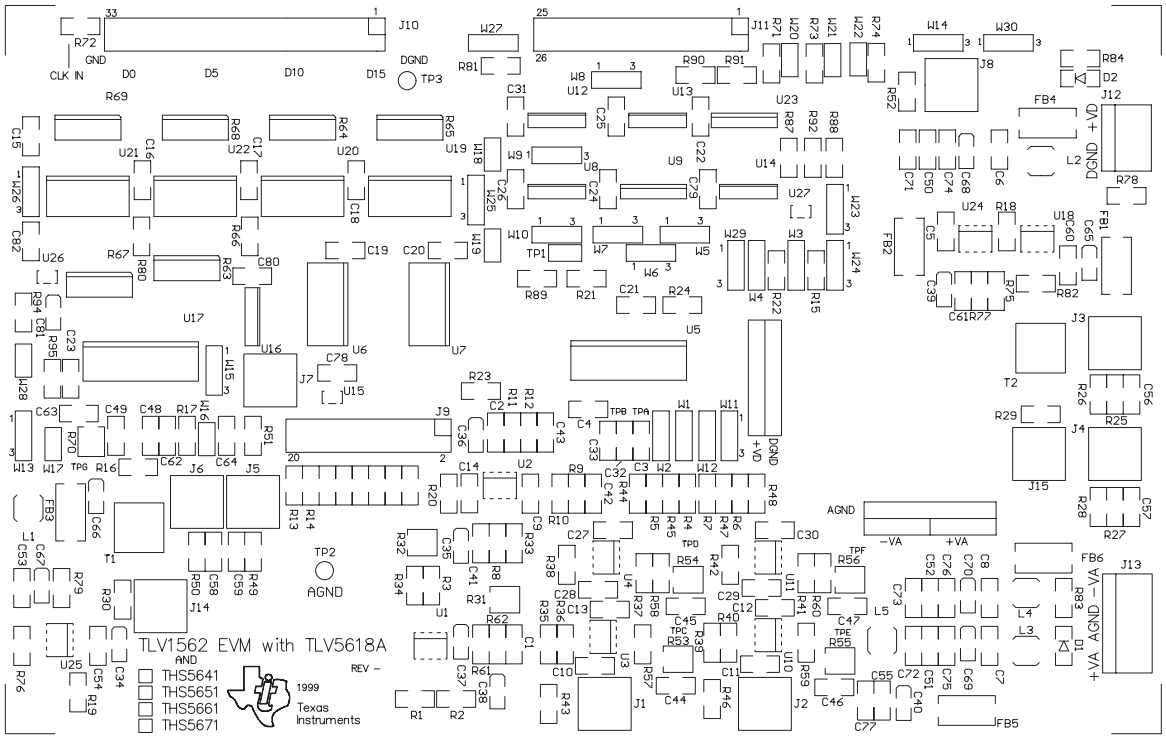
This chapter describes the physical characteristics and PCB layout of the EVM, and lists the components used on the module.

Topic **Page**

2.1 Physical Description

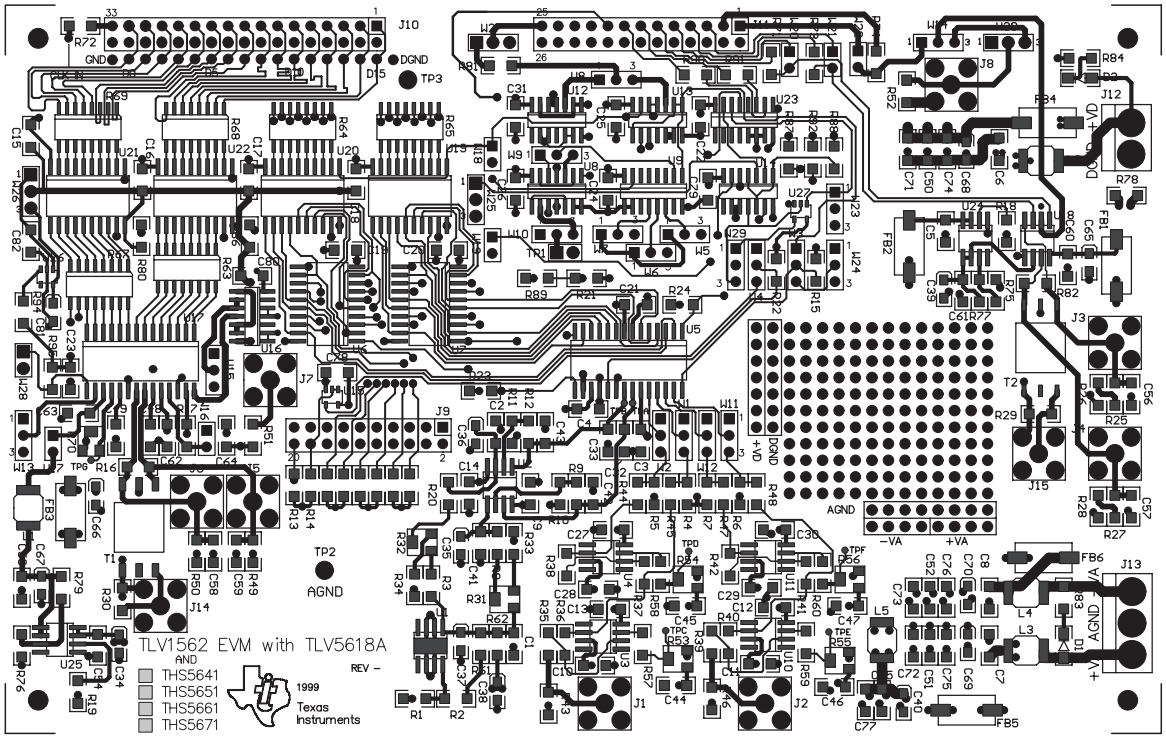
The PWB is constructed in four layers as shown in the following illustrations. The dimensions of the PWB are 7.00 in × 4.375 in × 472 in (177.80 mm × 111.10 mm × 12 mm). See Figure 2–1.

Figure 2–1. PWB Layers



Figures 2–2 through 2–5 show the tracking for each layer.

Figure 2–2. Layer 1



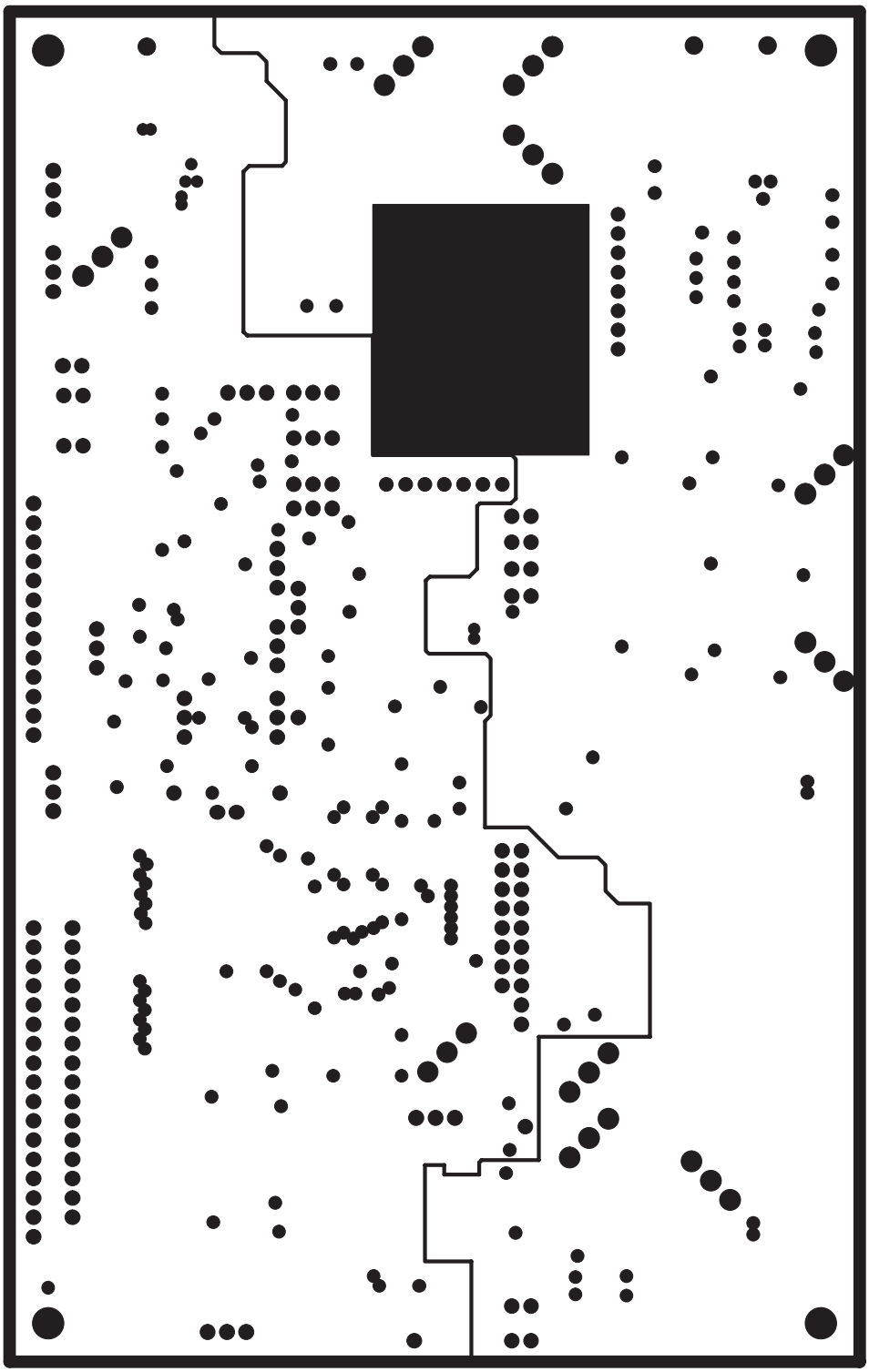


Figure 2–3. Layer 2

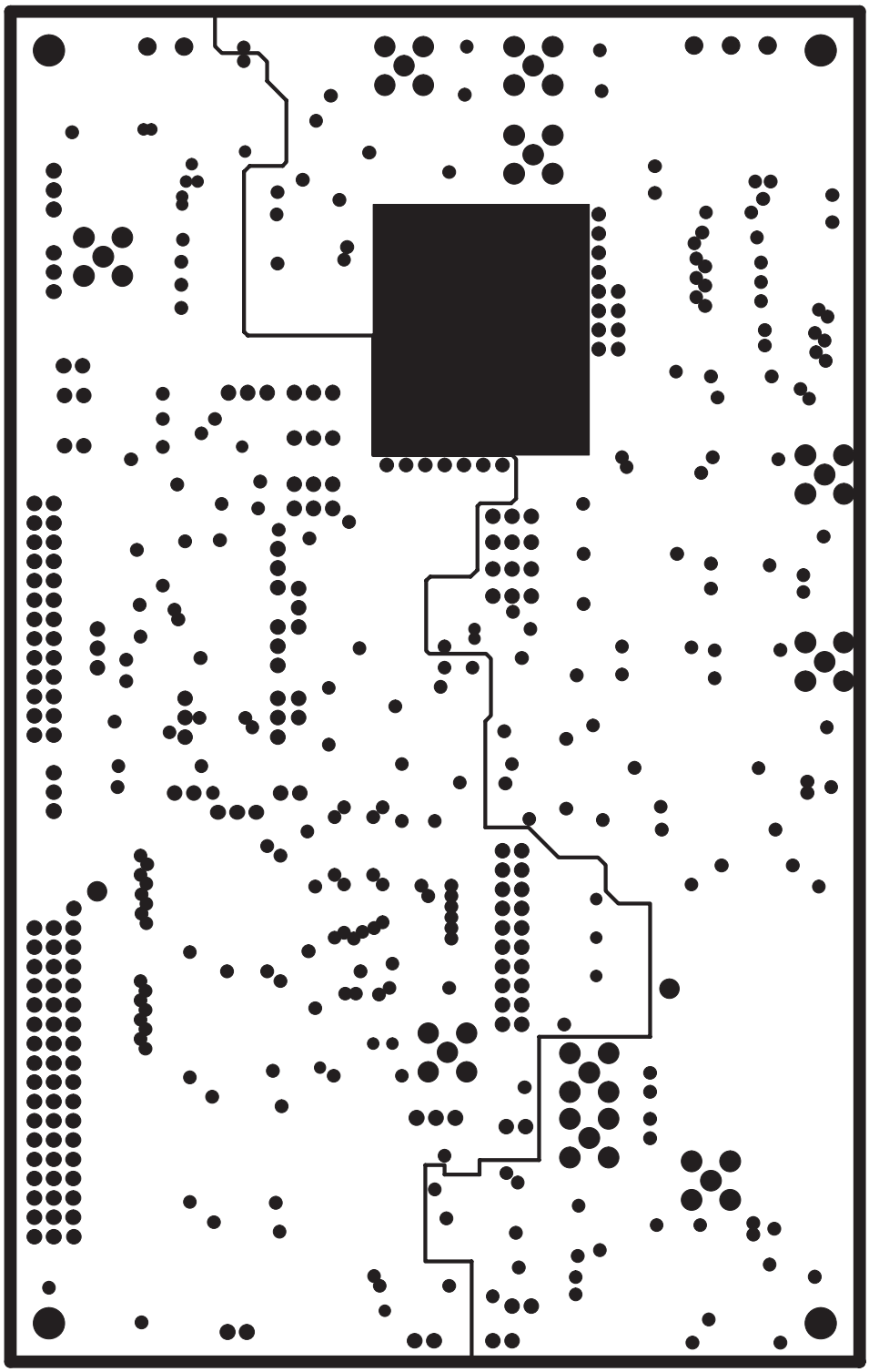


Figure 2–4. Layer 3

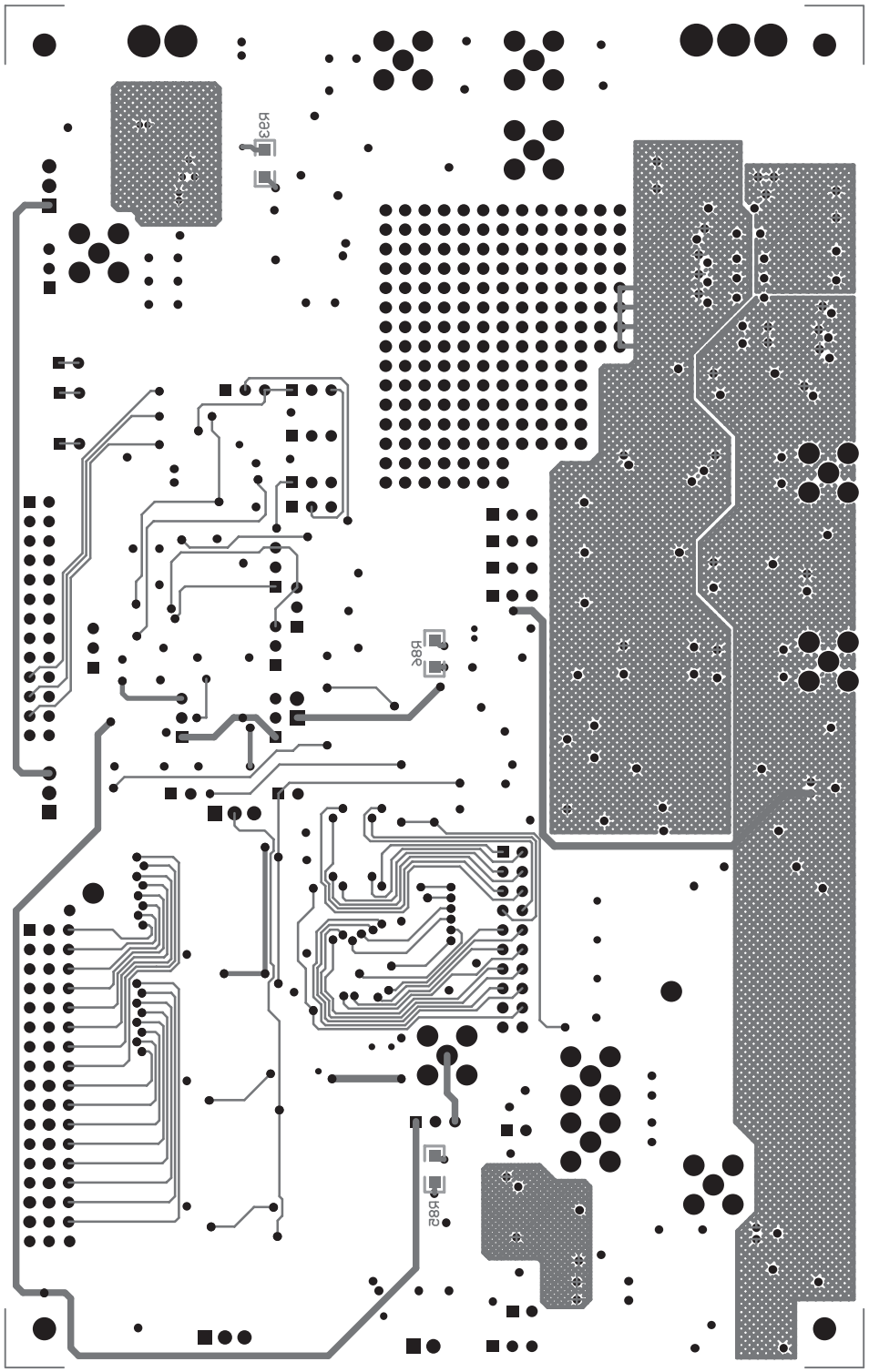


Figure 2–5. Layer 4

2.2 Parts List

Table 2–1 lists the parts required for the TLV1562 EVM.

Table 2–1. Parts List for the TLV1562 EVM

QTY					
5 V	3.3 V	REF. DES	Part Number	DESCRIPTION	MFG
1	1		TLV1562	REV – PCB Fabrication	Texas Instruments
54	54	C01 C02 C03 C04 C05 C06 C07 C08 C09 C10 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 C30 C31 C32 C33 C41 C44 C45 C46 C47 C48 C49 C50 C51 C52 C53 C54 C55 C60 C61 C62 C63 C64 C78 C79 C80	C1206C104K5RAC	Ceramic, 0.1 μF X7R, 50 V, 10%	Kemet
10	10	C34 C35 C36 C37 C38 C39 C40 C68 C69 C70	T491A106K010AS/ ECST1AY106	10 μF, 10 V, tantalum	Kemet/Panasonic
4	4	C42 C43 C56 C57	C1206C101K5GAC	Ceramic, 100 pF X7R, 50 V, 10%	Kemet
4	4	C65 C66 C67 C81	T491A475K016AS	4.7 μF, 16 V, tantalum	Kemet
4	4	C71 C72 C73 C82	C1206C105K4RAC	Ceramic, 1 μF X7R, 16 V, 10%	Kemet
4	4	C74 C75 C76 C77	C1206C103K5RAC	Ceramic, 0.01 μF X7R, 50 V, 10%	Kemet
2	2	D01, D02	CMD15–21VGC	Green 1206 size Chip LED	Chicago Miniature
6	6	FB1 FB2 FB3 FB4 FB5 FB6	27-43-037447	SM Ferrite bead, 27-43-037447	Fair Rite
7	7	J01 J02 J03 J04 J07 J08 J14	142–0701–206	PCB mount SMA jack connector	Johnson Components
1	1	J09	TWS–110–07–L–D	20 Pin dual row header	Samtec
1	1	J10	TSW–117–07–L–D	34 Pin header for IDC	Samtec
1	1	J11	TSW–113–07–L–D	26 Pin header dual row, 0.025 × .1	Samtec
1	1	J12	KRMZ2	2 Screw terminal – PCB mount	Lumberg
1	1	J13	KRMZ3	3 Screw terminal – PCB mount	Lumberg
5	5	L1 L2 L3 L4 L5	DO1608C–472	4.7 μH inductor, DO1608C–Series	Coil Craft
1	1	R01	CR1206–FX–2490	249, 1206 Chip resistor, 1%	Bourns
3	3	R02 R72 R78	CR1206–FX–000	1206 Chip resistor, 0 Ω, 5%	Bourns
1	1	R16	CR1206–FX–1000	1206 Chip resistor, 100, 1%	Bourns
7	7	R03 R04 R05 R06 R07 R26 R28	CR1206–FX–1001	1206 Chip resistor, 1K, 1%	Bourns
20	20	R08 R09 R10 R11 R12 R13 R14 R15 R17 R18 R19 R20 R21 R22 R23 R24 R66 R80 R94 R95	CR1206–FX–1002	1206 Chip resistor, 10 K, 1%	Bourns

Table 2–1. Parts List for the TLV1562 EVM (Continued)

QTY					
5 V	3.3 V	REF. DES	Part Number	DESCRIPTION	MFG
3	3	R31 R32 R70	3214W–1–502–W	4 mm, 5T, SM 5K Potentiometer	Bourns
1	1	R33	CR1206–FX–2491	1206 Chip resistor, 2.49K, 1%	Bourns
1	1	R34	CR1206–FX–3320	1206 Chip resistor, 332, 1%	Bourns
12	12	R25 R27 R35 R36 R37 R38 R39 R40 R41 R42 R83 R84	CR1206–FX–1501	1206 Chip resistor,1.5K, 1%	Bourns
10	10	R43 R44 R45 R46 R47 R48 R49 R50 R51 R52	CR1206–FX–49R9	1206 Chip resistor, 49.9, 1%	Bourns
4	4	R53 R54 R55 R56	3214W–1–103–W	4 mm, 5T, 10K SM Potentiometer	Bourns
4	4	R57 R58 R59 R60	CR1206–FX–7500	1206 Chip resistor, 750, 1%	Bourns
1	1	R61	CR1206–FX–45R3	1206 Chip resistor, 45.3, 1%	Bourns
11	11	R62 R71 R73 R74 R87 R81 R88 R89 R90 R91 R92	CR1206–FX–330	1206 Chip resistor, 33, 5%	Bourns
4	4	R63 R67 R68 R69	CTS766-163-(R)330-G-TR	CTS series 766, 33 Ω × 8	
2	2	R64 R65	CTS766-163-(R)331-G-TR, Bourns / 2NBS16–TJ1–331	CTS series 766, 330 Ω × 8	Bourns 2NBS Series
2	2	R75 R76	CR1206–FX–1693	1206 Chip resistor, 121K, 169K, 1%	Bourns
1	1	R77	CR1206–FX–1213	1206 Chip resistor, 1%	Bourns
1	1	R79	CR1206–FX–4021	1206 Chip resistor, 4.02 K, 1%	Bourns
6	6	R96 R97 R98 R99 R100 R101	CR1206–FX–105	1206 Chip resistor, 1M, 5%	Bourns
1	1	T1	T1–1T–KK81	RF transformer	MiniCircuits
2	2	TP2, TP3	180–7337–02–05	Turret type test pin	Cambion
1	1	U1	TL1431CD / TL1431QD	8–SOP (D), TL1431CD	Texas Instruments
1	1	U2	TLV2432CD / TLV2432ID / TLV2432AID	8–SOP (D), TLV2432	Texas Instruments
4	4	U3 U4 U10 U11	THS3001CD / THS3001ID	8–SOP (D), THS3001	Texas Instruments
1	1	U5	TLV1562IDW	28–SOIC (DW), TLV1562	Texas Instruments
2	2	U6 U7	SN74AHCT374DW / SN74AHC374DW	20–SOP (DW), SN74AHCT374	Texas Instruments
1	1	U8	SN74AHCT74D	14–SOP (D), SN74AHCT74	Texas Instruments
1	1	U9	SN74HC163D	16–SOP (D), SN74AHCT163	Texas Instruments
2	2	U12, U14	SN74AHCT32D	14–SOP (D), SN74AHCT32	Texas Instruments
2	2	U13	SN74AHCT00D	14–SOP (D), SN74AHCT00	Texas Instruments
1	1	U15	SN74AHCT1G32DBVR	5–SOT (DBV), SN74AHCT1G32	Texas Instruments
1		U16	SN74AHC08D	14–SOP (D), SN74AHC08	Texas Instruments
	1	U16	SN74ALVC08D	14–SOP (D), SN74ALVC08	Texas Instruments
1	1	U17	TLV5651IDW	28–SOIC (DW), TLV5651	Texas Instruments

Table 2–1. Parts List for the TLV1562 EVM (Continued)

QTY		REF. DES	Part Number	DESCRIPTION	MFG
5 V	3.3 V				
1	1	U18	TLV5618ACD	8–SOP (D), TLV5618A	Texas Instruments
4		U19 U20 U21 U22	SN74ABTH245DW	20–SOP (DW), SN74ABTH245	Texas Instruments
	4	U19 U20 U21 U22	SN74LVT245BDW	20–SOP (DW), SN74LVT245B	Texas Instruments
1	1	U23	SN74AHCT139D	16–SOP (D), SN74AHCT139	Texas Instruments
2	2	U24 U25	TPS7101QD	8–SOP (D), TPS7101QD	Texas Instruments
1	1	U26	TPS76133DBVR	5–SOT (DBV), TPS76133	Texas Instruments
1	1	U27	SN74AHC1G08DBVR	5–SOT (DBV), SN74AHC1G08	Texas Instruments
22	22	W01 W02 W03 W04 W05 W06 W07 W08 W09 W10 W11 W12 W13 W14 W15 W23 W24 W25 W26 W27 W29 W30	TWS–103–07–L–S	0.025” sq, 3 pin header, 0.1” centers, 3 position jumper	Samtec
5	5	W16 W17 W18 W19 W28	TWS–102–07–L–S	Single row 2 pin header, 2 position jumper	Samtec
Customer Installed Options					
3	3	J05 J06 J15	142–0701–206	PCB mount SMA jack connector	Johnson Components
3	3	R85 R86 R93	CR1206–FX–000	1206 Chip resistor, 5%	Bourns
1	1	R30	CR1206–FX–49R9	1206 Chip resistor, 0 Ω, 1%	Bourns
2	2	R29 R82	CR1206–FX–101	1206 Chip resistor, 49.9, 5%	Bourns
1	1	T2	T1–1T–KK81	RF transformer	MiniCircuits
2	2	C58 C59	C1206C101K5GAC	Ceramic, 22 pF, X7R, 50V, 10%	Kemet
1	1	TP1	TWS–102–07–L–S	Single row 2 pin header, 2 position jumper	Samtec

Note: MFG/PN are for reference only. Substitutions are allowed for all parts but integrated circuits.

Chapter 3

User Configurations

This chapter describes the user-definable options.

Topic **Page**

3.1 Schematic Diagram

Figure 3–1 Illustrates the EVM Schematic.

Figure 3–1. EVM Schematic

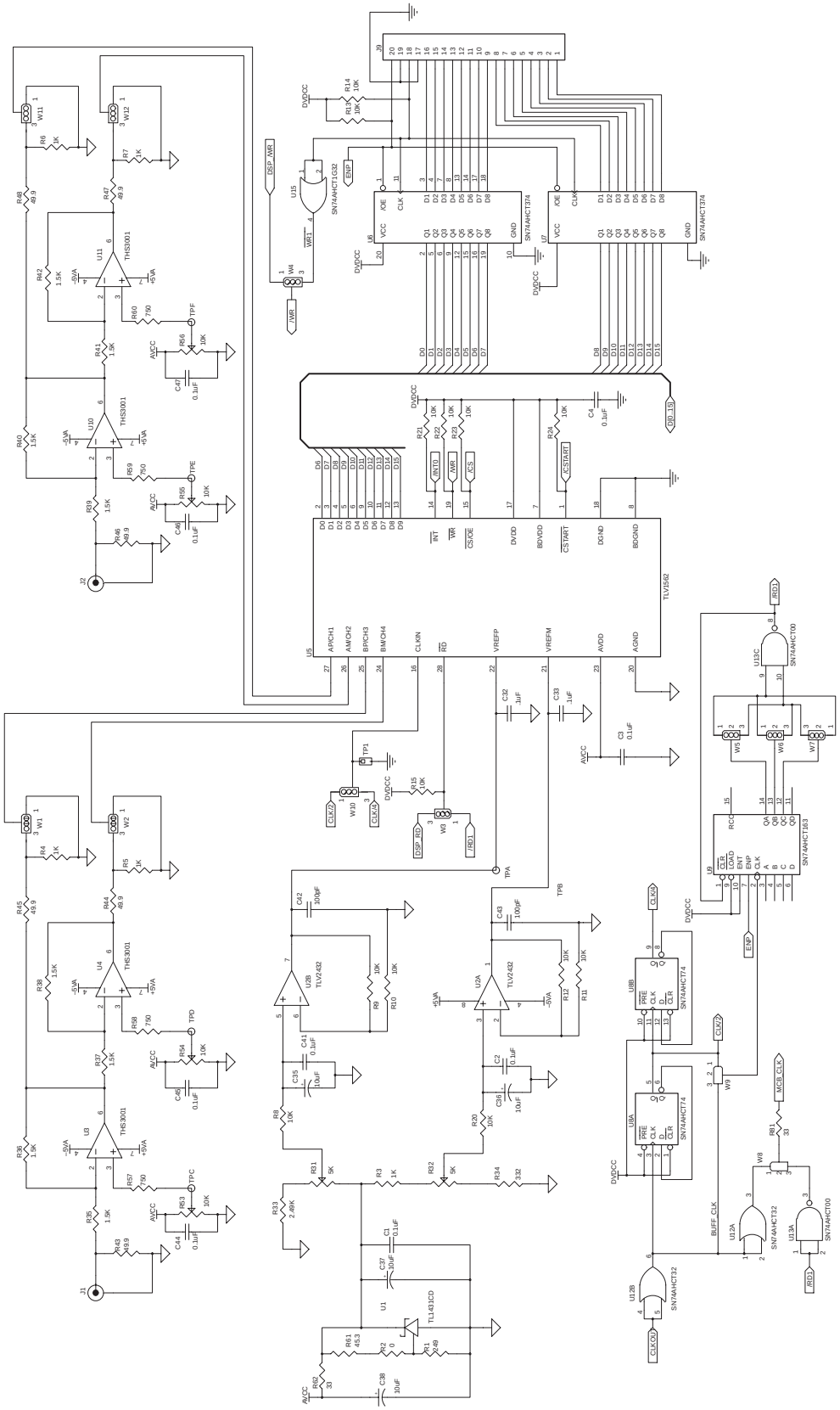


Figure 3–1. EVM Schematic (Continued)

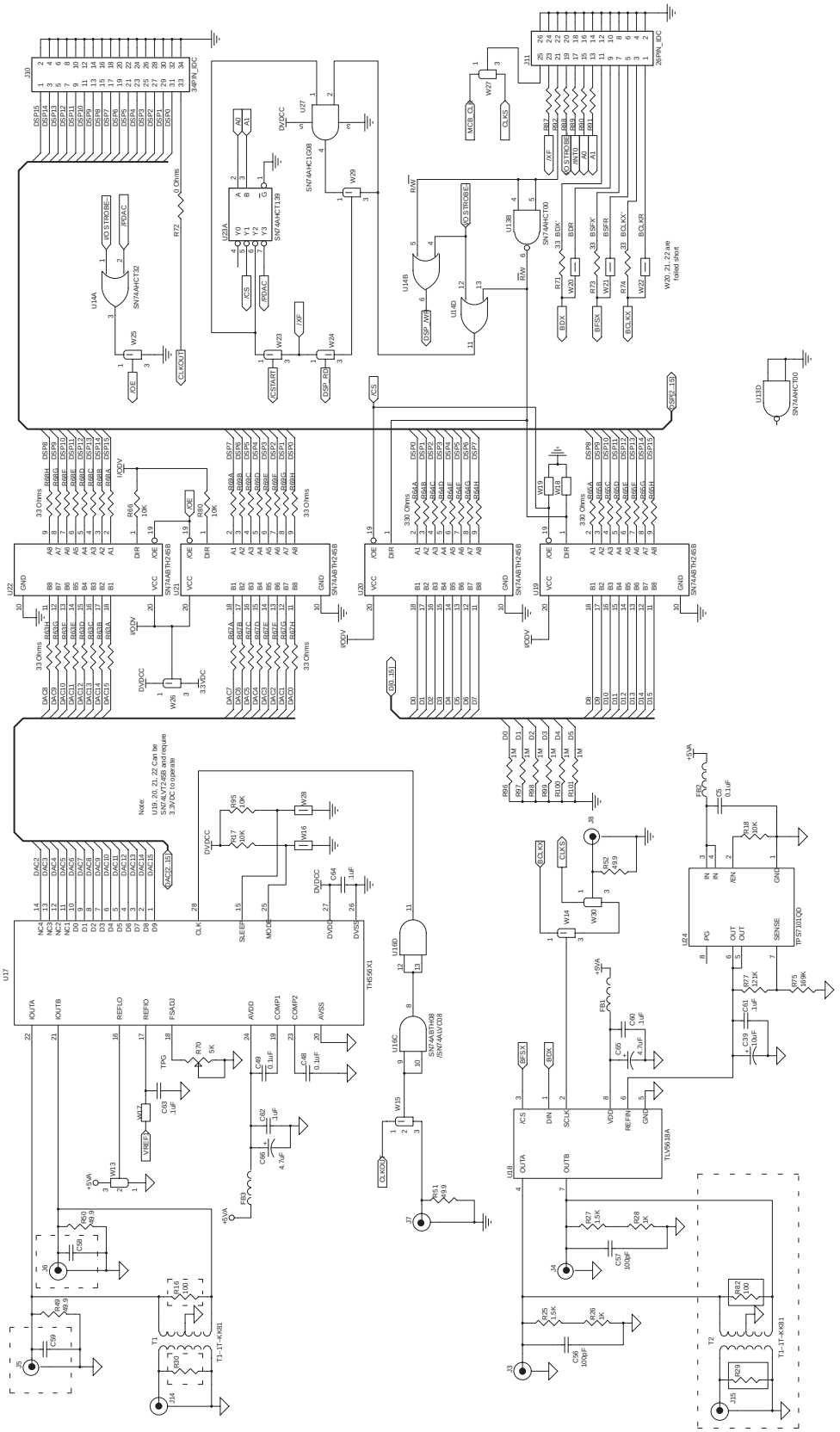
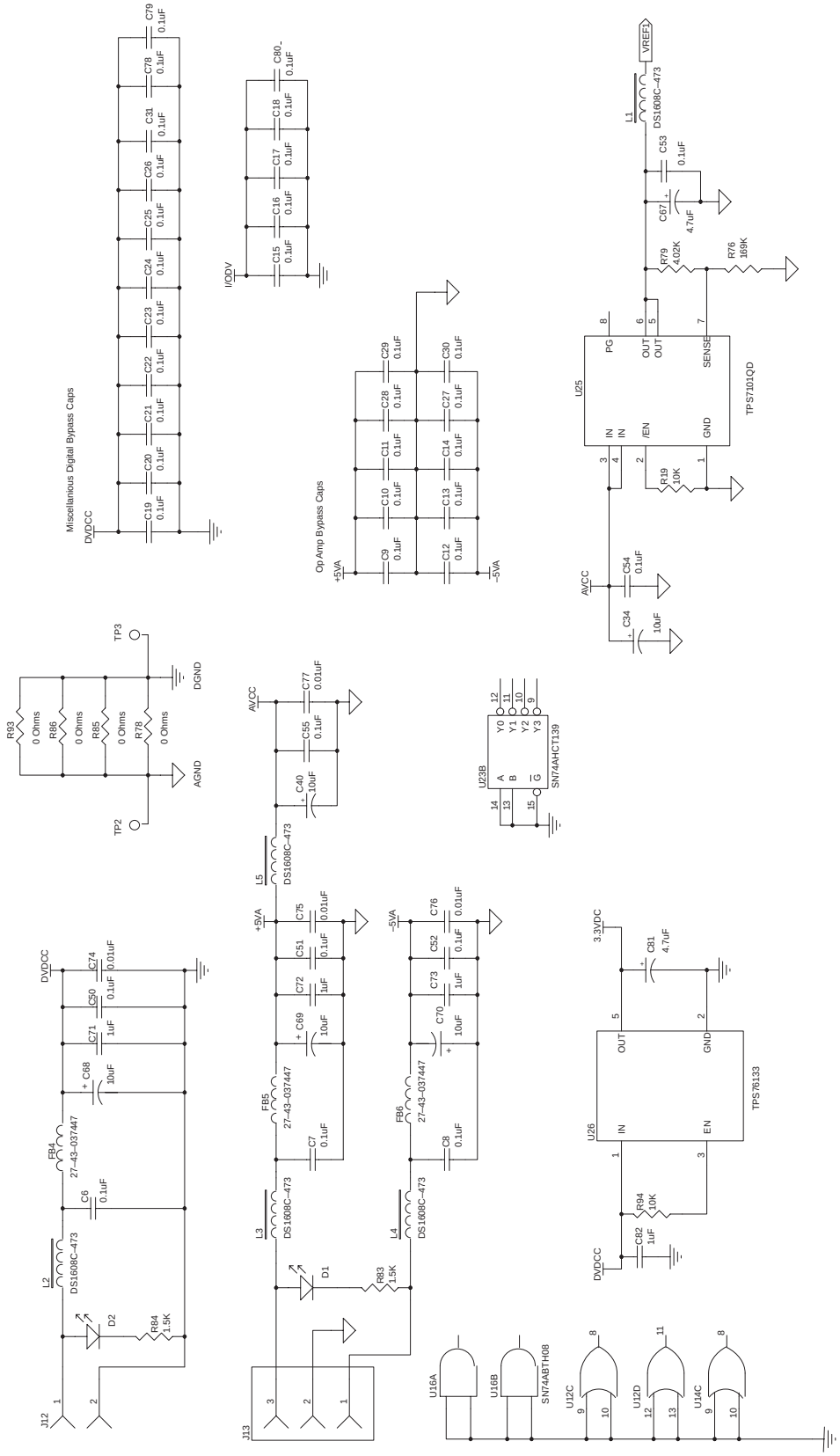


Figure 3–1. EVM Schematic (Continued)



3.2 User Options

The PCA ships in a state that enables immediate evaluation of the digital-to-analog converter (DAC). However, you can reconfigure various options through hardware. This chapter discusses these options to ensure that any reconfiguration is conducted properly.

The hardware on the PCA falls into various groups:

- ❑ 27 jumpers
- ❑ 3 wire links

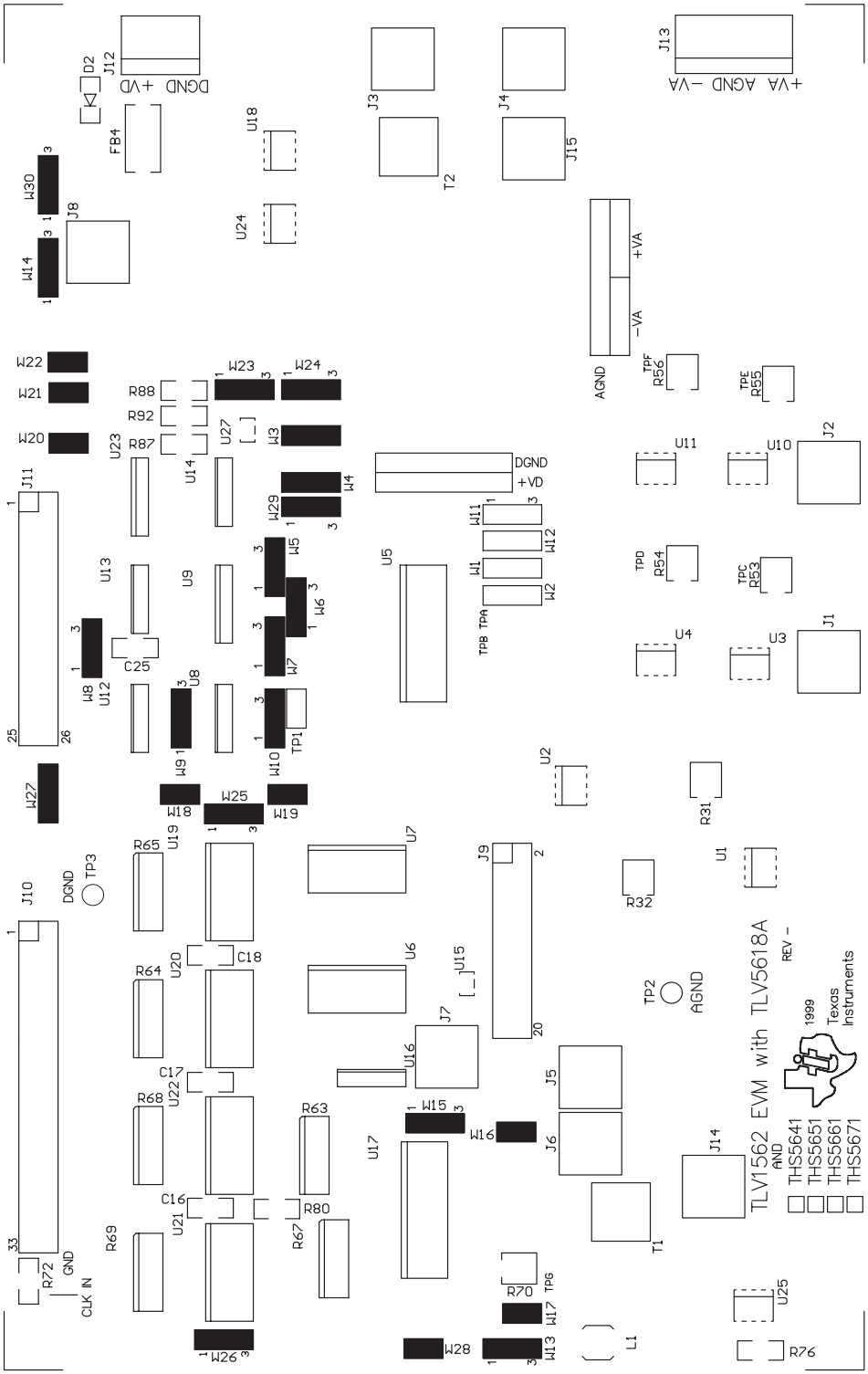
Table 3–1 lists jumper options, a brief description of each function, and information on where the option can be found.

Table 3–1. Jumper Functions

Jumper Reference	Function Description
W1	Connects U3 output to CH3 or GND CH 3
W2	Connects U4 output to CH4 or GND CH4
W3	Selects DSP_RD or $\overline{\text{RD1}}$ as input $\overline{\text{RD}}$
W4	Selects DSP_$\overline{\text{WR}}$ or $\overline{\text{WR1}}$ as input $\overline{\text{WR}}$
W5	Selects Qa as input to Q13c
W6	Selects Qb as input to Q13c
W7	Selects Qc as input to Q13c
W8	Selects either CLKOUT or RD1 to connect to pattern generator
W10	Selects either CLK/4 or CLK/2 as input to CLKIN
W11	Connects U10 input to CH1 or GND CH1
W12	Connects U11 output to CH2 or GND CH2
W13	Selects external or internal Vref
W14	Selects BCLKX coming from the DSP or CLK input from J8
W15	Selects CLOKOUT coming from the DSP or CLK input from J7
W16	Selects binary input mode or 2s compliment input mode (CommsDAC)
W17	Supplies external Vref to the CommsDAC
W18	Connects U19 and U20 DIR pin to GND
W19	Connects U19 and U20 $\overline{\text{OE}}$ pin to GND
W20	PCB foil short
W21	PCB foil short
W22	PCB foil short
W23	Connects XF or decoder output Y2 to $\overline{\text{CSTART}}$ input
W24	Connects XF, $\overline{\text{IOSTROBE}}$ or R/$\overline{\text{W}}$ to $\overline{\text{RD}}$ input
W25	Selects either $\overline{\text{IOSTROBE}}$ or $\overline{\text{PDAC}}$ as input U21 or U22 $\overline{\text{OE}}$ input
W26	Selects +5V or 3.3V Vcc supply voltage to U21 and U22
W27	MCB_CLK or CLKS to J11_25
W28	Selects U17 mode of operation
W29	Selects ADC input signal $\overline{\text{WR}}$
W30	Selects J8 input

Figure 3–2 indicates the physical locations of this hardware.

Figure 3–2. Reconfiguration Hardware Location



3.3 Analog/Digital Supply Voltages

Two options supply power to the digital section of the EVM:

- ❑ 3.3 V or 5V digital DVDD (**for 3.3-V operation replace U19 through U22 with SN74HC245)**
- ❑ 5 V or 3.3V analog AVDD

Configure the power supply voltages in accordance with the following tables.

Table 3–2. Analog Voltage Supply Configuration Options

J12	J13
J12–1 +5–V	J13–3 +5–V
J12–2 DGND	J13–2 AGND
	J13 – 1 –5 V

3.4 Digital Input Configurations

Several options are available to configure the digital inputs. This section describes these options, along with the jumper settings required.

The two alternatives for the digital inputs are given in the following table.

Table 3–3. Digital Input Options

	Connector Reference and Type
Analog Input Option	**IDC**
Apply input data/clock from DSP to J10	J10 – 2 x 17 plug
Control signals/serial data from DSP to J11	J11 – 2 x 13 plug
Apply input data/clock from pattern generator	J9 – 1 x 20 plug

The user selects either of the above configurations based on the test equipment available. These are discussed below.

Figure 3–3. Direct Connect Jumper Configuration for TLV1562 EVM

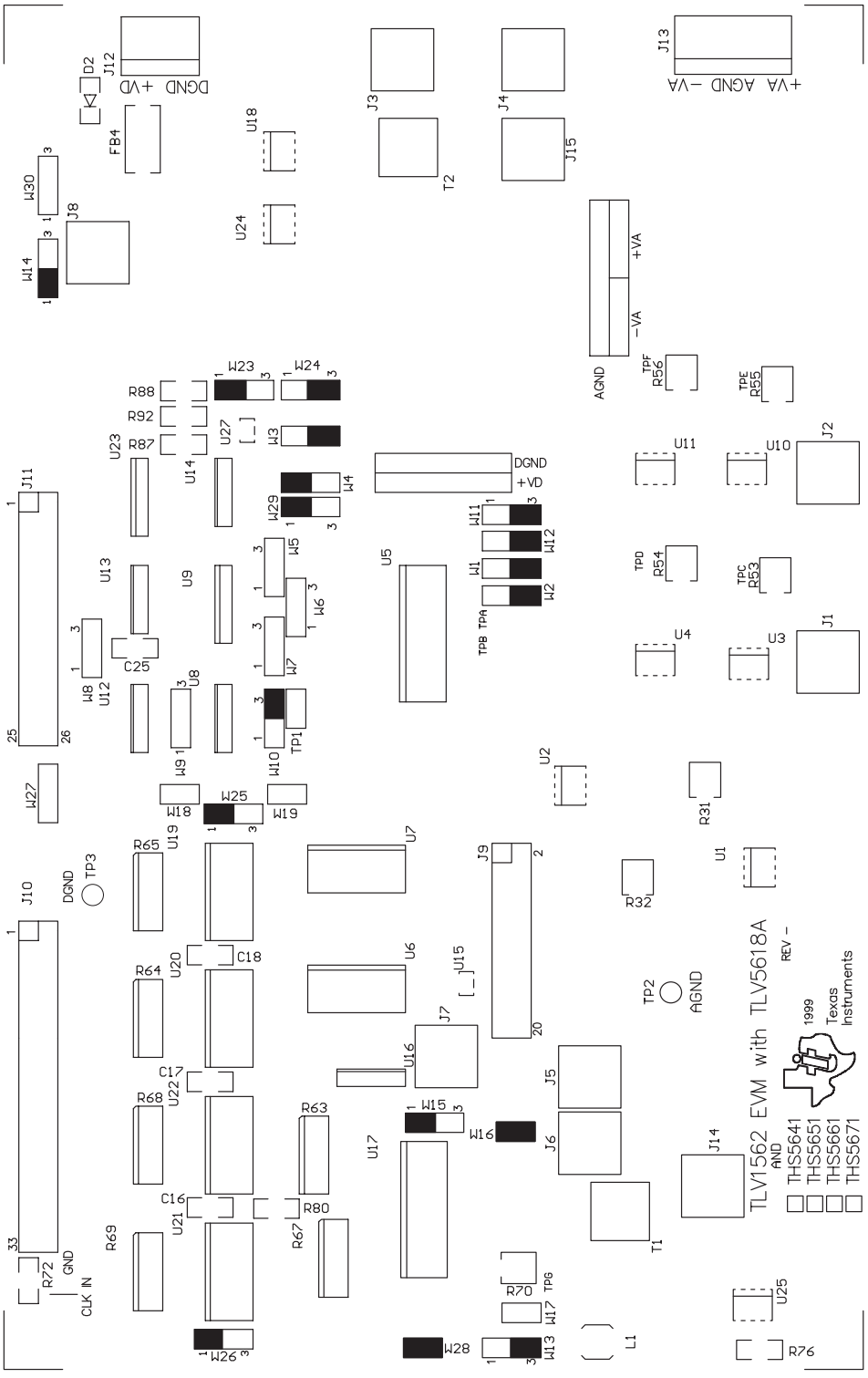


Table 3–4. Shipping Condition of Jumpers W1 Through W30

Jumper	Pins 1 and 2	Pins 2 and 3
W1	Jumper not installed	Jumper installed
W2	Jumper not installed	Jumper installed
W3	Jumper not installed	Jumper installed
W4	Jumper installed	Jumper not installed
W5	Jumper installed	Jumper not installed
W6	Jumper not installed	Jumper installed
W7	Jumper not installed	Jumper not installed
W8	Jumper installed	Jumper not installed
W9	Jumper installed	Jumper not installed
W10	Jumper not installed	Jumper installed
W11	Jumper not installed	Jumper installed
W12	Jumper not installed	Jumper Installed
W13	Jumper installed	Jumper not installed
W14	Jumper installed	Jumper not installed
W15	Jumper installed	Jumper not installed
W16	Jumper installed	N/A
W17	Jumper not installed	N/A
W18	Jumper not instlalled	N/A
W19	Jumper not installed	N/A
W20	Jumper installed	N/A
W21	Jumper installed	N/A
W22	Jumper installed	N./A
W23	Jumper not installed	Jumper installed
W24	Jumper not installed	Jumper installed
W25	Jumper installed	Jumper not installed
W26	Jumper installed	Jumper not installed
W27	Jumper installed	Jumper not installed
W28	Jumper installed	N/A
W29	Jumper not installed	Jumper installed
W30	Jumper not installed	Jumper installed

3.5 Generating a Voltage Reference

Two options provide the voltage reference:

- ❑ Internal reference
- ❑ Onboard external reference

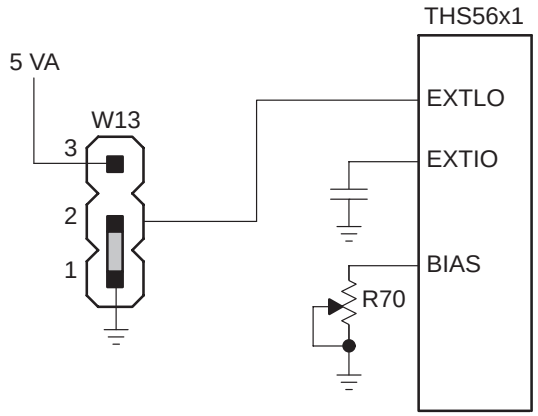
3.5.1 Internal Reference

To set the THS56X1 to use the internal 1.2V on–chip Vref requires the jumper configuration shown in Figure 3–4.

Table 3–5. Internal VREF for U17 Jumper Configuration

Jumper	Pins 1 and 2	Pins 2 and 3
VREF setting		
W13	Jumper installed	Jumper not installed
W17	Jumper not installed	N/A

Figure 3–4. Jumper Configuration for Internal Reference Voltage



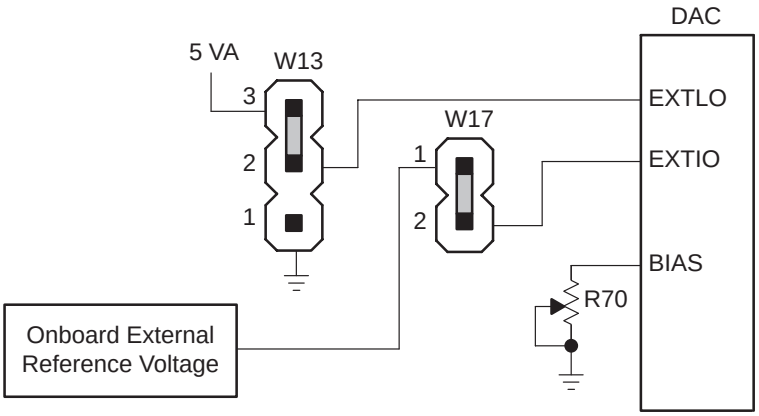
3.5.2 Onboard External Reference

To select the onboard external reference voltage, the user should follow the jumper configuration shown in Figure 3–5.

Table 3–6. External VREF for U17 Jumper Configuration

Jumper	Pins 1 and 2	Pins 2 and 3
VREFP setting		
W13	Jumper not installed	Jumper installed
W17	Jumper installed	N/A

Figure 3–5. Jumper Configuration for External Reference



It is important to understand that the reference voltage plays a fundamental part in the conversion process. Changes in the value of the reference voltage are reflected in the full-scale range of the device. The variation in voltage for the reference should ideally contribute less than 1/2 an LSB of error to the total conversion process.

3.6 Clock Source

The U17 (CommsDAC) requires an external clock. There are two possible external sources for the clock required by the U17. To obtain optimum device performance the user should adhere to the minimum data to clock transition setup and hold times specified in the data sheet SLAS 200. Violating these timing parameters may result in increased converter output noise level.

The clock for the serial DAC and ADC comes from the DSP or pattern generator.

3.6.1 External Clock Generation

The maximum operational speed of the U17 is 100 MHz when operating from a AVDD supply of 5 V and DVDD supply of 5 V. When the DVDD supply is 3.3 V, the maximum clock speed is 67 MHz. The clock signal is derived from either the DSP CLKOUT signal or from a signal generator connected to J7

3.6.2 Analog Output Circuits

The 1:1 RF transformer is used for impedance matching, dc isolation, and interfacing between U17 balanced differential pair output and an unbalanced single-ended output. The resistors R16, R49 and R50 are used to form a network that reflects 50 Ω across the primary circuit (across J14).

Potentiometer R70 is used to set the U17 full-scale output current. When R14 is set equal to 1.9 kΩ, the full-scale current is 20 mA.

A 1 V output voltage will appear at J5 and J6 when IOUT1 and IOUT2 are terminated into 50-Ω external resistor loads (output taken from J8 and J9 and W6 and W7 open). If 75-Ω external resistors are used the maximum IOUT1/IOUT2 output current is 16 mA.

3.7 Connector Pin and Function Assignments

This section details the pinouts and functions for all user connectors.

Table 3–7. Connector Pin and Function Assignments

Reference Designator	Function
J11, J10	DSP interface
J9	Pattern generator interface
J12	Digital circuit supply voltage
J13	Analog supply voltages
J3,J4,J5,J6,J14,J15	Output signal from DAC

Table 3–8. J4 and J2 Power Connectors

Pin Number	Function
J2–1	Digital power 3 V – 5 V
J2–2	DGND
J4–1	Analog power +5 V
J4–2	AGND
J4–3	Analog power –5 V

Table 3–9. J15, J14, J6, J5, J4, and J3 Analog Output Signal Connectors

SMA	Function	SMA	Function
J14–1	Differential to single-ended DAC output via transformer	J14–2	AGND
J6–1	DAC output IOUTB	J6–2	AGND
J5–1	DAC output IOUTA	J5–2	AGND
J4–1	DAC output OUTB	J4–2	AGND
J3–1	DAC output OUTA	J3–2	AGND
J15–1	Differential to single-ended DAC output via transformer	J15–2	AGND

Table 3–10. C542DSK/Microprocessor Control/Serial Data Connector

Pin Number	Function	Pin Number	Function
1	BCLKR	2	Ground (digital)
3	BCLKX	4	Ground (digital)
5	BSFR	6	Ground (digital)
7	BSFX	8	Ground (digital)
9	BDR	10	Ground (digital)
11	BDX	12	Ground (digital)
13	A1	14	Ground (digital)
15	A0	16	Ground (digital)
17	INT0	18	Ground (digital)
19	IOSRROBE	20	Ground (digital)
21	R/$\overline{W}$	22	Ground (digital)
23	XF	24	Ground (digital)
25	CLKS/MCB_CLK	26	Ground (digital)

Table 3–11. J10 Parallel Data Connector

Pin Number	Function	Pin Number	Function
1	DSP_15 (MSB)	2	Ground (digital)
3	DSP_14	4	Ground (digital)
5	DSP_13	6	Ground (digital)
7	DSP_12	8	Ground (digital)
9	DSP_11	10	Ground (digital)
11	DSP_10	12	Ground (digital)
13	DSP_09	14	Ground (digital)
15	DSP_08	16	Ground (digital)
17	DSP_07	18	Ground (digital)
19	DSP_06	20	Ground (digital)
21	DSP_05	22	Ground (digital)
23	DSP_04	24	Ground (digital)
25	DSP_03	26	Ground (digital)
27	DSP_02	28	Ground (digital)
29	DSP_01	30	Ground (digital)
31	DSP_00 (LSB)	32	Ground (digital)
33	CLKOUT	34	Ground (digital)

Table 3–12. Function of Connector J7 and J8

Reference Designator	Function
J8	Serial DAC or CLKS input via SMA connector
J7	DAC clock input signal via SMA connector

Chapter 4

Control Modes

The SLEEP, MODE, EXTLO, EXTIO, and BIASJ pins of the THS5671A/THS5661A/THS5651A/THS5641A control various DAC features and functions.

In the case of the TLV1562 ADC, the SLEEP and MODE pins control the device functions and features respectively.

This section describes the function of these pins.

Topic **Page**

4.1 SLEEP Input Pin

The SLEEP pin used to power down the device. It is an active high asynchronous power down input. The device has an internal pulldown. The device requires 5uS to power down and 3mS to power up. W28 is used to control the SLEEP input.

4.2 MODE Input Pin

4.2.1 Mode Bit = 1

When the Mode pin is connected to DVDD, the device is configured to read 2s complement input data.

4.2.2 Mode Bit = 0

When the Mode pin is connected to DGND, the device is configured to read binary input data.

4.3 BIASJ Input Pin

The potentiometer R70 is typically set to 1.8 KΩ, for a 50-Ω load and 20 mA of output current.

4.4 EXTLO Input Pin

The internal 1.2 V Vref is selected when the EXTLO (REFLO) pin is grounded (W13 pin1 and 2 shorted). When EXTLO (REFLO) pin is tied to +5 V (W13 pins 2 and 3 shorted) and W17 jumper is in place, the external 1.2 V Vref is selected.

4.5 EXTIO Input Pin

An external reference voltage is provided via the EXTIO(REFIO) input pin U25 is used to generate the external reference voltage. Jumper W17 is used to select the external reference voltage.