

120-V Boot, 4-A Peak, High Frequency High-Side and Low-Side Driver

 Check for Samples: [UCC27210A](#), [UCC27211A](#)

FEATURES

- Drives Two N-Channel MOSFETs in High-Side and Low-Side Configuration with Independent Inputs
- Maximum Boot Voltage 120-V DC
- 4-A Sink, 4-A Source Output Currents
- 0.9Ω Pull-Up and Pull-Down Resistance
- Input Pins can Tolerate -10 V to 20 V and are Independent of Supply Voltage Range
- TTL or Pseudo-CMOS Compatible Input Versions
- 8-V to 17-V VDD Operating Range, (20-V ABS MAX)
- 7.2-ns Rise and 5.5-ns Fall Time with 1000-pF Load
- Fast Propagation Delay Times (20 ns typical)
- 4-ns Delay Matching
- Symmetrical Under Voltage Lockout for High-Side and Low-Side Driver
- All Industry Standard Packages Available (SOIC-8, PowerPAD™ SOIC-8, 4-mm x 4-mm SON-8 and 4-mm x 4-mm SON-10)
- Specified from -40 to 140 °C

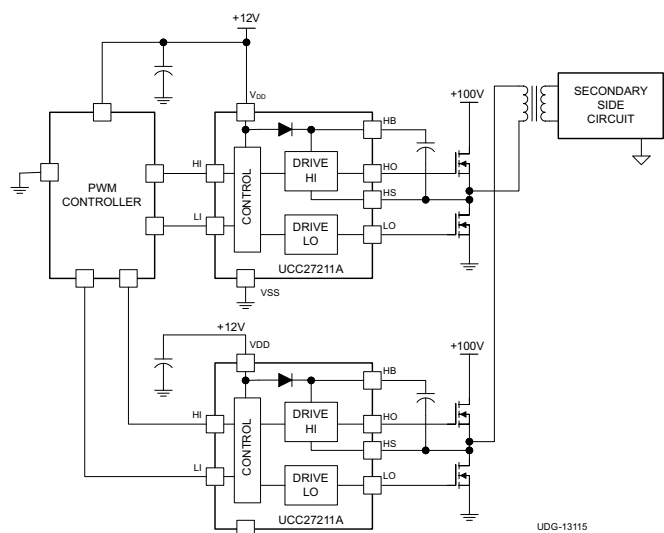
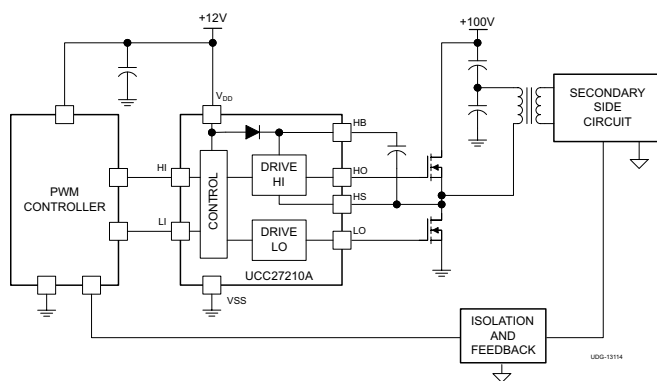
APPLICATIONS

- Power Supplies for Telecom, Datacom, and Merchant
- Half-Bridge and Full-Bridge Converters
- Push-Pull Converters
- High Voltage Synchronous-Buck Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- Class-D Audio Amplifiers

DESCRIPTION

The UCC27210A and UCC27211A Drivers are based on the popular UCC27200 and UCC27201 MOSFET drivers, but offer several significant performance improvements. Peak output pull-up and pull-down current has been increased to 4-A source and 4-A sink, and pull-up and pull-down resistance have been reduced to 0.9 Ω, thereby allowing for driving large power MOSFETs with minimized switching losses during the transition through the MOSFET's Miller Plateau. The input structure is now able to directly handle -10 VDC, which increases robustness and also allows direct interface to gate-drive transformers without using rectification diodes. The inputs are also independent of supply voltage and have a 20-V maximum rating.

Typical Application Diagrams



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DESCRIPTION (CONT.)

The UCC27210A and UCC27211A's switching node (HS pin) is able to handle -18 V maximum which allows the high-side channel to be protected from inherent negative voltages caused parasitic inductance and stray capacitance. The UCC27210A (Pseudo-CMOS inputs) and UCC27211A (TTL inputs) have increased hysteresis allowing for interface to analog or digital PWM controllers with enhanced noise immunity.

The low-side and high-side gate drivers are independently controlled and matched to 2 ns between the turn on and turn off of each other.

An on-chip 120-V rated bootstrap diode eliminates the external discrete diodes. Under-voltage lockout is provided for both the high-side and the low-side drivers providing symmetric turn-on/turn-off behavior and forcing the outputs low if the drive voltage is below the specified threshold.

Both devices are offered in 8-pin SOIC (D) and 4-mm x 4-mm SON-8 (DRM).



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

TEMPERATURE RANGE $T_A = T_J$	INPUT COMPATIBILITY	PACKAGED DEVICES ⁽¹⁾	
		SOIC-8 (D) ⁽²⁾	SON-8 (DRM) ⁽³⁾
-40°C to 140°C	Pseudo CMOS	UCC27210AD	UCC27210ADRM
	TTL	UCC27211AD	UCC27211ADRM

- (1) These products are packaged in Lead (Pb)-Free and green lead finish of PdNiAu which is compatible with MSL level 1 at 255°C to 260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
- (2) D (SOIC-8) package is available taped and reeled. Add R suffix to device type (e.g. UCC27210ADR/UCC27211ADR) to order quantities of 2,500 devices per reel.
- (3) DRM (SON-8) package comes either in a small reel of 250 pieces as part number UCC27210ADRMT/UCC27211ADRMT, or larger reels of 3000 pieces as part number UCC27210ADRMR/UCC27211ADRMR.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage range, $V_{DD}^{(1)}$, $V_{HB} - V_{HS}$		-0.3	20	V
Input voltages on LI and HI, V_{LI} , V_{HI}		-10	20	
Output voltage on LO, V_{LO}	DC	-0.3	$V_{DD} + 0.3$	
	Repetitive pulse <100 ns ⁽²⁾	-2	$V_{DD} + 0.3$	
Output voltage on HO, V_{HO}	DC	$V_{HS} - 0.3$	$V_{HB} + 0.3$	
	Repetitive pulse <100 ns ⁽²⁾	$V_{HS} - 2$	$V_{HB} + 0.3$	
Voltage on HS, V_{HS}	DC	-1	115	
	Repetitive pulse <100 ns ⁽²⁾	$-(24V-V_{DD})$	115	
Voltage on HB, V_{HB}		-0.3	120	
ESD	Human Body Model (HBM)		2	
	Field Induced Charged Device Model (FICDM)		1	
Operating virtual junction temperature range, T_J		-40	150	°C
Storage temperature, T_{STG}		-65	150	
Lead temperature (soldering, 10 sec.)			300	

(1) All voltages are with respect to VSS unless otherwise noted. Currents are positive into, negative out of the specified terminal.

(2) Verified at bench characterization. VDD is the value used in an application design.

RECOMMENDED OPERATING CONDITIONS

all voltages are with respect to V_{SS} ; currents are positive into and negative out of the specified terminal. $-40^{\circ}\text{C} < T_J = T_A < 140^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
Supply voltage range, V_{DD} , $V_{HB}-V_{HS}$	8	12	17	V
Voltage on HS, V_{HS}	-1		105	
Voltage on HS, V_{HS} (repetitive pulse <100 ns)	$-(24V-V_{DD})$		110	
Voltage on HB, V_{HB}	$V_{HS} + 8$, $V_{DD} - 1$		$V_{HS} + 17$, 115	
Voltage slew rate on HS			50	V/ns
Operating junction temperature range	-40		140	°C

THERMAL INFORMATION

THERMAL METRIC		UCC27210A/11A ⁽¹⁾		UNITS
		D	DDA	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance ⁽²⁾	111.8	37.7	°C/W
$\theta_{J\text{Ctop}}$	Junction-to-case (top) thermal resistance ⁽³⁾	56.9	47.2	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	53.0	9.6	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	7.8	2.8	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	52.3	9.4	
$\theta_{J\text{Cbot}}$	Junction-to-case (bottom) thermal resistance ⁽⁷⁾	n/a	3.6	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

ELECTRICAL CHARACTERISTICS

 $V_{DD} = V_{HB} = 12\text{ V}$, $V_{HS} = V_{SS} = 0\text{ V}$, no load on LO or HO, $T_A = T_J = -40^\circ\text{C}$ to 140°C , (unless otherwise noted)

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS	
Supply Currents							
I_{DD}	V_{DD} quiescent current	$V(LI) = V(HI) = 0\text{ V}$	0.05	0.085	0.17	mA	
I_{DDO}	V_{DD} operating current	UCC27210A	2.1	2.6	6.5		
		UCC27211A	2.1	2.5	6.5		
I_{HB}	Boot voltage quiescent current	$V(LI) = V(HI) = 0\text{ V}$	0.015	0.065	0.1		
I_{HBO}	Boot voltage operating current	$f = 500\text{ kHz}$, $C_{LOAD} = 0$	1.5	2.5	5.1		
I_{HBS}	HB to V_{SS} quiescent current	$V(HS) = V(HB) = 115\text{ V}$		0.0005	1.0		μA
I_{HBSO}	HB to V_{SS} operating current	$f = 500\text{ kHz}$, $C_{LOAD} = 0$		0.07	1.2	mA	
Input							
V_{HIT}	Input voltage threshold	UCC27210A	4.2	5.0	5.8	V	
		UCC27210A (DDA only)	4.2	5.0	5.9		
V_{LIT}	Input voltage threshold	UCC27210A	2.4	3.2	4.0		
		UCC27210A (DDA only)	2.4	3.2	4.0		
V_{IHYS}	Input voltage hysteresis	UCC27210A		1.8			
R_{IN}	Input pulldown resistance	UCC27210A		102			k Ω
V_{HIT}	Input voltage threshold	UCC27211A	1.9	2.3	2.7	V	
		UCC27211A (DDA only)	1.9	2.3	2.8		
V_{LIT}	Input voltage threshold	UCC27211A	1.3	1.6	1.9		
		UCC27211A (DDA only)	1.3	1.6	2.1		
V_{IHYS}	Input voltage hysteresis	UCC27211A		700			mV
R_{IN}	Input pulldown resistance	UCC27211A		68			k Ω
Under-Voltage Lockout (UVLO)							
V_{DDR}	V_{DD} turn-on threshold		6.2	7.0	7.8	V	
		DDA only	5.8	7.0	8.1		
V_{DDHYS}	Hysteresis			0.5			
V_{HBR}	V_{HB} turn-on threshold		5.6	6.7	7.9		
		DDA only	5.3	6.7	8.0		
V_{HBHYS}	Hysteresis			1.1			
Bootstrap Diode							
V_F	Low-current forward voltage	$I_{VDD-HB} = 100\ \mu\text{A}$		0.65	0.8	V	
V_{FI}	High-current forward voltage	$I_{VDD-HB} = 100\ \text{mA}$		0.85	0.95		
R_D	Dynamic resistance, $\Delta V_F/\Delta I$	$I_{VDD-HB} = 100\ \text{mA}$ and $80\ \text{mA}$	0.3	0.5	0.85	Ω	
LO Gate Driver							
V_{LOL}	Low-level output voltage	$I_{LO} = 100\ \text{mA}$	0.05	0.10	0.19	V	
V_{LOH}	High level output voltage	$I_{LO} = -100\ \text{mA}$, $V_{LOH} = V_{DD} - V_{LO}$	0.1	0.16	0.29	A	
	Peak pull-up current ⁽¹⁾	$V_{LO} = 0\ \text{V}$		3.7			
	Peak pull-down current ⁽¹⁾	$V_{LO} = 12\ \text{V}$		4.5			
HO GATE Driver							
V_{HOL}	Low-level output voltage	$I_{HO} = 100\ \text{mA}$	0.05	0.10	0.19	V	
V_{HOH}	High-level output voltage	$I_{HO} = -100\ \text{mA}$, $V_{HOH} = V_{HB} - V_{HO}$	0.1	0.16	0.29	A	
	Peak pull-up current ⁽¹⁾	$V_{HO} = 0\ \text{V}$		3.7			
	Peak pull-down current ⁽¹⁾	$V_{HO} = 12\ \text{V}$		4.5			

(1) Ensured by design.

ELECTRICAL CHARACTERISTICS (continued)

$V_{DD} = V_{HB} = 12\text{ V}$, $V_{HS} = V_{SS} = 0\text{ V}$, no load on LO or HO, $T_A = T_J = -40^\circ\text{C}$ to 140°C , (unless otherwise noted)

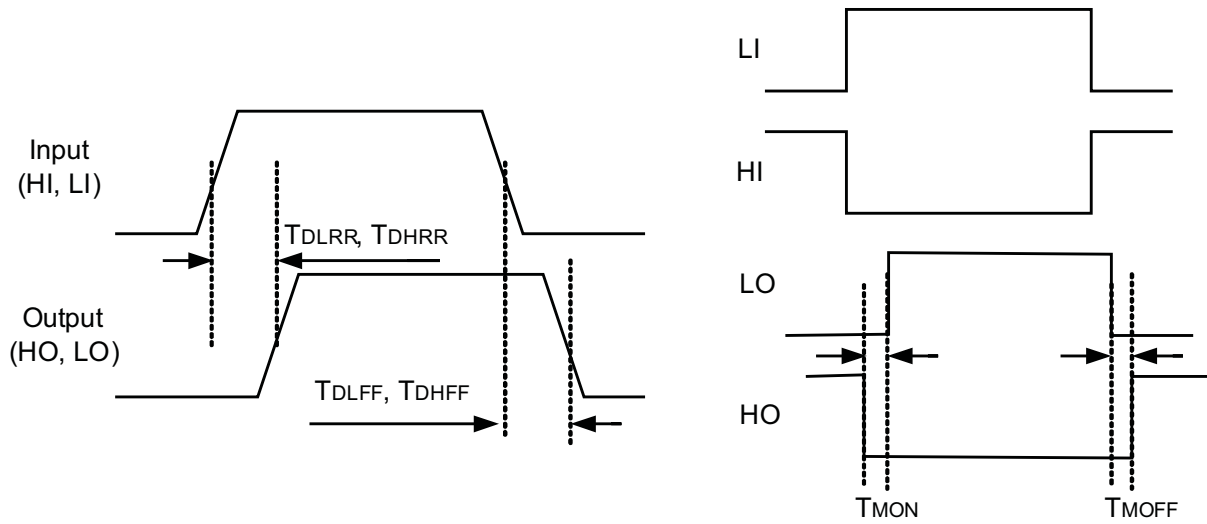
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS	
Switching Parameters: Propagation Delays							
T_{DLFF}	V_{LI} falling to V_{LO} falling	UCC27210A, $C_{LOAD} = 0$	15	21	37	ns	
T_{DHFF}	V_{HI} falling to V_{HO} falling		15	21	37		
T_{DLRR}	V_{LI} rising to V_{LO} rising		15	26	48		
T_{DHRR}	V_{HI} rising to V_{HO} rising		15	26	48		
T_{DLFF}	V_{LI} falling to V_{LO} falling	UCC27211A, $C_{LOAD} = 0$	10	16	30		
T_{DHFF}	V_{HI} falling to V_{HO} falling		10	16	30		
T_{DLRR}	V_{LI} rising to V_{LO} rising		10	20	42		
T_{DHRR}	V_{HI} rising to V_{HO} rising		10	20	42		
Switching Parameters: Delay Matching							
T_{MON}	From HO OFF to LO ON	UCC27210A	$T_J = 25^\circ\text{C}$		5	11	
			$T_J = -40^\circ\text{C}$ to 140°C		5	17	
T_{MOFF}	From LO OFF to HO ON		$T_J = 25^\circ\text{C}$		5	11	
			$T_J = -40^\circ\text{C}$ to 140°C		5	17	
T_{MON}	From HO OFF to LO ON	UCC27211A	$T_J = 25^\circ\text{C}$		4	9.5	
			$T_J = -40^\circ\text{C}$ to 140°C		4	17	
T_{MOFF}	From LO OFF to HO ON		$T_J = 25^\circ\text{C}$		4	9.5	
			$T_J = -40^\circ\text{C}$ to 140°C		4	17	
Switching Parameters: Output Rise and Fall Time							
t_R	LO rise time	$C_{LOAD} = 1000\text{ pF}$, from 10% to 90%			7.2	ns	
t_R	HO rise time				7.2		
t_F	LO fall time	$C_{LOAD} = 1000\text{ pF}$, from 90% to 10%			5.5		
t_F	HO fall time				5.5		
t_R	LO, HO	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (3 V to 9 V)			0.36	0.6	μs
t_F	LO, HO	$C_{LOAD} = 0.1\text{ }\mu\text{F}$, (9 V to 3 V)			0.15	0.4	
Switching Parameters: Miscellaneous							
	Minimum input pulse width that changes the output				50	ns	
	Bootstrap diode turn-off time ⁽²⁾⁽³⁾	$I_F = 20\text{ mA}$, $I_{REV} = 0.5\text{ A}$ ⁽⁴⁾			20		

(2) Ensured by design.

(3) I_F : Forward current applied to bootstrap diode, I_{REV} : Reverse current applied to bootstrap diode.

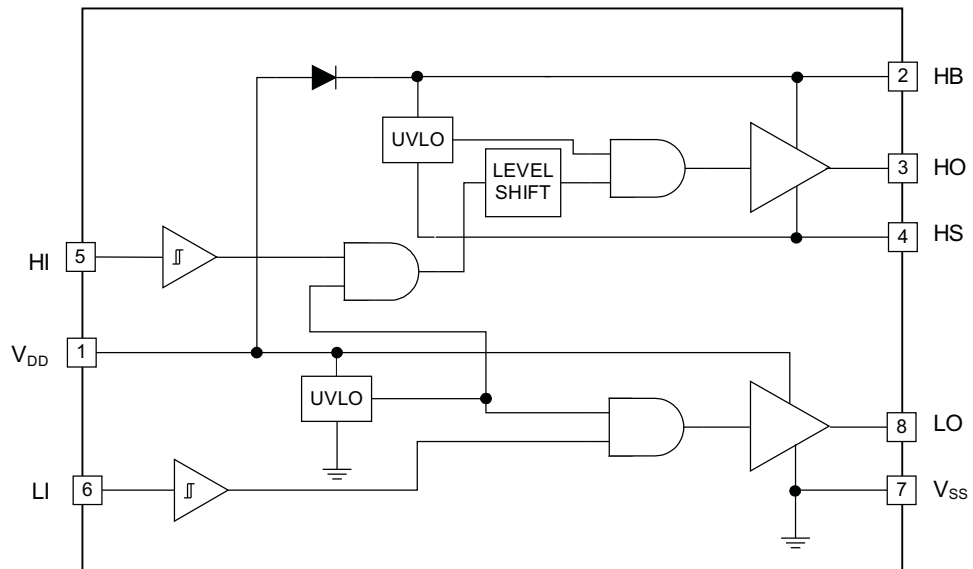
(4) Typical values for $T_A = 25^\circ\text{C}$.

Timing Diagrams

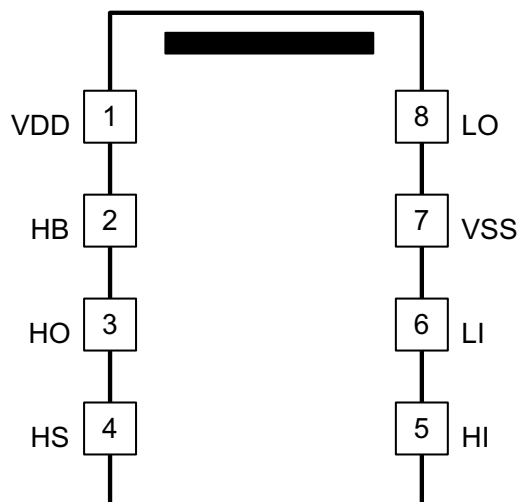


DEVICE INFORMATION

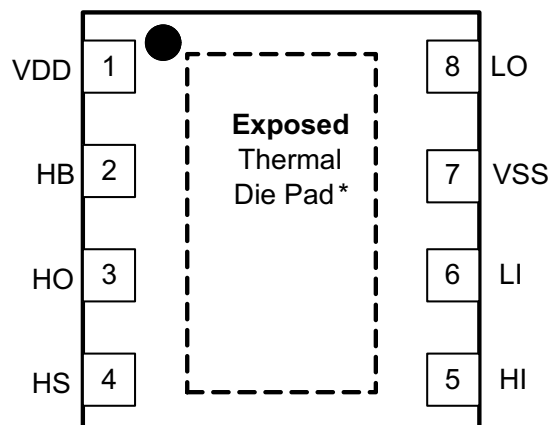
Functional Block Diagram



SOIC-8 (D)
TOP VIEW



SON-8 (DRM)
TOP VIEW

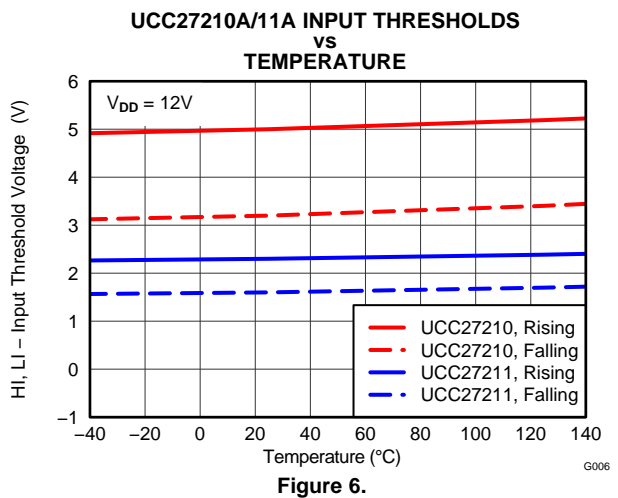
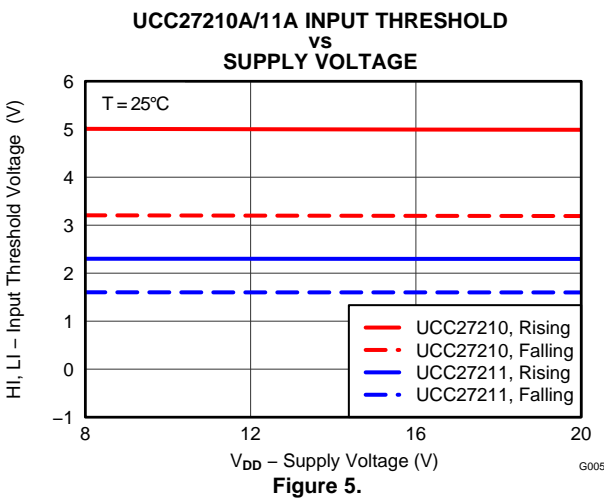
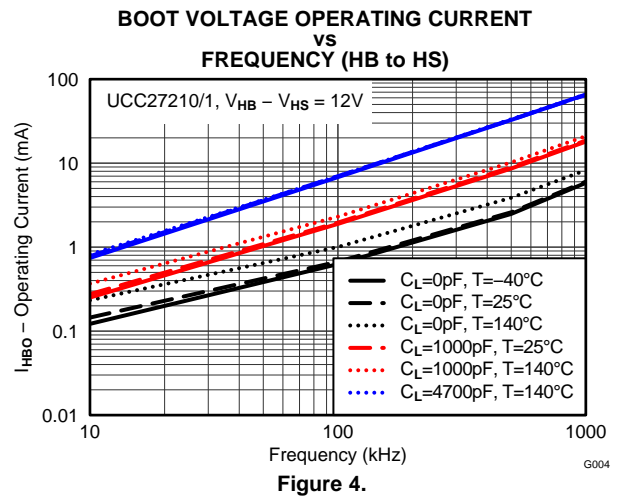
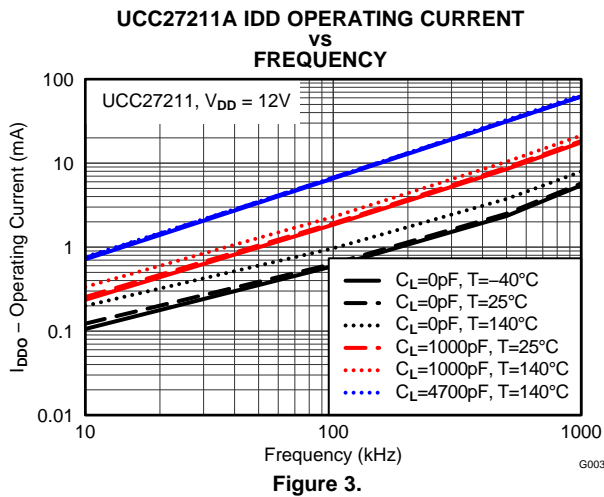
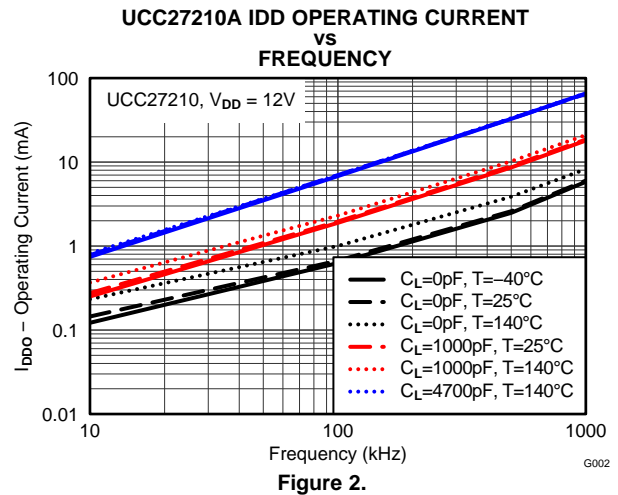
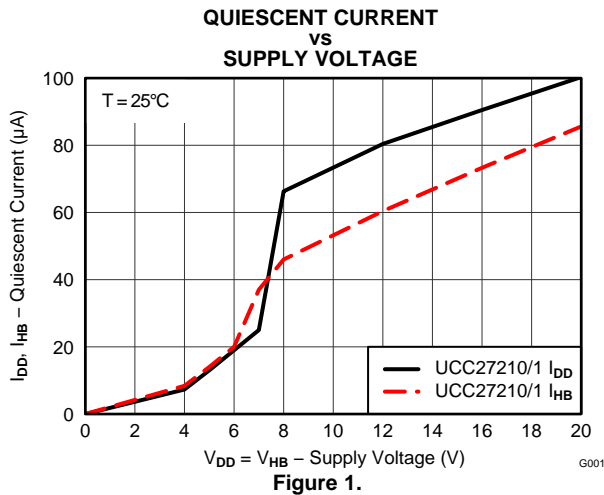


TERMINAL FUNCTIONS

PIN NAME	PIN	DESCRIPTION
	D/DRM	
VDD	1	Positive supply to the lower-gate driver. De-couple this pin to V_{SS} (GND). Typical decoupling capacitor range is 0.22 μ F to 4.7 μ F (See ⁽¹⁾).
HB	2	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 μ F to 0.1 μ F. The capacitor value is dependant on the gate charge of the high-side MOSFET and should also be selected based on speed and ripple criteria
HO	3	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	High-side source connection. Connect to source of high-side power MOSFET. Connect the negative side of bootstrap capacitor to this pin.
HI	5	High-side input. ⁽²⁾
LI	6	Low-side input. ⁽²⁾
VSS	7	Negative supply terminal for the device which is generally grounded.
LO	8	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	-	Not Connected.
PowerPAD™ ⁽³⁾	Pad	Utilized on the DRM package only. Electrically referenced to V_{SS} (GND). Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

- (1) For cold temperature applications we recommend the upper capacitance range. Attention should also be made to PCB layout - see [Layout Recommendations](#).
- (2) HI or LI input is assumed to connect to a low impedance source signal. The source output impedance is assumed less than 100 Ω . If the source impedance is greater than 100 Ω , add a bypassing capacitor, each, between HI and VSS and between LI and VSS. The added capacitor value depends on the noise levels presented on the pins, typically from 1 nF to 10 nF should be effective to eliminate the possible noise effect. When noise is present on two pins, HI or LI, the effect is to cause HO and LO malfunctions to have wrong logic outputs.
- (3) The PowerPAD™ is not directly connected to any leads of the package. However it is electrically and thermally connected to the substrate which is the ground of the device.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (continued)

LO AND HO HIGH LEVEL OUTPUT VOLTAGE VS TEMPERATURE

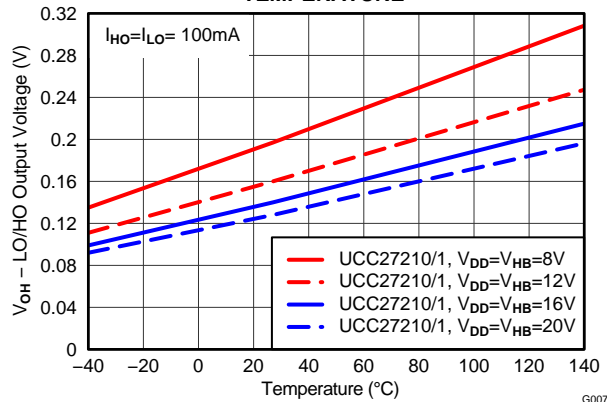


Figure 7.

LO AND HO LOW LEVEL OUTPUT VOLTAGE VS TEMPERATURE

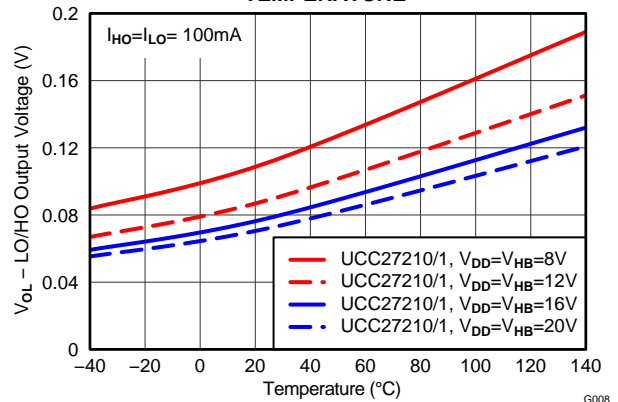


Figure 8.

UNDervoltage LOCKOUT THRESHOLD VS TEMPERATURE

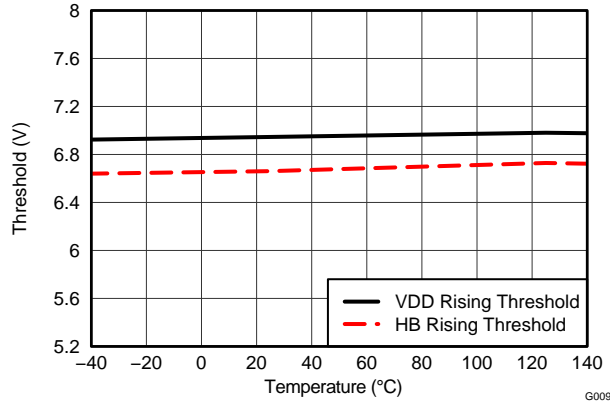


Figure 9.

UNDervoltage LOCKOUT THRESHOLD HYSTERESIS VS TEMPERATURE

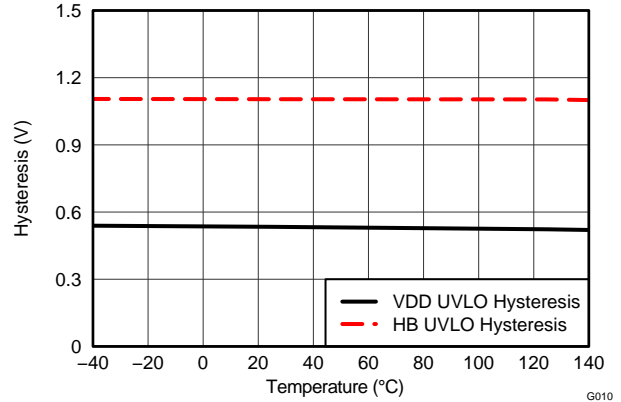


Figure 10.

UCC27210A PROPAGATION DELAYS VS TEMPERATURE

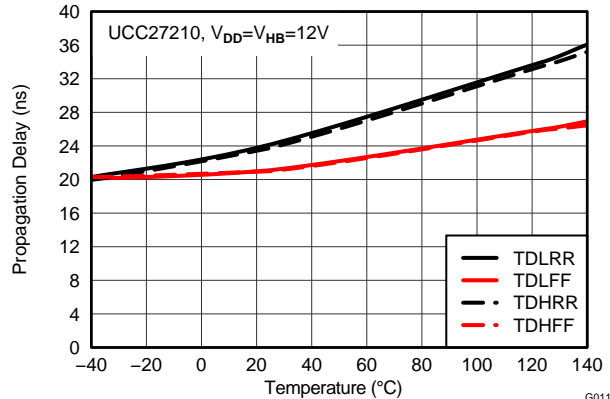


Figure 11.

UCC27211A PROPAGATION DELAYS VS TEMPERATURE

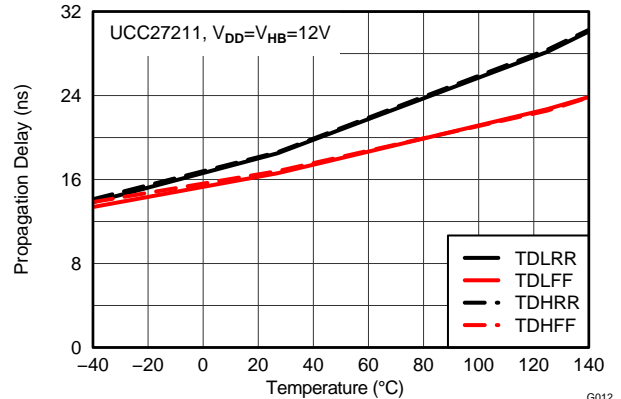


Figure 12.

TYPICAL CHARACTERISTICS (continued)

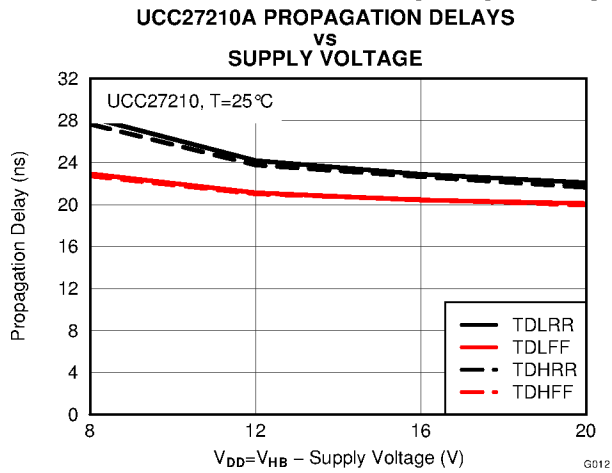


Figure 13.

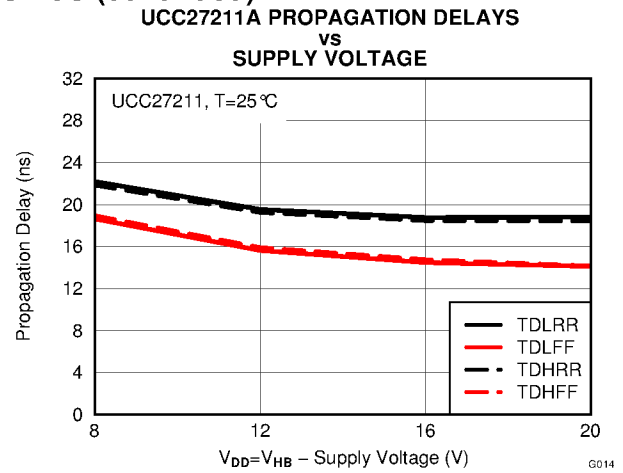


Figure 14.

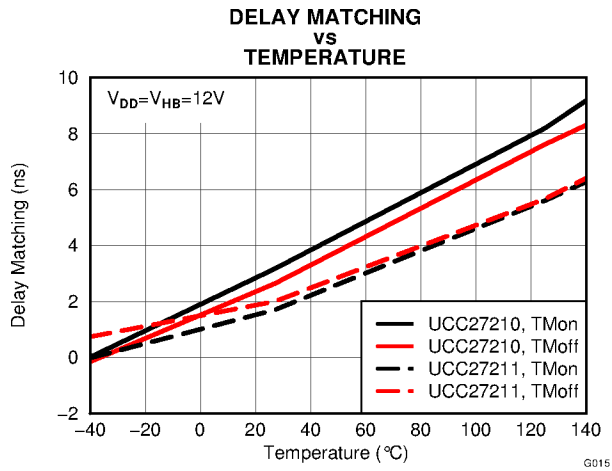


Figure 15.

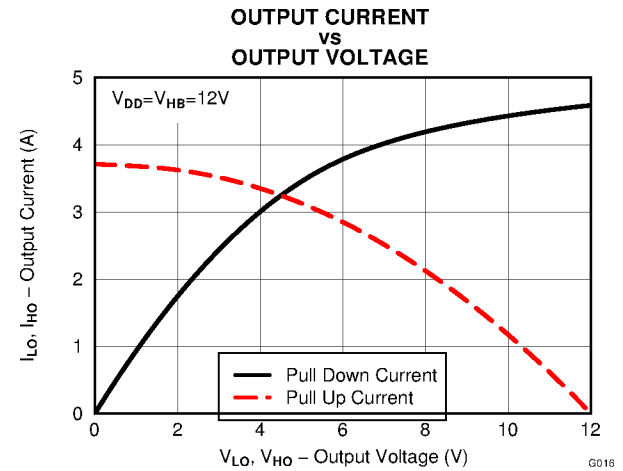


Figure 16.

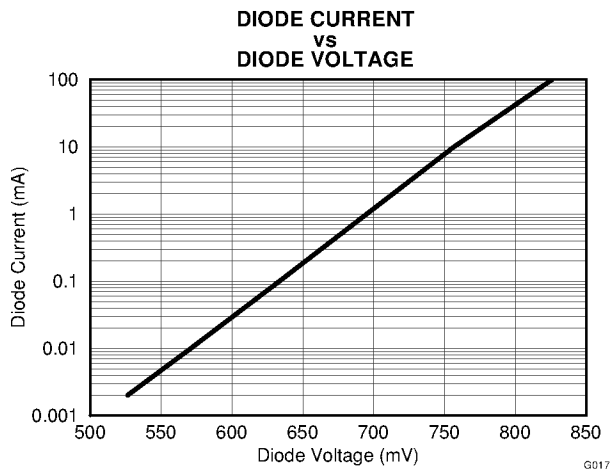


Figure 17.

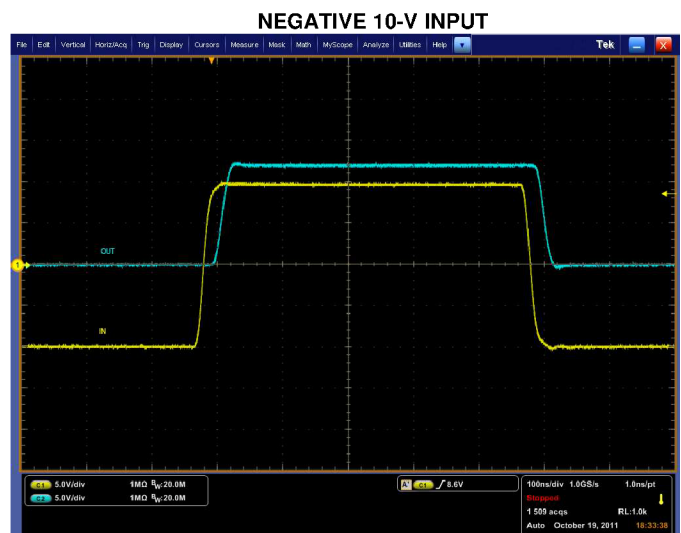


Figure 18.

TYPICAL CHARACTERISTICS (continued)
STEP INPUT

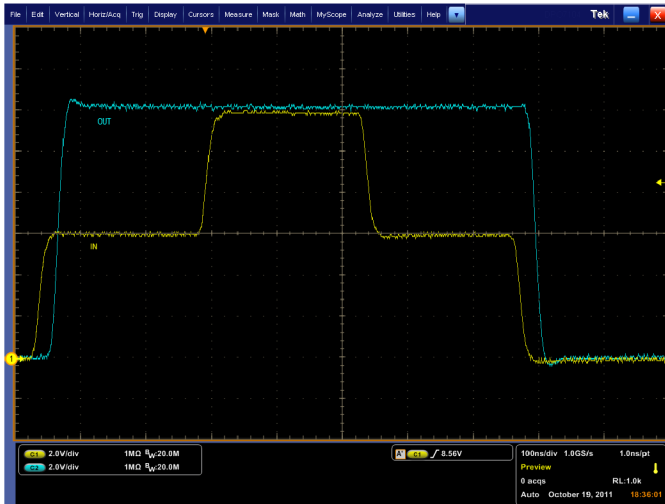


Figure 19.

SYMMETRICAL UVLO



Figure 20.

APPLICATION INFORMATION

Functional Description

The UCC27210A/11A represent Texas Instruments' latest generation of high voltage gate drivers which are designed to drive both the high-side and low-side of N-Channel MOSFETs in a half-/full-bridge or synchronous buck configuration. The floating high-side driver is capable of operating with supply voltages of up to 120 V. This allows for N-Channel MOSFET control in half-bridge, full-bridge, push pull, two-switch forward and active clamp forward converters.

The UCC27210A/11A feature 4-A source/sink capability, industry best-in-class switching characteristics and a host of other features listed in the table below. These features combine to ensure efficient, robust and reliable operation in high-frequency switching power circuits.

Table 1. UCC27210A/11A Highlights

FEATURE	BENEFIT
4-A source and sink current with 0.9-Ω output resistance	High peak current ideal for driving large power MOSFETs with minimal power loss (fast-drive capability at Miller plateau)
Input pins (HI and LI) can directly handle -10 VDC up to 20 VDC	Increased robustness and ability to handle under/overshoot. Can interface directly to gate-drive transformers without having to use rectification diodes
120-V internal boot diode	Provides voltage margin to meet telecom 100-V surge requirements
Switch node (HS pin) able to handle -18 V maximum for 100 ns	Allows the high-side channel to have extra protection from inherent negative voltages caused parasitic inductance and stray capacitance.
Robust ESD circuitry to handle voltage spikes	Excellent immunity to large dV/dT conditions
18-ns propagation delay with 7.2-ns / 5.5-ns rise/fall Times	Best-in-class switching characteristics and extremely low-pulse transmission distortion
2-ns (typ) delay matching between channels	Avoids transformer volt-second offset in bridge
Symmetrical UVLO circuit	Ensures high-side and low-side shut down at the same time
CMOS optimized threshold or TTL optimized thresholds with increased hysteresis	Complementary to analog or digital PWM controllers. Increased hysteresis offers added noise immunity

In UCC27210A/11A, the high side and low side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27210A and UCC27211A. The UCC27210A is the Pseudo-CMOS compatible input version and the UCC27211A is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high-side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to V_{SS} which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27210A is 100 k Ω nominal and input capacitance is approximately 2 pF. The 100 k Ω is a pull-down resistance to V_{SS} (ground). The UCC27210A Pseudo-CMOS input structure has been designed to provide large hysteresis and at the same time to allow interfacing to a multitude of analog or digital PWM controllers. In some CMOS designs, the input thresholds are determined as a percentage of VDD. By doing so, the high-level input threshold can become unreasonably high and unusable. The UCC27210A recognizes the fact that VDD levels are trending downward and it therefore provides a rising threshold with 5.0 V (typ) and falling threshold with 3.2 V (typ). The input hysteresis of the UCC27210A is 1.8 V (typ).

The input stages of the UCC27211A have impedance of 70 k Ω nominal and input capacitance is approximately 2 pF. Pull-down resistance to V_{SS} (ground) is 70 k Ω . The logic level compatible input provides a rising threshold of 2.3 V and a falling threshold of 1.6 V.

Under Voltage Lockout (UVLO)

The bias supplies for the high-side and low-side drivers have UVLO protection. V_{DD} as well as V_{HB} to V_{HS} differential voltages are monitored. The V_{DD} UVLO disables both drivers when V_{DD} is below the specified threshold. The rising V_{DD} threshold is 7.0 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the V_{HB} to V_{HS} differential voltage is below the specified threshold. The V_{HB} UVLO rising threshold is 6.7 V with 1.1-V hysteresis.

Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC27210A/11A family of drivers. The diode anode is connected to V_{DD} and cathode connected to V_{HB} . With the V_{HB} capacitor connected to HB and the HS pins, the V_{HB} capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from V_{DD} to V_{SS} and the high side is referenced from V_{HB} to V_{HS} .

Layout Recommendations

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the $V_{DD}-V_{SS}$ and $V_{HB}-V_{HS}$ (bootstrap) capacitors as close as possible to the device (see example layout below).
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.
- Use similar rules for the HS node as for GND for the high-side driver.
- For systems using multiple UCC27210A and UCC27211A devices we recommend that dedicated decoupling capacitors be located at $V_{DD}-V_{SS}$ for each device.
- Care should be taken to avoid VDD traces being close to LO, HS, and HO signals.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 to 100-mils width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid LI and HI (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.

Keep in mind that a poor layout can cause a significant drop in efficiency or system malfunction versus a good PCB layout and can even lead to decreased reliability of the whole system.

Example Component Placement

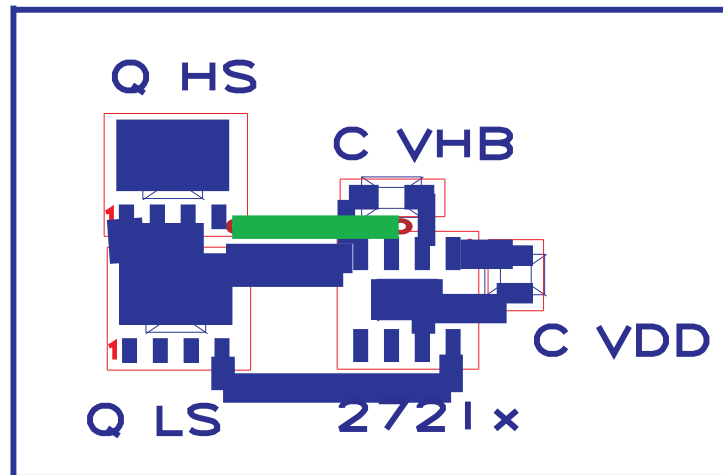


Figure 21. UCC27210A/11A Component Placement

Additional References

These references and links to additional information may be found at www.ti.com

- Additional layout guidelines for PCB land patterns may be found in, *QFN/SON PCB Attachment*, Application Brief (Texas Instrument's Literature Number SLUA271)
- Additional thermal performance guidelines may be found in, *PowerPAD™ Thermally Enhanced Package Application Report*, Application Report (Texas Instrument's Literature Number SLMA002A)
- Additional thermal performance guidelines may be found in, *PowerPAD™ Made Easy*, Application Report (Texas Instrument's Literature Number SLMA004)

REVISION HISTORY

Changes from Original (August, 2013) to Revision A Page

• Changed Repetitive pulse data from -18 V to -(24V-VDD).	3
• Added additional details to Note 2.	3
• Changed Voltage on HS, V_{HS} (repetitive pulse <100 ns) data from -15 to -(24V-VDD).	3
• Added Note 2 to the Terminal Functions Table.	9

Changes from Revision A (August 2013) to Revision B Page

• Changed marketing status from product preview to production data.	1
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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4,5)	Samples
UCC27211AD	PREVIEW	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211A	
UCC27211ADR	PREVIEW	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211A	
UCC27211ADRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211A	Samples
UCC27211ADRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27211A	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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PACKAGE OPTION ADDENDUM

11-Sep-2013

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27211ADRM	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27211ADRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS

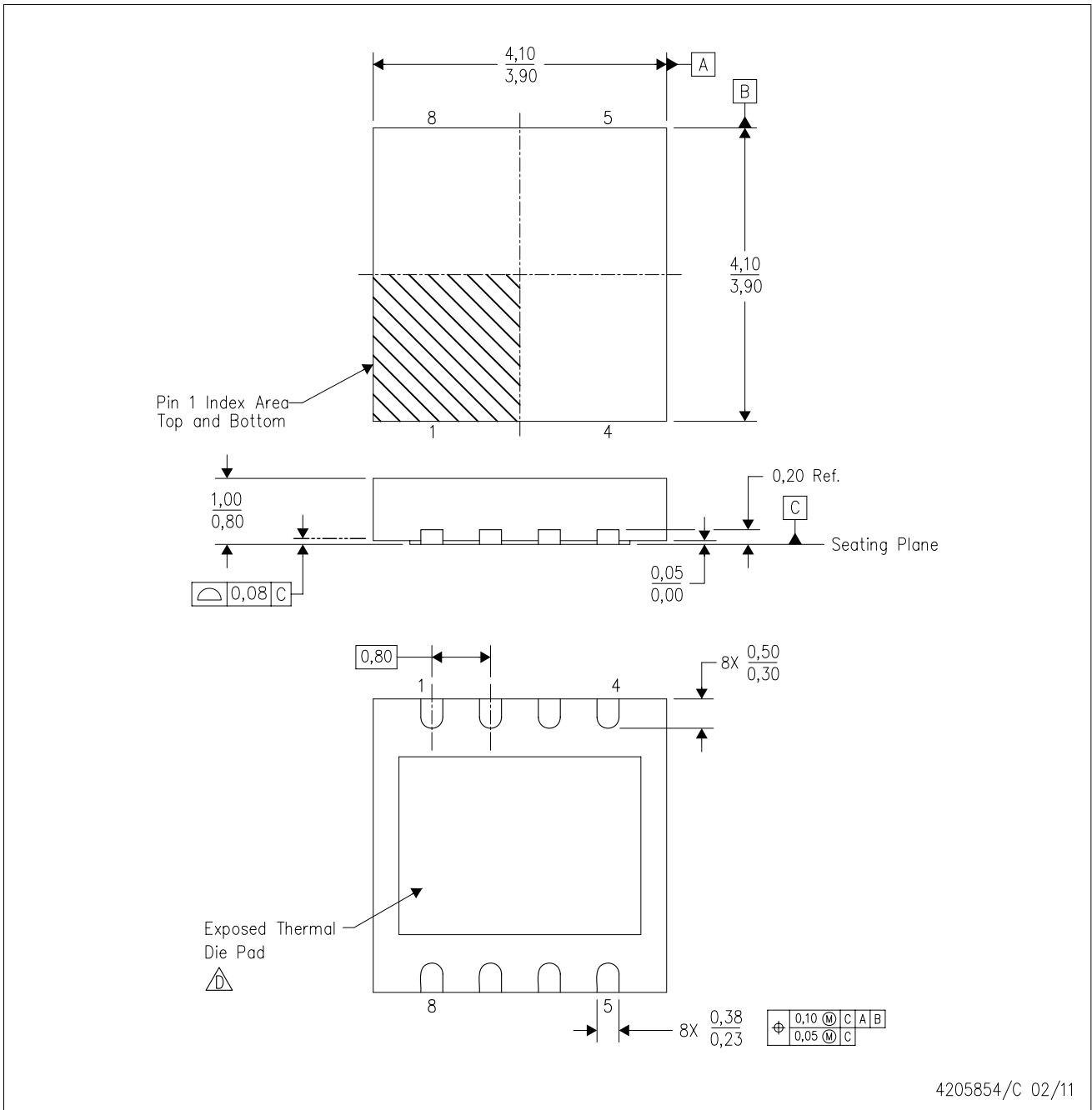


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27211ADRM	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27211ADRMT	VSON	DRM	8	250	210.0	185.0	35.0

DRM (S-PVSON-N8)

PLASTIC SMALL OUTLINE NO-LEAD



4205854/C 02/11

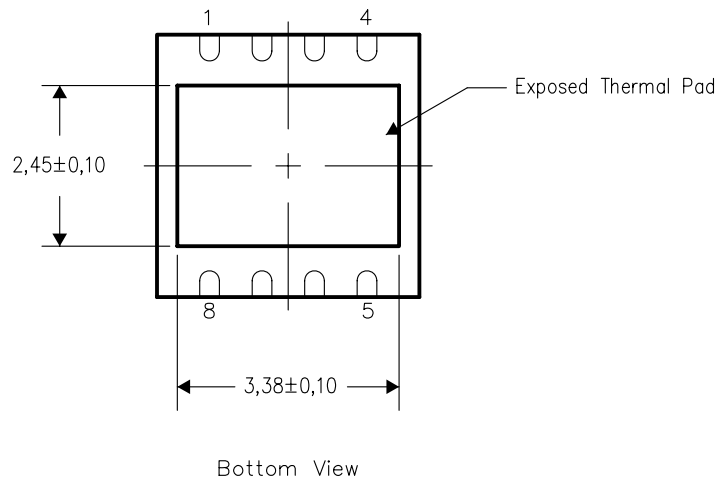
- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. SON (Small Outline No-Lead) package configuration.
 - \triangle D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

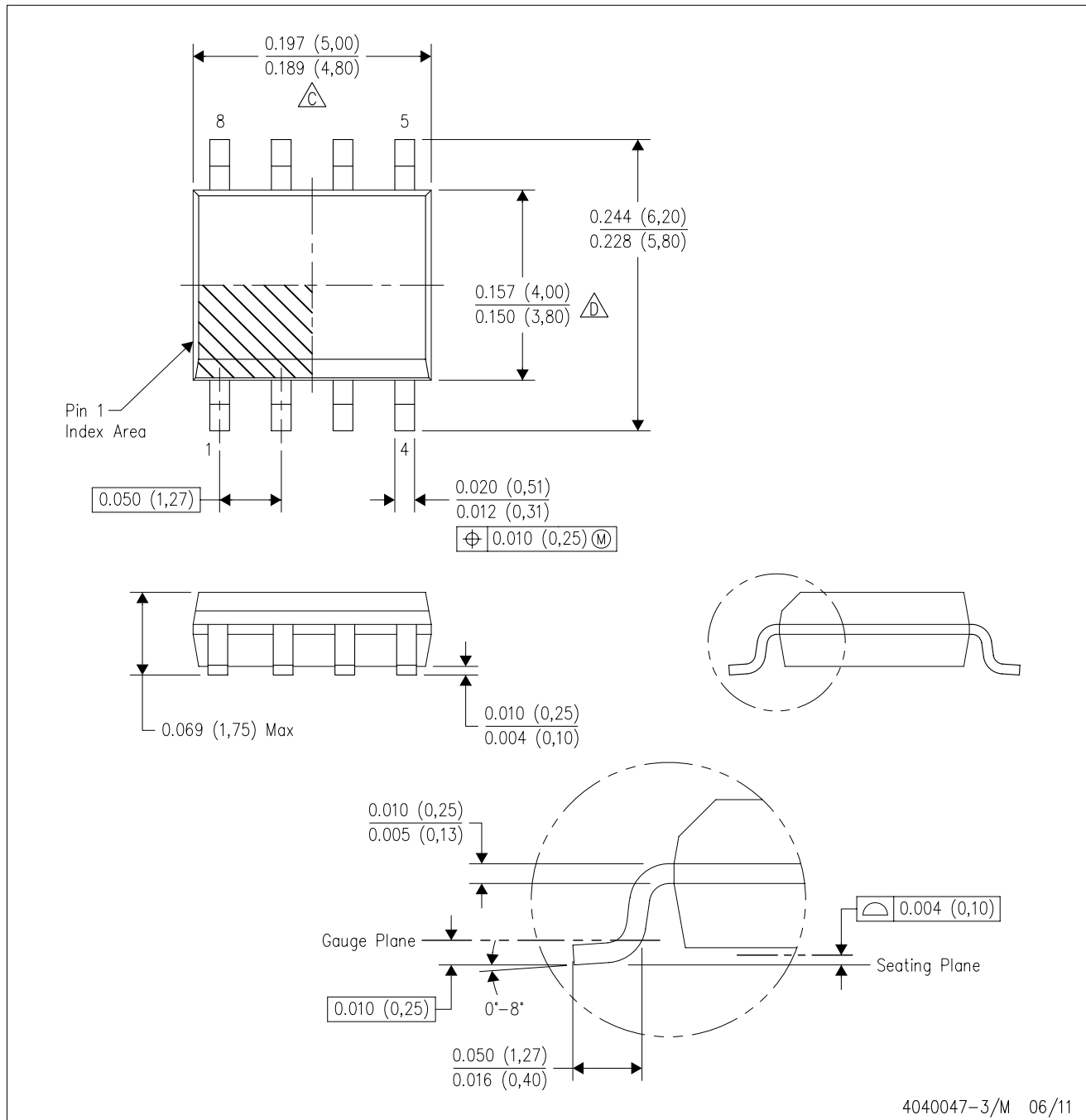




NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

D (R-PDSO-G8)

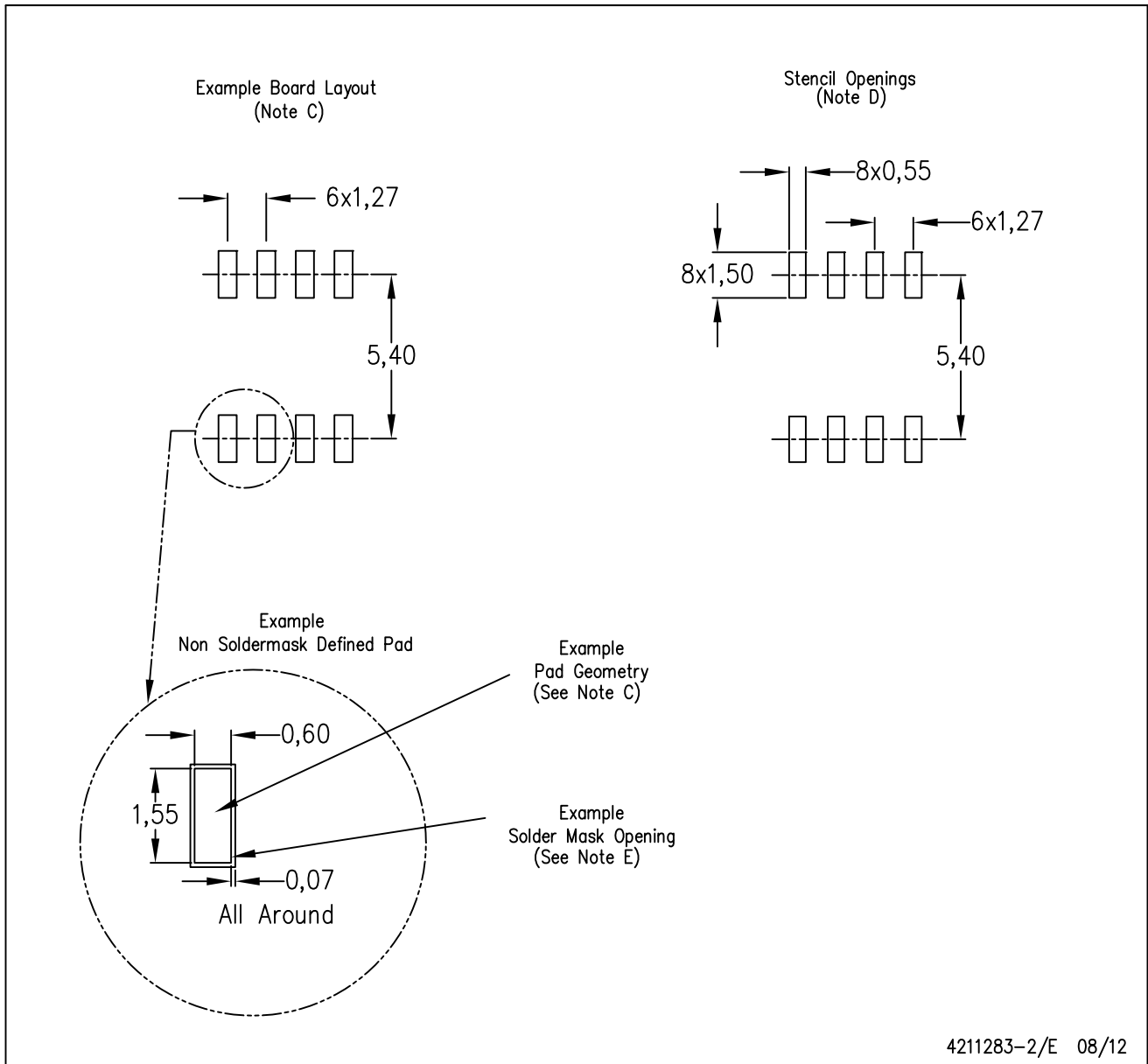
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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