120-V Boot, 3-A Peak, High Frequency, High-Side/Low-Side Driver

Check for Samples: UCC27200A, UCC27201A

FEATURES

- **Specified from -40 °C to 140 °C**
- **Drives Two N-Channel MOSFETs in High-Side/Low-Side Configuration**
- **Maximum Boot Voltage 120 V**
- **Maximum VDD Voltage 20 V**
- **On-Chip 0.65-V VF, 0.6-Ω RD Bootstrap Diode**
- **Greater than 1 MHz of Operation**
- **20-ns Propagation Delay Times**
- **3-A Sink, 3-A Source Output Currents**
- **8-ns Rise/7-ns Fall Time with 1000-pF Load**
- **1-ns Delay Matching**
- **Under Voltage Lockout for High-Side and Low-Side Driver**
- **Offered in 8-Pin SOIC (D), PowerPad™ SOIC-8 (DDA), SON-8 (DRM), SON-9 (DRC) and SON-10 (DPR) Packages**

APPLICATIONS

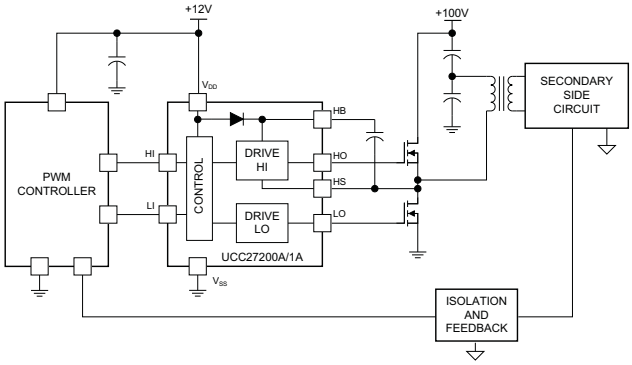
- **Power Supplies for Telecom, Datacom, and Merchant Markets**
- **Half-Bridge Applications and Full-Bridge Converters**
- **Isolated Bus Architecture**
- **Two-Switch Forward Converters**
- **Active-Clamp Forward Converters**
- **High Voltage Synchronous-Buck Converters**
- **Class-D Audio Amplifiers**

CONTENTS

DESCRIPTION

The UCC27200A/1A family of high frequency N-Channel MOSFET drivers include a 120-V bootstrap diode and high-side/low-side driver with independent inputs for maximum control flexibility. This allows for N-Channel MOSFET control in half-bridge, full-bridge, two-switch forward and active clamp forward converters. The low-side and the high-side gate drivers are independently controlled and matched to 1-ns between the turn-on and turn-off of each other. The UCC27200A/1A are based on the popular UCC27200/1 drivers, but offer some enhancements. In order to improve performance in noisy power supply environments the UCC27200A/1A has an enhanced ESD input structure and also has the ability to withstand a maximum of -18 V on its HS pin.

Simplified Application Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPad is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONT.)

An on-chip bootstrap diode eliminates the external discrete diodes. Under-voltage lockout is provided for both the high-side and the low-side drivers forcing the outputs low if the drive voltage is below the specified threshold.

Two versions of the UCC27200A are offered. The UCC27200A has high noise immune CMOS input thresholds while the UCC27201A has TTL compatible thresholds.

Both devices are offered in an 8-pin SOIC(D), PowerPad™ SOIC-8(DDA), SON-8(DRM) package, a 9-pin SON-9(DRC) package and a 10-pin SON-10(DPR) package.

ORDERING INFORMATION

PACKAGED DEVICES(1)						
TEMPERATURE RANGE $T_A = T_J$	**INPUT COMPATIBILITY**	**SOIC-8 (D)(2)**	**PowerPad™ SOIC-8 (DDA)(2)**	**SON-8 (DRM)(3)**	**SON-9 (DRC)(4)**	**SON-10 (DPR) (5)**
-40°C to +140°C	CMOS	UCC27200AD	UCC27200ADDA	UCC27200ADRM	UCC27200ADRC	N/A
	TTL	UCC27201AD	UCC27201ADDA	UCC27201ADRM	UCC27201ADRC	UCC27201ADPR

(1) These products are packaged in Lead (Pb)-Free and green lead finish of PdNiAu which is compatible with MSL level 1 at 255-260°C peak reflow temperature to be compatible with either lead free or Sn/Pb soldering operations.
(2) D (SOIC-8) and DDA (Power Pad™ SOIC-8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC27200ADR) to order quantities of 2,500 devices per reel.
(3) DRM (SON-8) package comes either in a small reel of 250 pieces as part number UCC27200ADRMT, or larger reels of 3000 pieces as part number UCC27200A DRMR.
(4) DRC(SON-9) package comes either in a small reel of 250 pieces as part number UCC27200ADRCT, or large reels pieces as part number UCC27200ADRCR.
(5) DPR(SON-10) package comes either in a small reel of 250 pieces as part number UCC27201ADPRT, or large reels pieces as part number UCC27201ADPRR.

DEVICE RATINGS

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature, unless noted, all voltages are with respect to V_{SS} (1)

PARAMETER		VALUE	UNIT
Supply voltage range, (2) V_{DD}		-0.3 to 20	V
Input voltages on LI and HI, V_{LI}, V_{HI}		-0.3 to 20	
Output voltage on LO, V_{LO}	DC	-0.3 to V_{DD} + 0.3,	
	Repetitive pulse <100 ns (3)	-2 to V_{DD} + 0.3	
Output voltage on HO, V_{HO}	DC	V_{HS} – 0.3 to V_{HB} + 0.3	
	Repetitive pulse <100 ns (3)	V_{HS} - 2 to V_{HB} + 0.3, (V_{HB} - V_{HS} <20)	
Voltage on HS, V_{HS}	DC	-1 to 120	
	Repetitive pulse <100 ns (3)	-18 to 120	
Voltage on HB, V_{HB}		-0.3 to 120	
Voltage On HB-HS		-0.3 to 20	
Operating virtual junction temperature range, T_J		-40 to +150	°C
Storage temperature, T_{STG}		-65 to +150	
Lead temperature (soldering, 10 sec.)		+300	
Power dissipation at T_A = 25°C (D package) (4)		1.3	W
Power dissipation at T_A = 25°C (DDA package) (4)		2.7	
Power dissipation at T_A = 25°C (DRM package) (4)		3.3	
Power dissipation at T_A = 25°C (DRC package) (4)		2.86	
Human body model		2000	V
CDM		1000	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to V_{ss}. Currents are positive into, negative out of the specified terminal.
(3) Values are verified by characterization and are not production tested.
(4) This data was taken using the JEDEC proposed high-K test PCB. See the THERMAL CHARACTERISTICS section for details.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	8	12	17	V
V_{HS}	Voltage on HS	-1		105	
	Voltage on HS, (repetitive pulse <100 ns)	-15		110	
V_{HB}	Voltage on HB	V_{HS} + 8, V_{DD} –1		V_{HS} + 17, 115	
	Voltage slew rate on HS			50	V / ns
T_J	Operating junction temperature range	-40		+140	°C

THERMAL INFORMATION

THERMAL METRIC(1) (2)		UCC27200A /UCC27201A	UCC27200A /UCC27201A	UCC27200A /UCC27201A	UNITS
		DRM	DRC	DPR	
		8 PINS	9 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	36.2	43.7	34.8	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	41.6	49.9	32.1	
θ_{JB}	Junction-to-board thermal resistance	13.2	19.1	11.9	
ψ_{JT}	Junction-to-top characterization parameter	0.6	0.6	0.2	
ψ_{JB}	Junction-to-board characterization parameter	13.4	19.3	12.2	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	3.1	3.8	1.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

THERMAL INFORMATION

THERMAL METRIC(1)(2)		UCC27200A /UCC27201A	UCC27200A /UCC27201A	UNITS
		D	DDA	
		8 PINS	8 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	106.5	40.5	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	52.9	49.0	
θ_{JB}	Junction-to-board thermal resistance	46.6	10.2	
ψ_{JT}	Junction-to-top characterization parameter	9.6	3.1	
ψ_{JB}	Junction-to-board characterization parameter	46.1	9.7	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	1.5	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) For thermal estimates of this device based on PCB copper area, see the TI PCB Thermal Calculator.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = -40°C to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Currents							
I_{DD}	VDD quiescent current		V_{LI} = V_{HI} = 0		0.4	0.8	mA
I_{DDO}	VDD operating current	UCC27200A	f = 500 kHz, C_{LOAD} = 0		2.5	4	
		UCC27201A	f = 500 kHz, C_{LOAD} = 0		3.8	5.5	
I_{HB}	Boot voltage quiescent current		V_{LI} = V_{HI} = 0 V		0.4	0.8	
I_{HBO}	Boot voltage operating current		f = 500 kHz, C_{LOAD} = 0		2.5	4	
I_{HBS}	HB to V_{SS} quiescent current		V_{HS} = V_{HB} = 110 V		0.0005	1	uA
I_{HBSO}	HB to V_{SS} operating current		f = 500 kHz, C_{LOAD} = 0		0.1		mA
Input							
V_{HIT}	Input rising threshold		UCC27200A		5.8	8	V
V_{LIT}	Input falling threshold			3	5.4		
V_{IHYS}	Input voltage hysteresis				0.4		
V_{HIT}	Input voltage threshold		UCC27201A		1.7	2.5	
V_{LIT}	Input voltage threshold			0.8	1.6		
V_{IHYS}	Input voltage Hysteresis				100		mV
R_{IN}	Input pulldown resistance			100	200	350	kΩ
Undervoltage Protection (UVLO)							
	VDD rising threshold			6.2	7.1	7.8	V
	VDD threshold hysteresis				0.5		
	VHB rising threshold			5.8	6.7	7.2	
	VHB threshold hysteresis				0.4		
Bootstrap Diode							
V_F	Low-current forward voltage		I_{VDD} - HB = 100 µA		0.65	0.85	V
V_{FI}	High-current forward voltage		I_{VDD} - HB = 100 mA		0.85	1.1	
R_D	Dynamic resistance, ΔVF/ΔI		I_{VDD} - HB = 100 mA and 80 mA		0.6	1.0	Ω
LO Gate Driver							
V_{LOL}	Low level output voltage		I_{LO} = 100 mA		0.18	0.4	V
V_{LOH}	High level output voltage	T_J = -40 to 125°C	I_{LO} = -100 mA, V_{LOH} = V_{DD} - V_{LO}		0.25	0.4	
		T_J = -40 to 140°C	I_{LO} = -100 mA, V_{LOH} = V_{DD} - V_{LO}		0.25	0.42	
	Peak pull-up current		V_{LO} = 0 V		3		A
	Peak pull-down current		V_{LO} = 12 V		3		
HO Gate Driver							
V_{HOL}	Low level output voltage		I_{HO} = 100 mA		0.18	0.4	V
V_{HOH}	High level output voltage	T_J = -40 to 125°C	I_{HO} = -100 mA, V_{HOH} = V_{HB}- V_{HO}		0.25	0.4	
		T_J = -40 to 140°C	I_{HO} = -100 mA, V_{HOH} = V_{HB}- V_{HO}		0.25	0.42	
	Peak pull-up current		V_{HO} = 0 V		3		A
	Peak pull-down current		V_{HO} = 12 V		3		
Propagation Delays							

ELECTRICAL CHARACTERISTICS (continued)

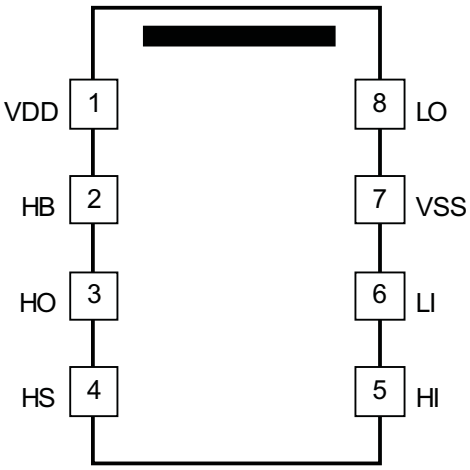
over operating free-air temperature range, V_{DD} = V_{HB} = 12 V, V_{HS} = V_{SS} = 0 V, No load on LO or HO, T_A = T_J = -40°C to +140°C, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DLFF}	V_{LI} falling to V_{LO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	ns
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DHFF}	V_{HI} falling to V_{HO} falling	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DLRR}	V_{LI} rising to V_{LO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
t_{DHRR}	V_{HI} rising to V_{HO} rising	T_J = -40 to 125°C	C_{LOAD} = 0		20	45	
		T_J = -40 to 140°C	C_{LOAD} = 0		20	50	
Delay Matching							
t_{MON}	LI ON, HI OFF				1	7	ns
t_{MOFF}	LI OFF, HI ON				1	7	
Output Rise and Fall Time							
t_R	LO, HO		C_{LOAD} = 1000 pF		8		ns
t_F	LO, HO		C_{LOAD} = 1000 pF		7		
t_R	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.35	0.6	us
t_F	LO, HO (3 V to 9 V)		C_{LOAD} = 0.1 µF		0.3	0.6	
Miscellaneous							
	Minimum input pulse width that changes the output				50		ns
	Bootstrap diode turn-off time		I_F = 20 mA, I_{REV} = 0.5 A(1) (2)		20		

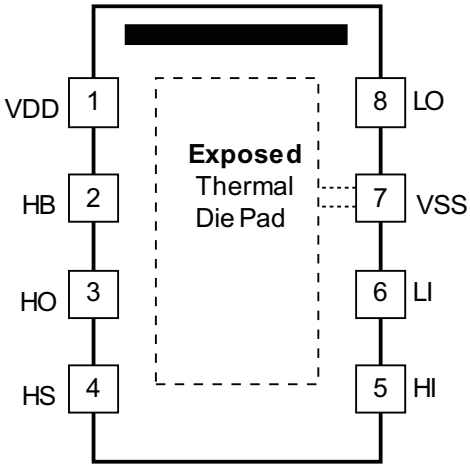
(1) Typical values for T_A = 25°C
(2) I_F: Forward current applied to bootstrap diode, I_{REV}: Reverse current applied to bootstrap diode.

DEVICE INFORMATION

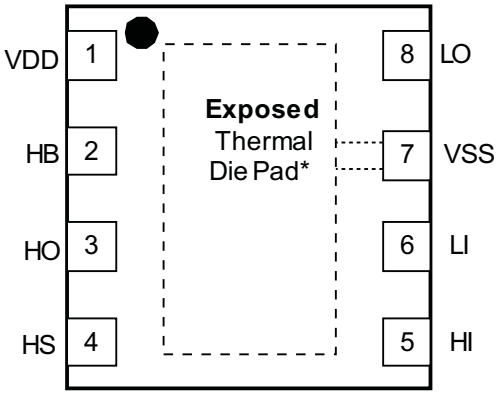
SOIC-8(D)
TOP VIEW



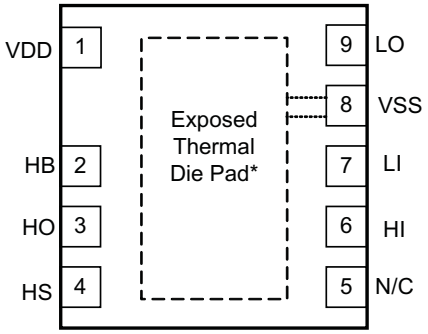
Power Pad™ SOIC-8(DDA)
TOP VIEW



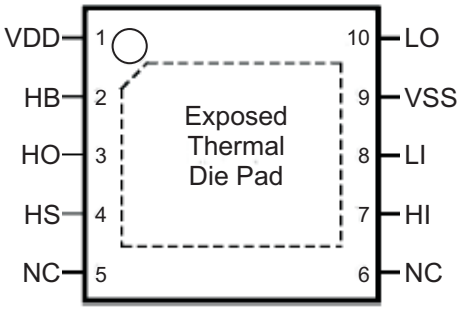
SON-8 (DRM)
TOP VIEW



SON-9 (DRC)
TOP VIEW



SON-10 (DPR)
TOP VIEW



NOTE

Pin VSS and the exposed thermal die pad are internally connected.

PIN FUNCTIONS

PIN				I/O	DESCRIPTION
PIN NAME	DRM/D/DDA	DRC	DPR		
VDD	1	1	1	I	Positive supply to the lower gate driver. De-couple this pin to VSS (GND). Typical decoupling capacitor range is 0.22 µF to 1.0 µF.
HB	2	2	2	I	High-side bootstrap supply. The bootstrap diode is on-chip but the external bootstrap capacitor is required. Connect positive side of the bootstrap capacitor to this pin. Typical range of HB bypass capacitor is 0.022 µF to 0.1 µF, the value is dependant on the gate charge of the high-side MOSFET however.
HO	3	3	3	O	High-side output. Connect to the gate of the high-side power MOSFET.
HS	4	4	4	I	High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin.
HI	5	6	7	I	High-side input.
LI	6	7	8	I	Low-side input.
VSS	7	8	9	O	Negative supply terminal for the device which is generally grounded.
LO	8	9	10	O	Low-side output. Connect to the gate of the low-side power MOSFET.
N/C	-	5	5/6	-	No connection. Pins labeled N/C have no connection.
PowerPAD™	Pad(1)	Pad	Pad	-	Connect to a large thermal mass trace or GND plane to dramatically improve thermal performance.

(1) Pin VSS and the exposed thermal die pad are internally connected on the DDA and DRM packages only. Electrically referenced to VSS (GND).

FUNCTIONAL BLOCK DIAGRAM

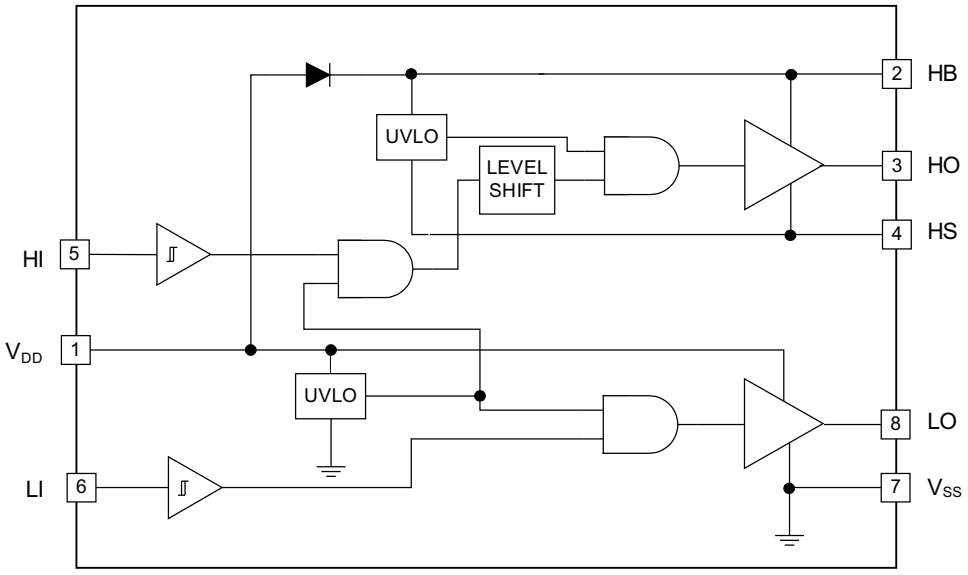


Figure 1.

TIMING DIAGRAMS

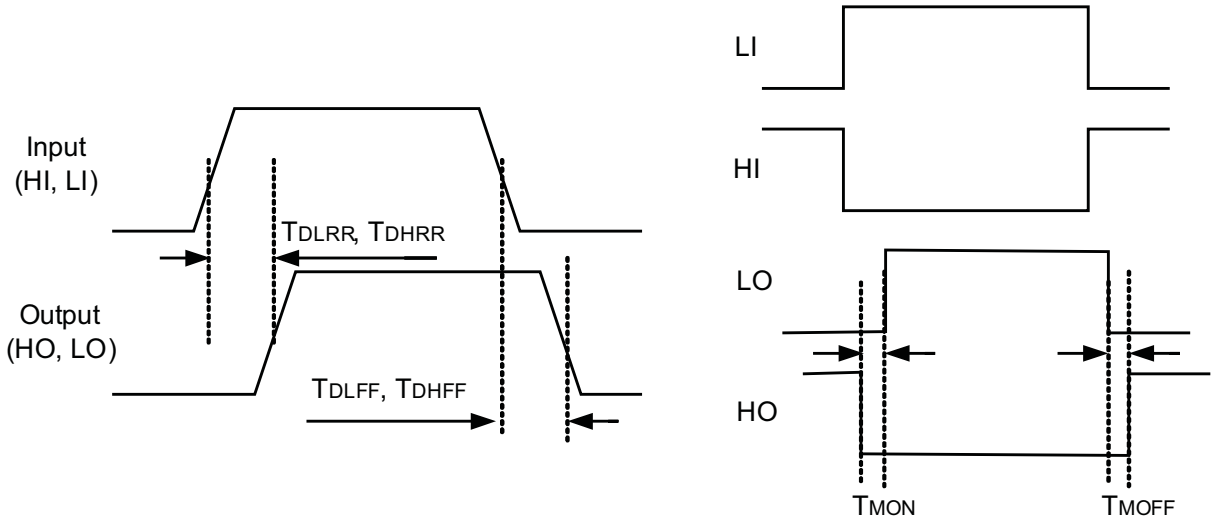


Figure 2.

TYPICAL CHARACTERISTICS

UCC27200A IDD OPERATING CURRENT vs FREQUENCY

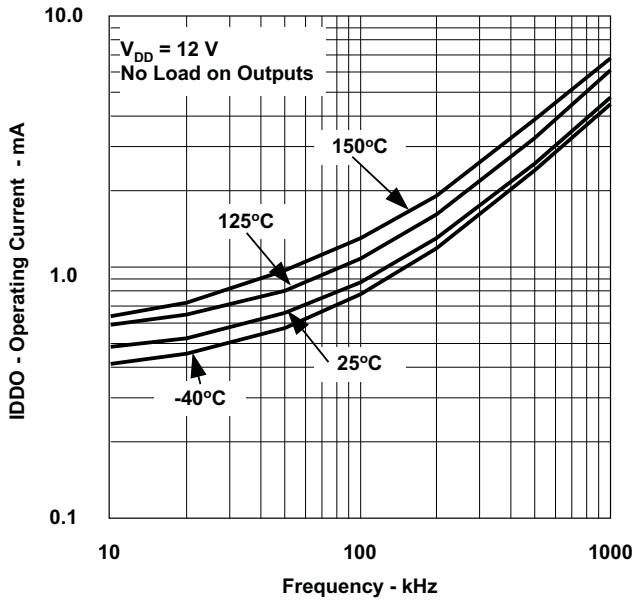


Figure 3.

UCC27201A IDD OPERATING CURRENT vs FREQUENCY

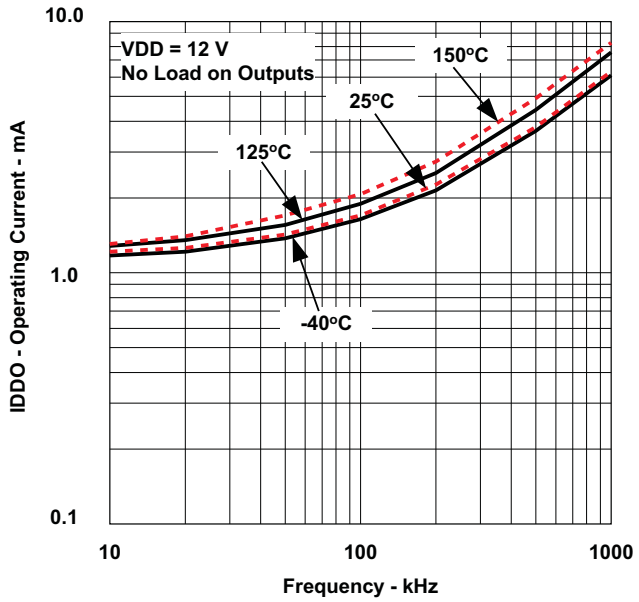


Figure 4.

BOOT VOLTAGE OPERATING CURRENT vs FREQUENCY

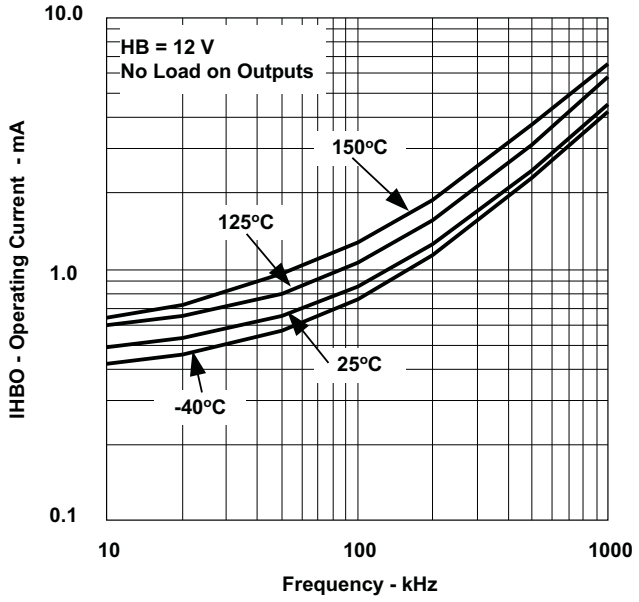


Figure 5.

HB TO VSS OPERATING CURRENT vs FREQUENCY

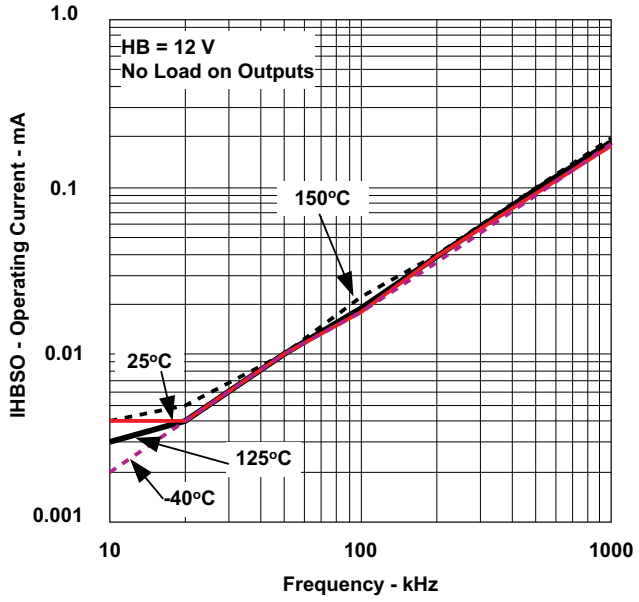


Figure 6.

TYPICAL CHARACTERISTICS (continued)

UCC27200A INPUT THRESHOLD vs SUPPLY VOLTAGE

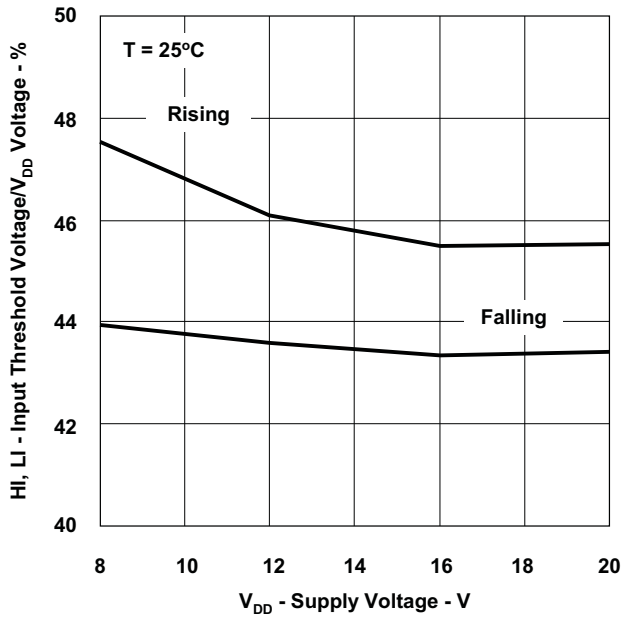


Figure 7.

UCC27201A INPUT THRESHOLD vs SUPPLY VOLTAGE

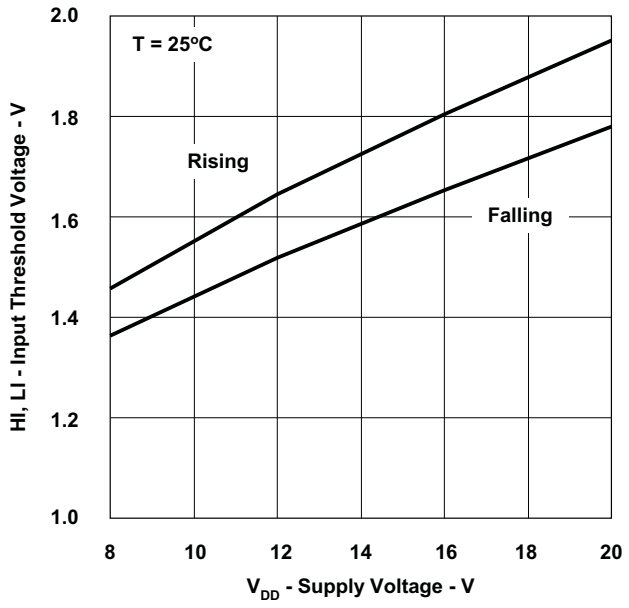


Figure 8.

UCC27200A INPUT THRESHOLD vs TEMPERATURE

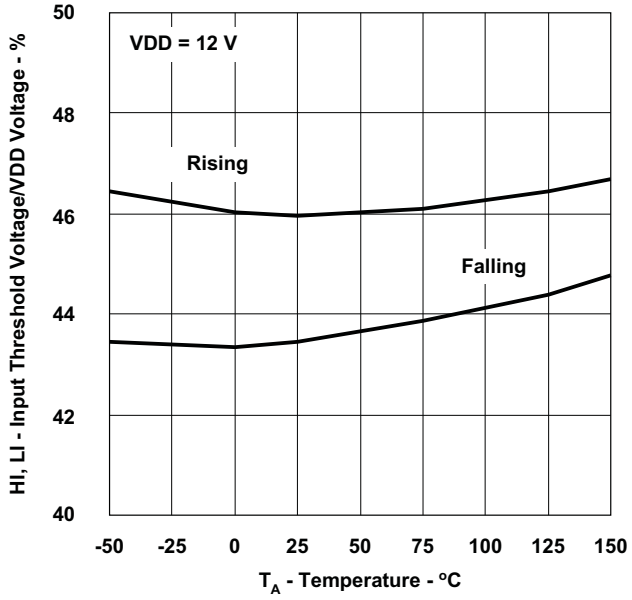


Figure 9.

UCC27201A INPUT THRESHOLD vs TEMPERATURE

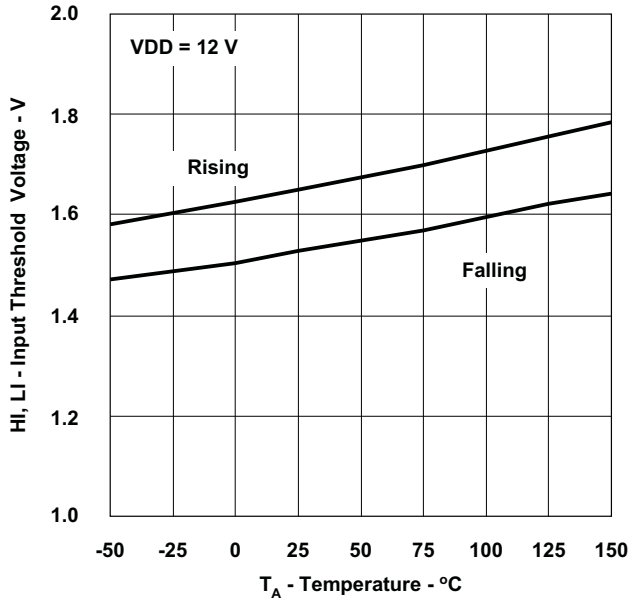


Figure 10.

TYPICAL CHARACTERISTICS (continued)

LO AND HO HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

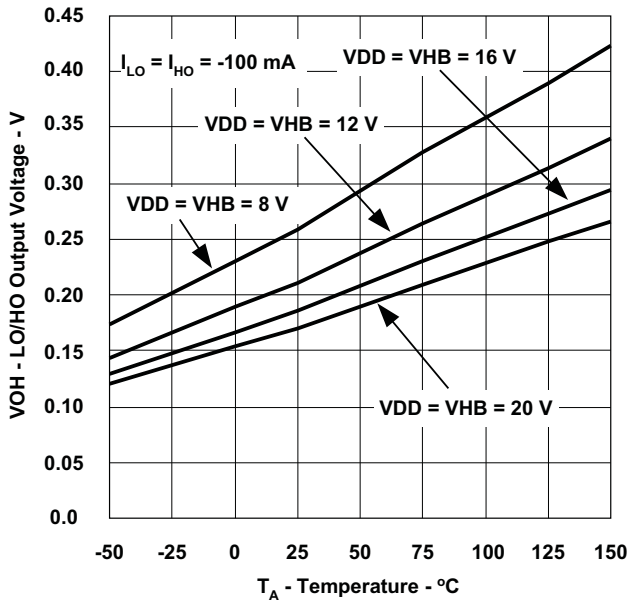


Figure 11.

LO AND HO LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

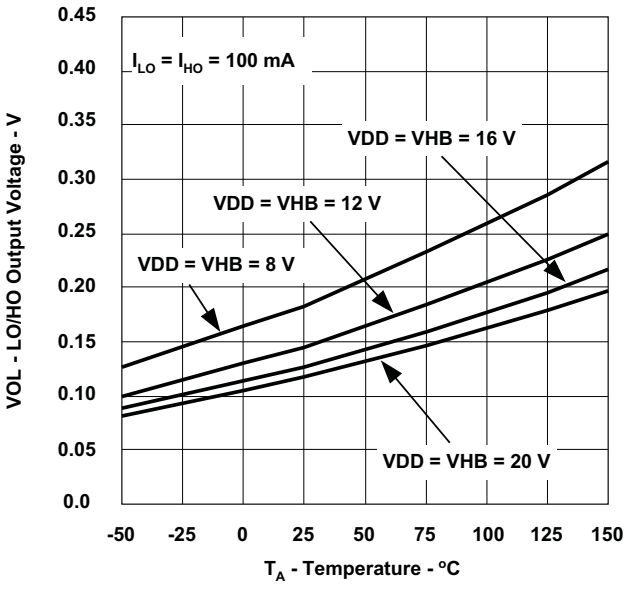


Figure 12.

UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

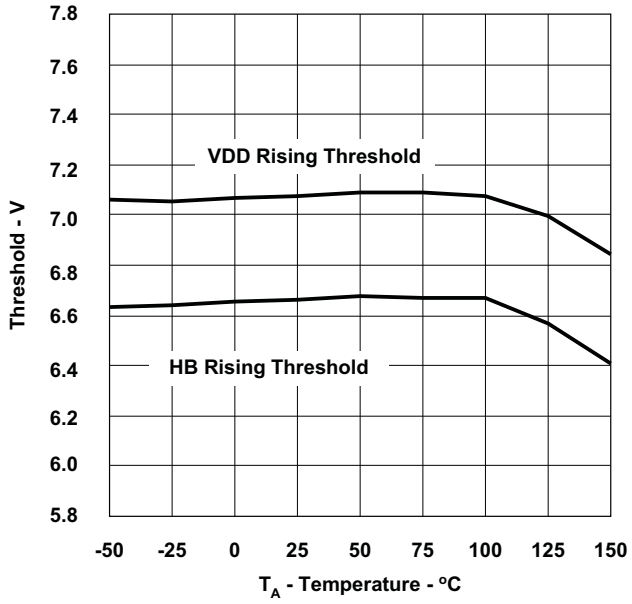


Figure 13.

UNDERVOLTAGE LOCKOUT THRESHOLD HYSTERESIS vs TEMPERATURE

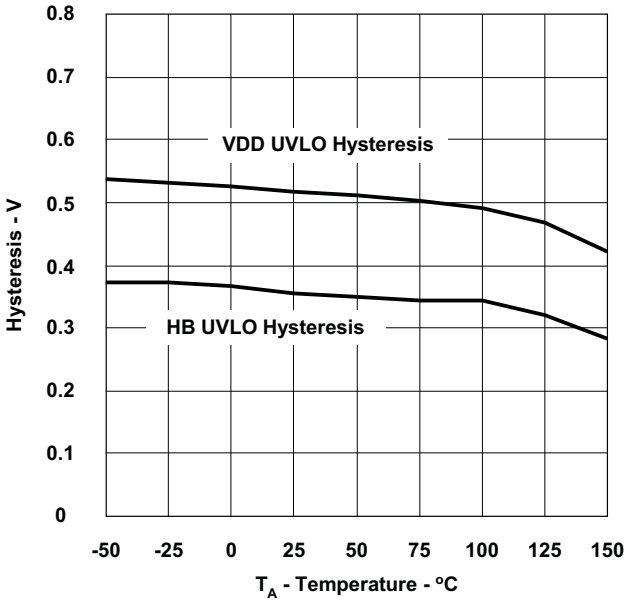


Figure 14.

TYPICAL CHARACTERISTICS (continued)

UCC27200A PROPAGATION DELAYS vs TEMPERATURE

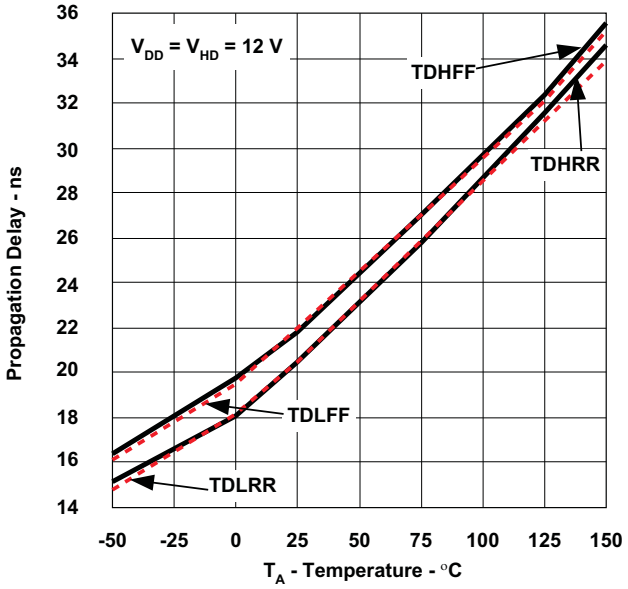


Figure 15.

UCC27201A PROPAGATION DELAYS vs TEMPERATURE

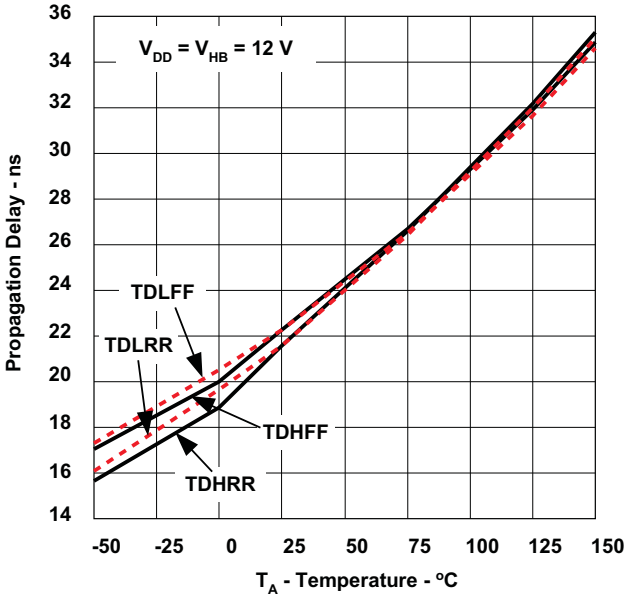


Figure 16.

UCC27200A PROPAGATION DELAY vs SUPPLY VOLTAGE

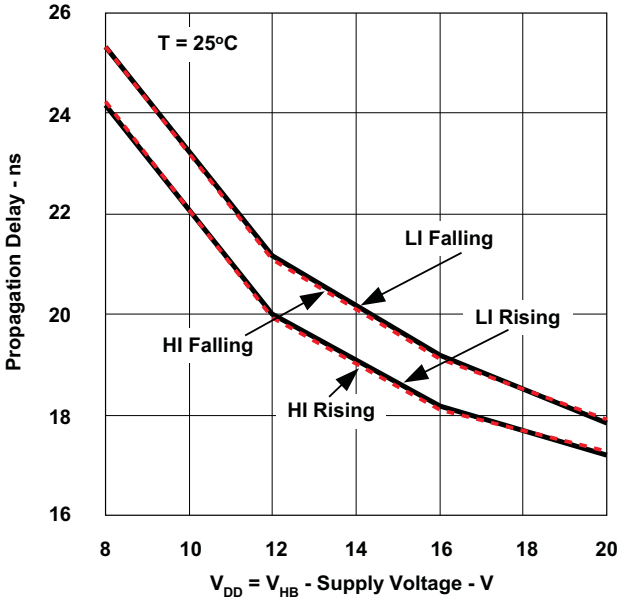


Figure 17.

UCC27201A PROPAGATION DELAY vs SUPPLY VOLTAGE

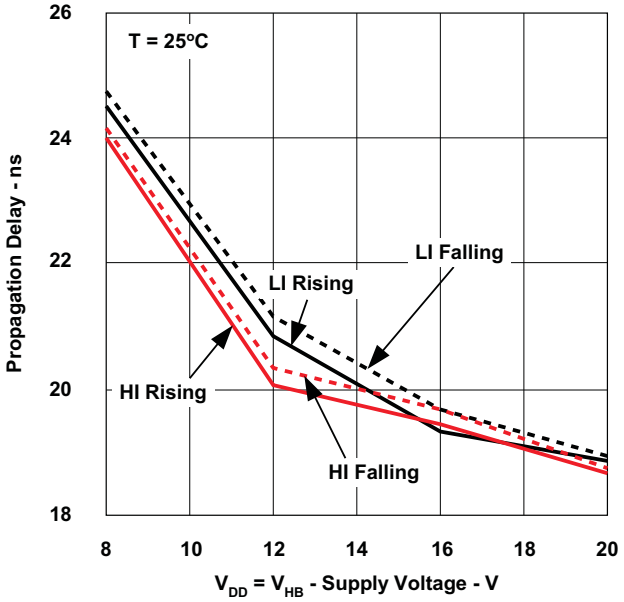


Figure 18.

TYPICAL CHARACTERISTICS (continued)

DELAY MATCHING vs TEMPERATURE

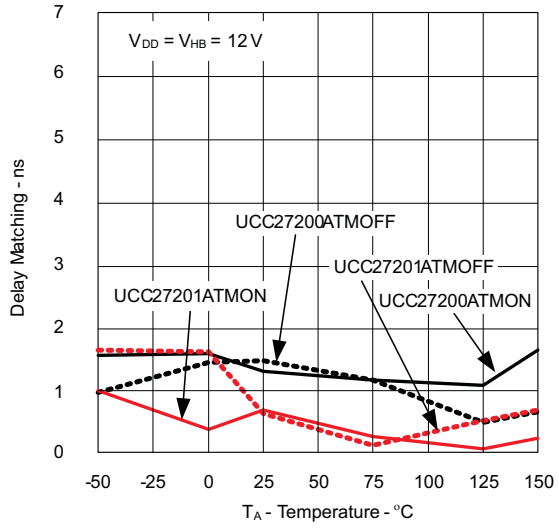


Figure 19.

OUTPUT CURRENT vs OUTPUT VOLTAGE

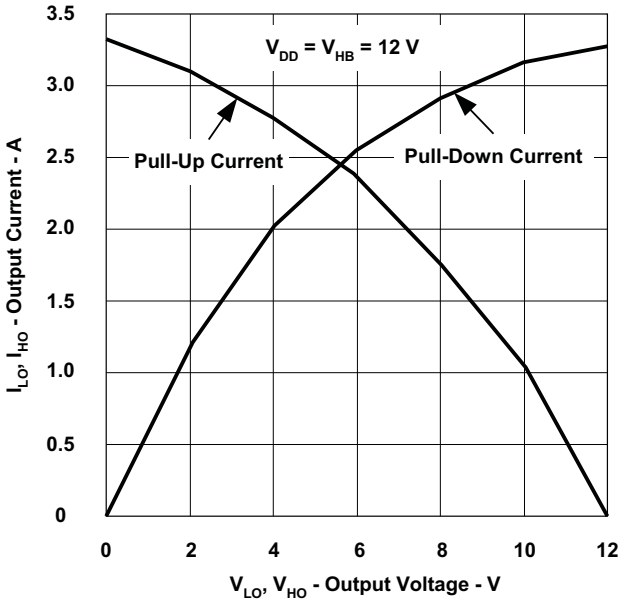


Figure 20.

DIODE CURRENT vs DIODE VOLTAGE

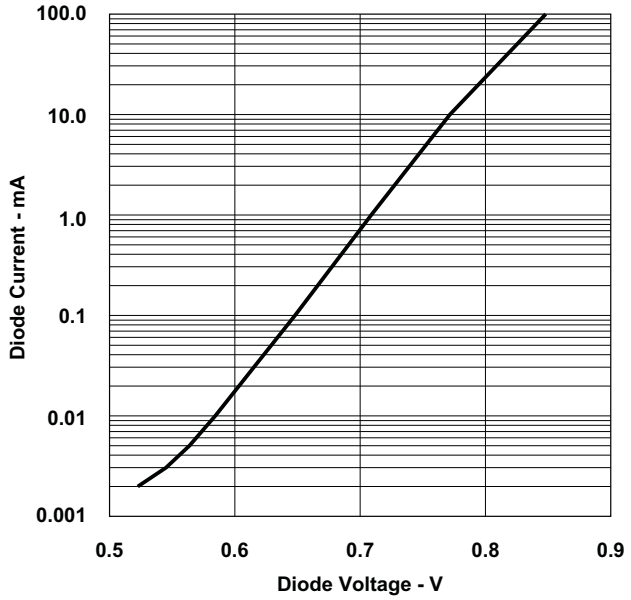


Figure 21.

QUIESCENT CURRENT vs SUPPLY VOLTAGE

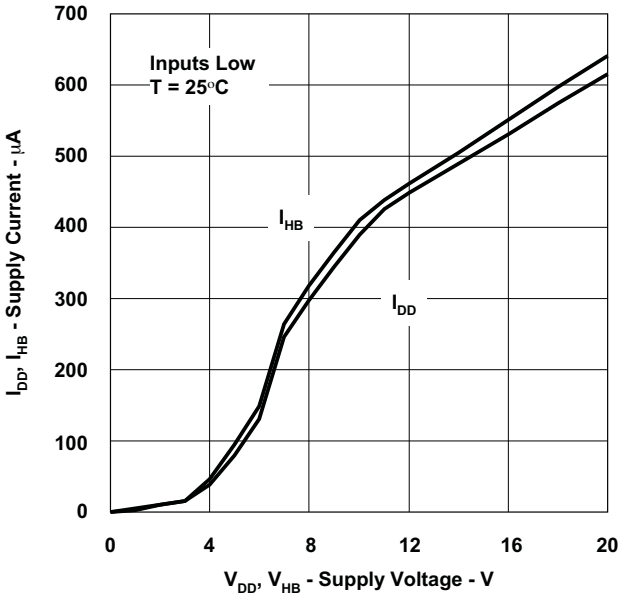


Figure 22.

APPLICATION INFORMATION

Functional Description

The UCC27200A and UCC27201A are high-side/low-side drivers. The high-side and low-side each have independent inputs which allow maximum flexibility of input control signals in the application. The boot diode for the high-side driver bias supply is internal to the UCC27200A and UCC27201A. The UCC27200A is the CMOS compatible input version and the UCC27201A is the TTL or logic compatible version. The high-side driver is referenced to the switch node (HS) which is typically the source pin of the high side MOSFET and drain pin of the low-side MOSFET. The low-side driver is referenced to VSS which is typically ground. The functions contained are the input stages, UVLO protection, level shift, boot diode, and output driver stages.

NOTE

The term “UCC2720x” applies to both the UCC27200A and UCC27201A.

Input Stages

The input stages provide the interface to the PWM output signals. The input impedance of the UCC27200A is 200 kΩ nominal and input capacitance is approximately 2 pF. The 200 kΩ is a pull-down resistance to Vss (ground). The CMOS compatible input of the UCC27200A provides a rising threshold of 48% of VDD and falling threshold of 45% of VDD. The inputs of the UCC27200A are intended to be driven from 0 to VDD levels.

The input stages of the UCC27201A incorporate an open drain configuration to provide the lower input thresholds. The input impedance is 200 kΩ nominal and input capacitance is approximately 4 pF. The 200 kΩ is a pull-down resistance to VSS (ground). The logic level compatible input provides a rising threshold of 1.7 V and a falling threshold of 1.6 V.

UVLO (Under Voltage Lockout)

The bias supplies for the high-side and low-side drivers have UVLO protection. VDD as well as VHB to VHS differential voltages are monitored. The VDD UVLO disables both drivers when VDD is below the specified threshold. The rising VDD threshold is 7.1 V with 0.5-V hysteresis. The VHB UVLO disables only the high-side driver when the VHB to VHS differential voltage is below the specified threshold. The VHB UVLO rising threshold is 6.7 V with 0.4-V hysteresis.

Level Shift

The level shift circuit is the interface from the high-side input to the high-side driver stage which is referenced to the switch node (HS). The level shift allows control of the HO output referenced to the HS pin and provides excellent delay matching with the low-side driver.

Boot Diode

The boot diode necessary to generate the high-side bias is included in the UCC2720x family of drivers. The diode anode is connected to VDD and cathode connected to VHB. With the VHB capacitor connected to HB and the HS pins, the VHB capacitor charge is refreshed every switching cycle when HS transitions to ground. The boot diode provides fast recovery times, low diode resistance, and voltage rating margin to allow for efficient and reliable operation.

Output Stages

The output stages are the interface to the power MOSFETs in the power train. High slew rate, low resistance and high peak current capability of both output drivers allow for efficient switching of the power MOSFETs. The low-side output stage is referenced from VDD to VSS and the high-side is referenced from VHB to VHS.

Design Tips

Switching the MOSFETs

Achieving optimum drive performance at high frequency efficiently requires special attention to layout and minimizing parasitic inductances. Care must be taken at the driver die and package level as well as the PCB layout to reduce parasitic inductances as much as possible. Figure 23 shows the main parasitic inductance elements and current flow paths during the turn ON and OFF of the MOSFET by charging and discharging its CGS capacitance.

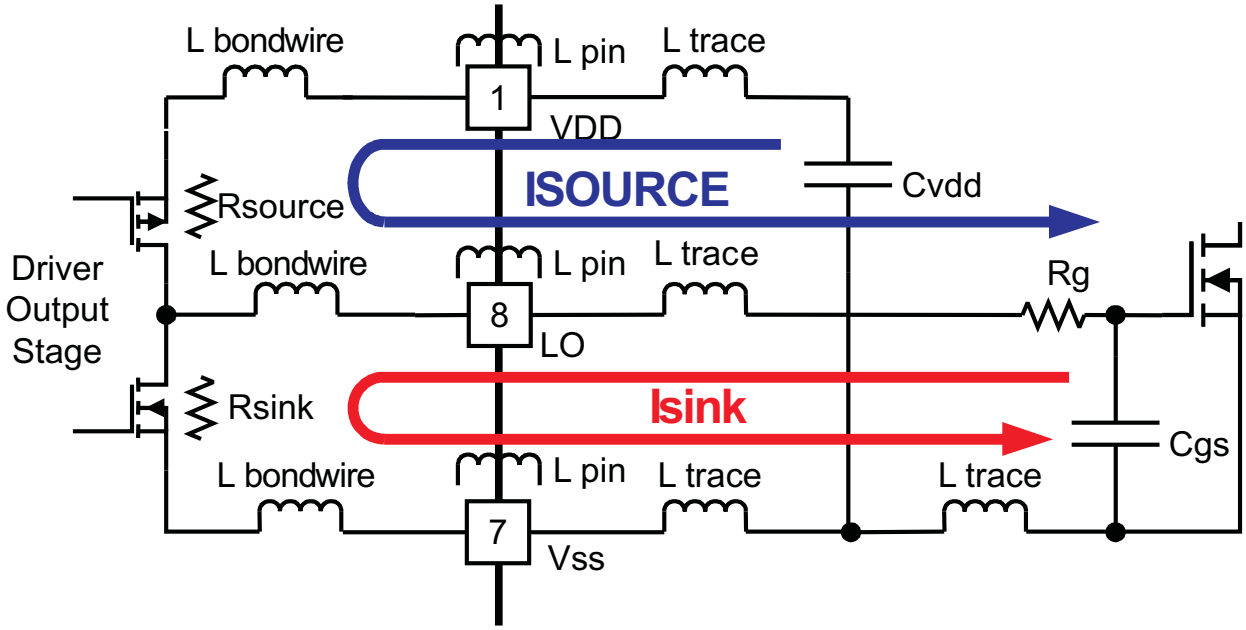


Figure 23. MOSFET Drive Paths and Circuit Parasitics

The I_{SOURCE} current charges the C_{GS} gate capacitor and the I_{SINK} current discharges it. The rise and fall time of the voltage across the gate to source defines how quickly the MOSFET can be switched. Based on actual measurements, the analytical curves in Figure 24 and Figure 25 indicate the output voltage and current of the drivers during the discharge of the load capacitor. Figure 24 shows voltage and current as a function of time. Figure 25 indicates the relationship of voltage and current during fast switching. These figures demonstrate the actual switching process and limitations due to parasitic inductances.

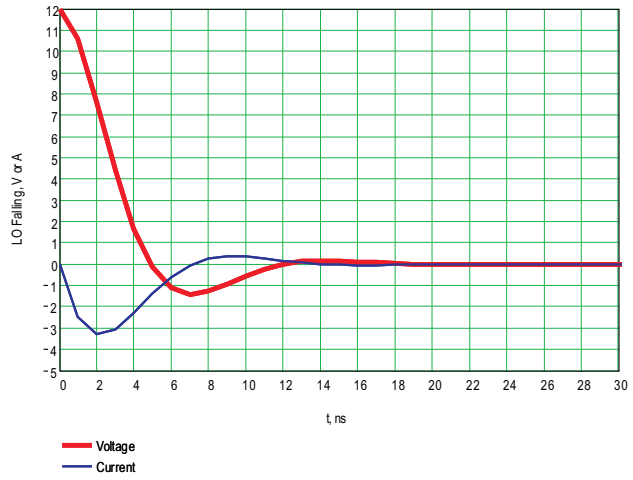


Figure 24. Turn-Off Voltage and Current vs Time

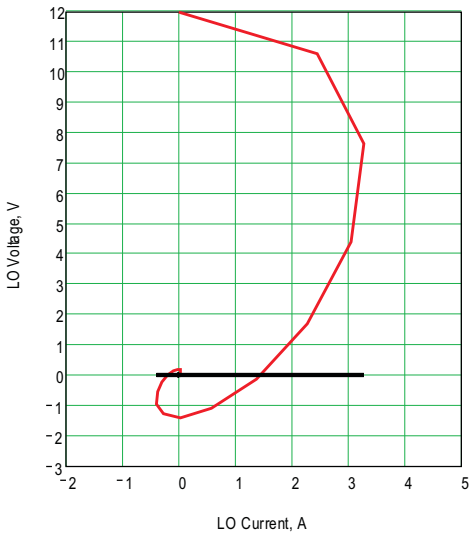


Figure 25. Turn-Off Voltage and Current Switching Diagram

Turning off the MOSFET needs to be achieved as fast as possible to minimize switching losses. For this reason the UCC2720x drivers are designed for high peak currents and low output resistance. The sink capability is specified as 0.18 V at 100-mA dc current implying 1.8-Ω $R_{DS(on)}$. With 12-V drive voltage, no parasitic inductance and a linear resistance, one would expect initial sink current amplitude of 6.7 A for both high-side and low-side drivers. Assuming a pure R-C discharge circuit of the gate capacitor, one would expect the voltage and current waveforms to be exponential. Due to the parasitic inductances and non-linear resistance of the driver MOSFET'S, the actual waveforms have some ringing and the peak-sink current of the drivers is approximately 3.3 A as shown in Figure 20. The overall parasitic inductance of the drive circuit is estimated at 4 nH. The internal parasitic inductance of the SOIC-8 package is estimated to be 2 nH including bond wires and leads. The SON-8 package reduces the internal parasitic inductances by more than 50%.

Actual measured waveforms are shown in Figure 26 and Figure 27. As shown, the typical rise time of 8 ns and fall time of 7 ns is conservatively rated.

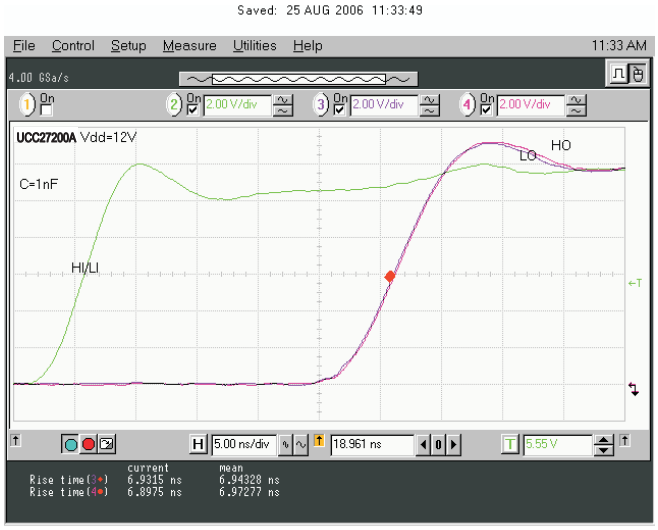


Figure 26. V_{LO} and V_{HO} Rise Time, 1-nF Load, 5 ns/Div

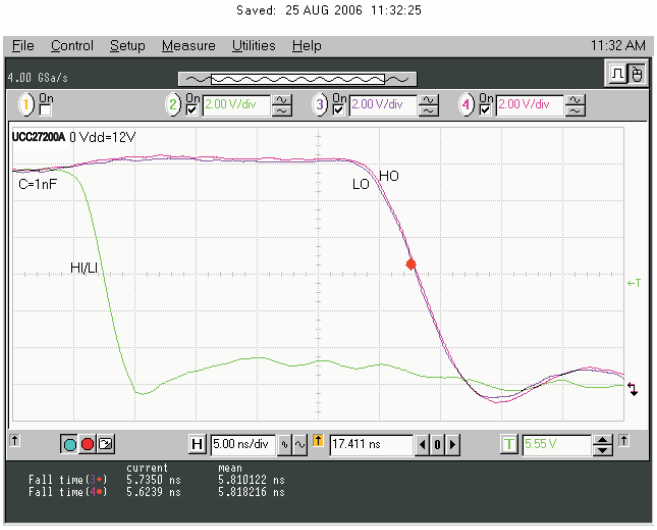


Figure 27. V_{LO} and V_{HO} Fall Time, 1-nF Load, 5-ns/Div

Dynamic Switching of the MOSFETs

The true behavior of MOSFETS presents a dynamic capacitive load primarily at the gate to source threshold voltage. Using the turn off case as the example, when the gate to source threshold voltage is reached the drain voltage starts rising, the drain to gate parasitic capacitance couples charge into the gate resulting in the turn off plateau. The relatively low threshold voltages of many MOSFETS and the increased charge that has to be removed (Miller charge) makes good driver performance necessary for efficient switching. An open loop half bridge power converter was utilized to evaluate performance in actual applications. The schematic of the half-bridge converter is shown in Figure 30. The turn off waveforms of the UCC27200A driving two MOSFETs in parallel is shown in Figure 28 and Figure 29.

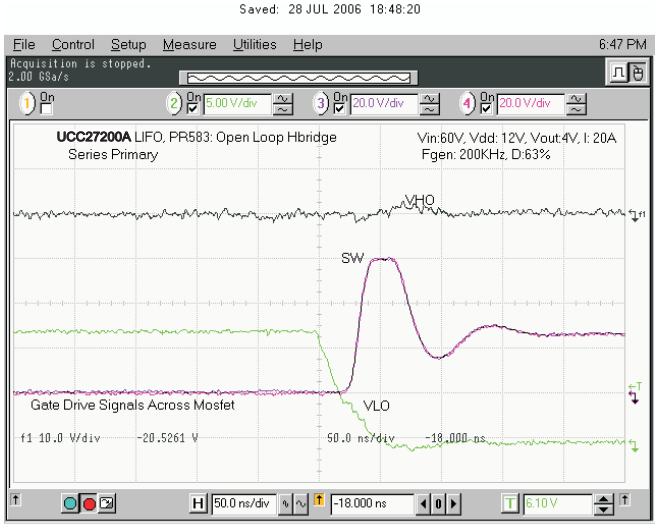


Figure 28. V_{LO} Fall Time in Half-Bridge Converter

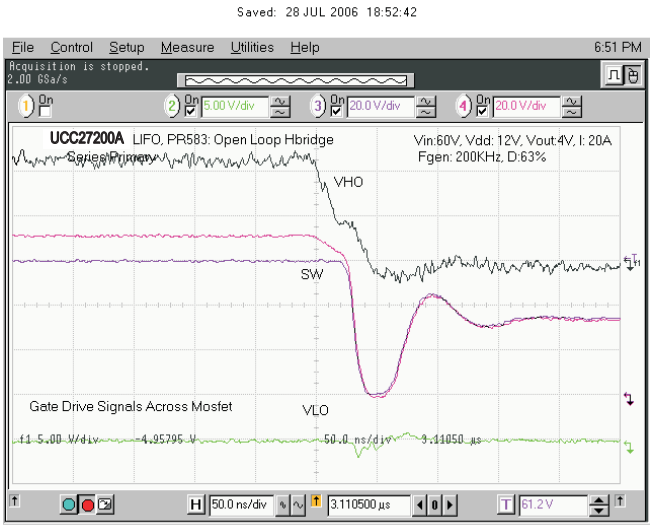


Figure 29. V_{HO} Fall Time in Half-Bridge Converter

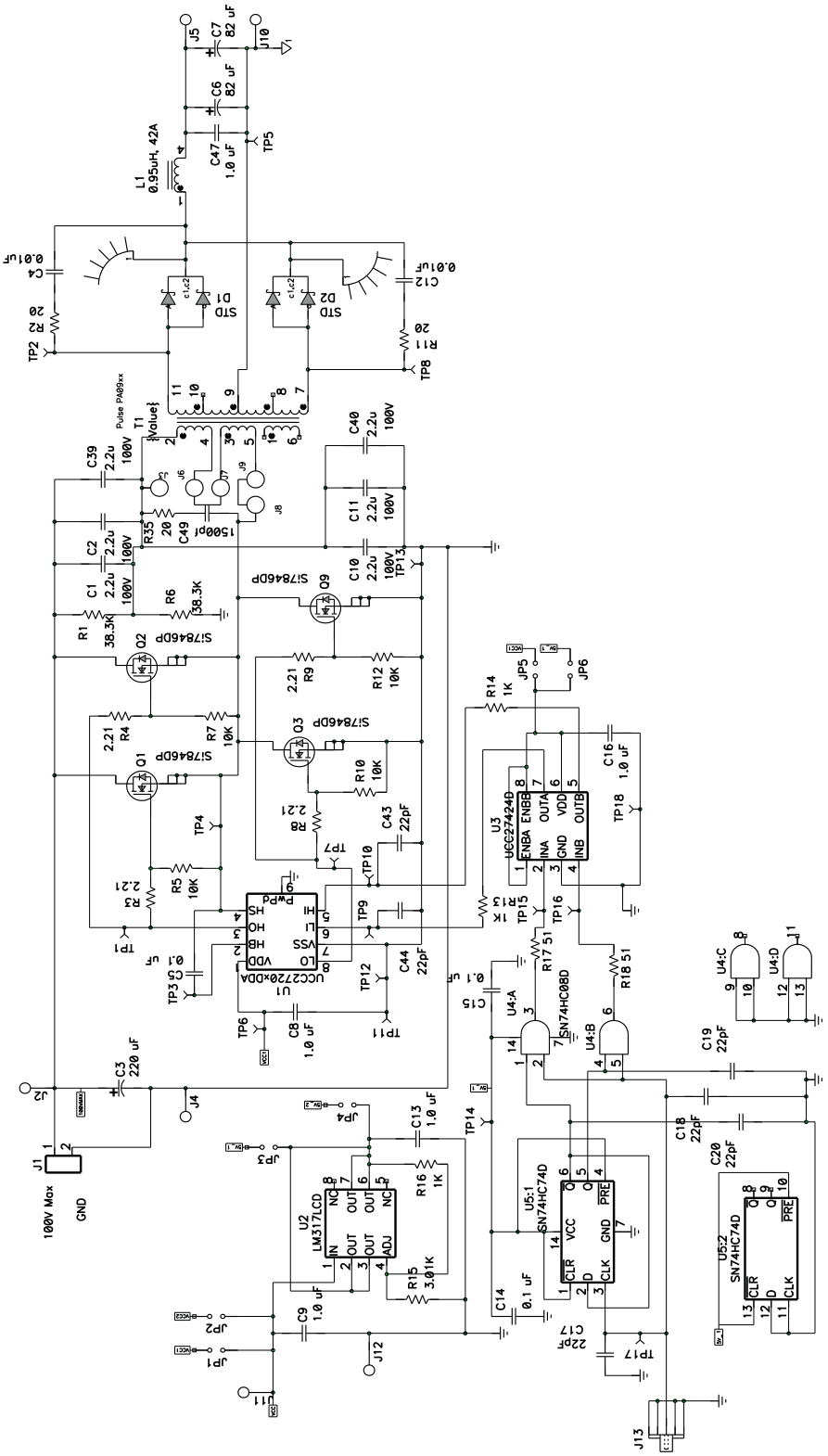


Figure 30. Open Loop Half-Bridge Converter

Delay Matching and Narrow Pulse Widths

The total delays encountered in the PWM, driver and power stage need to be considered for a number of reasons, primarily delay in current limit response. Also to be considered are differences in delays between the drivers which can lead to various concerns depending on the topology. The sync-buck topology switching requires careful selection of dead-time between the high- and low-side switches to avoid 1) cross conduction and 2) excessive body diode conduction. Bridge topologies can be affected by a resulting volt-sec imbalance on the transformer if there is imbalance in the high and low side pulse widths in a steady state condition.

Narrow pulse width performance is an important consideration when transient and short circuit conditions are encountered. Although there may be relatively long steady state PWM output-driver-MOSFET signals, very narrow pulses may be encountered in 1) soft start, 2) large load transients, and 3) short circuit conditions.

The UCC2720x driver family offers excellent performance regarding high and low-side driver delay matching and narrow pulse width performance. The delay matching waveforms are shown in Figure 31 and Figure 32. The UCC2720x driver narrow pulse performance is shown in Figure 33 and Figure 34.

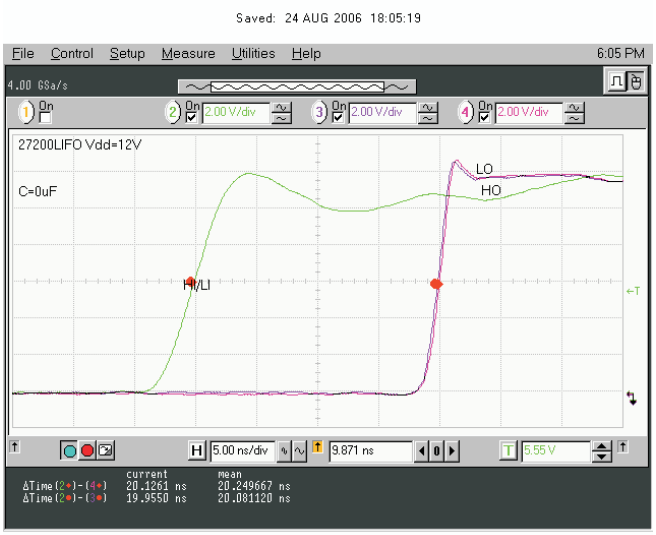


Figure 31. V_{LO} and V_{HO} Rising Edge Delay Matching

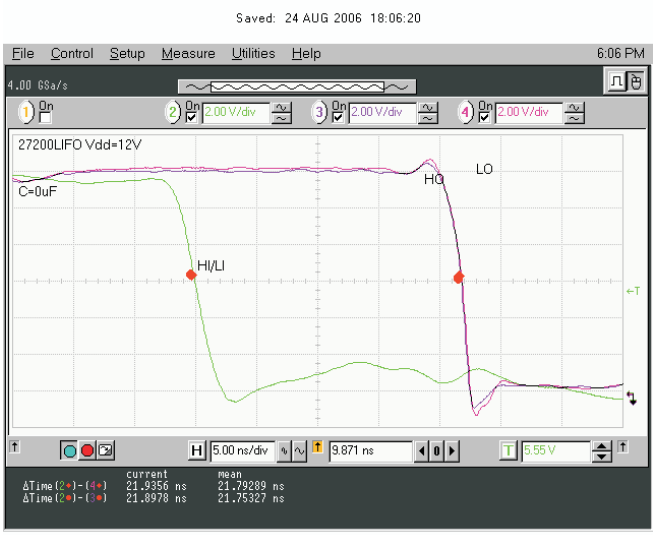


Figure 32. V_{LO} and V_{HO} Falling Edge Delay Matching

Figure 33. 20-ns Input Pulse Delay Matching

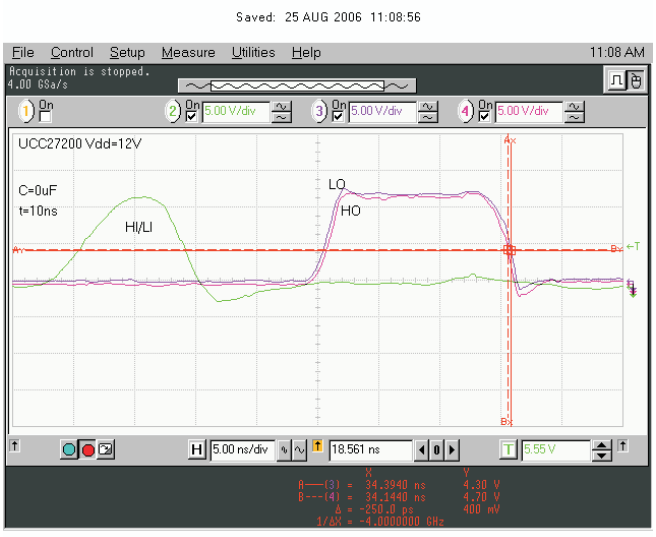


Figure 34. 10-ns Input Pulse Delay Matching

Boot Diode Performance

The UCC2720x family of drivers incorporates the bootstrap diode necessary to generate the high side bias internally. The characteristics of this diode are important to achieve efficient, reliable operation. The dc characteristics to consider are V_F and dynamic resistance. A low V_F and high dynamic resistance results in a high forward voltage during charging of the bootstrap capacitor. The UCC2720x has a boot diode rated at 0.65-V V_F and dynamic resistance of 0.6 Ω for reliable charge transfer to the bootstrap capacitor. The dynamic characteristics to consider are diode recovery time and stored charge. Diode recovery times that are specified with no conditions can be misleading. Diode recovery times at no forward current (I_F) can be noticeably less than with forward current applied. The UCC2720x boot diode recovery is specified at 20ns at I_F = 20 mA, I_{REV} = 0.5 A. At 0 mA I_F the reverse recovery time is 15 ns.

Another less obvious consideration is how the stored charge of the diode is affected by applied voltage. On every switching transition when the HS node transitions from low to high, charge is removed from the boot capacitor to charge the capacitance of the reverse biased diode. This is a portion of the driver power losses and reduces the voltage on the HB capacitor. At higher applied voltages, the stored charge of the UCC2720x PN diode is often less than a comparable Schottky diode.

Layout Recommendations

To improve the switching characteristics and efficiency of a design, the following layout rules should be followed.

- Locate the driver as close as possible to the MOSFETs.
- Locate the V_{DD} and V_{HB} (bootstrap) capacitors as close as possible to the driver.
- Pay close attention to the GND trace. Use the thermal pad of the DDA and DRM package as GND by connecting it to the VSS pin (GND). *Note: The GND trace from the driver goes directly to the source of the MOSFET but should not be in the high current path of the MOSFET(S) drain or source current.*
- Use similar rules for the HS node as for GND for the high side driver.
- Use wide traces for LO and HO closely following the associated GND or HS traces. 60 mil to 100 mil width is preferable where possible.
- Use as least two or more vias if the driver outputs or SW node needs to be routed from one layer to another. For GND the number of vias needs to be a consideration of the thermal pad requirements as well as parasitic inductance.
- Avoid L_I and H_I (driver input) going close to the HS node or any other high dV/dT traces that can induce significant noise into the relatively high impedance leads.
- Keep in mind that a poor layout can cause a significant drop in efficiency versus a good PCB layout and can even lead to decreased reliability of the whole system.

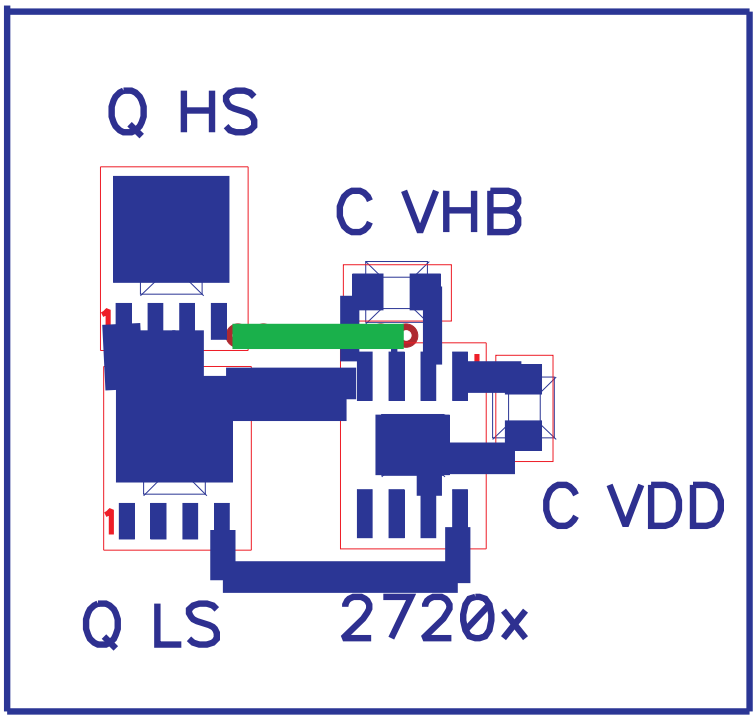


Figure 35. Example Component Placement

Additional References

These references and links to additional information may be found at www.ti.com.

1. Additional layout guidelines for PCB land patterns may be found in Application Brief SLUA271
2. Additional thermal performance guidelines may be found in Application Reports SLMA002A and SLMA004

REVISION HISTORY

Changes from Original (February 2011) to Revision A **Page**

- Added SON-10 (DPR) Package to the List of FEATURES 1
- Added SON-10 (DPR) Package to the DESCRIPTION 2
- Added the SON-10 package to the ORDERING INFORMATION table 2
- Added ordering information for the SON-10 (DPR) 2
- Added note, "DPR(SON-10) package comes either in a small reel of 250 pieces as part number UCC27200ADPRT, or large reels pieces as part number UCC27200ADPRR." 2
- Added the SON-10 package to the THERMAL INFORMATION table 4
- Changed the "Minimum input pulse width" value From: 50 ns Max To: 50 ns Typ 6
- Added the SON-10 package Pinout 7
- Changed the PIN FUNCTIONS table 8
- Added Additional PIN FUNCTIONS information. 8

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
UCC27200AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27200ADRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27200A	Samples
UCC27201AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADDA	ACTIVE	SO PowerPAD	DDA	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADDAR	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADPRR	ACTIVE	WSON	DPR	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	UCC 27201A	Samples
UCC27201ADPRT	ACTIVE	WSON	DPR	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	UCC 27201A	Samples
UCC27201ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADRCR	ACTIVE	SON	DRC	9	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	201A	Samples
UCC27201ADRCT	ACTIVE	SON	DRC	9	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 140	201A	Samples
UCC27201ADRMR	ACTIVE	VSON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples
UCC27201ADRMT	ACTIVE	VSON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 140	27201A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

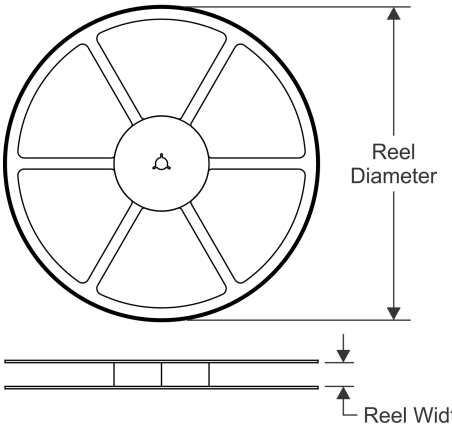
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

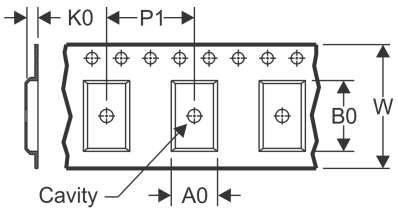
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

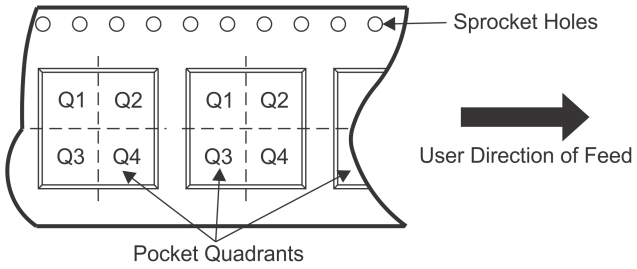


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

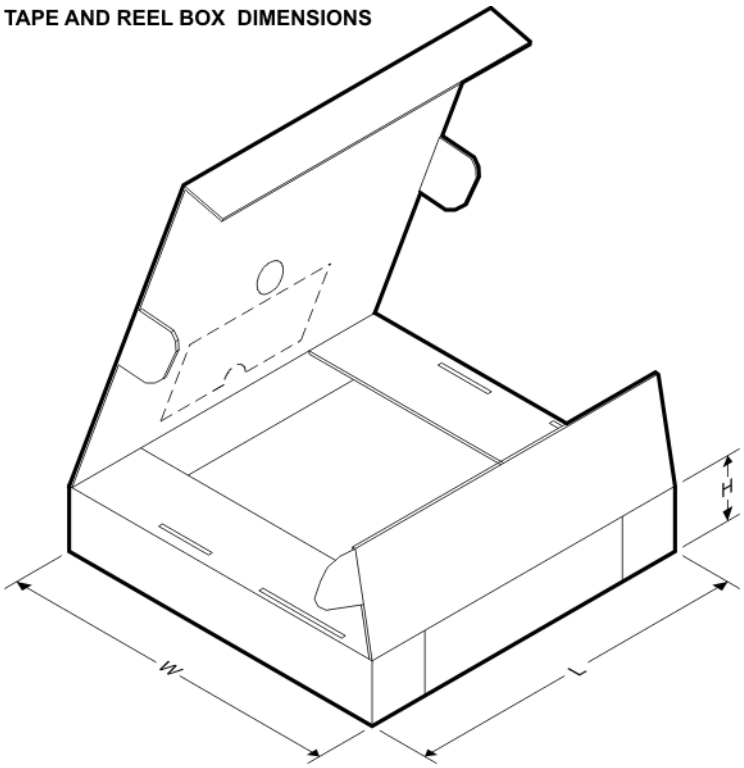
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC27200ADDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27200ADRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27200ADRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADDAR	SO Power PAD	DDA	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC27201ADPRR	WSON	DPR	10	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADPRT	WSON	DPR	10	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADRCR	SON	DRC	9	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27201ADRCT	SON	DRC	9	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
UCC27201ADRMR	VSON	DRM	8	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
UCC27201ADRMT	VSON	DRM	8	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

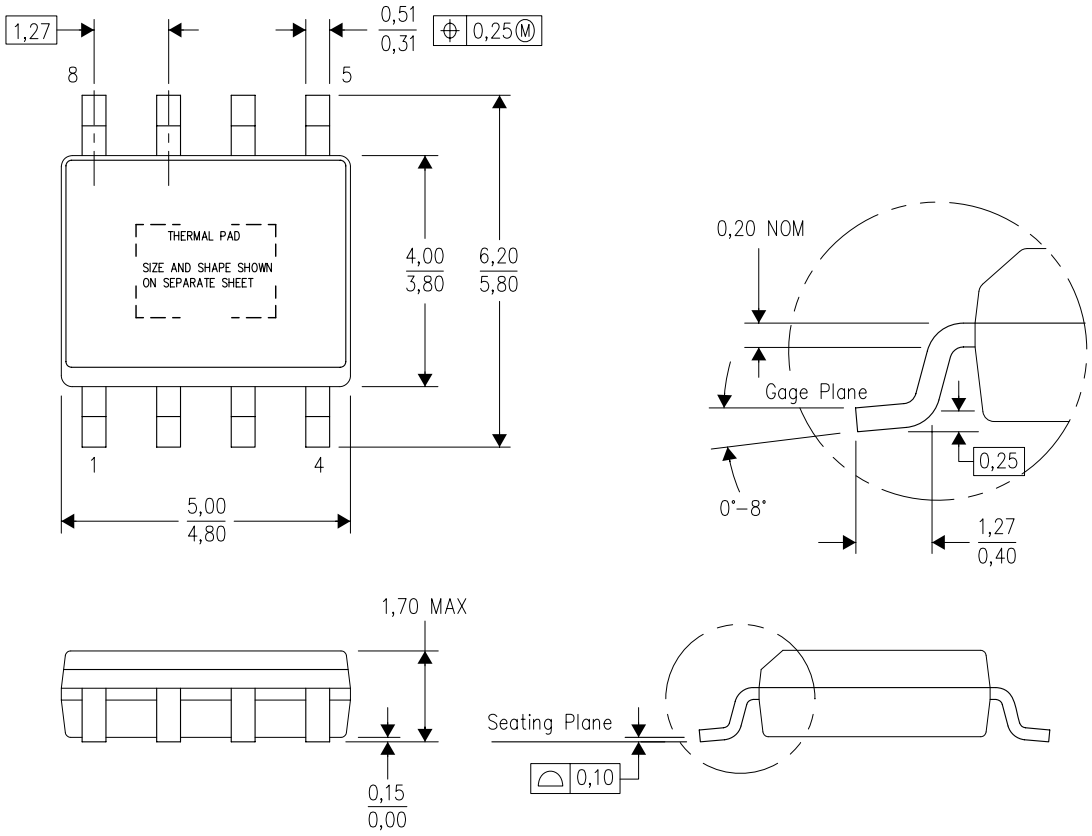
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC27200ADDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
UCC27200ADRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27200ADRMT	VSON	DRM	8	250	210.0	185.0	35.0
UCC27201ADDAR	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
UCC27201ADPRR	WSON	DPR	10	3000	367.0	367.0	35.0
UCC27201ADPRT	WSON	DPR	10	250	210.0	185.0	35.0
UCC27201ADRCR	SON	DRC	9	3000	367.0	367.0	35.0
UCC27201ADRCT	SON	DRC	9	250	210.0	185.0	35.0
UCC27201ADRMR	VSON	DRM	8	3000	367.0	367.0	35.0
UCC27201ADRMT	VSON	DRM	8	250	210.0	185.0	35.0

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL–OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. This package complies to JEDEC MS–012 variation BA

PowerPAD is a trademark of Texas Instruments.

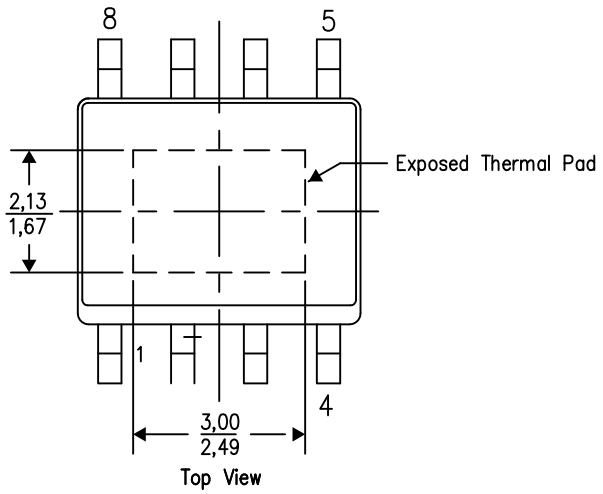
DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



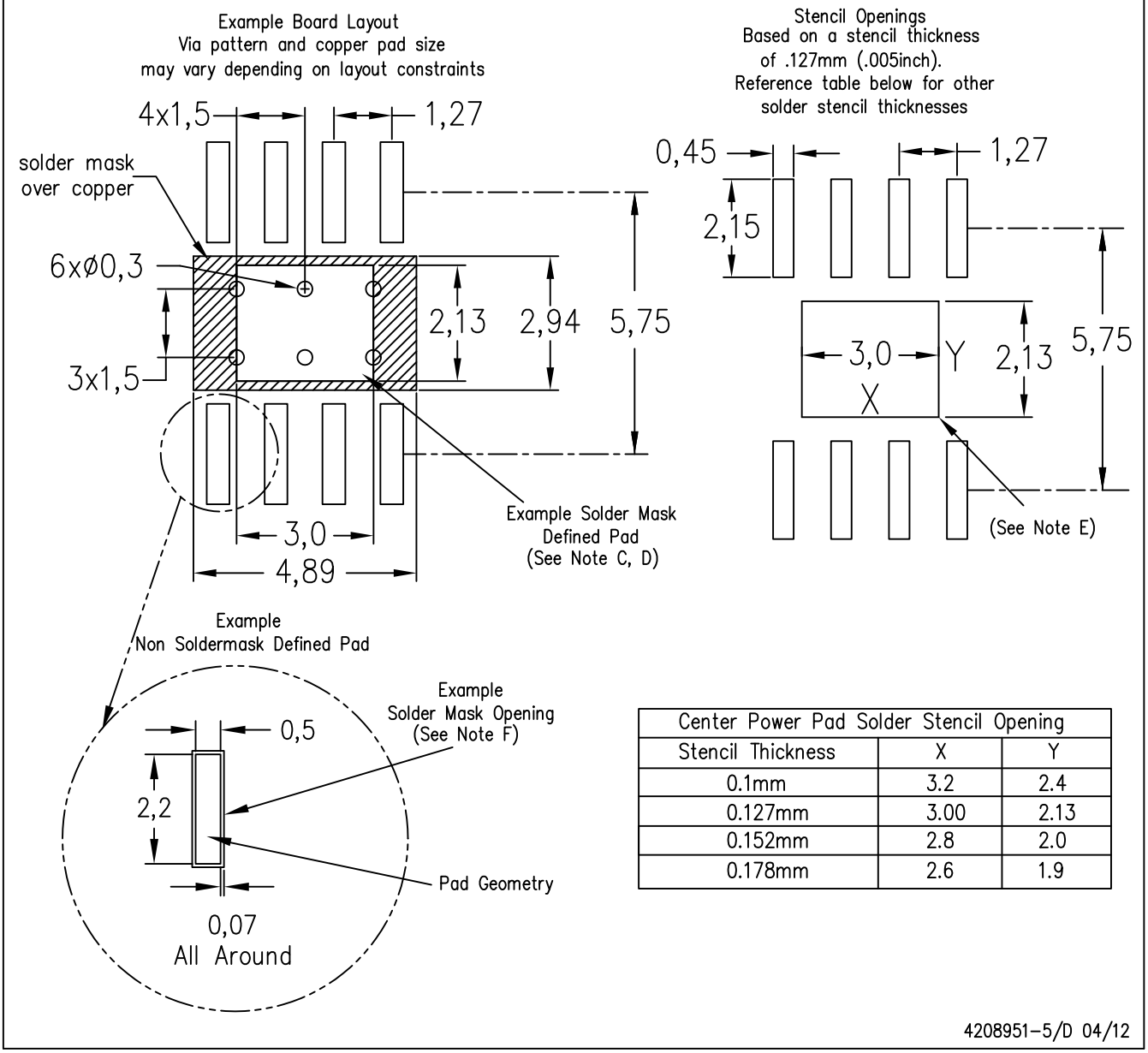
Exposed Thermal Pad Dimensions

4206322–5/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

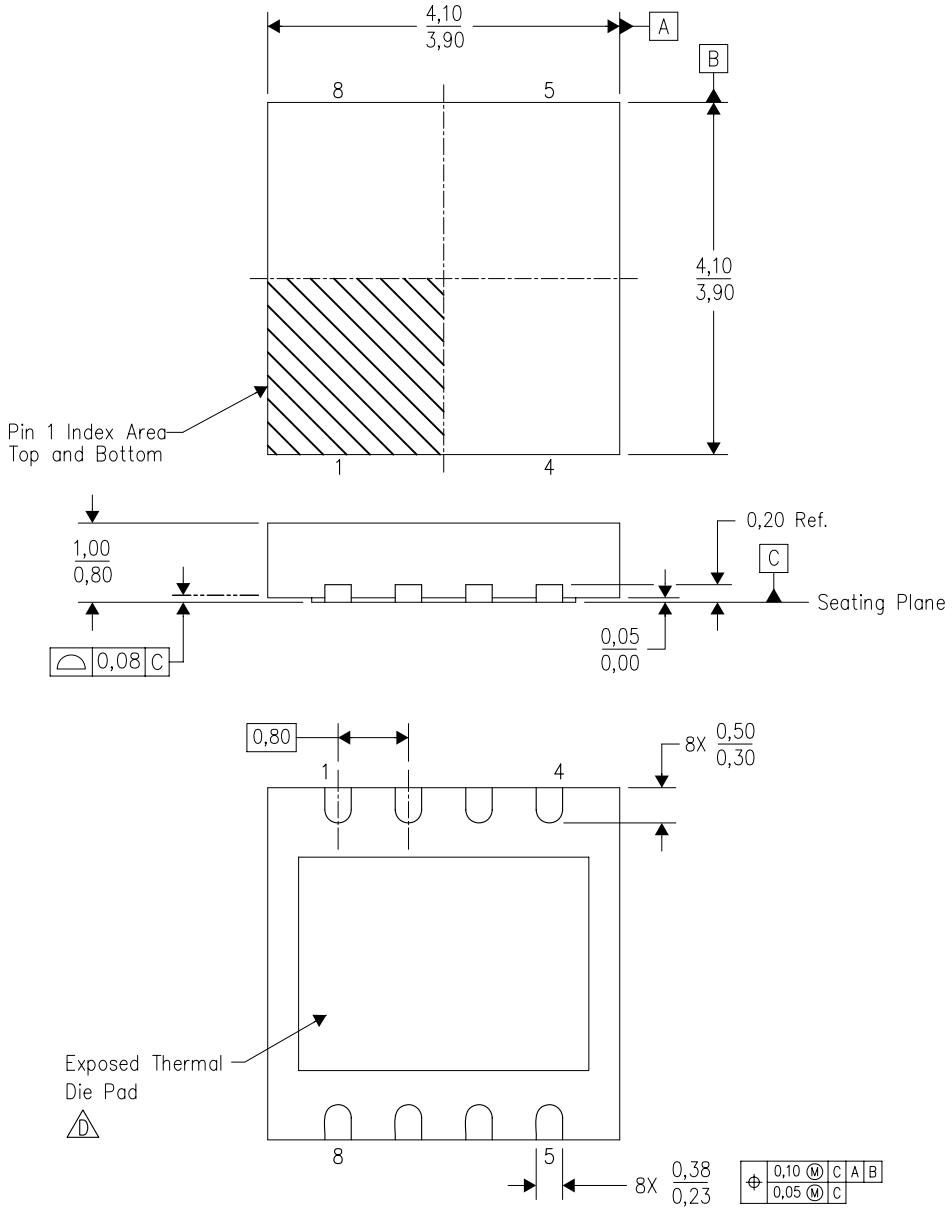


Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	3.2	2.4
0.127mm	3.00	2.13
0.152mm	2.8	2.0
0.178mm	2.6	1.9

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

DRM (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

THERMAL PAD MECHANICAL DATA

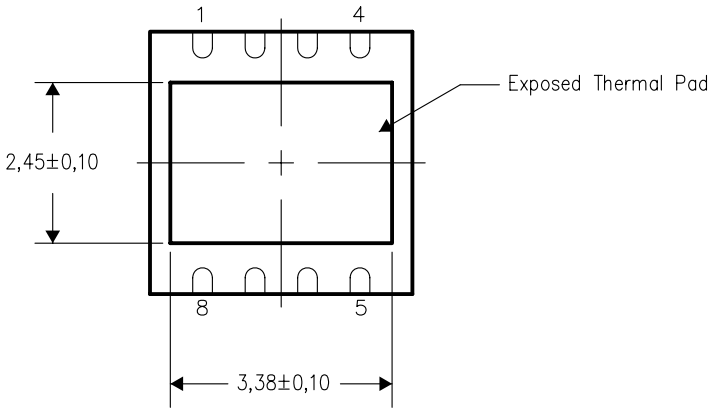
DRM (S–PDSO–N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

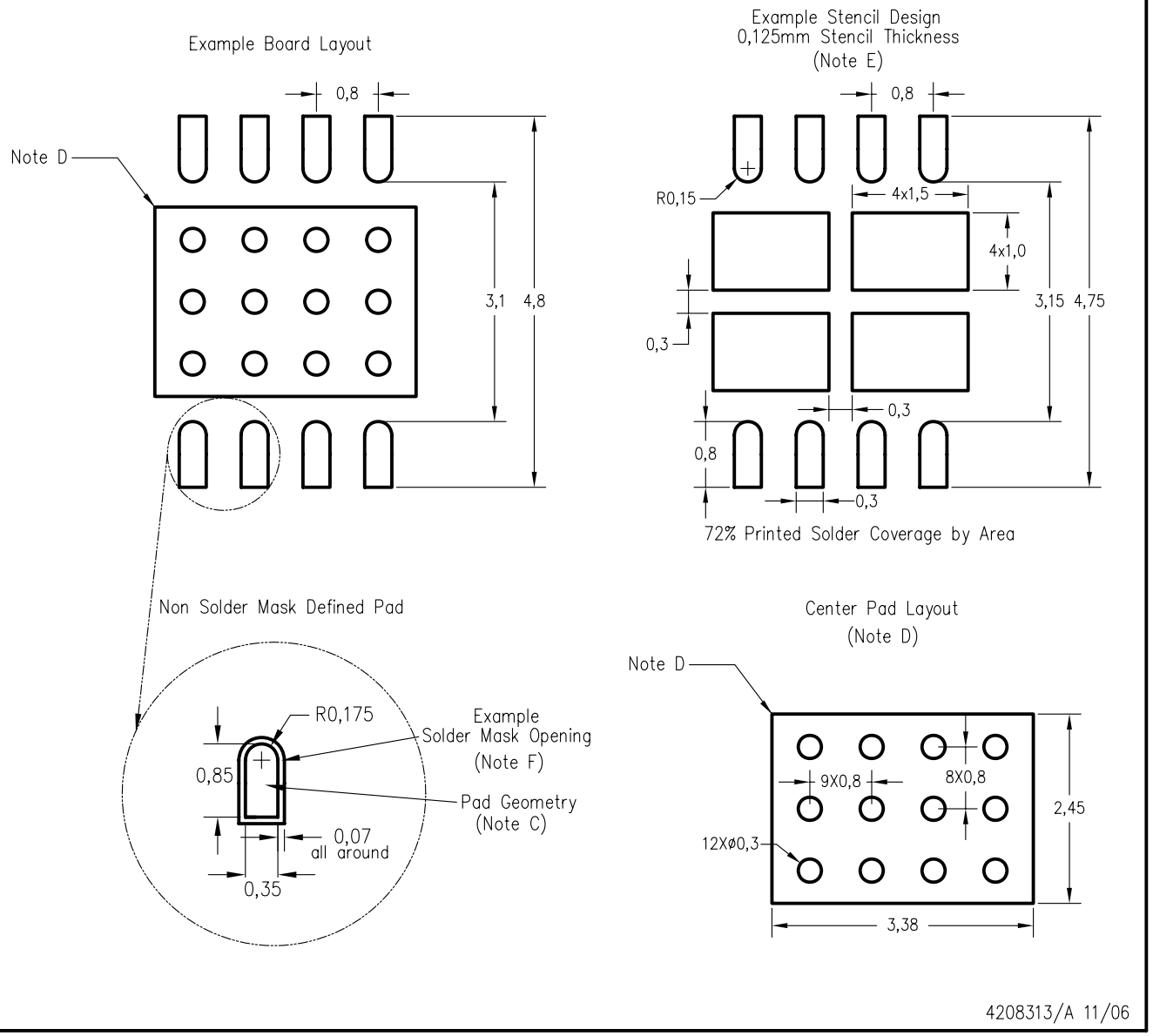


Bottom View

NOTE: All linear dimensions are in millimeters

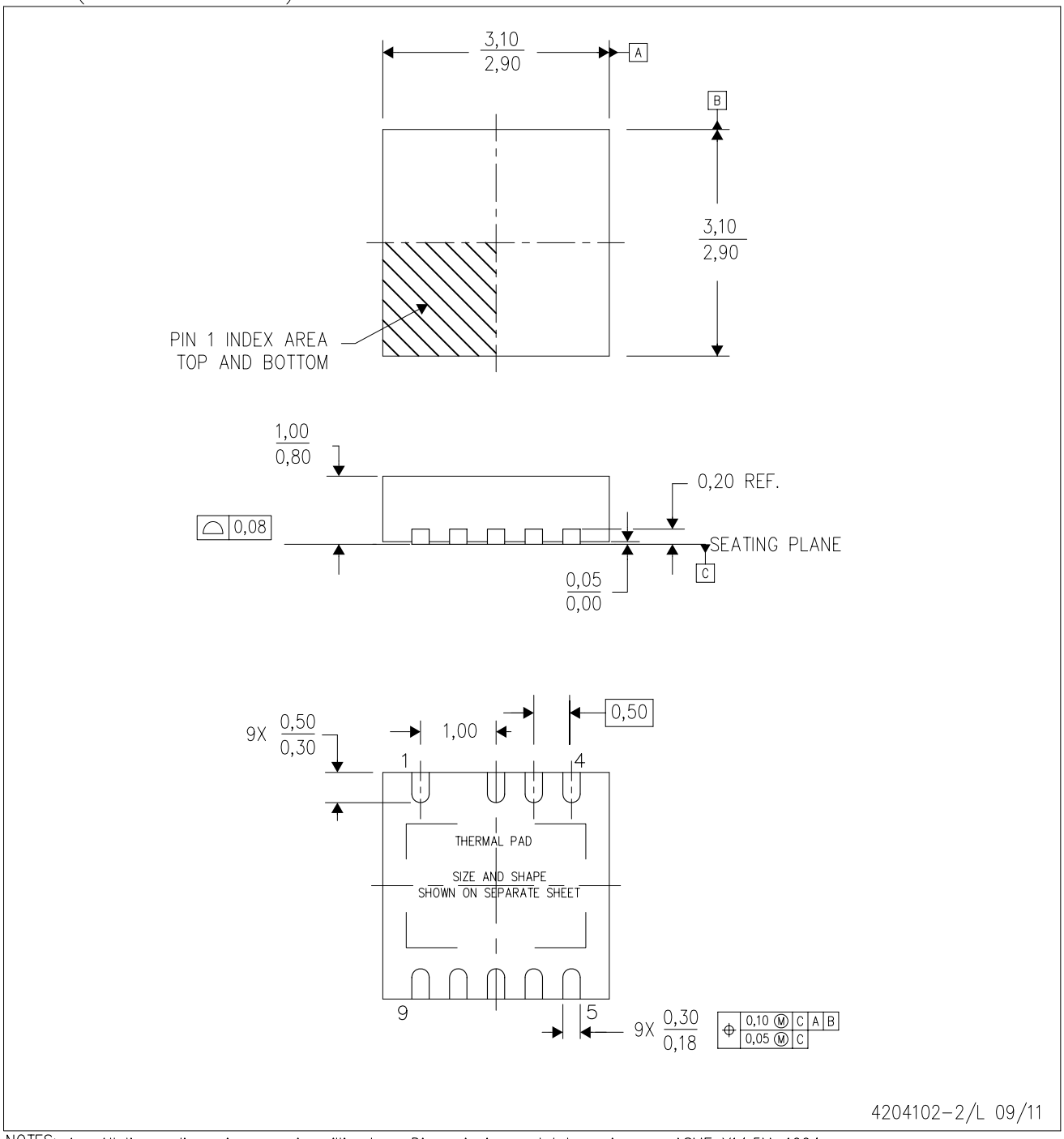
Exposed Thermal Pad Dimensions

DRM (S–PDSO–N8)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

DRC (S–PVSON–N9) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance, if present.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions, if present

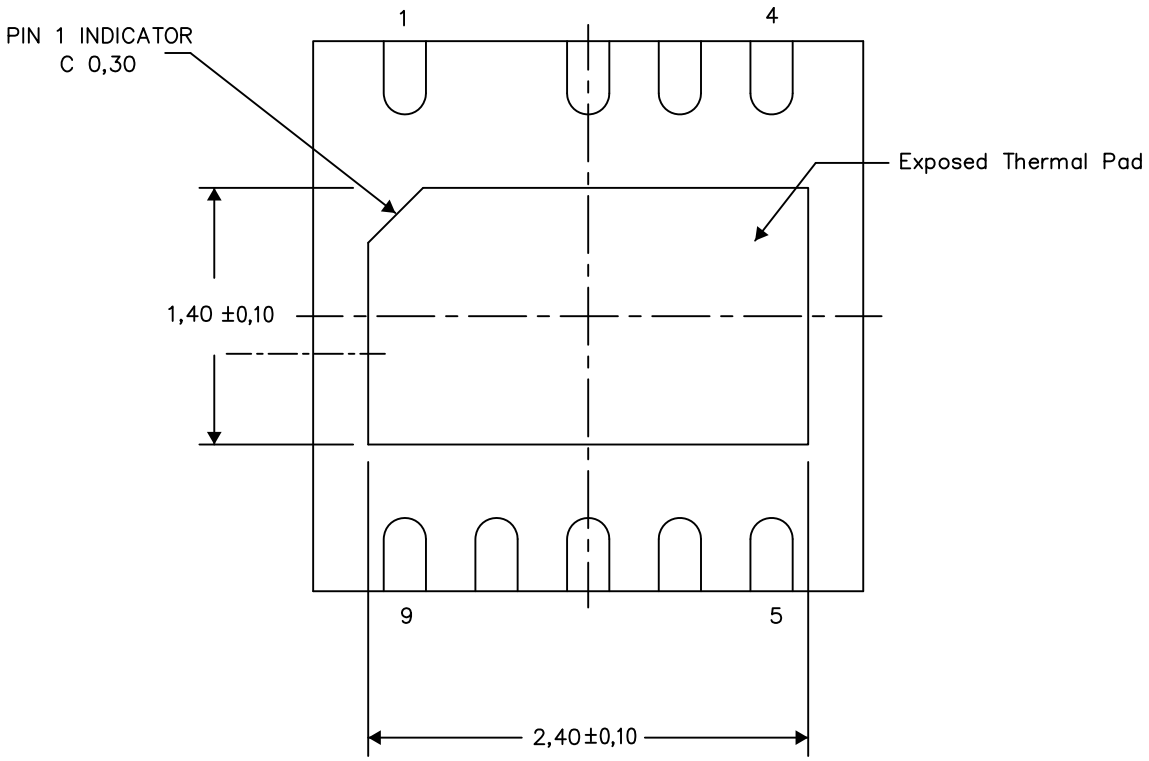
DRC (S–PVSON–N9) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



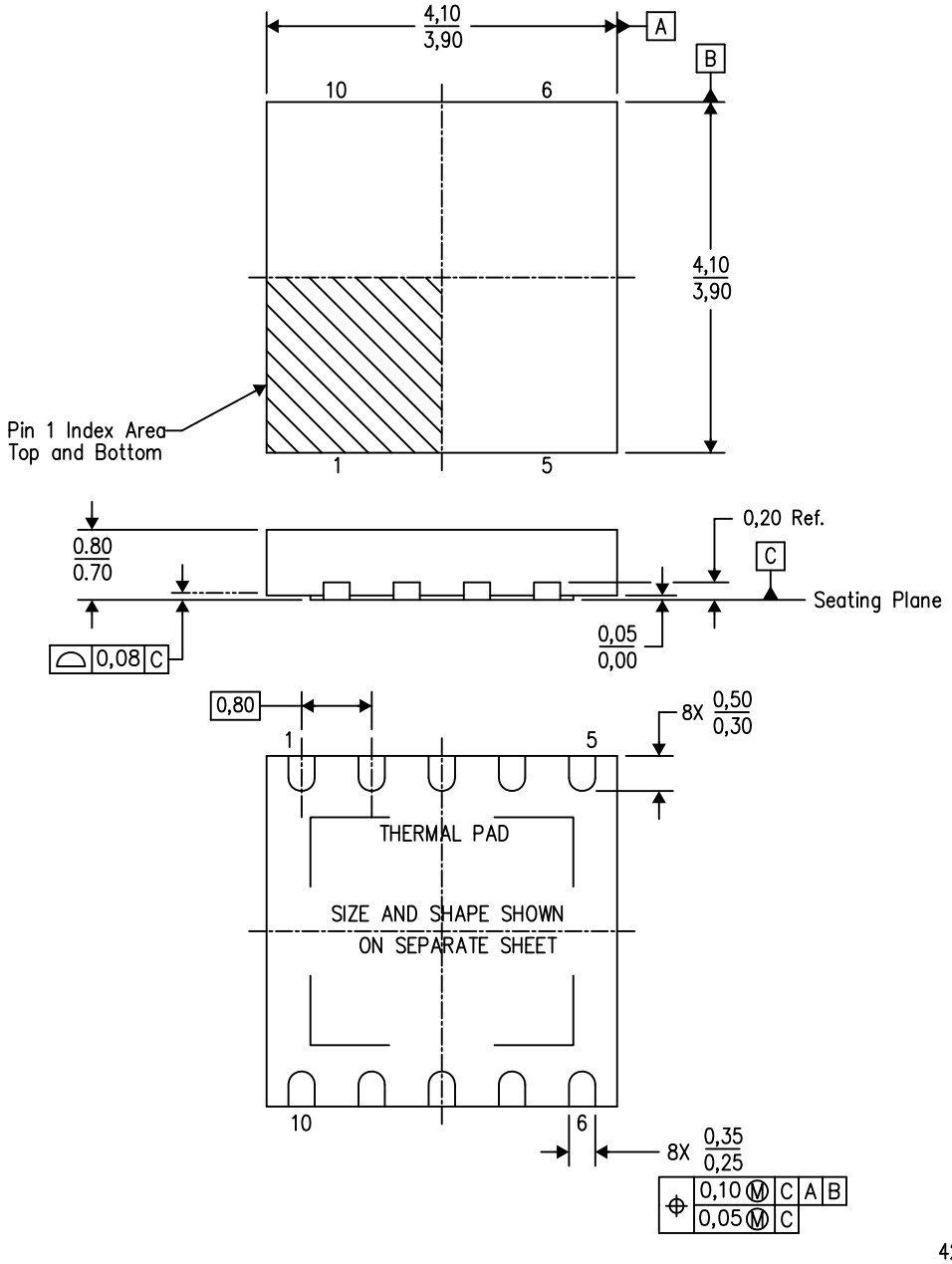
Bottom View

Exposed Thermal Pad Dimensions

4206565–2/Q 12/12

NOTE: A. All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. SON (Small Outline No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

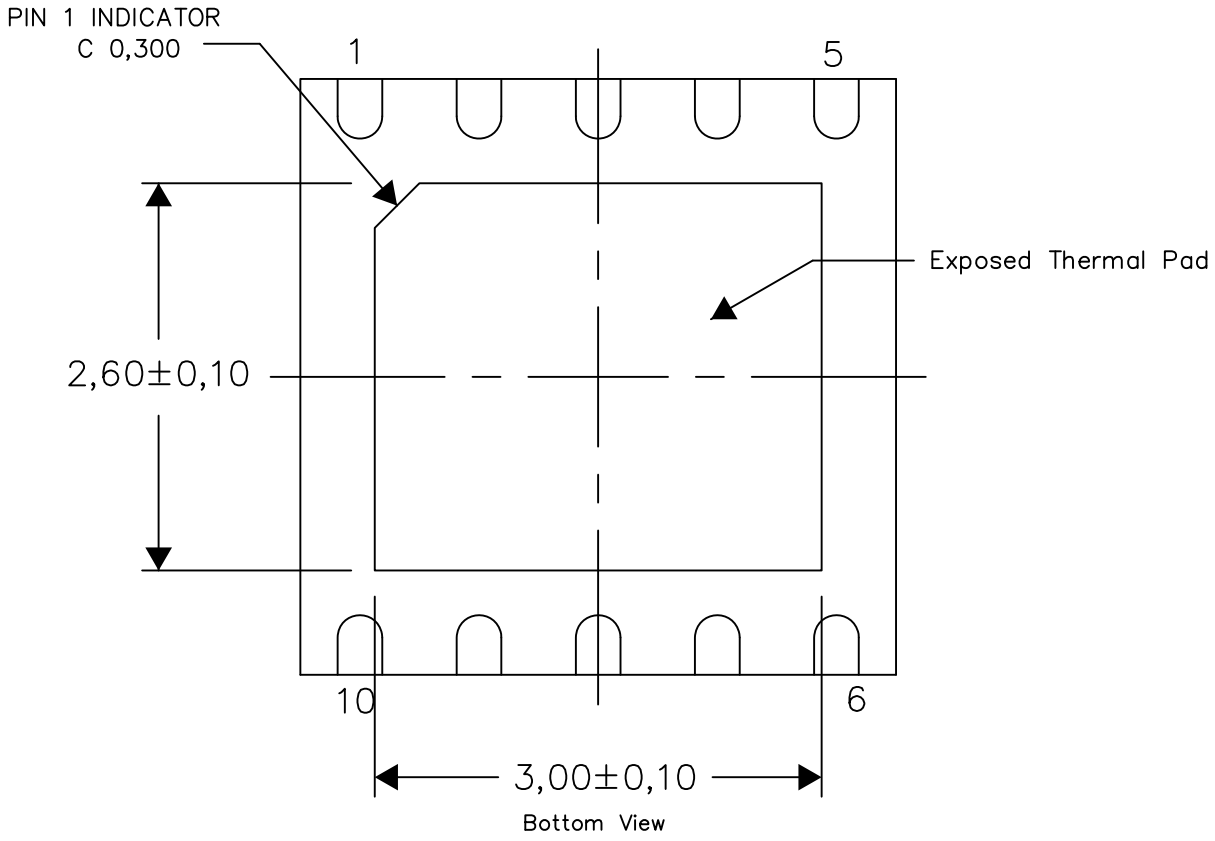
DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

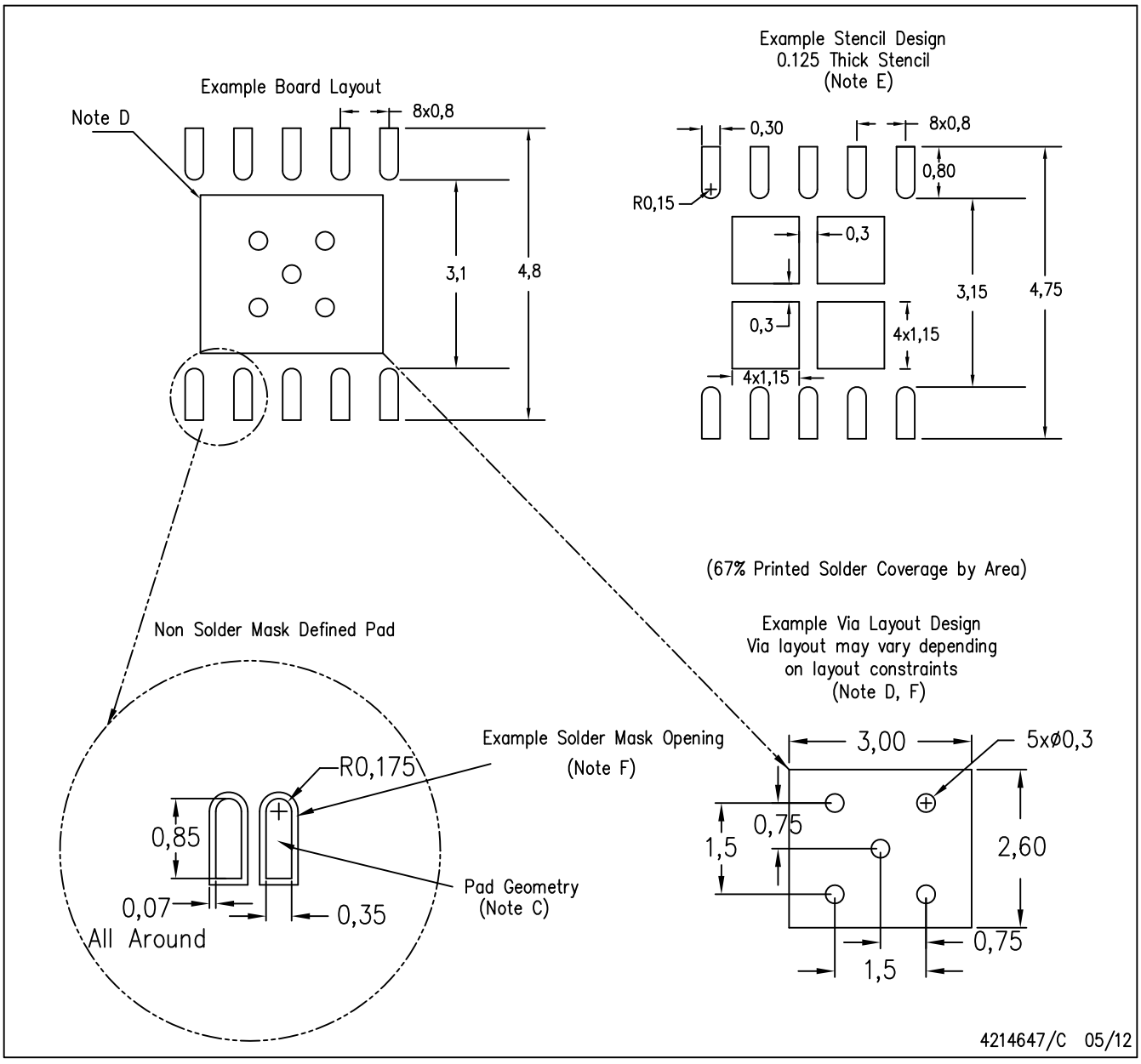


Exposed Thermal Pad Dimensions

4211551/B 04/12

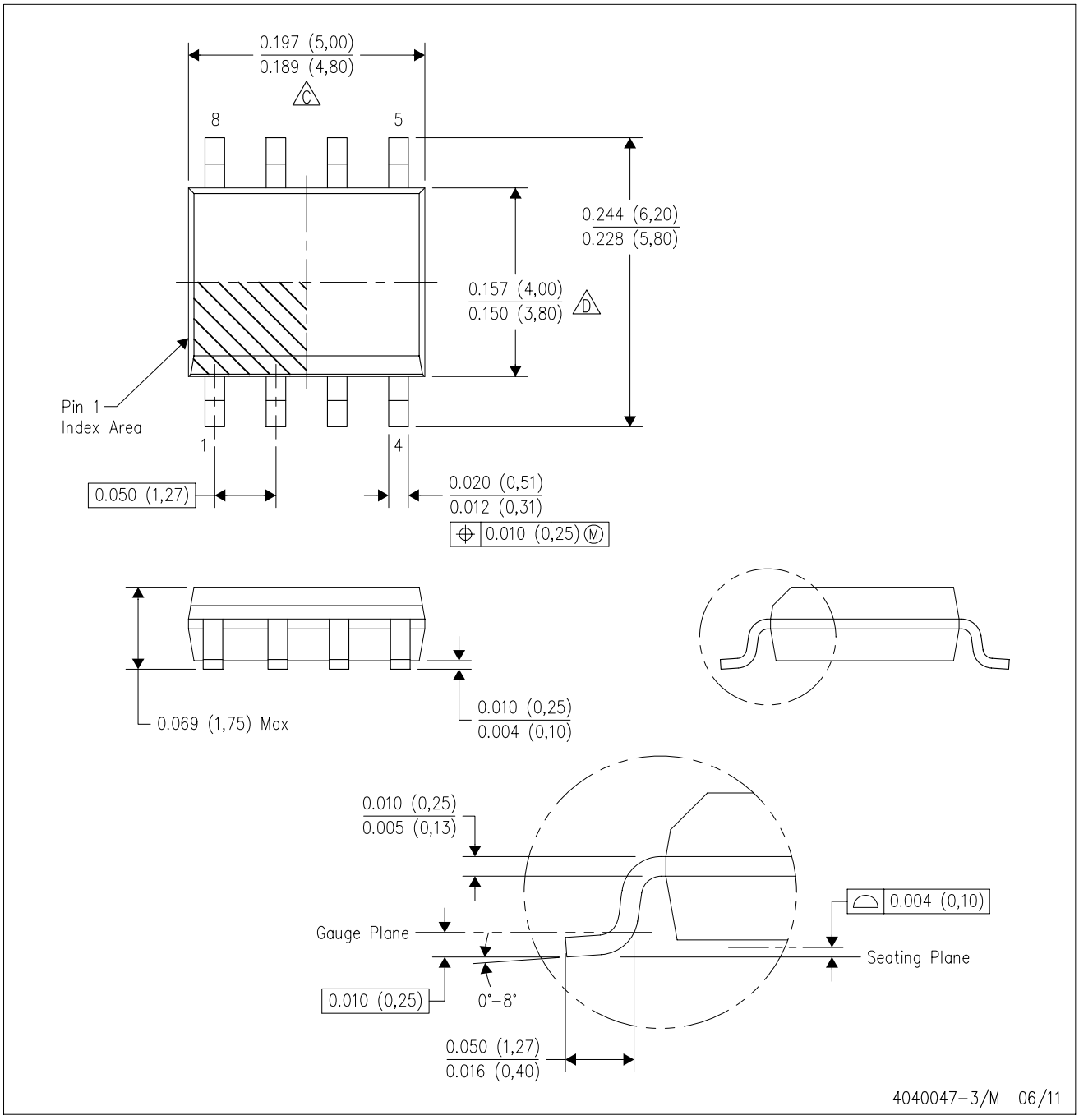
NOTES: All linear dimensions are in millimeters

DPR (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



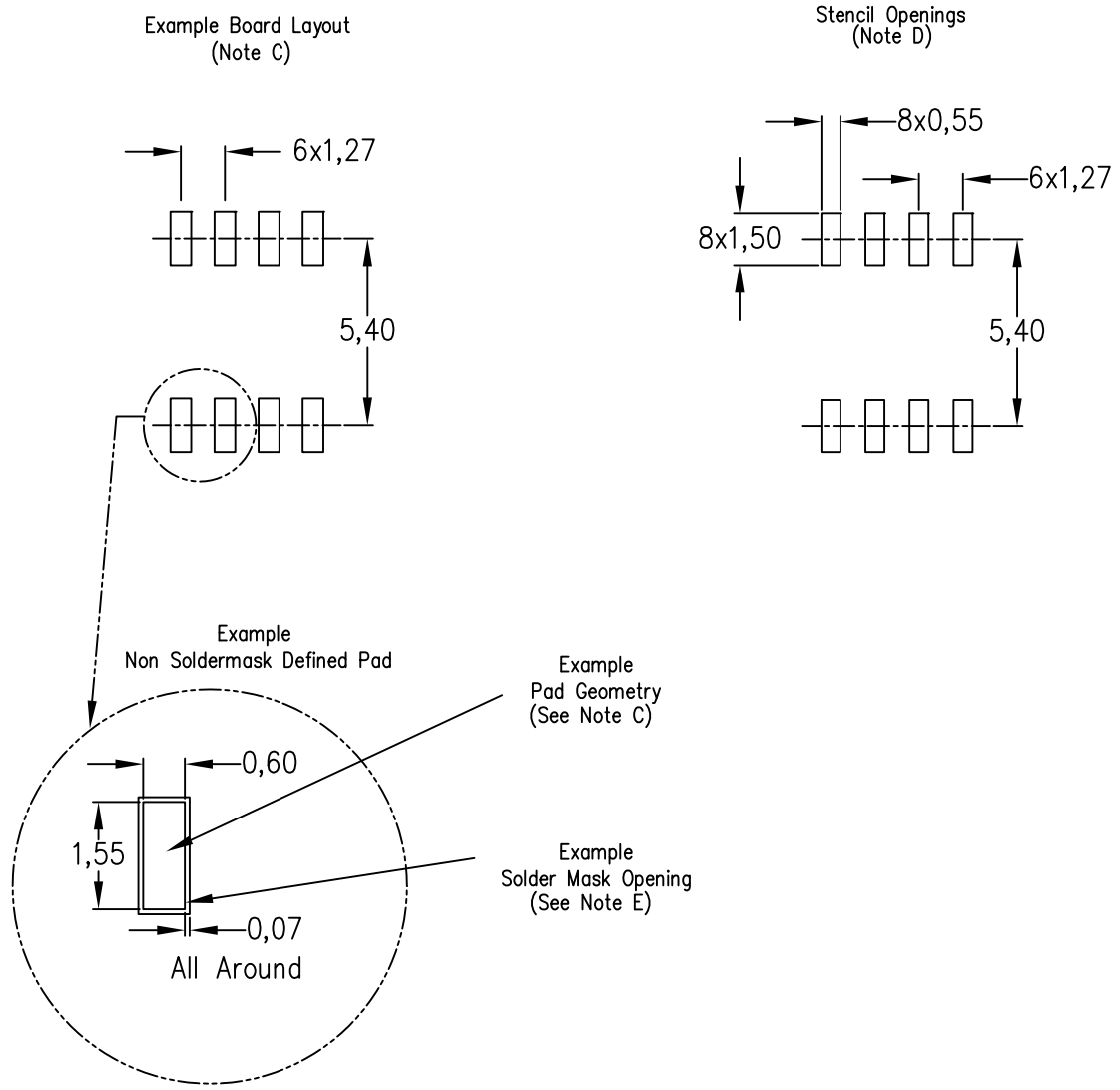
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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