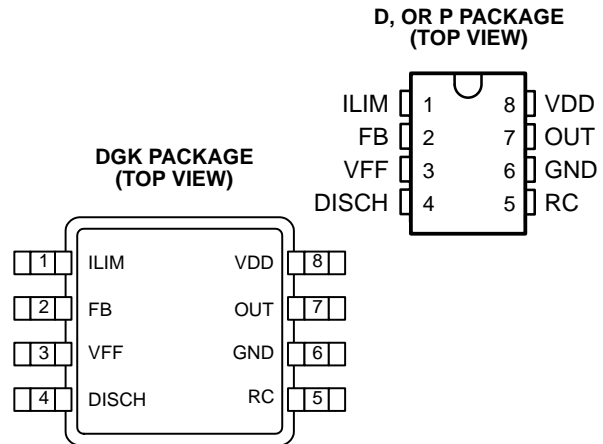


# UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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- Greater Than 4-MHz Operation
- Integrated Oscillator / Voltage Feed Forward Compensation
- >4:1 Input Voltage Range
- 25-ns Current Limit Delay
- Programmable Maximum Duty Cycle Clamp
- Optocoupler Interface
- 50- $\mu$ A Start-Up Current
- 4.2-mA Operating Current @ 1 MHz
- Smallest Footprint of the 8-pin MSOP Package Minimizes Board Area and Height



## description

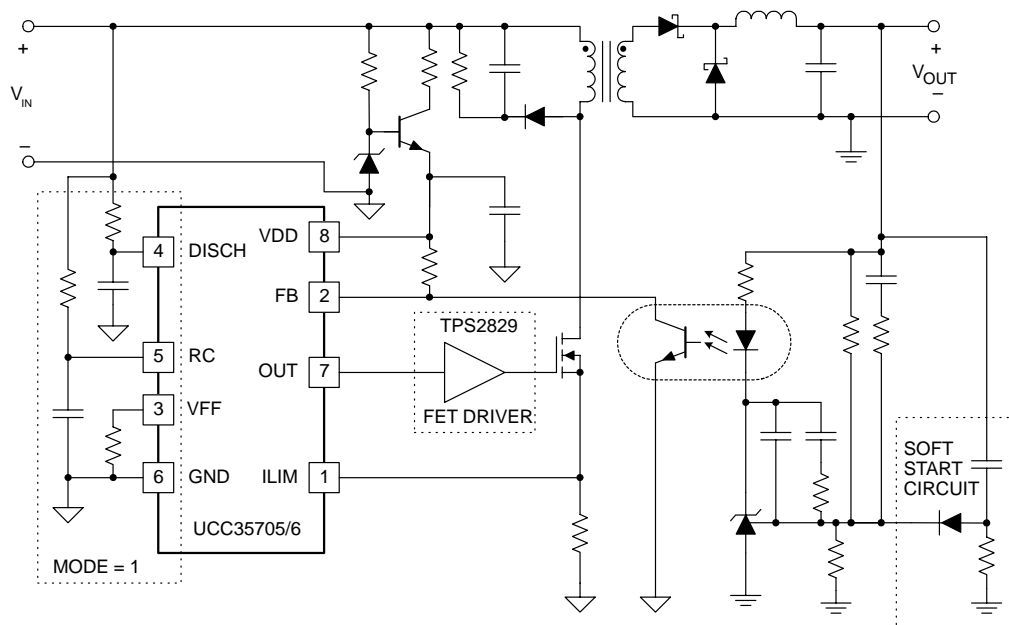
The UCC35705 and UCC35706 devices are 8-pin voltage mode primary side controllers with fast over-current protection. These devices are used as core high-speed building blocks in high performance isolated and non-isolated power converters.

UCC35705/UCC35706 devices feature a high speed oscillator with integrated feed-forward compensation for improved converter performance. A typical current sense to output delay time of 25 ns provides fast response to overload conditions. The IC also provides an accurate programmable maximum duty cycle clamp for increased protection which can also be disabled for the oscillator to run at maximum possible duty cycle.

Two UVLO options are offered. The UCC35705 with lower turn-on voltage is intended for dc-to-dc converters while the higher turn-on voltage and the wider UVLO range of the UCC35706 is better suited for offline applications.

The UCC35705/UCC35706 family is offered in 8-pin MSOP (DGK), SOIC (D) and PDIP (P) packages.

## typical application schematic



UDG-99181



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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# UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

|                                       |                |
|---------------------------------------|----------------|
| Supply voltage                        | 15 V           |
| Input voltage (VFF,RC,ILIM)           | 7 V            |
| Input voltage (FB)                    | 15 V           |
| Input current (DISCH)                 | 1 mA           |
| Output current (OUT) dc               | ±20 mA         |
| Storage temperature, T <sub>stg</sub> | –65°C to 150°C |
| Junction temperature, T <sub>J</sub>  | –55°C to 150°C |
| Lead temperature (soldering, 10 sec.) | 300°C          |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

‡ All voltages are with respect to GND. Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)* for thermal limitations and considerations of packages.

## AVAILABLE OPTIONS

| T <sub>A</sub> | Packaged Devices |                              |                           |                                   |
|----------------|------------------|------------------------------|---------------------------|-----------------------------------|
|                | UVLO Option      | SOIC-8<br>Small Outline (D)† | PDIP-8<br>Plastic Dip (P) | MSOP-8<br>Small Outline<br>(DGK)† |
| –40°C to 85°C  | 8.8V/8V          | UCC25705D                    | UCC25705P                 | UCC25705DGK                       |
|                | 12V/8V           | UCC25706D                    | UCC25706P                 | UCC25706DGK                       |
| 0°C to 70°C    | 8.8V/8V          | UCC35705D                    | UCC35705P                 | UCC35705DGK                       |
|                | 12V/8V           | UCC35706D                    | UCC35706P                 | UCC35706DGK                       |

† D (SOIC–8) and DGK (MSOP–8) packages are available taped and reeled. Add R suffix to device type (e.g. UCC35705DR) to order quantities of 2500 devices per reel for SOIC-8 and 2000 devices per reel for the MSOP-8.

electrical characteristics, V<sub>DD</sub> = 11 V, V<sub>IN</sub> = 30 V, R<sub>T</sub> = 47 k, R<sub>DISCH</sub> = 400 k, R<sub>FF</sub> = 14 k, C<sub>T</sub> = 220 pF, C<sub>VDD</sub> = 0.1 μF, and no load on the outputs, (unless otherwise specified)

### UVLO section (UCCx5705)

| PARAMETER       | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|-----------------|-----------------|-----|-----|-----|-------|
| Start threshold |                 | 8.0 | 8.8 | 9.6 | V     |
| Stop threshold  |                 | 7.4 | 8.2 | 9.0 | V     |
| Hysteresis      |                 | 0.3 | 0.6 | 1.0 | V     |

### UVLO section (UCCx5706)

| PARAMETER       | TEST CONDITIONS | MIN  | TYP  | MAX  | UNITS |
|-----------------|-----------------|------|------|------|-------|
| Start threshold |                 | 11.2 | 12.0 | 12.8 | V     |
| Stop threshold  |                 | 7.2  | 8.0  | 8.8  | V     |
| Hysteresis      |                 | 3.5  | 4.0  | 4.5  | V     |

### supply current section

| PARAMETER              | TEST CONDITIONS  | MIN | TYP | MAX | UNITS |
|------------------------|--|-----|-----|-----|-------|
| Start-up current       | V <sub>DD</sub> = UVLO start – 1 V, V <sub>DD</sub> comparator off |     | 30  | 90  | μA    |
| I <sub>DD</sub> active | V <sub>DD</sub> comparator on, oscillator running at 1 MHz         |     | 4.2 | 5.0 | mA    |



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electrical characteristics,  $V_{DD} = 11\text{ V}$ ,  $V_{IN} = 30\text{ V}$ ,  $R_T = 47\text{ k}$ ,  $R_{DISCH} = 400\text{ k}$ ,  $R_{FF} = 14\text{ k}$ ,  $C_T = 220\text{ pF}$ ,  $C_{VDD} = 0.1\text{ }\mu\text{F}$ , and no load on the outputs, (unless otherwise specified)

## line sense section

| PARAMETER                     | TEST CONDITIONS | MIN  | TYP  | MAX  | UNITS |
|-------------------------------|-----------------|------|------|------|-------|
| Low line comparator threshold |                 | 0.95 | 1.00 | 1.05 | V     |
| Input bias current (VFF)      |                 | -100 |      | 100  | nA    |

## oscillator section

| PARAMETER         | TEST CONDITIONS         | MIN | TYP | MAX | UNITS |
|-------------------|-------------------------|-----|-----|-----|-------|
| Frequency         | VFF = 1.2 V to 4.8 V    | 0.9 | 1.0 | 1.1 | MHz   |
| CT peak voltage   | VFF = 1.2 V, See Note 1 |     | 1.2 |     | V     |
|                   | VFF = 4.8 V, See Note 1 |     | 4.8 |     | V     |
| CT valley voltage | See Note 1              |     | 0   |     | V     |

NOTE 1: Ensured by design. Not production tested.

## current limit section

| PARAMETER                      | TEST CONDITIONS | MIN | TYP  | MAX | UNITS         |
|--------------------------------|-----------------|-----|------|-----|---------------|
| Input bias current             |                 | 0.2 | -0.2 | -1  | $\mu\text{A}$ |
| Current limit threshold        |                 | 180 | 200  | 220 | mV            |
| Propagation delay, ILIM to OUT | 50 mV overdrive |     | 25   | 35  | ns            |

## pulse width modulator section

| PARAMETER                     | TEST CONDITIONS                                     | MIN | TYP | MAX | UNITS            |
|-------------------------------|---|-----|-----|-----|------------------|
| FB input impedance            | $V_{FB} = 3\text{ V}$                               | 30  | 50  | 90  | $\text{k}\Omega$ |
| Minimum duty cycle            | $V_{FB} < 2\text{ V}$                               |     |     | 0   | %                |
| Maximum duty cycle            | $V_{FB} = V_{DD}$ , $F_{OSC} = 1\text{ MHz}$        | 70  | 75  | 80  | %                |
|                               | $V_{DISCH} = 0\text{ V}$ , $F_{OSC} = 1\text{ MHz}$ |     | 93  |     | %                |
| PWM gain                      | $V_{FF} = 2.5\text{ V}$ , $MODE = 1$                |     | 12  |     | %/V              |
| Propagation delay, PWM to OUT |   |     | 65  | 120 | ns               |

## output section

| PARAMETER | TEST CONDITIONS                              | MIN | TYP  | MAX | UNITS |
|-----------|--|-----|------|-----|-------|
| VOH       | $I_{OUT} = -5\text{ mA}$ , $V_{DD}$ – output |     | 0.3  | 0.6 | V     |
| VOL       | $I_{OUT} = 5\text{ mA}$                      |     | 0.15 | 0.4 | V     |
| Rise time | $C_{LOAD} = 50\text{ pF}$                    |     | 10   | 25  | ns    |
| Fall time | $C_{LOAD} = 50\text{ pF}$                    |     | 10   | 25  | ns    |



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## pin descriptions

**DISCH:** A resistor to VIN sets the oscillator discharge current programming a maximum duty cycle. When grounded, an internal comparator switches the oscillator to a quick discharge mode. A small 100-pF capacitor between DISCH and GND may reduce oscillator jitter without impacting feed-forward performance.  $I_{DISCH}$  must be between 25  $\mu$ A and 250  $\mu$ A over the entire  $V_{IN}$  range.

**FB:** Input to the PWM comparator. This pin is intended to interface with an optocoupler. Input impedance is 50-k $\Omega$  typical.

**GND:** Ground return pin.

**ILIM:** Provides a pulse-by-pulse current limit by terminating the PWM pulse when the input is above 200 mV. This provides a high speed (25 ns typical) path to reset the PWM latch, allowing for a pulse-by-pulse current limit.

**OUT:** The output is intended to drive an external FET driver or other high impedance circuits, but is not intended to directly drive a power MOSFET. This improves the controller's noise immunity. The output resistance of the PWM controller, typically 60  $\Omega$  pull-up and 30  $\Omega$  pull-down, will result in excessive rise and fall times if a power MOSFET is directly driven at the speeds for which the UCC35705/6 is optimized.

**RC:** The oscillator can be configured to provide a maximum duty cycle clamp. In this mode the on-time is set by RT and CT, while the off-time is set by RDISCH and CT. Since the voltage ramp on CT is proportional to VIN, feed-forward action is obtained. Since the peak oscillator voltage is also proportional to VIN, constant frequency operation is maintained over the full power supply input range. When the DISCH pin is grounded, the duty cycle clamp is disabled. The RC pin then provides a low impedance path to ground CT during the off time.

**VDD:** Power supply pin. This pin should be bypassed with a 0.1- $\mu$ F capacitor for proper operation. The undervoltage lockout function of the UCC35705/6 allows for a low current startup mode and ensures that all circuits become active in a known state. The UVLO thresholds on the UCC35705 are appropriate for a dc-to-dc converter application. The wider UVLO hysteresis of the UCC35706 (typically 4 V) is optimized for a bootstrap startup mode from a high impedance source.

**VFF:** The feed-forward pin provides the controller with a voltage proportional to the power supply input voltage. When the oscillator is providing a duty cycle clamp, a current of  $2 \times I_{DISCH}$  is sourced from the VFF pin. A single resistor RFF between VFF and GND then set VFF to:

$$VFF \approx VIN \times \left( \frac{2 \times R_{FF}}{2 \times R_{FF} + R_{DISCH}} \right)$$

When the DISCH pin is grounded and the duty cycle clamp is not used, the internal current source is disabled and a resistor divider from VIN is used to set VFF. In either case, when the voltage on VFF is less than 1.0 V, both the output and oscillator are disabled.

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## pin descriptions (continued)

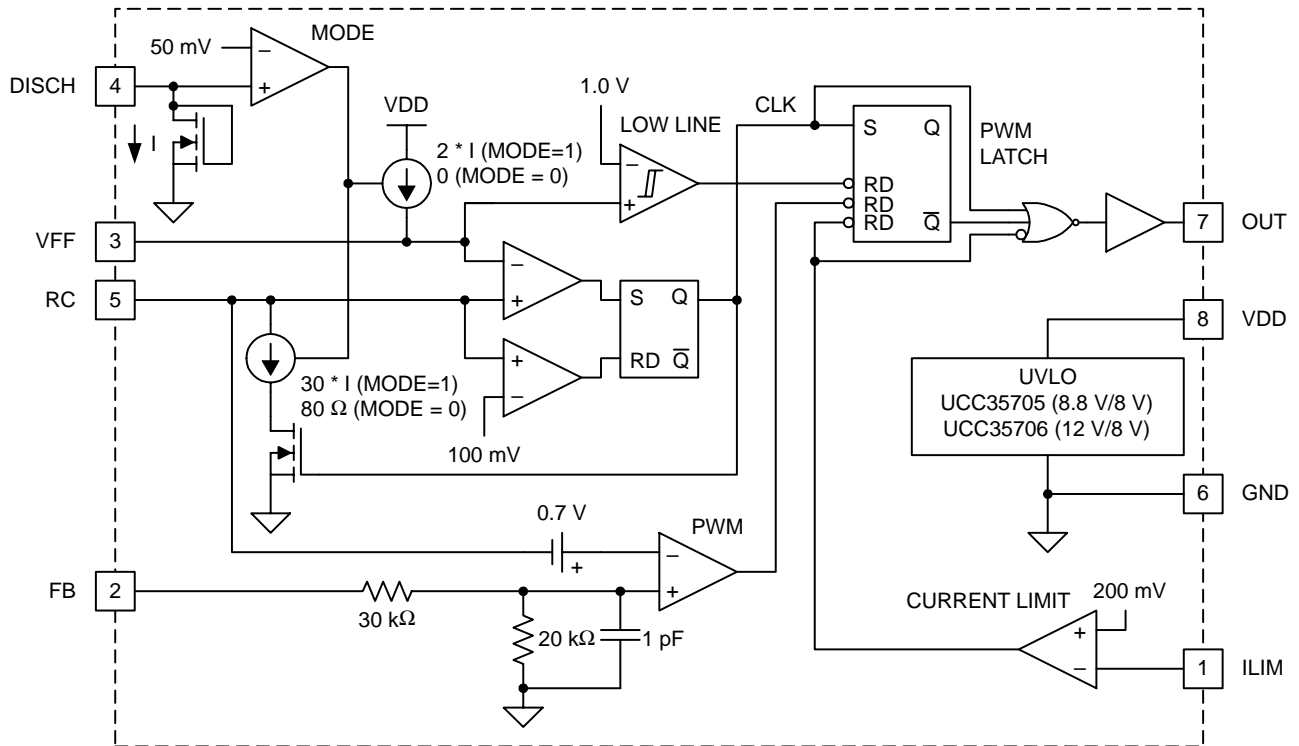


Figure 1. Block Diagram

## FUNCTIONAL DESCRIPTION

### oscillator and PWM

The oscillator can be programmed to provide a duty cycle clamp or be configured to run at the maximum possible duty cycle.

The PWM latch is set during the oscillator discharge and is reset by the PWM comparator when the  $C_T$  waveform is greater than the feedback voltage. The voltage at the FB pin is attenuated before it is applied to the PWM comparator. The oscillator ramp is shifted by approximately 0.65-V at room temperature at the PWM comparator. The offset has a temperature coefficient of approximately  $-2 \text{ mV}/^\circ\text{C}$ .

The ILIM comparator adds a pulse by pulse current limit by resetting the PWM latch when  $V_{ILIM} > 200 \text{ mV}$ . The PWM latch is also reset by a low line condition ( $V_{FF} < 1.0 \text{ V}$ ).

All reset conditions are dominant; asserting any output will force a zero duty cycle output.

### oscillator with duty cycle clamp (MODE = 1)

The timing capacitor  $C_T$  is charged from ground to VFF through  $R_T$ . The discharge path is through an on-chip current sink that has a value of  $30 \times I_{DISCH}$ , where  $I_{DISCH}$  is the current through the external resistor  $R_{DISCH}$ . Since the charge and discharge currents are both proportional to  $V_{IN}$ , their ratio, and the maximum duty cycle remains constant as  $V_{IN}$  varies.



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## FUNCTIONAL DESCRIPTION

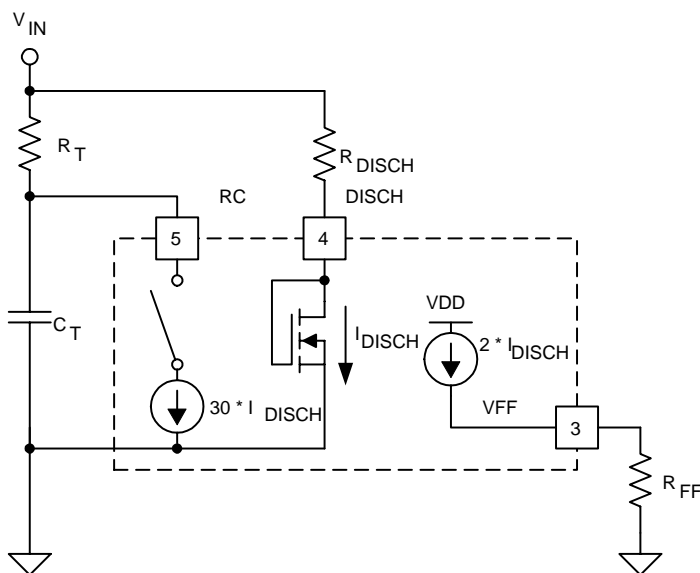


Figure 2. Duty Cycle Clamp (MODE = 1)

The on-time is approximately:

$$T_{ON} = \alpha \times R_T \times C_T \quad \text{where } \alpha = \frac{V_{FF}}{V_{IN}} \approx \frac{2 \times R_{FF}}{R_{DISCH}}$$

The off-time is:

$$T_{OFF} = \alpha \times \frac{C_T \times (R_T \times R_{DISCH})}{30 \times (R_T - R_{DISCH})}$$

The frequency is:

$$f = \left( \frac{1}{\alpha \times R_T \times C_T} \right) \times \frac{1}{1 + \frac{R_{DISCH}}{30 \times (R_T - R_{DISCH})}}$$

The maximum duty cycle is:

$$\text{Duty Cycle} = \frac{T_{ON}}{T_{ON} + T_{OFF}} = \left( 1 - \frac{R_{DISCH}}{30 \times R_T} \right)$$

**FUNCTIONAL DESCRIPTION**

**component selection for oscillator with duty cycle clamp (MODE = 1)**

For a power converter with the following specifications:

- $V_{IN(min)} = 18 \text{ V}$
- $V_{IN(max)} = 75 \text{ V}$
- $V_{IN(shutdown)} = 15 \text{ V}$
- $F_{OSC} = 1 \text{ MHz}$
- $D_{MAX} = 0.78$  at  $V_{IN(min)}$

In this mode, the on-time is approximately:

- $T_{ON(max)} = 780 \text{ ns}$
- $T_{OFF(min)} = 220 \text{ ns}$
- $V_{FF(min)} = \frac{18}{15} = 1.20 \text{ V}$

(1) Pick  $C_T = 220 \text{ pF}$ .

(2) Calculate  $R_T$ .

$$R_T = \frac{V_{IN(min)} \times T_{ON(max)}}{V_{FF(min)} \times C_T}$$

$$R_T = 51.1 \text{ k}\Omega$$

(3)  $R_{DISCH}$

$$R_{DISCH} = \frac{30 \times R_T}{1 + \left[ \frac{\left( \frac{V_{FF(min)}}{V_{IN(min)}} \right) \times R_T \times C_T}{T_{OFF(min)}} \right]}$$

$$R_{DISCH} = 383 \text{ k}\Omega.$$

$I_{DISCH}$  must be between  $25 \mu\text{A}$  and  $250 \mu\text{A}$  over the entire  $V_{IN}$  range.

With the calculated values,  $I_{DISCH}$  ranges from  $44 \mu\text{A}$  to  $193 \mu\text{A}$ , within the allowable range. If  $I_{DISCH}$  is too high,  $C_T$  must be decreased.

(4)  $R_{FF}$

$$R_{FF} = \frac{V_{FF(min)} \times R_{DISCH}}{2 \times (V_{IN(min)} - 1)}$$

The nearest 1% standard value to the calculated value is 13.7 k.

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## FUNCTIONAL DESCRIPTION

### oscillator without duty cycle clamp (MODE = 0)

In this mode, the timing capacitor is discharged through a low impedance directly to ground. The DISCH pin is externally grounded. A comparator connected to DISCH senses the ground connection and disables both the discharge current source and VFF current source. A resistor divider is now required to set VFF.

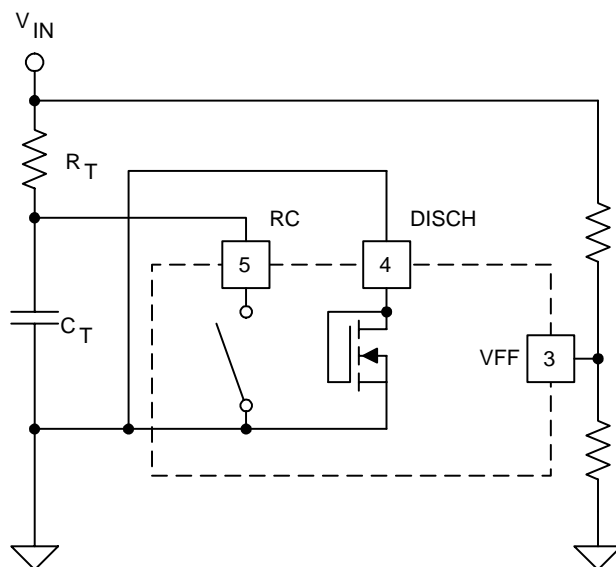


Figure 3. Oscillator Without Clamp (MODE = 0)

In this mode, the on-time is approximately:

$$T_{ON} = \alpha \times R_T \times C_T \quad \text{where } \alpha = \frac{V_{FF}}{V_{IN}}$$

The off-time is:

$$T_{OFF} \approx 75 \text{ ns}$$

The frequency is:

$$f = \frac{1}{\alpha \times R_T \times C_T + 75 \text{ ns}}$$



# UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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## FUNCTIONAL DESCRIPTION

### component selection for oscillator without duty cycle clamp (MODE = 0)

For a power converter with the following specifications:

- $V_{IN(min)} = 18\text{ V}$
- $V_{IN(max)} = 75\text{ V}$
- $V_{IN(shutdown)} = 15\text{ V}$
- $F_{OSC} = 1\text{ MHz}$

With these specifications,

$$V_{FF(min)} = \frac{18}{15} = 1.2\text{ V}$$

(1) Pick  $C_T = 220\text{ pF}$

(2) Calculate  $R_T$ .

$$R_T = \frac{\frac{V_{IN(min)}}{V_{FF(min)}} \times \left( \frac{1}{F_{OSC}} - 75\text{ ns} \right)}{C_T}$$

## TYPICAL CHARACTERISTICS

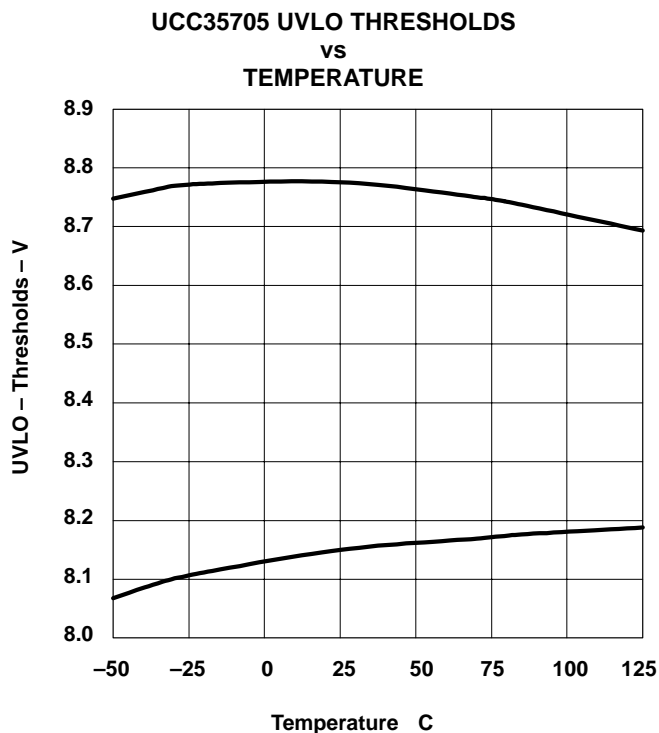


Figure 4

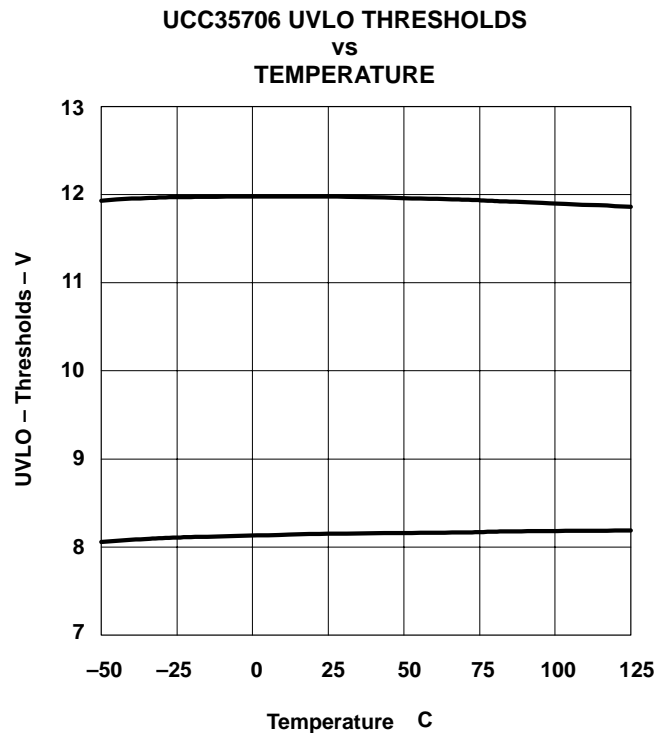


Figure 5



# UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

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## TYPICAL CHARACTERISTICS

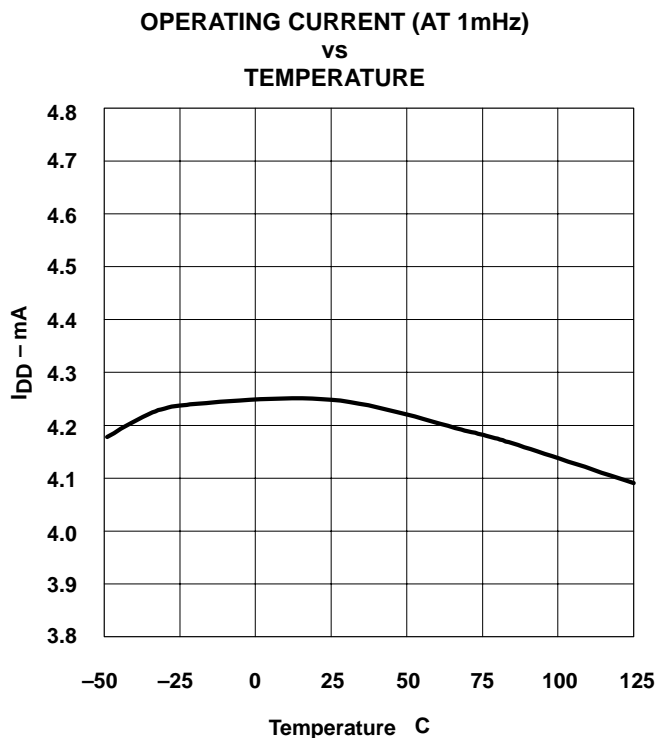


Figure 6

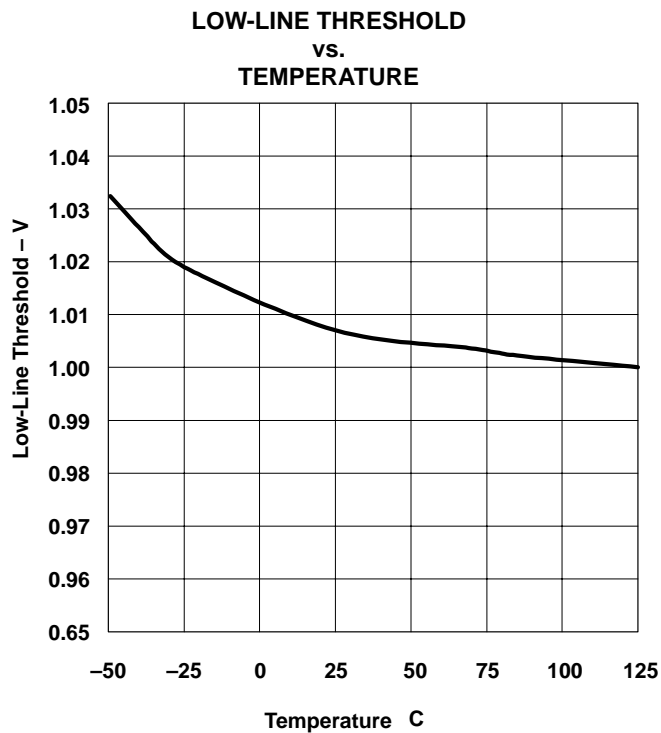


Figure 7

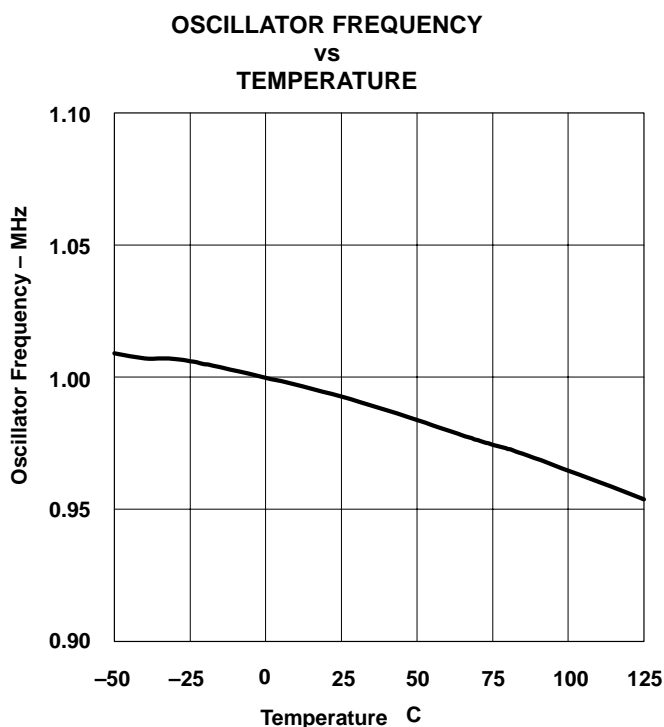


Figure 8

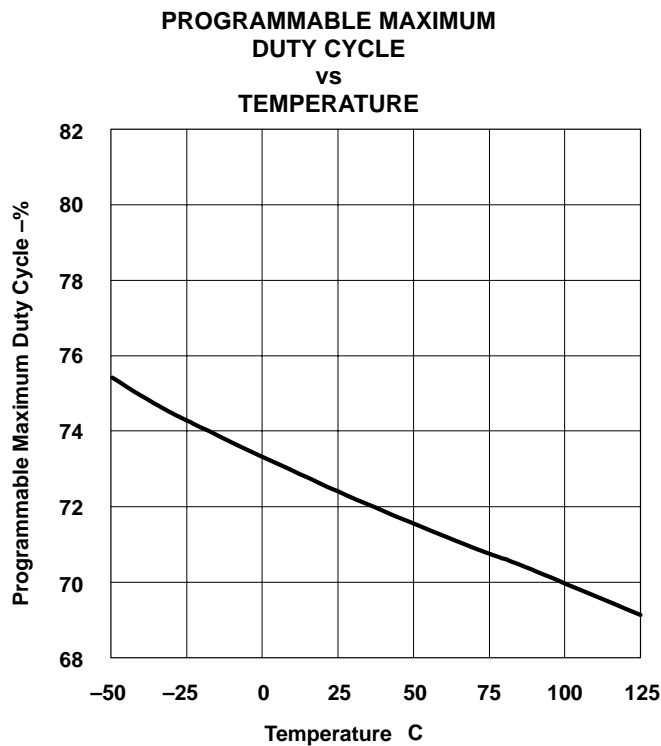


Figure 9



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## TYPICAL CHARACTERISTICS

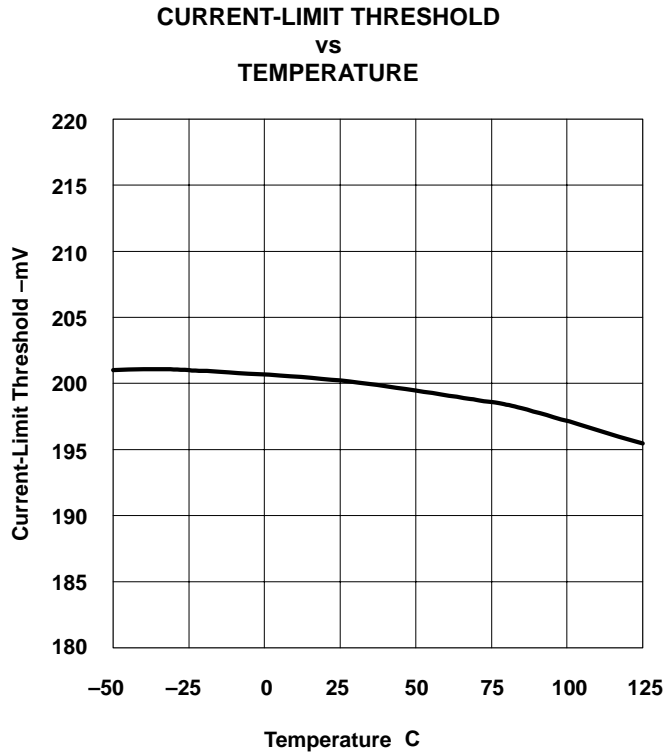


Figure 10

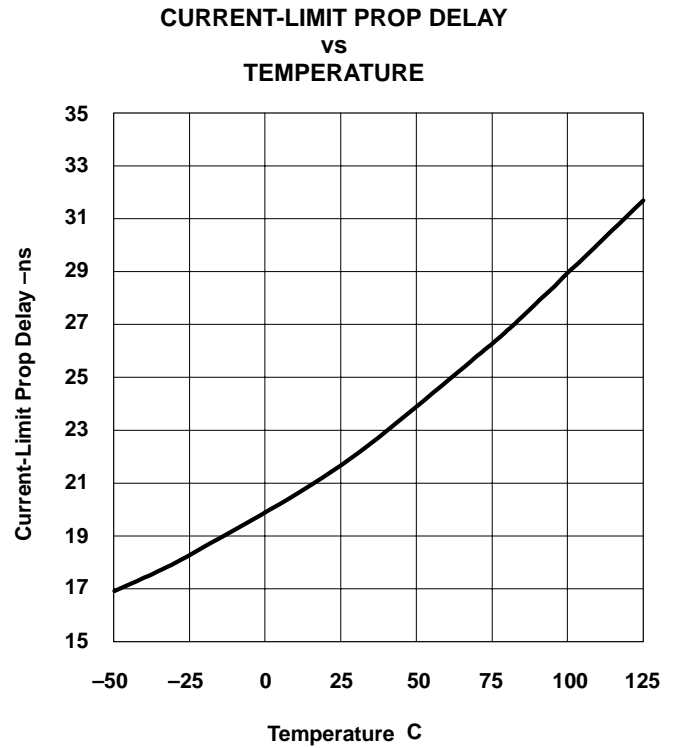


Figure 11

# UCC25705, UCC25706, UCC35705, UCC35706 HIGH-SPEED VOLTAGE MODE PULSE WIDTH MODULATOR

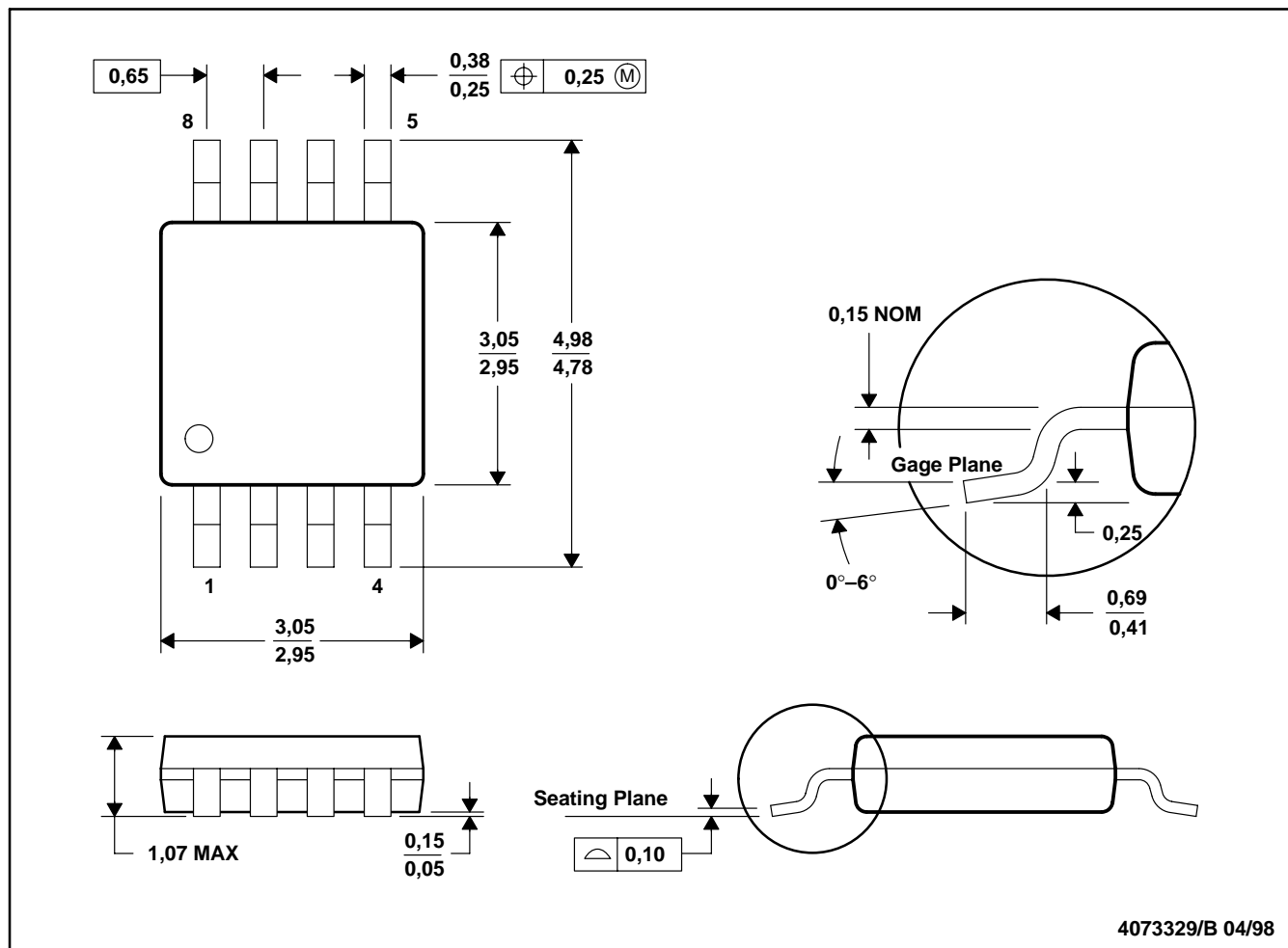
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## MECHANICAL DATA

Detailed package drawing for MSOP-8 (DGK) is shown below. For SOIC-8 (D) and PDIP-8 (P) package drawings, consult Packaging Section of the *Power Supply Control Data Book (TI Literature Number SLUD003)*.

### DGK (MSOP-8)

### MINI SMALL OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion.
  - D. Falls within JEDEC MO-187

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