

TUSB1210

Standalone USB Transceiver Chip Silicon

Data Manual



PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Literature Number: SLLSE09F
November 2009–Revised August 2012

Contents

| | | |
|----------|--|-----------|
| 1 | Features | 6 |
| 2 | Description | 7 |
| 2.1 | Terminal Description | 7 |
| 2.2 | TUSB1210 Block Diagram | 9 |
| 3 | Electrical Characteristics | 10 |
| 3.1 | Absolute Maximum Ratings | 10 |
| 3.2 | Recommended Operating Conditions | 10 |
| 3.3 | ESD Electrical Parameters | 10 |
| 4 | Clock System | 11 |
| 4.1 | USB PLL Reference Clock | 11 |
| 4.2 | ULPI Input Clock Configuration | 11 |
| 4.3 | ULPI Output Clock Configuration | 11 |
| 4.4 | Clock 32 kHz | 12 |
| 4.5 | Reset | 12 |
| 5 | Power Module | 13 |
| 5.1 | Power Providers | 13 |
| 5.1.1 | V _{DD33} Regulator | 13 |
| 5.1.2 | V _{DD18} Supply | 13 |
| 5.1.3 | V _{DD15} Regulator | 13 |
| 5.2 | Power Consumption | 14 |
| 5.3 | Power Management | 15 |
| 5.3.1 | Power On Sequence | 15 |
| 5.3.1.1 | Timing Diagram | 15 |
| 5.3.2 | Timers and Debounce | 16 |
| 6 | USB Connectivity | 17 |
| 6.1 | Timing Parameter Definitions | 17 |
| 6.2 | Interface Target Frequencies | 17 |
| 6.3 | USB Transceiver | 17 |
| 6.3.1 | TUSB1210 Modes vs ULPI Pin Status | 18 |
| 6.3.2 | ULPI Interface Timing | 19 |
| 6.3.3 | PHY Electrical Characteristics | 19 |
| 6.3.3.1 | LS/FS Single-Ended Receivers | 20 |
| 6.3.3.2 | LS/FS Differential Receiver | 20 |
| 6.3.3.3 | LS/FS Transmitter | 20 |
| 6.3.3.4 | HS Differential Receiver | 22 |
| 6.3.3.5 | HS Differential Transmitter | 22 |
| 6.3.3.6 | UART Transceiver | 23 |
| 6.3.4 | OTG Electrical Characteristics | 24 |
| 7 | I/O Electrical Characteristics | 26 |
| 7.1 | Analog I/O Electrical Characteristics | 26 |
| 7.2 | Digital I/O Electrical Characteristics | 26 |
| 7.3 | Electrical Characteristics: Digital IO Pins (Non-ULPI) | 26 |
| 8 | External Components | 27 |
| 9 | Register Map | 28 |
| 9.1 | TUSB1210 Product | 28 |
| 9.1.1 | VENDOR_ID_LO | 29 |
| 9.1.2 | VENDOR_ID_HI | 29 |
| 9.1.3 | PRODUCT_ID_LO | 29 |
| 9.1.4 | PRODUCT_ID_HI | 30 |
| 9.1.5 | FUNC_CTRL | 30 |
| 9.1.6 | FUNC_CTRL_SET | 31 |

| | | |
|-----------|--|---------------------------|
| 9.1.7 | FUNC_CTRL_CLR | 31 |
| 9.1.8 | IFC_CTRL | 32 |
| 9.1.9 | IFC_CTRL_SET | 33 |
| 9.1.10 | IFC_CTRL_CLR | 34 |
| 9.1.11 | OTG_CTRL | 34 |
| 9.1.12 | OTG_CTRL_SET | 36 |
| 9.1.13 | OTG_CTRL_CLR | 36 |
| 9.1.14 | USB_INT_EN_RISE | 37 |
| 9.1.15 | USB_INT_EN_RISE_SET | 38 |
| 9.1.16 | USB_INT_EN_RISE_CLR | 38 |
| 9.1.17 | USB_INT_EN_FALL | 39 |
| 9.1.18 | USB_INT_EN_FALL_SET | 40 |
| 9.1.19 | USB_INT_EN_FALL_CLR | 40 |
| 9.1.20 | USB_INT_STS | 41 |
| 9.1.21 | USB_INT_LATCH | 42 |
| 9.1.22 | DEBUG | 43 |
| 9.1.23 | SCRATCH_REG | 43 |
| 9.1.24 | SCRATCH_REG_SET | 44 |
| 9.1.25 | SCRATCH_REG_CLR | 44 |
| 9.1.26 | VENDOR_SPECIFIC1 | 45 |
| 9.1.27 | VENDOR_SPECIFIC1_SET | 45 |
| 9.1.28 | VENDOR_SPECIFIC1_CLR | 46 |
| 9.1.29 | VENDOR_SPECIFIC2 | 47 |
| 9.1.30 | VENDOR_SPECIFIC2_SET | 48 |
| 9.1.31 | VENDOR_SPECIFIC2_CLR | 48 |
| 9.1.32 | VENDOR_SPECIFIC1_STS | 49 |
| 9.1.33 | VENDOR_SPECIFIC1_LATCH | 49 |
| 9.1.34 | VENDOR_SPECIFIC3 | 50 |
| 9.1.35 | VENDOR_SPECIFIC3_SET | 51 |
| 9.1.36 | VENDOR_SPECIFIC3_CLR | 51 |
| 10 | Application Information | 53 |
| 10.1 | Host or OTG, ULPI Input Clock Mode Application | 53 |
| 10.2 | Device, ULPI Output Clock Mode Application | 53 |
| 11 | Glossary | 55 |
| 12 | TUSB1210 Package | 57 |
| 12.1 | TUSB1210 Standard Package Symbolization | 57 |
| 12.2 | Package Thermal Resistance Characteristics | 57 |

List of Figures

| | | |
|------|--|--------------------|
| 5-1 | TUSB1210 Power-Up Timing (ULPI Clock Input Mode) | 15 |
| 6-1 | USB UART Data Flow | 23 |
| 10-1 | Host or OTG, ULPI Input Clock Mode Application Diagram | 53 |
| 10-2 | Device, ULPI Output Clock Mode Application Diagram | 54 |
| 12-1 | Printed Device Reference | 57 |

List of Tables

| | | |
|------|---|--------------------|
| 2-1 | Terminal Functions | 8 |
| 4-1 | Electrical Characteristics: Clock Input | 11 |
| 4-2 | Electrical Characteristics: REFCLK | 11 |
| 4-3 | Performances | 12 |
| 5-1 | Summary of TUSB1210 Power Providers..... | 13 |
| 5-2 | V _{DD33} Internal LDO Regulator Characteristics | 13 |
| 5-3 | V _{DD15} Internal LDO Regulator Characteristics | 14 |
| 5-4 | Power Consumption | 14 |
| 6-1 | Timing Parameter Definitions | 17 |
| 6-2 | TUSB1210 Interface Target Frequencies | 17 |
| 6-3 | TUSB1210 Modes vs ULPI Pin Status:ULPI Synchronous Mode Power-Up | 18 |
| 6-4 | TUSB1210 Modes vs ULPI Pin Status: USB Suspend Mode | 18 |
| 6-5 | TUSB1210 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode | 19 |
| 6-6 | ULPI Interface Timing..... | 19 |
| 6-7 | LS/FS Single-Ended Receivers | 20 |
| 6-8 | LS/FS Differential Receiver | 20 |
| 6-9 | LS Transmitter | 20 |
| 6-10 | FS Transmitter | 22 |
| 6-11 | HS Differential Receiver | 22 |
| 6-12 | HS Transmitter..... | 23 |
| 6-13 | USB UART Interface Timing Parameters | 23 |
| 6-14 | CEA-2011/UART Transceiver | 23 |
| 6-15 | Pullup/Pulldown Resistors..... | 24 |
| 6-16 | OTG V _{BUS} Electrical | 24 |
| 6-17 | OTG ID Electrical..... | 25 |
| 7-1 | Electrical Characteristics: Analog Output Pins | 26 |
| 8-1 | TUSB1210 External Components..... | 27 |
| 8-2 | TUSB1210 V _{BUS} Capacitors..... | 27 |
| 9-1 | USB Register Summary | 28 |
| 12-1 | TUSB1210 Nomenclature Description..... | 57 |
| 12-2 | TUSB1210 Thermal Resistance Characteristics | 57 |

Standalone USB Transceiver Chip Silicon

Check for Samples: [TUSB1210](#)

1 Features

- **USB2.0 PHY Transceiver Chip, Designed to Interface With a USB Controller via a ULPI Interface, Fully Compliant With:**
 - *Universal Serial Bus Specification Rev. 2.0*
 - *On-The-Go Supplement to the USB 2.0 Specification Rev. 1.3*
 - *UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1*
 - *ULPI 12-pin SDR Interface*
 - **DP/DM Line External Component Compensation (TI Patent Pending)**
 - **Interfaces to Host, Peripheral and OTG Device Cores; Optimized for Portable Devices or System ASICs with Built-in USB OTG Device Core**
 - **Complete USB OTG Physical Front-End that Supports Host Negotiation Protocol (HNP) and Session Request Protocol (SRP)**
 - **V_{BUS} Overvoltage Protection Circuitry Protects V_{BUS} Pin in Range –2 V to 20 V**
 - **Internal 5 V Short-Circuit Protection of DP, DM, and ID Pins for Cable Shorting to V_{BUS} Pin**
 - **ULPI Interface:**
 - **I/O Interface (1.8V) Optimized for Non-Terminated 50 Ω Line Impedance**
 - **ULPI CLOCK Pin (60 MHz) Supports Both Input and Output Clock Configurations**
 - **Fully Programmable ULPI-Compliant Register Set**
 - **Full Industrial Grade Operating Temperature Range from –40°C to 85°C**
 - **Available in a 32-Pin Quad Flat No Lead [QFN (RHB)] Package**
 - **Can Be Interfaced to Peripheral, Host or OTG Controller Devices via ULPI. Suited to Portable Devices or System ASICs with Built-In**
- Controller Core.**
- **Complete HS-USB Physical Front-End:**
 - **Supports High Speed (480 Mbit/s), Full Speed (12 Mbit/s) and Low Speed (1.5 Mbit/s)**
 - **Integrated Phase-Locked Loop (PLL) Supporting 2 Clock Frequencies 19.2 MHz/26 MHz**
 - **Integrated 45 Ω ±10% High-Speed Termination Resistors, 1.5 kΩ Full-Speed Device Pull-up Resistor, 15 kΩ Host Termination Resistors**
 - **Integrated Transmit and Receive Paths for Parallel-to-Serial and Serial-to-Parallel Data Conversion**
 - **USB Data Recovery to Allow Recovery of USB Data up to ±500 ppm Frequency Drift**
 - **Bit-Stuffing Insertion During Transmit and Removal During Receive**
 - **Non-Return-to-Zero Inverted (NRZI) Encoding and Decoding**
 - **Supports Bus Reset, Suspend, Resume and High-Speed Detection Handshake (Chirp)**
 - **HS USB DP/DM Impedance Programmability for External Component Compensation**
 - **OTG Ver1.3 :**
 - **Control of External V_{BUS} Switch or Charge Pump**
 - **Both Session Request Protocol (SRP) Methods Supported: Data Pulsing and V_{BUS} Pulsing**
 - **Integrated V_{BUS} Detectors and Cable Detection (ID)**
 - **Internal Power-On Reset (POR) Circuit**
 - **Flexible System Integration and Very Low Current Consumption, Optimized for Portable Devices**

2 Description

The TUSB1210 is a USB2.0 transceiver chip, designed to interface with a USB controller via a ULPI interface. It supports all USB2.0 data rates (High-Speed 480Mbps, Full-Speed 12 Mbps and Low-Speed 1.5Mbps), and is compliant to both Host and Peripheral modes. It additionally supports a UART mode and legacy ULPI serial modes.

TUSB1210 also supports the OTG (Ver1.3) optional addendum to the USB 2.0 Specification, including Host Negotiation Protocol (HNP) and Session Request Protocol (SRP).

TUSB1210 is optimized to be interfaced through a 12-pin SDR UTMI Low Pin Interface (ULPI), supporting both input clock and output clock modes, with 1.8 V interface supply voltage.

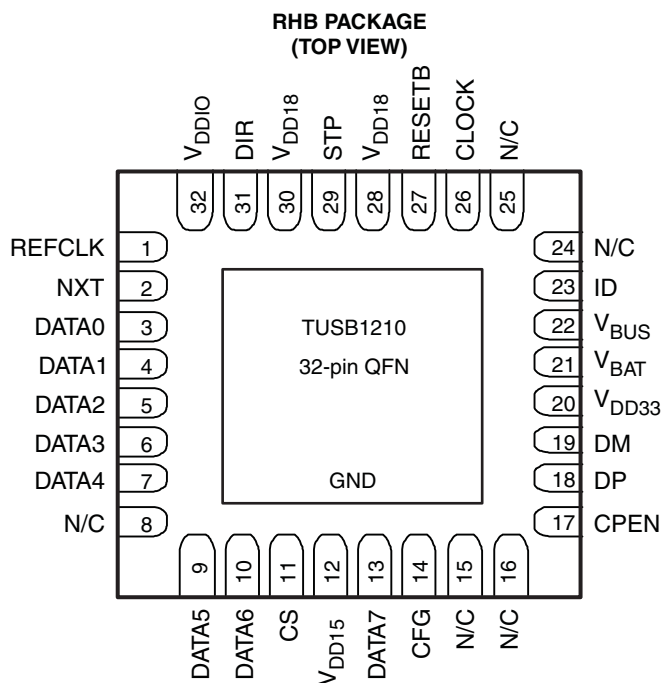
TUSB1210 integrates a 3.3 V LDO, which makes it flexible to work with either battery operated systems or pure 3.3 V supplied systems. Both the main supply and the 3.3 V power domain can be supplied through an external switched-mode converter for optimized power efficiency.

TUSB1210 includes a POR circuit to detect supply presence on V_{BAT} and V_{DDIO} pins. TUSB1210 can be disabled or configured in low power mode for energy saving.

TUSB1210 is protected against accidental shorts to 5 V or ground on its exposed interface (DP/DM/ID). It is also protected against up to 20 V surges on V_{BUS} .

TUSB1210 integrates a high-performance low-jitter 480 MHz PLL and supports two clock configurations. Depending on the required link configuration, TUSB1210 supports both ULPI input and output clock mode : input clock mode, in which case a square-wave 60 MHz clock is provided to TUSB1210 at the ULPI interface CLOCK pin; and output clock mode in which case TUSB1210 can accept a square-wave reference clock at REFCLK of either 19.2 MHz, 26 MHz. Frequency is indicated to TUSB1210 via the configuration pin CFG. This can be useful if a reference clock is already available in the system.

2.1 Terminal Description

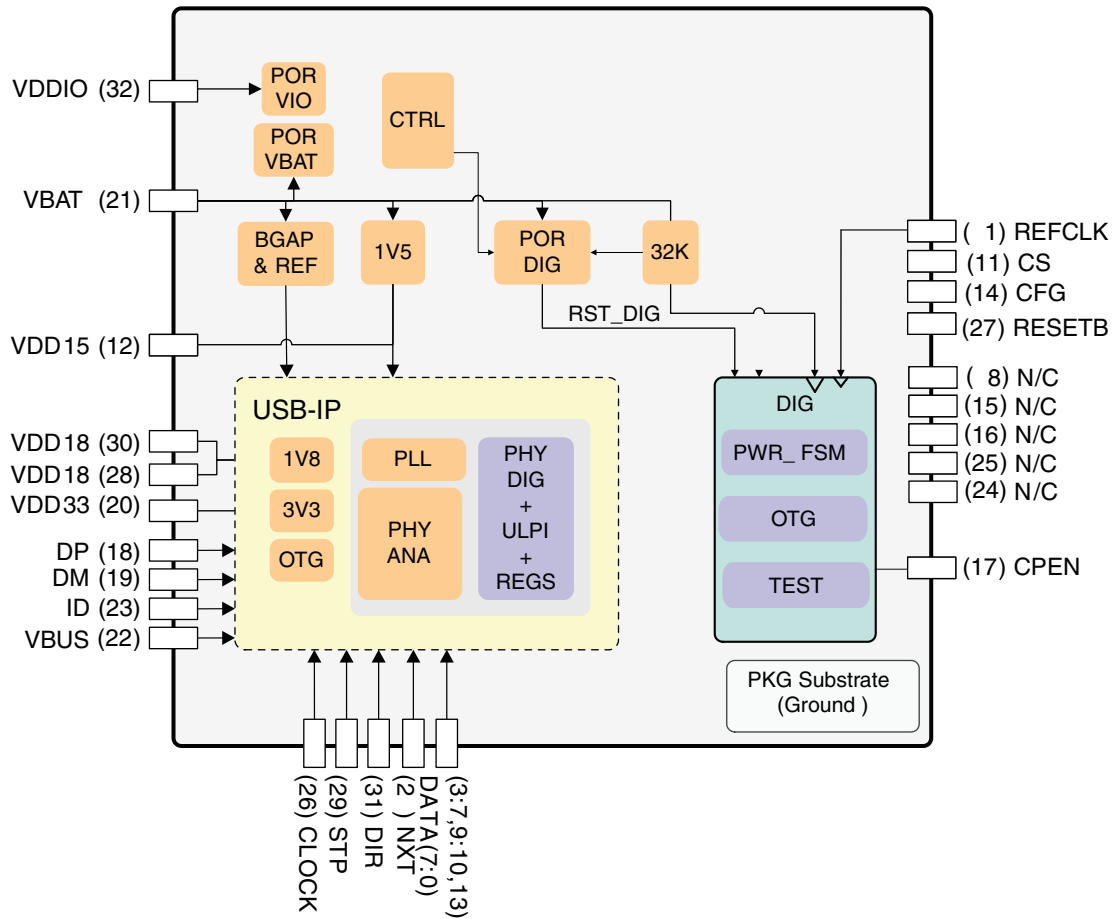


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Table 2-1. Terminal Functions

| TERMINAL | | A/D | TYPE | LEVEL | DESCRIPTION |
|----------|-------------------|-----|-------|-------------------|--|
| NO. | NAME | | | | |
| 1 | REFCLK | A | I | 3.3 V | V _{DD33} Reference clock input (square-wave only). Tie to GND when pin 26 (CLOCK) is required to be Input mode. Connect to square-wave reference clock of amplitude in the range of 3 V to 3.6 V when Pin 26 (CLOCK) is required to be Output mode. See pin 14 (CFG) description for REFCLK input frequency settings. |
| 2 | NXT | D | O | V _{DDIO} | ULPI NXT output signal |
| 3 | DATA0 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 0 synchronized to CLOCK |
| 4 | DATA1 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 1 synchronized to CLOCK |
| 5 | DATA2 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 2 synchronized to CLOCK |
| 6 | DATA3 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 3 synchronized to CLOCK |
| 7 | DATA4 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 4 synchronized to CLOCK |
| 8 | N/C | – | – | V _{DDIO} | No connect |
| 9 | DATA5 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 5 synchronized to CLOCK |
| 10 | DATA6 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 6 synchronized to CLOCK |
| 11 | CS | D | I | V _{DDIO} | Active-high chip select pin. When low the IC is in power down and ULPI bus is tri-stated. When high normal operation. Tie to V _{DDIO} if unused. |
| 12 | VDD15 | A | power | | 1.5-V internal LDO output. Connect to external filtering capacitor. |
| 13 | DATA7 | D | I/O | V _{DDIO} | ULPI DATA input/output signal 7 synchronized to CLOCK |
| 14 | CFG | D | I | V _{DDIO} | REFCLK clock frequency configuration pin. Two frequencies are supported: 19.2 MHz when 0, or 26 MHz when 1. |
| 15 | N/C | – | – | – | No connect |
| 16 | N/C | – | – | – | No connect |
| 17 | CPEN | D | O | V _{DD33} | CMOS active-high digital output control of external 5V VBUS supply |
| 18 | DP | A | I/O | V _{DD33} | DP pin of the USB connector |
| 19 | DM | A | I/O | V _{DD33} | DM pin of the USB connector |
| 20 | V _{DD33} | A | power | V _{DD33} | 3.3-V internal LDO output. Connect to external filtering capacitor. |
| 21 | V _{BAT} | A | power | V _{BAT} | Input supply voltage or battery source |
| 22 | V _{BUS} | A | power | V _{BUS} | V _{BUS} pin of the USB connector |
| 23 | ID | A | I/O | V _{DD33} | Identification (ID) pin of the USB connector |
| 24 | N/C | – | – | – | No connect |
| 25 | N/C | – | – | – | No connect |
| 26 | CLOCK | D | O | V _{DDIO} | ULPI 60 MHz clock on which ULPI data is synchronized. Two modes are possible: Input Mode: CLOCK defaults as an input. Output Mode: When an input clock is detected on REFCLK pin (after 4 rising edges) then CLOCK will change to an output. |
| 27 | RESETB | D | I | V _{DDIO} | When low, all digital logic (except 32 kHz logic required for power up sequencing) including registers are reset to their default values, and ULPI bus is tri-stated. When high, normal USB operation. |
| 28 | V _{DD18} | A | power | V _{DD18} | External 1.8-V supply input. Connect to external filtering capacitor. |
| 29 | STP | D | I | V _{DDIO} | ULPI STP input signal |
| 30 | V _{DD18} | A | power | V _{DD18} | External 1.8-V supply input. Connect to external filtering capacitor. |
| 31 | DIR | D | O | V _{DDIO} | ULPI DIR output signal |
| 32 | V _{DDIO} | A | I | V _{DDIO} | External 1.8V supply input for digital I/Os. Connect to external filtering capacitor. |

2.2 TUSB1210 Block Diagram



3 Electrical Characteristics

3.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | CONDITIONS | MIN | MAX | UNIT |
|-------------------|---|--|------|---------------------------|------|
| V _{CC} | Main battery supply voltage ⁽²⁾ | | 0 | 5 | V |
| | Voltage on any input ⁽³⁾ | Where supply represents the voltage applied to the power supply pin associated with the input | -0.3 | 1 × V _{CC} + 0.3 | V |
| | V _{BUS} input | | -2 | 20 | V |
| | ID, DP, DM inputs | Stress condition guaranteed 24h | -0.3 | 5.25 | V |
| V _{DDIO} | IO supply voltage | Continuous | | 1.98 | V |
| T _{stg} | Storage temperature range | | -55 | 125 | °C |
| T _A | Ambient temperature range | | -40 | 85 | °C |
| T _J | Ambient temperature range | Absolute maximum rating | -40 | 150 | °C |
| | | For parametric compliance | -40 | 125 | |
| | Ambient temperature for parametric compliance | With max 125°C as junction temperature | -40 | 85 | °C |
| | DP, DM, ID high voltage short circuit | DP, DM or ID pins short circuited to V _{BUS} supply, in any mode of TUSB1210 operation, continuously for 24 hours | | 5.25 | V |
| | DP, DM, ID low voltage short circuit | DP, DM or ID pins short circuited to GND in any mode of TUSB1210 operation, continuously for 24 hours | 0 | | V |

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The product will have negligible reliability impact if voltage spikes of 5.5 V occur for a total (cumulative over lifetime) duration of 5 milliseconds.
- (3) Except V_{BAT} input, V_{BUS}, ID, DP, and DM pads

3.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|--------------------------|---|--|------|-----|------|------|
| V _{BAT} | Battery supply voltage | | 2.7 | 3.6 | 4.8 | V |
| V _{BAT} CERT | Battery supply voltage for USB 2.0 compliancy (USB 2.0 certification) | When V _{DD33} is supplied internally | 3.15 | | | V |
| | | When V _{DD33} is shorted to V _{BAT} externally | 3.05 | | | |
| V _{DDIO} | Digital IO pin supply | | 1.71 | | 1.98 | V |
| T _A | Ambient temperature range | | -40 | | 85 | °C |

3.3 ESD Electrical Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------|-------------------------------------|-----------------|-----|-----|------|------|
| CDM | Charged-Device Model stress voltage | All pads | | | 500 | V |
| HBM | Human-Body Model stress voltage | All pads | | | 2000 | V |

4 Clock System

4.1 USB PLL Reference Clock

The USB PLL block generates the clocks used to synchronize :

- the ULPI interface (60 MHz clock)
- the USB interface (depending on the USB data rate, 480 Mbps, 12 Mbps or 1.5 Mbps)

TUSB1210 requires an external reference clock which is used as an input to the 480 MHz USB PLL block. Depending on the clock configuration, this reference clock can be provided either at REFCLK pin or at CLOCK pin. By default CLK pin is configured as an input.

Two clock configurations are possible:

- Input clock configuration (see [Section 4.2](#))
- Output clock configuration (see [Section 4.3](#))

4.2 ULPI Input Clock Configuration

In this mode REFCLK must be externally tied to GND. CLOCK remains configured as an input.

When the ULPI interface is used in “input clock configuration”, i.e., the 60 MHz ULPI clock is provided to TUSB1210 on Clock pin, then this is used as the reference clock for the 480 MHz USB PLL block.

Table 4-1. Electrical Characteristics: Clock Input

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------------------|--|-----|-----|-----|--------|
| Clock input duty cycle | | 40 | | 60 | % |
| f_{CLK} Clock nominal frequency | | | 60 | | MHz |
| Clock input rise/fall time | In % of clock period $t_{CLK} (= 1/f_{CLK})$ | | | 10 | % |
| Clock input frequency accuracy | | | | 250 | ppm |
| Clock input integrated jitter | | | | 600 | ps rms |

4.3 ULPI Output Clock Configuration

In this mode a reference clock must be externally provided on REFCLK pin. When an input clock is detected on REFCLK pin then CLK will automatically change to an output, i.e., 60 MHz ULPI clock is output by TUSB1210 on CLK pin.

Two reference clock input frequencies are supported. REFCLK input frequency is communicated to TUSB1210 via a configuration pin, CFG, see f_{REFCLK} in [Table 8-1](#) for frequency correspondence. TUSB1210 supports square-wave reference clock input only. Reference clock input must be square-wave of amplitude in the range 3.0 V to 3.6 V.

Table 4-2. Electrical Characteristics: REFCLK

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|--|-----|------|-----|--------|
| REFCLK input duty cycle | | 40 | | 60 | % |
| f_{REFCLK} REFCLK nominal frequency | When CFG pin is tied to GND | | 19.2 | | MHz |
| | When CFG pin is tied to V_{DDIO} | | 26 | | |
| REFCLK input rise/fall time | In % of clock period $t_{REFCLK} (= 1/f_{REFCLK})$ | | | 20 | % |
| REFCLK input frequency accuracy | | | | 250 | ppm |
| REFCLK input integrated jitter | | | | 600 | ps rms |

4.4 Clock 32 kHz

An internal clock generator running at 32 kHz has been implemented to provide a low-speed, low-power clock to the system

Table 4-3. Performances

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------|-------------------------|-----|-----|-----|------|
| Output duty cycle | Input duty cycle 40–60% | 48 | 50 | 52 | % |
| Output frequency | | 23 | 32 | 38 | kHz |

4.5 Reset

All logic is reset if CS = 0 or V_{BAT} are not present.

All logic (except 32 kHz logic) is reset if V_{DDIO} is not present.

PHY logic is reset when any supplies are not present (V_{DDIO} , V_{DD15} , V_{DD18} , V_{DD33}) or if RESETB pin is low.

TUSB1210 may be reset manually by toggling the RESETB pin to GND for at least 200 ns.

If manual reset via RESETB is not required then RESETB pin may be tied to V_{DDIO} permanently.

5 Power Module

This chapter describes the electrical characteristics of the voltage regulators and timing characteristics of the supplies digitally controlled within the TUSB1210.

5.1 Power Providers

Table 5-1. Summary of TUSB1210 Power Providers⁽¹⁾

| NAME | USAGE | TYPE | TYPICAL VOLTAGE (V) | MAXIMUM CURRENT (mA) |
|-------------------|----------|------|---------------------|----------------------|
| V _{DD15} | Internal | LDO | 1.5 | 50 |
| V _{DD18} | External | LDO | 1.8 | 30 |
| V _{DD33} | Internal | LDO | 3.1 | 15 |

(1) V_{DD33} may be supplied externally, or by shorting the V_{DD33} pin to V_{BAT} pin provided V_{BAT} min is in range [3.2 V : 3.6 V]. Note that the V_{DD33} LDO will always power-on when the chip is enabled, irrespective of whether V_{DD33} is supplied externally or not. In the case the V_{DD33} pin is not supplied externally in the application, the electrical specs for this LDO are provided below.

5.1.1 V_{DD33} Regulator

The V_{DD33} internal LDO regulator powers the USB PHY, charger detection, and OTG functions of the USB subchip inside TUSB1210. [Table 5-2](#) describes the regulator characteristics.

V_{DD33} regulator takes its power from V_{BAT}.

Since the USB2.0 standard requires data lines to be biased with pullups biased from a supply greater than 3 V, and since V_{DD33} regulator has an inherent voltage drop from its input, V_{BAT}, to its regulated output, TUSB1210 will not meet USB 2.0 Standard if operated from a battery whose voltage is lower than 3.3 V.

Table 5-2. V_{DD33} Internal LDO Regulator Characteristics

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|----------------------|----------------------|----------------------|-------------------------------|------------------------------|------|------|------|
| V _{INVDD33} | Input voltage | V _{BAT} USB | | V _{VDD33} typ + 0.2 | 3.6 | 4.5 | V |
| V _{VDD33} | Output voltage | ON mode, | VUSB3V3_VSEL = '000 | 2.4 | 2.5 | 2.6 | V |
| | | | VUSB3V3_VSEL = '001 | 2.65 | 2.75 | 2.85 | |
| | | | VUSB3V3_VSEL = '010 | 2.9 | 3.0 | 3.1 | |
| | | | VUSB3V3_VSEL = '011 (default) | 3.0 | 3.1 | 3.2 | |
| | | | VUSB3V3_VSEL = '100 | 3.1 | 3.2 | 3.3 | |
| | | | VUSB3V3_VSEL = '101 | 3.2 | 3.3 | 3.4 | |
| | | | VUSB3V3_VSEL = '110 | 3.3 | 3.4 | 3.5 | |
| I _{VDD33} | Rated output current | V _{BAT} USB | Active mode | | | 15 | mA |
| | | | Suspend/reset mode | | | 1 | |

5.1.2 V_{DD18} Supply

The V_{DD18} supply is powered externally at the V_{DD18} pin. See [Table 8-1](#) for external components.

5.1.3 V_{DD15} Regulator

The V_{DD15} internal LDO regulator powers the USB subchip inside TUSB1210. [Table 5-3](#) describes the regulator characteristics.

Table 5-3. V_{DD15} Internal LDO Regulator Characteristics

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|------|------|------|------|
| V _{IN VDD15} Input voltage | On mode, V _{IN VDD15} = V _{BAT} | 2.7 | 3.6 | 4.5 | V |
| V _{VDD15} Output voltage | V _{INVDD15 min} – V _{INVDD15 max} | 1.45 | 1.56 | 1.65 | V |
| I _{VDD15} Rated output current | On mode | | | 30 | mA |

5.2 Power Consumption

Table 5-4 describes the power consumption depending on the use cases.

NOTE

The typical power consumption is obtained in the nominal operating conditions and with the TUSB1210 standalone.

Table 5-4. Power Consumption

| MODE | CONDITIONS | SUPPLY | TYPICAL CONSUMPTION | UNIT |
|-------------------------------------|---|--------------------|---------------------|------|
| OFF Mode | V _{BAT} = 3.6 V, V _{DDIO} = 1.8 V, V _{DD18} = 1.8 V, CS = 0 V | I _{VBAT} | 8 | μA |
| | | I _{VDDIO} | 3 | |
| | | I _{VDD18} | 5 | |
| | | I _{TOTAL} | 16 | |
| Suspend Mode | V _{BUS} = 5 V, V _{BAT} = 3.6 V, V _{DDIO} = 1.8 V, No clock | I _{VBAT} | 204 | μA |
| | | I _{VDDIO} | 3 | |
| | | I _{VDD18} | 3 | |
| | | I _{TOTAL} | 210 | |
| HS USB Operation (Synchronous Mode) | V _{BAT} = 3.6 V, V _{DDIO} = 1.8 V, V _{DD18} = 1.8 V, active USB transfer | I _{VBAT} | 24.6 | mA |
| | | I _{VDDIO} | 1.89 | |
| | | I _{VDD18} | 21.5 | |
| | | I _{TOTAL} | 48 | |
| FS USB Operation (Synchronous Mode) | V _{BAT} = 3.6 V, V _{DDIO} = 1.8 V, active USB transfer | I _{VBAT} | 25.8 | mA |
| | | I _{VDDIO} | 1.81 | |
| | | I _{VDD18} | 4.06 | |
| | | I _{TOTAL} | 31.7 | |
| Reset Mode | RESETB = 0 V, V _{BUS} = 5 V, V _{BAT} = 3.6 V, V _{DDIO} = 1.8 V, No clock | I _{VBAT} | 237 | μA |
| | | I _{VDDIO} | 3 | |
| | | I _{VDD18} | 3 | |
| | | I _{TOTAL} | 243 | |

5.3 Power Management

5.3.1 Power On Sequence

5.3.1.1 Timing Diagram

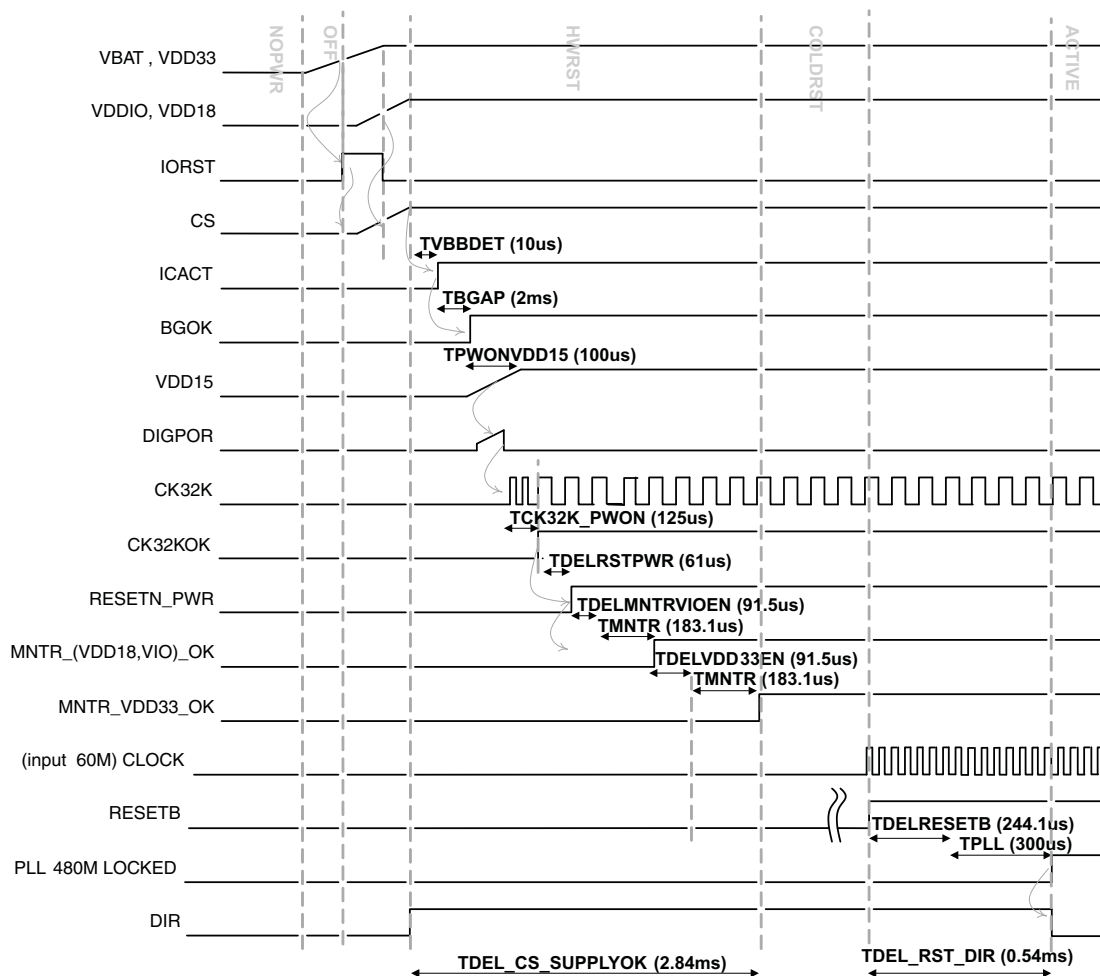


Figure 5-1. TUSB1210 Power-Up Timing (ULPI Clock Input Mode)

5.3.2 Timers and Debounce

| | PARAMETER | COMMENTS | MIN | TYP | MAX | UNIT |
|--|------------------------------|---|-----|-------|-------|------|
| | T _{DEL_CS_SUPPLYOK} | Chip-select-to-supplies OK delay | | 2.84 | 4.10 | ms |
| | T _{DEL_RST_DIR} | RESETB to PHY PLL locked and DIR falling-edge delay | | 0.54 | 0.647 | ms |
| | T _{VBBDET} | V _{BAT} detection delay | | 10 | | us |
| | T _{BGAP} | Bandgap power-on delay | | 2 | | ms |
| | T _{PWONVDD15} | V _{DD15} power-on delay | | 100 | | us |
| | T _{PWONCK32K} | 32-KHz RC-OSC power-on delay | | 125 | | us |
| | T _{DELRSTPWR} | Power control reset delay | | 61 | | us |
| | T _{DELMNTRVIOEN} | Monitor enable delay | | 91.5 | | us |
| | T _{MNTR} | Supply monitoring debounce | | 183.1 | | us |
| | T _{DELVDD33EN} | V _{DD33} LDO enable delay | | 93.75 | | us |
| | T _{DELRESETB} | RESETB internal delay | | 244.1 | | us |
| | T _{PLL} | PLL lock time | | 300 | | us |

6 USB Connectivity

6.1 Timing Parameter Definitions

The timing parameter symbols used in the timing requirement and switching characteristic tables are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated as shown in [Table 6-1](#).

Table 6-1. Timing Parameter Definitions

| LOWERCASE SUBSCRIPTS | |
|----------------------|--|
| SYMBOL | PARAMETER |
| C | Cycle time (period) |
| D | Delay time |
| Dis | Disable time |
| En | Enable time |
| H | Hold time |
| Su | Setup time |
| START | Start bit |
| T | Transition time |
| V | Valid time |
| W | Pulse duration (width) |
| X | Unknown, changing, or don't care level |
| H | High |
| L | Low |
| V | Valid |
| IV | Invalid |
| AE | Active edge |
| FE | First edge |
| LE | Last edge |
| Z | High impedance |

6.2 Interface Target Frequencies

Table [Table 6-2](#) assumes testing over the recommended operating conditions.

Table 6-2. TUSB1210 Interface Target Frequencies

| IO INTERFACE | INTERFACE DESIGNATION | | TARGET FREQUENCY 1.5 V |
|--------------|-----------------------|------------|---------------------------|
| USB | Universal serial bus | High speed | 480 Mbits/s |
| | | Full speed | 12 Mbits/s |
| | | Low speed | 1.5 Mbits/s |

6.3 USB Transceiver

The TUSB1210 device includes a universal serial bus (USB) on-the-go (OTG) transceiver that supports USB 480 Mb/s high-speed (HS), 12 Mb/s full-speed (FS), and USB 1.5 Mb/s low-speed (LS) through a 12-pin UTMI+ low pin interface (ULPI).

NOTE

LS device mode is not allowed by a USB2.0 HS capable PHY, therefore it is not supported by TUSB1210. This is clearly stated in USB2.0 standard Chapter 7, page 119, second paragraph: “A high-speed capable upstream facing transceiver must not support low-speed signaling mode..” There is also some related commentary in Chapter 7.1.2.3.

6.3.1 TUSB1210 Modes vs ULPI Pin Status

Table 6-3, Table 6-4, and Table 6-5 show the status of each of the 12 ULPI pins including input/output direction and whether output pins are driven to ‘0’ or to ‘1’, or pulled up/pulled down via internal pullup/pulldown resistors.

Note that pullup/pulldown resistors are automatically replaced by driven ‘1’/‘0’ levels respectively once internal IORST is released, with the exception of the pullup on STP which is maintained in all modes.

Pin assignment changes in ULPI 3-pin serial mode, ULPI 6-pin serial mode, and UART mode. Unused pins are tied low in these modes as shown below.

Table 6-3. TUSB1210 Modes vs ULPI Pin Status:ULPI Synchronous Mode Power-Up

| | | ULPI SYNCHRONOUS MODE POWER-UP | | | | | | | |
|---------|----------|--------------------------------|-------|----------|-------|-------------------|-------|------------------|-------|
| | | UNTIL IORST RELEASE | | PLL OFF | | PLL ON + STP HIGH | | PLL ON + STP LOW | |
| PIN NO. | PIN NAME | DIR | PU/PD | DIR | PU/PD | DIR | PU/PD | DIR | PU/PD |
| 26 | CLOCK | Hiz | PD | I | PD | IO | - | IO | - |
| 31 | DIR | Hiz | PU | O, ('1') | - | O, ('0') | - | O | - |
| 2 | NXT | Hiz | PD | O, ('0') | - | O, ('0') | - | O | - |
| 29 | STP | Hiz | PU | I | PU | I | PU | I | PU |
| 3 | DATA0 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 4 | DATA1 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 5 | DATA2 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 6 | DATA3 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 7 | DATA4 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 9 | DATA5 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 10 | DATA6 | Hiz | PD | O, ('0') | - | I | PD | IO | - |
| 13 | DATA7 | Hiz | PD | O, ('0') | - | I | PD | IO | - |

Table 6-4. TUSB1210 Modes vs ULPI Pin Status: USB Suspend Mode

| | | SUSPEND MODE | | LINK / EXTERNAL RECOMMENDED SETTING DURING SUSPEND MODE | |
|----|-------|--------------------|-------------------|---|-------|
| | | DIR | PU/PD | DIR | PU/PD |
| 26 | CLOCK | I | - | O | - |
| 31 | DIR | O, ('1') | - | I | - |
| 2 | NXT | O, ('0') | - | I | - |
| 29 | STP | I | PU ⁽¹⁾ | O, ('0') | - |
| 3 | DATA0 | O, (LINESTATE0) | - | I | - |
| 4 | DATA1 | O, (LINESTATE1) | - | I | - |
| 5 | DATA2 | O, ('0') | - | I | - |
| 6 | DATA3 | O, (INT) | - | I | - |

(1) Can be disabled by software before entering Suspend Mode to reduce current consumption

**Table 6-4. TUSB1210 Modes vs ULPI Pin Status: USB Suspend Mode
(continued)**

| | | SUSPEND MODE | | LINK / EXTERNAL RECOMMENDED SETTING DURING SUSPEND MODE | |
|---------|----------|--------------|-------|---|-------|
| PIN NO. | PIN NAME | DIR | PU/PD | DIR | PU/PD |
| 7 | DATA4 | O, ('0') | - | I | - |
| 9 | DATA5 | O, ('0') | - | I | - |
| 10 | DATA6 | O, ('0') | - | I | - |
| 13 | DATA7 | O, ('0') | - | I | - |

Table 6-5. TUSB1210 Modes vs ULPI Pin Status: ULPI 6-Pin Serial Mode and UART Mode

| PIN NO. | ULPI 6-PIN SERIAL MODE | | | ULPI 3-PIN SERIAL MODE | | | UART MODE | | |
|---------|------------------------|-----|-------|------------------------|-----|-------|-----------|-----|-------|
| | PIN NAME | DIR | PU/PD | PIN NAME | DIR | PU/PD | PIN NAME | DIR | PU/PD |
| 26 | CLOCK (1) | IO | - | CLOCK (1) | IO | - | CLOCK (1) | IO | - |
| 31 | DIR | O | - | DIR | O | - | DIR | O | - |
| 2 | NXT | O | - | NXT | O | - | NXT | O | - |
| 29 | STP | I | PU | STP | I | PU | STP | I | PU |
| 3 | TX_ENABLE | I | - | TX_ENABLE | I | - | TXD | I | - |
| 4 | TX_DAT | I | - | DAT | IO | - | RXD | IO | - |
| 5 | TX_SE0 | I | - | SE0 | IO | - | tie low | O | - |
| 6 | INT | O | - | INT | O | - | INT | O | - |
| 7 | RX_DP | O | - | tie low | O | - | tie low | O | - |
| 9 | RX_DM | O | - | tie low | O | - | tie low | O | - |
| 10 | RX_RCV | O | - | tie low | O | - | tie low | O | - |
| 13 | tie low | O | - | tie low | O | - | tie low | O | - |

6.3.2 ULPI Interface Timing

Table 6-6. ULPI Interface Timing

| PARAMETER | | INPUT CLOCK | | OUTPUT CLOCK | | UNIT |
|--------------|--|-------------|-----|--------------|-----|------|
| | | MIN | MAX | MIN | MAX | |
| $T_{SC,TSD}$ | Set-up time (control in, 8-bit data in) | | 3 | | 6 | ns |
| $T_{SC,THD}$ | Hold time (control in, 8-bit data in) | 1.5 | | 0 | | ns |
| $T_{DC,TDD}$ | Output delay (control out, 8-bit data out) | | 6 | | 9 | ns |

6.3.3 PHY Electrical Characteristics

The PHY is the physical signaling layer of the USB 2.0. It essentially contains all the drivers and receivers required for physical data and protocol signaling on the DP and DM lines.

The PHY interfaces to the USB controller through a standard 12-pin digital interface called UTMI+ low pin interface (ULPI).

The transmitters and receivers inside the PHY are classified into two main classes.

- The full-speed (FS) and low-speed (LS) transceivers. These are the legacy USB1.x transceivers.
- The HS (HS) transceivers

In order to bias the transistors and run the logic, the PHY also contains reference generation circuitry which consists of:

- A DPLL which does a frequency multiplication to achieve the 480-MHz low-jitter lock necessary for USB and also the clock required for the switched capacitor resistance block.
- A switched capacitor resistance block which is used to replicate an external resistor on chip.

Built-in pullup and pulldown resistors are used as part of the protocol signaling.

Apart from this, the PHY also contains circuitry which protects it from accidental 5-V short on the DP and DM lines.

6.3.3.1 LS/FS Single-Ended Receivers

In addition to the differential receiver, there is a single-ended receiver (SE–, SE+) for each of the two data lines D+/–. The main purpose of the single-ended receivers is to qualify the D+ and D– signals in the full-speed/low-speed modes of operation.

Table 6-7. LS/FS Single-Ended Receivers

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|----------------------------|-------------------------|-------------------------|-----|-----|-----|------|
| USB single-ended receivers | | | | | | |
| SK _{WVP_VM} | Skew between VP and VM | Driver outputs unloaded | –2 | 0 | 2 | ns |
| V _{SE_HYS} | Single-ended hysteresis | | 50 | | | mV |
| V _{IH} | High (driven) | | 2 | | | V |
| V _{IL} | Low | | | | 0.8 | V |
| V _{TH} | Switching threshold | | 0.8 | | 2 | V |

6.3.3.2 LS/FS Differential Receiver

A differential input receiver (Rx) retrieves the LS/FS differential data signaling. The differential voltage on the line is converted into digital data by a differential comparator on DP/DM. This data is then sent to a clock and data recovery circuit which recovers the clock from the data. An additional serial mode exists in which the differential data is directly output on the RXRCV pin.

Table 6-8. LS/FS Differential Receiver

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------|-------------|-----|-----|-----|------|
| V _{DI} | Differential input sensitivity | Ref. USB2.0 | 200 | | | mV |
| V _{CM} | Differential Common mode range | Ref. USB2.0 | 0.8 | | 2.5 | V |

6.3.3.3 LS/FS Transmitter

The USB transceiver (Tx) uses a differential output driver to drive the USB data signal D+/– onto the USB cable. The driver's outputs support 3-state operation to achieve bidirectional half-duplex transactions.

Table 6-9. LS Transmitter

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---------------------|---|-------------------------------------|-------------------------------------|-----|--------|------|
| V _{OL} | Low | Ref. USB2.0 | 0 | | 300 | mV |
| V _{OH} | High (driven) | Ref. USB2.0 | 2.8 | | 3.6 | V |
| V _{CRS} | Output signal crossover voltage | Ref. USB2.0, covered by eye diagram | 1.3 | | 2 | V |
| T _{FR} | Rise time | Ref. USB2.0, covered by eye diagram | 75 | | 300 | ns |
| T _{FF} | Fall time | | 75 | | 300 | ns |
| T _{FRFM} | Differential rise and fall time matching | | 80 | | 125 | % |
| T _{FDRATE} | Low-speed data rate | Ref. USB2.0, covered by eye diagram | 1.4775 | | 1.5225 | Mb/s |
| T _{DJ1} | Source jitter total (including frequency tolerance) | To next transition | Ref. USB2.0, covered by eye diagram | | 25 | ns |
| T _{DJ2} | | For paired transitions | | | 10 | |
| T _{FEOPT} | Source SE0 interval of EOP | Ref. USB2.0, covered by eye diagram | 1.25 | | 1.5 | us |

Table 6-9. LS Transmitter (continued)

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|-----------|--------------------------------|-------------------------------------|-----|-----|-----|------|
| | Downstream eye diagram | Ref. USB2.0, covered by eye diagram | | | | |
| V_{CM} | Differential common mode range | Ref. USB2.0 | 0.8 | | 2.5 | V |

Table 6-10. FS Transmitter

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---------------------|---|-------------------------------------|-------|-----|------------|------|
| V _{OL} | Low | Ref. USB2.0 | 0 | | 300 | mV |
| V _{OH} | High (driven) | Ref. USB2.0 | 2.8 | | 3.6 | V |
| VC _{RS} | Output signal crossover voltage | Ref. USB2.0, covered by eye diagram | 1.3 | | 2 | V |
| t _{FR} | Rise time | Ref. USB2.0 | 4 | | 20 | ns |
| t _{FF} | Fall time | Ref. USB2.0 | 4 | | 20 | ns |
| t _{FRFM} | Differential rise and fall time matching | Ref. USB2.0, covered by eye diagram | 90 | | 111.1 1 | % |
| Z _{DRV} | Driver output resistance | Ref. USB2.0 | 28 | | 44 | Ω |
| TF _{DRATE} | Full-speed data rate | Ref. USB2.0, covered by eye diagram | 11.97 | | 12.03 | Mb/s |
| T _{DJ1} | Source jitter total (including frequency tolerance) | To next transition | -2 | | 2 | ns |
| T _{DJ2} | | For paired transitions | | -1 | | |
| TF _{EOPT} | Source SE0 interval of EOP | Ref. USB2.0, covered by eye diagram | 160 | | 175 | ns |
| | Downstream eye diagram | Ref. USB2.0, covered by eye diagram | | | | |
| | Upstream eye diagram | | | | | |

6.3.3.4 HS Differential Receiver

The HS receiver consists of the following blocks:

A differential input comparator to receive the serial data

- A squelch detector to qualify the received data
- An oversampler-based clock data recovery scheme followed by a NRZI decoder, bit unstuffing, and serial-to-parallel converter to generate the ULPI DATAOUT

Table 6-11. HS Differential Receiver

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|--------------------|---|---|-----|-----|-----|------|
| VH _{SSQ} | High-speed squelch detection threshold (differential signal amplitude) | Ref. USB2.0 | 100 | | 150 | mV |
| VH _{SDSC} | High-speed disconnect detection threshold (differential signal amplitude) | Ref. USB2.0 | 525 | | 625 | mV |
| | High-speed differential input signaling levels | Ref. USB2.0, specified by eye pattern templates | | | | mV |
| VH _{SCM} | High-speed data signaling common mode voltage range (guidelines for receiver) | Ref. USB2.0 | -50 | | 500 | mV |
| | Receiver jitter tolerance | Ref. USB2.0, specified by eye pattern templates | | | 150 | ps |

6.3.3.5 HS Differential Transmitter

The HS transmitter is always operated via the ULPI parallel interface. The parallel data on the interface is serialized, bit stuffed, NRZI encoded, and transmitted as a dc output current on DP or DM depending on the data. Each line has an effective 22.5-Ω load to ground, which generates the voltage levels for signaling.

A disconnect detector is also part of the HS transmitter. A disconnect on the far end of the cable causes the impedance seen by the transmitter to double thereby doubling the differential amplitude seen on the DP/DM lines.

Table 6-12. HS Transmitter

| PARAMETER | COMMENTS | MIN | TYP | MAX | UNIT |
|-------------------|--|-------------------------------------|--------|--------|------|
| V _{HSOI} | High-speed idle level | Ref. USB2.0 | -10 | 10 | mV |
| V _{HSOH} | High-speed data signaling high | Ref. USB2.0 | 360 | 440 | mV |
| V _{HSOL} | High-speed data signaling low | Ref. USB2.0 | -10 | 10 | mV |
| VCHIRPJ | Chirp J level (differential voltage) | Ref. USB2.0 | 700 | 1100 | mV |
| VCHIRPK | Chirp K level (differential voltage) | Ref. USB2.0 | -900 | -500 | mV |
| THSR | Rise Time (10% - 90%) | Ref. USB2.0, covered by eye diagram | 500 | | ps |
| THSR | Fall time (10% - 90%) | Ref. USB2.0, covered by eye diagram | 500 | | ps |
| ZHSDRV | Driver output resistance (which also serves as high-speed termination) | Ref. USB2.0 | 40.5 | 49.5 | Ω |
| THSDRAT | High-speed data range | Ref. USB2.0, covered by eye diagram | 479.76 | 480.24 | Mb/s |
| | Data source jitter | Ref. USB2.0, covered by eye diagram | | | |
| | Downstream eye diagram | Ref. USB2.0, covered by eye diagram | | | |
| | Upstream eye diagram | Ref. USB2.0, covered by eye diagram | | | |

6.3.3.6 UART Transceiver

In this mode, the ULPI data bus is redefined as a 2-pin UART interface, which exchanges data through a direct access to the FS/LS analog transmitter and receiver.

Table 6-13. USB UART Interface Timing Parameters

| PARAMETER | MIN | MAX | UNIT |
|--------------------------|-----|------|------|
| t _{PH_DP_CON} | 100 | | ms |
| t _{PH_DISC_DET} | 150 | | ms |
| f _{UART_DFLT} | | 9600 | bps |

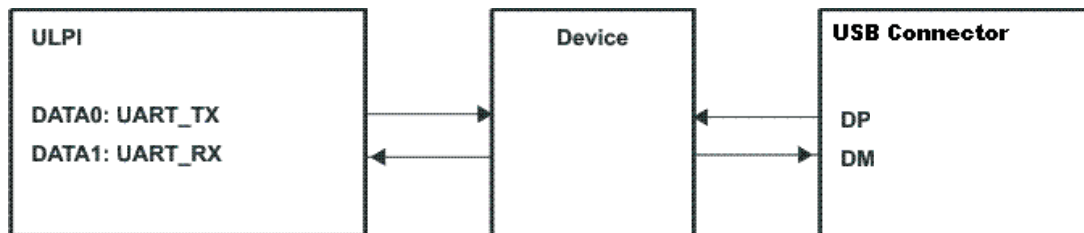


Figure 6-1. USB UART Data Flow

Table 6-14. CEA-2011/UART Transceiver

| PARAMETER | COMMENTS | MIN | TYP | MAX | UNIT | |
|---------------------------|------------------------------|----------------------|-----|-----|------|---|
| UART Transmitter CEA-2011 | | | | | | |
| t _{PH_UART_EDGE} | Phone UART edge rates | | | 1 | Ms | |
| V _{OH_SER} | Serial interface output high | ISOURCE = 4 mA | 2.4 | 3.3 | 3.6 | V |
| V _{OL_SER} | Serial interface output low | ISINK = -4 mA | 0 | 0.1 | 0.4 | V |
| UART Receiver CEA-2011 | | | | | | |
| V _{IH_SER} | Serial interface input high | DP_PULLDOWN asserted | 2 | | V | |
| V _{IL_SER} | Serial interface input low | DP_PULLDOWN asserted | | 0.8 | V | |
| V _{TH} | Switching threshold | | 0.8 | 2 | V | |

Table 6-15. Pullup/Pulldown Resistors

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|----------------|--|---|-------|-----|-------|------|
| RPUI | Bus pullup resistor on upstream port (idle bus) | Bus idle | 0.9 | 1.1 | 1.575 | kΩ |
| RPUA | Bus pullup resistor on upstream port (receiving) | Bus driven/driver's outputs unloaded | 1.425 | 2.2 | 3.09 | |
| VIHZ | High (floating) | Pullups/pulldowns on both DP and DM lines | 2.7 | | 3.6 | V |
| VPH_DP_UP | Phone D+ pullup voltage | Driver's outputs unloaded | 3 | 3.3 | 3.6 | V |
| | Pulldown resistors | | | | | |
| RPH_DP_DWN | Phone D+/- pulldown | Driver's outputs unloaded | 14.25 | 18 | 24.8 | kΩ |
| RPH_DM_DWN | | | | | | |
| VIHZ | High (floating) | Pullups/pulldowns on both DP and DM lines | 2.7 | | 3.6 | V |
| | D+/- Data line | | | | | |
| CINUB | Upstream facing port | [1.0] | | 22 | 75 | pF |
| VOTG_DATA_LK G | On-the-go device leakage | [2] | | | 0.342 | V |
| ZINP | Input impedance exclusive of pullup/pulldown | Driver's outputs unloaded | 300 | | | kΩ |

6.3.4 OTG Electrical Characteristics

The on-the-go (OTG) block integrates three main functions:

- The USB plug detection function on V_{BUS} and ID
- The ID resistor detection
- The V_{BUS} level detection

Table 6-16. OTG V_{BUS} Electrical

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|---|---|---|-------|-----|-------|------|
| V_{BUS} Comparators | | | | | | |
| VA_SESS_VLD | A-device session valid | | 0.8 | 1.4 | 2.0 | V |
| VA_VBUS_VLD | A-device V_{BUS} valid | | 4.4 | 4.5 | 4.625 | V |
| VB_SESS_END | B-device session end | | 0.2 | 0.5 | 0.8 | V |
| VB_SESS_VLD | B-device session valid | | 2.1 | 2.4 | 2.7 | V |
| V_{BUS} Line | | | | | | |
| RA_BUS_IN | A-device V_{BUS} input impedance to ground | SRP (V_{BUS} pulsing) capable A-device not driving V_{BUS} | 40 | 70 | 100 | kΩ |
| RB_SRP_DWN | B-device V_{BUS} SRP pulldown | 5.25 V / 8 mA, Pullup voltage = 3 V | 0.656 | 10 | | kΩ |
| RB_SRP_UP | B-device V_{BUS} SRP pullup | (5.25 V – 3 V) / 8 mA, Pullup voltage = 3 V | 0.281 | 1 | 2 | kΩ |
| $t_{RISE_SRP_UP_MAX}$ | B-device V_{BUS} SRP rise time maximum for OTG-A communication | 0 to 2.1 V with < 13 μ F load | | | TBD | ms |
| $t_{RISE_SRP_UP_MIN}$ | B-device V_{BUS} SRP rise time minimum for standard host connection | 0.8 to 2.0 V with > 97 μ F load | TBD | | | ms |

Table 6-17. OTG ID Electrical

| PARAMETER | | COMMENTS | MIN | TYP | MAX | UNIT |
|--|--|----------------------------------|-----|-----|------|------|
| ID Comparators — ID External Resistors Specifications | | | | | | |
| R _{ID_GND} | ID ground comparator | ID_GND interrupt | 12 | 20 | 28 | kΩ |
| R _{ID_FLOAT} | ID Float comparator | ID_FLOAT interrupt | 200 | | 500 | kΩ |
| | ID Line | | | | | |
| R _{PH_ID_UP} | Phone ID pullup to V _{PH_ID_UP} | ID unloaded (V _{RUSB}) | 70 | 90 | 286 | kΩ |
| V _{PH_ID_UP} | Phone ID pullup voltage | Connected to V _{RUSB} | 2.5 | | 3.2 | V |
| | ID line maximum voltage | | | | 5.25 | V |

7 I/O Electrical Characteristics

7.1 Analog I/O Electrical Characteristics

Table 7-1. Electrical Characteristics: Analog Output Pins

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------|--------------------------------|--------------------------|----------------|-----|-----|------|
| CPEN Output Pin | | | | | | |
| V_{OL_CPEN} | CPEN low-level output voltage | $I_{OL} = 3 \text{ mA}$ | | | 0.3 | V |
| V_{OH_CPEN} | CPEN high-level output voltage | $I_{OH} = -3 \text{ mA}$ | $V_{DD33}-0.3$ | | | V |

7.2 Digital I/O Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PIN NAME | V_{OL} (V) | | V_{OH} (V) | | V_{IL} (V) | | V_{IH} (V) | | MAX FREQ (MHz) | MAX LOAD (pF) OUTPUT MODE | MAX RISE TIME (ns) | MAX FALL TIME (ns) |
|----------|--------------|-----|-----------------|-----|-----------------------|-----|-----------------------|-----|----------------|---------------------------|--------------------|--------------------|
| | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | | | | |
| CLOCK | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 60 | 10 | 1 | 1 |
| STP | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DIR | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| NXT | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA0 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA1 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA2 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA3 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA4 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA5 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA6 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |
| DATA7 | 0.45 | | $V_{DDIO}-0.45$ | | $0.35 \cdot V_{DDIO}$ | | $0.65 \cdot V_{DDIO}$ | | 30 | 10 | 1 | 1 |

7.3 Electrical Characteristics: Digital IO Pins (Non-ULPI)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | TYP | MAX | UNIT |
|-------------------------------------|-------------------------------------|--|-----------------------|-----|-------------------------|---------------|
| CS, CFG, RESETB Input Pins | | | | | | |
| V_{IL} | Maximum low-level input voltage | | | | $0.35 \cdot V_{DDIO}^*$ | V |
| V_{IH} | Minimum high-level input voltage | | $0.65 \cdot V_{DDIO}$ | | | V |
| RESETB Input Pin Timing Spec | | | | | | |
| $t_{w(POR)}$ | Internal power-on reset pulse width | | 0.2 | | | μs |
| $t_{w(RESET)}$ | External RESETB pulse width | Applied to external RESETB pin when CLOCK is toggling. | 8 | | | CLOCK cycles |

8 External Components

Table 8-1. TUSB1210 External Components

| FUNCTION | COMPONENT | REFERENCE | VALUE | NOTE | LINK |
|-------------------|-----------|-----------------|-----------------------|--|-----------------------------|
| V _{DDIO} | Capacitor | CVDDIO | 100 nF | Suggested value, application dependent | Figure 10-1 |
| V _{DD33} | Capacitor | CVDD33 | 2.2 μF | Range: [0.45 μF : 6.5 μF] , ESR = [0 : 600 mΩ] for f > 10 kHz | Figure 10-1 |
| V _{DD15} | Capacitor | CVDD15 | 2.2 μF | Range: [0.45 μF : 6.5 μF] , ESR = [0 : 600 mΩ] for f > 10 kHz | Figure 10-1 |
| V _{DD18} | Capacitor | Ext 1.8V supply | 100 nF | Suggested value, application dependent | Figure 10-1 |
| | | CVDD18 | | | |
| V _{BAT} | Capacitor | CBYP | 100 nF ⁽¹⁾ | Range: [0.45 μF : 6.5 μF] , ESR = [0 : 600 mΩ] for f > 10 kHz | Figure 10-1 |
| V _{BUS} | Capacitor | CVBUS | See table 1.2 | Place close to USB connector | Figure 10-1 |

(1) Recommended value but 2.2 uF may be sufficient in some applications

Table 8-2. TUSB1210 V_{BUS} Capacitors

| FUNCTION | COMPONENT | REFERENCE | VALUE | NOTE | LINK |
|---------------|-----------|-----------|---------|--------------------------|-----------------------------|
| VBUS - HOST | Capacitor | CVBUS | >120 μF | | Figure 10-1 |
| VBUS – DEVICE | Capacitor | CVBUS | 4.7 μF | Range: 1.0 μF to 10.0 μF | Figure 10-1 |
| VBUS - OTG | Capacitor | CVBUS | 4.7 μF | Range: 1.0 μF to 6.5 μF | Figure 10-1 |

9 Register Map

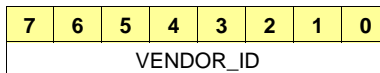
9.1 TUSB1210 Product

Table 9-1. USB Register Summary

| REGISTER NAME | TYPE | REGISTER WIDTH (BITS) | PHYSICAL ADDRESS |
|------------------------|------|-----------------------|------------------|
| VENDOR_ID_LO | R | 8 | 0x00 |
| VENDOR_ID_HI | R | 8 | 0x01 |
| PRODUCT_ID_LO | R | 8 | 0x02 |
| PRODUCT_ID_HI | R | 8 | 0x03 |
| FUNC_CTRL | RW | 8 | 0x04 |
| FUNC_CTRL_SET | RW | 8 | 0x05 |
| FUNC_CTRL_CLR | RW | 8 | 0x06 |
| IFC_CTRL | RW | 8 | 0x07 |
| IFC_CTRL_SET | RW | 8 | 0x08 |
| IFC_CTRL_CLR | RW | 8 | 0x09 |
| OTG_CTRL | RW | 8 | 0x0A |
| OTG_CTRL_SET | RW | 8 | 0x0B |
| OTG_CTRL_CLR | RW | 8 | 0x0C |
| USB_INT_EN_RISE | RW | 8 | 0x0D |
| USB_INT_EN_RISE_SET | RW | 8 | 0x0E |
| USB_INT_EN_RISE_CLR | RW | 8 | 0x0F |
| USB_INT_EN_FALL | RW | 8 | 0x10 |
| USB_INT_EN_FALL_SET | RW | 8 | 0x11 |
| USB_INT_EN_FALL_CLR | RW | 8 | 0x12 |
| USB_INT_STS | R | 8 | 0x13 |
| USB_INT_LATCH | R | 8 | 0x14 |
| DEBUG | R | 8 | 0x15 |
| SCRATCH_REG | RW | 8 | 0x16 |
| SCRATCH_REG_SET | RW | 8 | 0x17 |
| SCRATCH_REG_CLR | RW | 8 | 0x18 |
| Reserved | R | 8 | 0x19 0x2E |
| ACCESS_EXT_REG_SET | RW | 8 | 0x2F |
| Reserved | R | 8 | 0x30 0x3C |
| VENDOR_SPECIFIC1 | RW | 8 | 0x3D |
| VENDOR_SPECIFIC1_SET | RW | 8 | 0x3E |
| VENDOR_SPECIFIC1_CLR | RW | 8 | 0x3F |
| VENDOR_SPECIFIC2 | RW | 8 | 0x80 |
| VENDOR_SPECIFIC2_SET | RW | 8 | 0x81 |
| VENDOR_SPECIFIC2_CLR | RW | 8 | 0x82 |
| VENDOR_SPECIFIC1_STS | R | 8 | 0x83 |
| VENDOR_SPECIFIC1_LATCH | R | 8 | 0x84 |
| VENDOR_SPECIFIC3 | RW | 8 | 0x85 |
| VENDOR_SPECIFIC3_SET | RW | 8 | 0x86 |
| VENDOR_SPECIFIC3_CLR | RW | 8 | 0x87 |

9.1.1 VENDOR_ID_LO

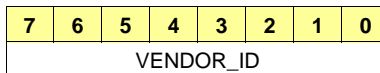
| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x00 | | |
| PHYSICAL ADDRESS | 0x00 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Lower byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451) | | |
| TYPE | R | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | VENDOR_ID | | R | 0x51 |

9.1.2 VENDOR_ID_HI

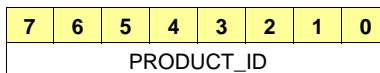
| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x01 | | |
| PHYSICAL ADDRESS | 0x01 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Upper byte of vendor ID supplied by USB-IF (TI Vendor ID = 0x0451) | | |
| TYPE | R | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | VENDOR_ID | | R | 0x04 |

9.1.3 PRODUCT_ID_LO

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x02 | | |
| PHYSICAL ADDRESS | 0x02 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Lower byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507). | | |
| TYPE | R | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | PRODUCT_ID | | R | 0x07 |

9.1.4 PRODUCT_ID_HI

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x03 | | |
| PHYSICAL ADDRESS | 0x03 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Upper byte of Product ID supplied by Vendor (TUSB1210 Product ID is 0x1507). | | |
| TYPE | R | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PRODUCT_ID | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | PRODUCT_ID | | R | 0x15 |

9.1.5 FUNC_CTRL

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x04 | | |
| PHYSICAL ADDRESS | 0x04 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Controls UTMI function settings of the PHY. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|----------|----------|-------|--------|------------|------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | SUSPENDM | RESET | OPMODE | TERMSELECT | XCVRSELECT | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|--|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | Active low PHY suspend. Put PHY into Low Power Mode. In Low Power Mode the PHY power down all blocks except the full speed receiver, OTG comparators, and the ULPI interface pins. The PHY automatically set this bit to '1' when Low Power Mode is exited. | RW | 1 |
| 5 | RESET | Active high transceiver reset. Does not reset the ULPI interface or ULPI register set. Once set, the PHY asserts the DIR signal and reset the UTMI core. When the reset is completed, the PHY de-asserts DIR and clears this bit. After de-asserting DIR, the PHY re-assert DIR and send an RX command update. Note: This bit is auto-cleared, this explain why it can't be read at '1'. | RW | 0 |
| 4:03 | OPMODE | Select the required bit encoding style during transmit 0x0: Normal operation 0x1: Non-driving 0x2: Disable bit-stuff and NRZI encoding 0x3: Reserved (No SYNC and EOP generation feature not supported) | RW | 0x0 |
| 2 | TERMSELECT | Controls the internal 1.5Kohms pull-up resistor and 45ohms HS terminations. Control over bus resistors changes depending on XcvrSelect, OpMode, DpPulldown and DmPulldown. | RW | 0 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|--|------|-------|
| 1:00 | XCVRSELECT | Select the required transceiver speed. 0x0: Enable HS transceiver 0x1: Enable FS transceiver 0x2: Enable LS transceiver 0x3: Enable FS transceiver for LS packets (FS preamble is automatically pre-pended) | RW | 0x1 |

9.1.6 FUNC_CTRL_SET

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x05 | | |
| PHYSICAL ADDRESS | 0x05 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|-------|--------|------------|------------|---|---|
| Reserved | SUSPENDM | RESET | OPMODE | TERMSELECT | XCVRSELECT | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | | RW | 1 |
| 5 | RESET | | RW | 0 |
| 4:03 | OPMODE | | RW | 0x0 |
| 2 | TERMSELECT | | RW | 0 |
| 1:00 | XCVRSELECT | | RW | 0x1 |

9.1.7 FUNC_CTRL_CLR

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x06 | | |
| PHYSICAL ADDRESS | 0x06 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|-------|--------|------------|------------|---|---|
| Reserved | SUSPENDM | RESET | OPMODE | TERMSELECT | XCVRSELECT | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | SUSPENDM | | RW | 1 |
| 5 | RESET | | RW | 0 |
| 4:03 | OPMODE | | RW | 0x0 |
| 2 | TERMSELECT | | RW | 0 |
| 1:00 | XCVRSELECT | | RW | 0x1 |

9.1.8 IFC_CTRL

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x07 | | |
| PHYSICAL ADDRESS | 0x07 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Enables alternative interfaces and PHY features. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------|-------------------|---------------------|------------|---------------|------------|---------------------|---------------------|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------------|--|------|-------|
| 7 | INTERFACE_PROTECT_DISABLE | Controls circuitry built into the PHY for protecting the ULPI interface when the link tri-states stp and data. 0b: Enables the interface protect circuit 1b: Disables the interface protect circuit | RW | 0 |
| 6 | INDICATORPASSTHRU | Controls whether the complement output is qualified with the internal vbusvalid comparator before being used in the VBUS State in the RXCMD. 0b: Complement output signal is qualified with the internal VBUSVALID comparator. 1b: Complement output signal is not qualified with the internal VBUSVALID comparator. | RW | 0 |
| 5 | INDICATORCOMPLEMENT | Tells the PHY to invert EXTERNALVBUSINDICATOR input signal, generating the complement output. 0b: PHY will not invert signal EXTERNALVBUSINDICATOR (default) 1b: PHY will invert signal EXTERNALVBUSINDICATOR | RW | 0 |
| 4 | AUTORESUME | Enables the PHY to automatically transmit resume signaling. Refer to USB specification 7.1.7.7 and 7.9 for more details. 0 = AutoResume disabled 1 = AutoResume enabled (default) | RW | 1 |
| 3 | CLOCKSUSPENDM | Active low clock suspend. Valid only in Serial Modes. Powers down the internal clock circuitry only. Valid only when SuspendM = 1b. The PHY must ignore ClockSuspend when SuspendM = 0b. By default, the clock will not be powered in Serial and Carkit Modes. 0b : Clock will not be powered in Serial and UART Modes. 1b : Clock will be powered in Serial and UART Modes. | RW | 0 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|--|------|-------|
| 2 | CARKITMODE | Changes the ULPI interface to UART interface. The PHY automatically clear this field when UART mode is exited. 0b: UART disabled. 1b: Enable serial UART mode. | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | Changes the ULPI interface to 3-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 4-pin serial interface | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | Changes the ULPI interface to 6-pin Serial. The PHY must automatically clear this field when serial mode is exited. 0b: FS/LS packets are sent using parallel interface 1b: FS/LS packets are sent using 6-pin serial interface | RW | 0 |

9.1.9 IFC_CTRL_SET

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x08 | | |
| PHYSICAL ADDRESS | 0x08 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the ifc_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------|-------------------|---------------------|------------|---------------|------------|---------------------|---------------------|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------------|-------------|------|-------|
| 7 | INTERFACE_PROTECT_DISABLE | | RW | 0 |
| 6 | INDICATORPASSTHRU | | RW | 0 |
| 5 | INDICATORCOMPLEMENT | | RW | 0 |
| 4 | AUTORESUME | | RW | 1 |
| 3 | CLOCKSUSPENDM | | RW | 0 |
| 2 | CARKITMODE | | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | | R | 0 |

9.1.10 IFC_CTRL_CLR

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x09 | | |
| PHYSICAL ADDRESS | 0x09 | INSTANCE | USB_SCUSB |
| DESCRIPTION | <p>This register doesn't physically exist.</p> <p>It is the same as the ifc_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action).</p> | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------------------|-------------------|---------------------|------------|---------------|------------|---------------------|---------------------|
| INTERFACE_PROTECT_DISABLE | INDICATORPASSTHRU | INDICATORCOMPLEMENT | AUTORESUME | CLOCKSUSPENDM | CARKITMODE | FSLSSERIALMODE_3PIN | FSLSSERIALMODE_6PIN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------------|-------------|------|-------|
| 7 | INTERFACE_PROTECT_DISABLE | | RW | 0 |
| 6 | INDICATORPASSTHRU | | RW | 0 |
| 5 | INDICATORCOMPLEMENT | | RW | 0 |
| 4 | AUTORESUME | | RW | 1 |
| 3 | CLOCKSUSPENDM | | RW | 0 |
| 2 | CARKITMODE | | RW | 0 |
| 1 | FSLSSERIALMODE_3PIN | | RW | 0 |
| 0 | FSLSSERIALMODE_6PIN | | R | 0 |

9.1.11 OTG_CTRL

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x0A | | |
| PHYSICAL ADDRESS | 0x0A | INSTANCE | USB_SCUSB |
| DESCRIPTION | Controls UTMI+ OTG functions of the PHY. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|-----------------|---------|----------|-------------|------------|------------|----------|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------------------|---|------|-------|
| 7 | USEEXTERNALVBUSINDICATOR | Tells the PHY to use an external VBUS over-current indicator. 0b: Use the internal OTG comparator (VA_VBUS_VLD) or internal VBUS valid indicator (default) 1b: Use external VBUS valid indicator signal. | RW | 0 |
| 6 | DRVVBUSEXTERNAL | Selects between the internal and the external 5 V VBUS supply. 0b: Pin17 (CPEN) is disabled (output GND level). TUSB1210 does not support internal VBUS supply. 1b: Pin17 (CPEN) is set to '1' (output VDD33 voltage level) if DRVVBUS bit is '1', else Pin17 (CPEN) is disabled (output GND level) if DRVVBUS bit is '0' | RW | 0 |
| 5 | DRVVBUS | VBUS output control bit 0b : do not drive VBUS 1b : drive 5V on VBUS Note: Both DRVVBUS and DRVVBUSEXTERNAL bits must be set to 1 in order to to set Pin17 (CPEN). CPEN pin can be used to enable an external VBUS supply | RW | 0 |
| 4 | CHRGVBUS | Charge VBUS through a resistor. Used for VBUS pulsing SRP. The Link must first check that VBUS has been discharged (see DischrgVbus register bit), and that both D+ and D- data lines have been low (SE0) for 2ms. 0b : do not charge VBUS 1b : charge VBUS | RW | 0 |
| 3 | DISCHRGVBUS | Discharge VBUS through a resistor. If the Link sets this bit to 1, it waits for an RX CMD indicating SessEnd has transitioned from 0 to 1, and then resets this bit to 0 to stop the discharge. 0b : do not discharge VBUS 1b : discharge VBUS | RW | 0 |
| 2 | DMPULLDOWN | Enables the 15k Ohm pull-down resistor on D-. 0b : Pull-down resistor not connected to D-. 1b : Pull-down resistor connected to D-. | RW | 1 |
| 1 | DPPULLDOWN | Enables the 15k Ohm pull-down resistor on D+. 0b : Pull-down resistor not connected to D+. 1b : Pull-down resistor connected to D+. | RW | 1 |
| 0 | IDPULLUP | Connects a pull-up to the ID line and enables sampling of the signal level. 0b : Disable sampling of ID line. 1b : Enable sampling of ID line. | RW | 0 |

9.1.12 OTG_CTRL_SET

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x0B | | |
| PHYSICAL ADDRESS | 0x0B | INSTANCE | USB_SCUSB |
| DESCRIPTION | <p>This register doesn't physically exist.</p> <p>It is the same as the otg_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action).</p> | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|-----------------|---------|----------|-------------|------------|------------|----------|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------------------|-------------|------|-------|
| 7 | USEEXTERNALVBUSINDICATOR | | RW | 0 |
| 6 | DRVVBUSEXTERNAL | | RW | 0 |
| 5 | DRVVBUS | | RW | 0 |
| 4 | CHRGVBUS | | RW | 0 |
| 3 | DISCHRGVBUS | | RW | 0 |
| 2 | DMPULLDOWN | | RW | 1 |
| 1 | DPPULLDOWN | | RW | 1 |
| 0 | IDPULLUP | | RW | 0 |

9.1.13 OTG_CTRL_CLR

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x0C | | |
| PHYSICAL ADDRESS | 0x0C | INSTANCE | USB_SCUSB |
| DESCRIPTION | <p>This register doesn't physically exist.</p> <p>It is the same as the otg_ctrl register with read/Clear-only property (write '1' to clear a particular bit, a write '0' has no-action).</p> | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------------|-----------------|---------|----------|-------------|------------|------------|----------|
| USEEXTERNALVBUSINDICATOR | DRVVBUSEXTERNAL | DRVVBUS | CHRGVBUS | DISCHRGVBUS | DMPULLDOWN | DPPULLDOWN | IDPULLUP |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------------------|-------------|------|-------|
| 7 | USEEXTERNALVBUSINDICATOR | | RW | 0 |
| 6 | DRVVBUSEXTERNAL | | RW | 0 |
| 5 | DRVVBUS | | RW | 0 |
| 4 | CHRGVBUS | | RW | 0 |
| 3 | DISCHRGVBUS | | RW | 0 |
| 2 | DMPULLDOWN | | RW | 1 |
| 1 | DPPULLDOWN | | RW | 1 |
| 0 | IDPULLUP | | RW | 0 |

9.1.14 USB_INT_EN_RISE

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x0D | | |
| PHYSICAL ADDRESS | 0x0D | INSTANCE | USB_SCUSB |
| DESCRIPTION | If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|-------------|----------------|----------------|---------------------|
| Reserved | Reserved | Reserved | IDGND_RISE | SESEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|-------------|--|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | Generate an interrupt event notification when IdGnd changes from low to high. | RW | 1 |
| | | Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. | | |
| 3 | SESEND_RISE | Generate an interrupt event notification when SessEnd changes from low to high. | RW | 1 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|---|------|-------|
| 2 | SESSVALID_RISE | Generate an interrupt event notification when SessValid changes from low to high. SessValid is the same as UTMI+ AValid. | RW | 1 |
| 1 | VBUSVALID_RISE | Generate an interrupt event notification when VbusValid changes from low to high. | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | Generate an interrupt event notification when Hostdisconnect changes from low to high. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). | RW | 1 |

9.1.15 USB_INT_EN_RISE_SET

| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x0E | | |
| PHYSICAL ADDRESS | 0x0E | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|--------------|----------------|----------------|---------------------|
| Reserved | Reserved | Reserved | IDGND_RISE | SESSEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | | RW | 1 |
| 3 | SESSEND_RISE | | RW | 1 |
| 2 | SESSVALID_RISE | | RW | 1 |
| 1 | VBUSVALID_RISE | | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | | RW | 1 |

9.1.16 USB_INT_EN_RISE_CLR

| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x0F | | |
| PHYSICAL ADDRESS | 0x0F | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the usb_int_en_rise register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|-------------|----------------|----------------|---------------------|
| Reserved | Reserved | Reserved | IDGND_RISE | SESEND_RISE | SESSVALID_RISE | VBUSVALID_RISE | HOSTDISCONNECT_RISE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_RISE | | RW | 1 |
| 3 | SESEND_RISE | | RW | 1 |
| 2 | SESSVALID_RISE | | RW | 1 |
| 1 | VBUSVALID_RISE | | RW | 1 |
| 0 | HOSTDISCONNECT_RISE | | RW | 1 |

9.1.17 USB_INT_EN_FALL

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x10 | | |
| PHYSICAL ADDRESS | 0x10 | INSTANCE | USB_SCUSB |
| DESCRIPTION | If set, the bits in this register cause an interrupt event notification to be generated when the corresponding PHY signal changes from low to high. By default, all transitions are enabled. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|-------------|----------------|----------------|---------------------|
| Reserved | Reserved | Reserved | IDGND_FALL | SESEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|----------------|---|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | Generate an interrupt event notification when IdGnd changes from high to low. Event is automatically masked if IdPullup bit is clear to 0 and for 50ms after IdPullup is set to 1. | RW | 1 |
| 3 | SESEND_FALL | Generate an interrupt event notification when SessEnd changes from high to low. | RW | 1 |
| 2 | SESSVALID_FALL | Generate an interrupt event notification when SessValid changes from high to low. SessValid is the same as UTMI+ AValid. | RW | 1 |
| 1 | VBUSVALID_FALL | Generate an interrupt event notification when VbusValid changes from high to low. | RW | 1 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|---|------|-------|
| 0 | HOSTDISCONNECT_FALL | Generate an interrupt event notification when Hostdisconnect changes from high to low. Applicable only in host mode (DpPulldown and DmPulldown both set to 1b). | RW | 1 |

9.1.18 USB_INT_EN_FALL_SET

| | | | |
|------------------|--|----------|-----------|
| ADDRESS OFFSET | 0x11 | | |
| PHYSICAL ADDRESS | 0x11 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action) | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|------------|-------------|----------------|----------------|---------------------|
| Reserved | Reserved | Reserved | IDGND_FALL | SESEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | | RW | 1 |
| 3 | SESEND_FALL | | RW | 1 |
| 2 | SESSVALID_FALL | | RW | 1 |
| 1 | VBUSVALID_FALL | | RW | 1 |
| 0 | HOSTDISCONNECT_FALL | | RW | 1 |

9.1.19 USB_INT_EN_FALL_CLR

| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x12 | | |
| PHYSICAL ADDRESS | 0x12 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the usb_int_en_fall register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|----------|----------|----------|------------|--------------|----------------|----------------|---------------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | IDGND_FALL | SESSEND_FALL | SESSVALID_FALL | VBUSVALID_FALL | HOSTDISCONNECT_FALL |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|---------------------|-------------|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_FALL | | RW | 1 |
| 3 | SESSEND_FALL | | RW | 1 |
| 2 | SESSVALID_FALL | | RW | 1 |
| 1 | VBUSVALID_FALL | | RW | 1 |
| 0 | HOSTDISCONNECT_FALL | | RW | 1 |

9.1.20 USB_INT_STS

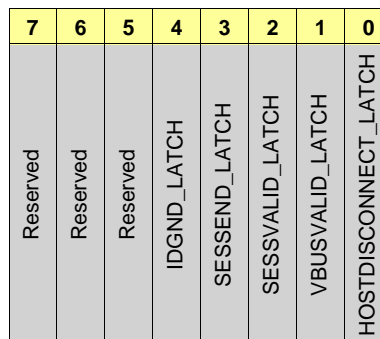
| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x13 | | |
| PHYSICAL ADDRESS | 0x13 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Indicates the current value of the interrupt source signal. | | |
| TYPE | R | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|----------|----------|----------|-------|---------|-----------|-----------|----------------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | IDGND | SESSEND | SESSVALID | VBUSVALID | HOSTDISCONNECT |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|----------------|---|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND | Current value of UTMI+ IdGnd output. This bit is not updated if IdPullup bit is reset to 0 and for 50 ms after IdPullup is set to 1. | R | 0 |
| 3 | SESEND | Current value of UTMI+ SessEnd output. | R | 0 |
| 2 | SESSVALID | Current value of UTMI+ SessValid output. SessValid is the same as UTMI+ AValid. | R | 0 |
| 1 | VBUSVALID | Current value of UTMI+ VbusValid output. | R | 0 |
| 0 | HOSTDISCONNECT | Current value of UTMI+ Hostdisconnect output. Applicable only in host mode. Automatically reset to 0 when Low Power Mode is entered. NOTE: Reset value is '0' when host is connected. Reset value is '1' when host is disconnected. | R | 0 |

9.1.21 USB_INT_LATCH

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x14 | | |
| PHYSICAL ADDRESS | 0x14 | INSTANCE | USB_SCUSB |
| DESCRIPTION | <p>These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial Mode or CarKit Mode is entered regardless of the value of ClockSuspendM.</p> <p>The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit. It is important to note that if register read data is returned to the Link in the same cycle that a USB Interrupt Latch bit is to be set, the interrupt condition is given immediately in the register read data and the Latch bit is not set.</p> <p>Note that it is optional for the Link to read the USB Interrupt Latch register in Synchronous Mode because the RX CMD byte already indicates the interrupt source directly</p> | | |
| TYPE | R | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|-------------|---|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | IDGND_LATCH | Set to 1 by the PHY when an unmasked event occurs on IdGnd. Cleared when this register is read. | R | 0 |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|----------------------|---|------|-------|
| 3 | SESEND_LATCH | Set to 1 by the PHY when an unmasked event occurs on SessEnd. Cleared when this register is read. | R | 0 |
| 2 | SESSVALID_LATCH | Set to 1 by the PHY when an unmasked event occurs on SessValid. Cleared when this register is read. SessValid is the same as UTMI+ AValid. | R | 0 |
| 1 | VBUSVALID_LATCH | Set to 1 by the PHY when an unmasked event occurs on VbusValid. Cleared when this register is read. | R | 0 |
| 0 | HOSTDISCONNECT_LATCH | Set to 1 by the PHY when an unmasked event occurs on Hostdisconnect. Cleared when this register is read. Applicable only in host mode. NOTE: As this IT is enabled by default, the reset value depends on the host status Reset value is '0' when host is connected. Reset value is '1' when host is disconnected. | R | 0 |

9.1.22 DEBUG

| | | | |
|------------------|--|----------|-----------|
| ADDRESS OFFSET | 0x15 | | |
| PHYSICAL ADDRESS | 0x15 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Indicates the current value of various signals useful for debugging. | | |
| TYPE | R | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|----------|----------|----------|----------|----------|-----------|
| Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | Reserved | LINESTATE |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|--|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | Reserved | | R | 0 |
| 5 | Reserved | | R | 0 |
| 4 | Reserved | | R | 0 |
| 3 | Reserved | | R | 0 |
| 2 | Reserved | | R | 0 |
| 1:00 | LINESTATE | These signals reflect the current state of the single ended receivers. They directly reflect the current state of the DP (LineState[0]) and DM (LineState[1]) signals. Read 0x0: SE0 (LS/FS), Squelch (HS/Chirp) Read 0x1: LS: 'K' State, FS: 'J' State, HS: !Squelch, Chirp: !Squelch & HS_Differential_Receiver_Output Read 0x2: LS: 'J' State, FS: 'K' State, HS: Invalid, Chirp: !Squelch & !HS_Differential_Receiver_Output Read 0x3: SE1 (LS/FS), Invalid (HS/Chirp) | R | 0x0 |

9.1.23 SCRATCH_REG

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x16 | | |
| PHYSICAL ADDRESS | 0x16 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Empty register byte for testing purposes. Software can read, write, set, and clear this register and the PHY functionality will not be affected. | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|---------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|---------------|------|-------|
| 7:00 | SCRATCH | Scratch data. | RW | 0x00 |

9.1.24 SCRATCH_REG_SET

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x17 | | |
| PHYSICAL ADDRESS | 0x17 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the scratch_reg register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|---------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | SCRATCH | | RW | 0x00 |

9.1.25 SCRATCH_REG_CLR

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x18 | | |
| PHYSICAL ADDRESS | 0x18 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the scratch_reg with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|---------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SCRATCH | | | | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|-------------|------|-------|
| 7:00 | SCRATCH | | RW | 0x00 |

9.1.26 VENDOR_SPECIFIC1

| | | | |
|-------------------------|--------------------------|-----------------|-----------|
| ADDRESS OFFSET | 0x3D | | |
| PHYSICAL ADDRESS | 0x3D | INSTANCE | USB_SCUSB |
| DESCRIPTION | Power Control register . | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------------|-------------|-----------|-------------|-------------|-------|-------------------|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|-------------------|--|------|-------|
| 7 | SPARE | Reserved. The link must never write a 1b to this bit. | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on MNTR_VUSBIN_OK. This bit is provided for debugging purposes. | RW | 0 |
| 5 | ID_FLOAT_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_FLOAT. This bit is provided for debugging purposes. | RW | 0 |
| 4 | ID_RES_EN | When set to 1, it enables RX CMDs for high to low or low to high transitions on ID_RESA, ID_RESB and ID_RESC. This bit is provided for debugging purposes. | RW | 0 |
| 3 | BVALID_FALL | Enables RX CMDs for high to low transitions on BVALID. When BVALID changes from high to low, the USB TRANS will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default. | RW | 0 |
| 2 | BVALID_RISE | Enables RX CMDs for low to high transitions on BVALID. When BVALID changes from low to high, the USB Trans will send an RX CMD to the link with the alt_int bit set to 1b. This bit is optional and is not necessary for OTG devices. This bit is provided for debugging purposes. Disabled by default. | RW | 0 |
| 1 | SPARE | Reserved. The link must never write a 1b to this bit. | RW | 0 |
| 0 | ABNORMALSTRESS_EN | When set to 1, it enables RX CMDs for low to high and high to low transitions on ABNORMALSTRESS. This bit is provided for debugging purposes. | RW | 0 |

9.1.27 VENDOR_SPECIFIC1_SET

| | | | |
|-------------------------|---|-----------------|-----------|
| ADDRESS OFFSET | 0x3E | | |
| PHYSICAL ADDRESS | 0x3E | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the func_ctrl register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------------|-------------|-----------|-------------|-------------|-------|-------------------|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|-------------------|-------------|------|-------|
| 7 | SPARE | | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | | RW | 0 |
| 5 | ID_FLOAT_EN | | RW | 0 |
| 4 | ID_RES_EN | | RW | 0 |
| 3 | BVALID_FALL | | RW | 0 |
| 2 | BVALID_RISE | | RW | 0 |
| 1 | SPARE | | RW | 0 |
| 0 | ABNORMALSTRESS_EN | | RW | 0 |

9.1.28 VENDOR_SPECIFIC1_CLR

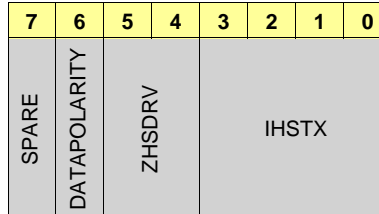
| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x3F | | |
| PHYSICAL ADDRESS | 0x3F | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the func_ctrl register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------|-------------------|-------------|-----------|-------------|-------------|-------|-------------------|
| SPARE | MNTR_VUSBIN_OK_EN | ID_FLOAT_EN | ID_RES_EN | BVALID_FALL | BVALID_RISE | SPARE | ABNORMALSTRESS_EN |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|-------------------|-------------|------|-------|
| 7 | SPARE | | RW | 0 |
| 6 | MNTR_VUSBIN_OK_EN | | RW | 0 |
| 5 | ID_FLOAT_EN | | RW | 0 |
| 4 | ID_RES_EN | | RW | 0 |
| 3 | BVALID_FALL | | RW | 0 |
| 2 | BVALID_RISE | | RW | 0 |
| 1 | SPARE | | RW | 0 |
| 0 | ABNORMALSTRESS_EN | | RW | 0 |

9.1.29 VENDOR_SPECIFIC2

| | | | |
|------------------|--|----------|-----------|
| ADDRESS OFFSET | 0x80 | | |
| PHYSICAL ADDRESS | 0x80 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Eye diagram programmability and DP/DM swap control . | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------|--|------|-------|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | Control data polarity on dp/dm | RW | 1 |
| 5:04 | ZHSDRV | High speed output impedance configuration for eye diagram tuning : 00 45.455 Ω 01 43.779 Ω 10 42.793 Ω 11 42.411 Ω | RW | 0x0 |
| 3:00 | IHSTX | High speed output drive strength configuration for eye diagram tuning : 0000 17.928 mA 0001 18.117 mA 0010 18.306 mA 0011 18.495 mA 0100 18.683 mA 0101 18.872 mA 0110 19.061 mA 0111 19.249 mA 1000 19.438 mA 1001 19.627 mA 1010 19.816 mA 1011 20.004 mA 1100 20.193 mA 1101 20.382 mA 1110 20.570 mA 1111 20.759 mA IHSTX[0] is also the AC BOOST enable IHSTX[0] = 0 à AC BOOST is disabled IHSTX[0] = 1 à AC BOOST is enabled | RW | 0x1 |

9.1.30 VENDOR_SPECIFIC2_SET

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x81 | | |
| PHYSICAL ADDRESS | 0x81 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/set-only property (write '1' to set a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|-------|--------------|--------|-------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPARE | DATAPOLARITY | ZHSDRV | IHSTX | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------|-------------|------|-------|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | | RW | 1 |
| 5:04 | ZHSDRV | | RW | 0x0 |
| 3:00 | IHSTX | | RW | 0x1 |

9.1.31 VENDOR_SPECIFIC2_CLR

| | | | |
|-------------------------|--|-----------------|-----------|
| ADDRESS OFFSET | 0x82 | | |
| PHYSICAL ADDRESS | 0x82 | INSTANCE | USB_SCUSB |
| DESCRIPTION | This register doesn't physically exist. It is the same as the VENDOR_SPECIFIC1 register with read/clear-only property (write '1' to clear a particular bit, a write '0' has no-action). | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

| | | | | | | | |
|-------|--------------|--------|-------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| SPARE | DATAPOLARITY | ZHSDRV | IHSTX | | | | |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------|-------------|------|-------|
| 7 | SPARE | | RW | 0 |
| 6 | DATAPOLARITY | | RW | 1 |
| 5:04 | ZHSDRV | | RW | 0x0 |
| 3:00 | IHSTX | | RW | 0x1 |

9.1.32 VENDOR_SPECIFIC1_STS

| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x83 | | |
| PHYSICAL ADDRESS | 0x83 | INSTANCE | USB_SCUSB |
| DESCRIPTION | Indicates the current value of the interrupt source signal. | | |
| TYPE | R | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------------|--------------------|--------------|-------------|-------------|-------------|------------|
| Reserved | MNTR_VUSBIN_OK_STS | ABNORMALSTRESS_STS | ID_FLOAT_STS | ID_RESC_STS | ID_RESB_STS | ID_RESA_STS | BVALID_STS |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------------|--|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | MNTR_VUSBIN_OK_STS | Current value of MNTR_VUSBIN_OK output | R | 0 |
| 5 | ABNORMALSTRESS_STS | Current value of ABNORMALSTRESS output | R | 0 |
| 4 | ID_FLOAT_STS | Current value of ID_FLOAT output | R | 0 |
| 3 | ID_RESC_STS | Current value of ID_RESC output | R | 0 |
| 2 | ID_RESB_STS | Current value of ID_RESB output | R | 0 |
| 1 | ID_RESA_STS | Current value of ID_RESA output | R | 0 |
| 0 | BVALID_STS | Current value of VB_SESS_VLD output | R | 0 |

9.1.33 VENDOR_SPECIFIC1_LATCH

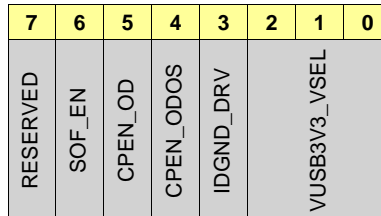
| | | | |
|------------------|---|----------|-----------|
| ADDRESS OFFSET | 0x84 | | |
| PHYSICAL ADDRESS | 0x84 | INSTANCE | USB_SCUSB |
| DESCRIPTION | <p>These bits are set by the PHY when an unmasked change occurs on the corresponding internal signal. The PHY will automatically clear all bits when the Link reads this register, or when Low Power Mode is entered. The PHY also clears this register when Serial mode is entered regardless of the value of ClockSuspendM.</p> <p>The PHY follows the rules defined in Table 26 of the ULPI spec for setting any latch register bit.</p> | | |
| TYPE | R | | |
| WRITE LATENCY | | | |

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------------------|----------------------|----------------|---------------|---------------|---------------|--------------|
| Reserved | MNTR_VUSBIN_OK_LATCH | ABNORMALSTRESS_LATCH | ID_FLOAT_LATCH | ID_RESC_LATCH | ID_RESB_LATCH | ID_RESA_LATCH | BVALID_LATCH |

| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|----------------------|---|------|-------|
| 7 | Reserved | | R | 0 |
| 6 | MNTR_VUSBIN_OK_LATCH | Set to 1 when an unmasked event occurs on MNTR_VUSBIN_OK_LATCH. Clear on read register. | R | 0 |
| 5 | ABNORMALSTRESS_LATCH | Set to 1 when an unmasked event occurs on ABNORMALSTRESS. Clear on read register. | R | 0 |
| 4 | ID_FLOAT_LATCH | Set to 1 when an unmasked event occurs on ID_FLOAT. Clear on read register. | R | 0 |
| 3 | ID_RESC_LATCH | Set to 1 when an unmasked event occurs on ID_RESC. Clear on read register. | R | 0 |
| 2 | ID_RESB_LATCH | Set to 1 when an unmasked event occurs on ID_RESB. Clear on read register. | R | 0 |
| 1 | ID_RESA_LATCH | Set to 1 when an unmasked event occurs on ID_RESA. Clear on read register. | R | 0 |
| 0 | BVALID_LATCH | Set to 1 when an unmasked event occurs on VB_SESS_VLD. Clear on read register. | R | 0 |

9.1.34 VENDOR_SPECIFIC3

| | | | |
|------------------|------|----------|-----------|
| ADDRESS OFFSET | 0x85 | | |
| PHYSICAL ADDRESS | 0x85 | INSTANCE | USB_SCUSB |
| DESCRIPTION | | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

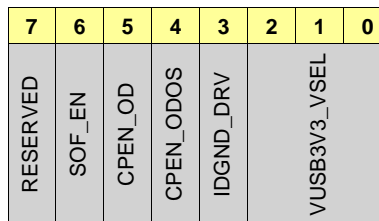


| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|------------|---|------|-------|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | 0: HS USB SOF detector disabled. 1: Enable HS USB SOF detection when PHY is set in device mode. SOF are output on CPEN pin. HS USB SOF (start-of-frame) output clock is available on CPEN pin when this bit is set. HS USB SOF packet rate is 8 kHz. This bit is provided for debugging purpose only. It must never be write to '1' in functional mode | RW | 0 |
| 5 | CPEN_OD | This bit has no effect when CPEN_ODOS = '0', else : 0: CPEN pad is in OS (Open Source) mode. In this case CPEN pin has an internal NMOS driver, and will be active LOW. Externally there should be a pullup resistor on CPEN (min 1kohm) to a supply voltage (max 3.6V). 1: CPEN pad is in OD (Open Drain) mode In this case CPEN pin has an internal PMOS driver, and will be active HIGH. Externally there should be a pull-down resistor on CPEN (min 1 kΩ to GND. | RW | 0 |

| | | | | |
|------|--------------|--|----|-----|
| 4 | CPEN_ODOS | Mode selection bit for CPEN pin. 0 : CPEN pad is in CMOS mode 1: CPEN pad is in OD (Open Drain) or OS (Open Source) mode (controlled by CPEN_OD bit) | RW | 0 |
| 3 | IDGND_DRV | Drives ID pin to ground | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | 000 VRUSB3P1V = 2.5 V 001 VRUSB3P1V = 2.75 V 010 VRUSB3P1V = 3.0 V 011 VRUSB3P1V = 3.10 V (default) 100 VRUSB3P1V = 3.20 V 101 VRUSB3P1V = 3.30 V 110 VRUSB3P1V = 3.40 V 111 VRUSB3P1V = 3.50 V | RW | 0x3 |

9.1.35 VENDOR_SPECIFIC3_SET

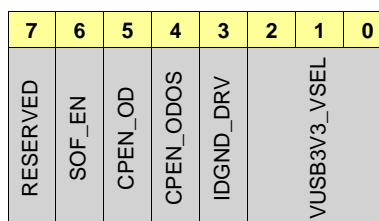
| | | | |
|------------------|------|----------|-----------|
| ADDRESS OFFSET | 0x86 | | |
| PHYSICAL ADDRESS | 0x86 | INSTANCE | USB_SCUSB |
| DESCRIPTION | | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |



| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------|-------------|------|-------|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | | RW | 0 |
| 5 | CPEN_OD | | RW | 0 |
| 4 | CPEN_ODOS | | RW | 0 |
| 3 | IDGND_DRV | | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | | RW | 0x3 |

9.1.36 VENDOR_SPECIFIC3_CLR

| | | | |
|------------------|------|----------|-----------|
| ADDRESS OFFSET | 0x87 | | |
| PHYSICAL ADDRESS | 0x87 | INSTANCE | USB_SCUSB |
| DESCRIPTION | | | |
| TYPE | RW | | |
| WRITE LATENCY | | | |

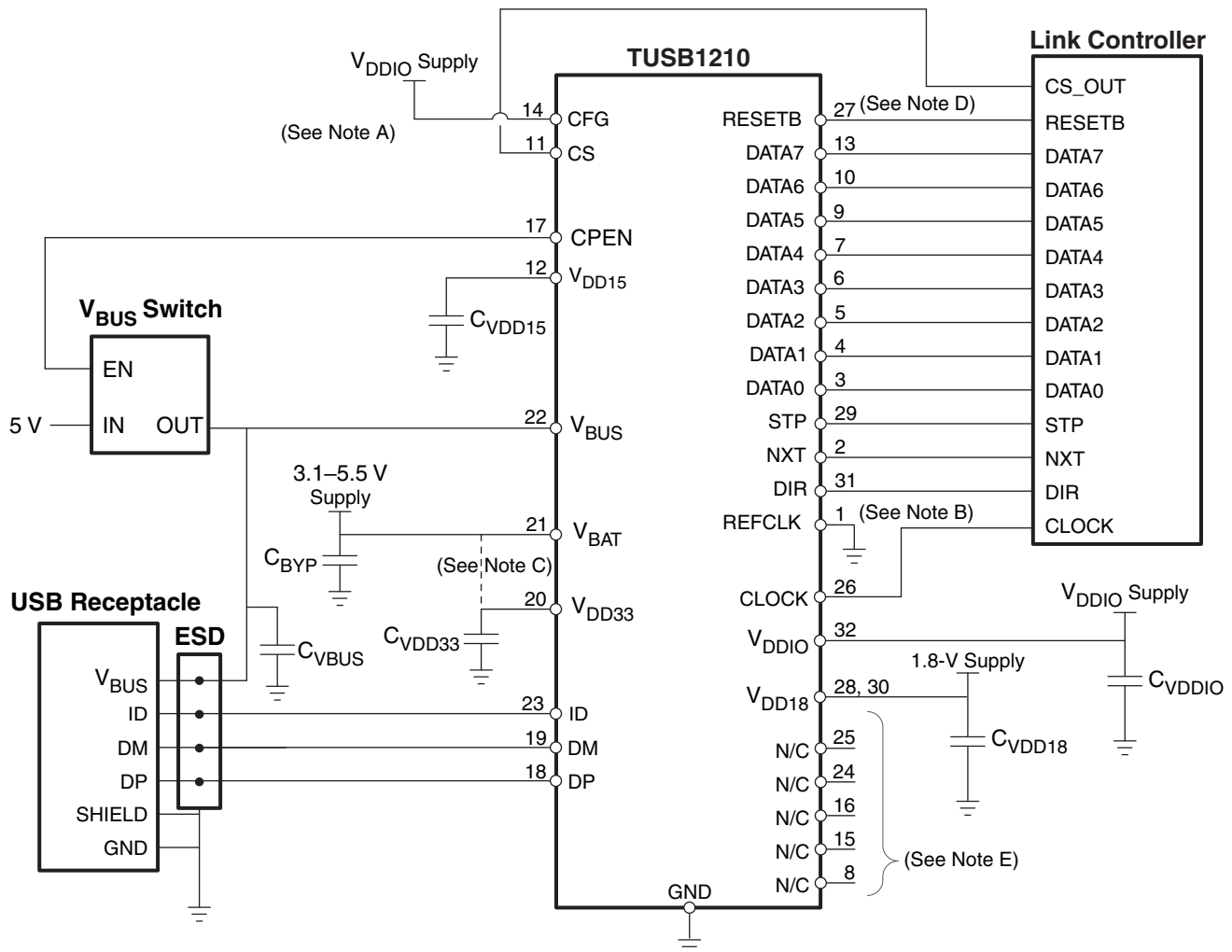


| BITS | FIELD NAME | DESCRIPTION | TYPE | RESET |
|------|--------------|-------------|------|-------|
| 7 | Reserved | | RW | 0 |
| 6 | SOF_EN | | RW | 0 |
| 5 | CPEN_OD | | RW | 0 |
| 4 | CPEN_ODOS | | RW | 0 |
| 3 | IDGND_DRV | | RW | 0x0 |
| 2:00 | VUSB3V3_VSEL | | RW | 0x3 |

10 Application Information

10.1 Host or OTG, ULPI Input Clock Mode Application

Figure 10-1 shows a suggested application diagram for TUSB1210 in the case of ULPI input-clock mode (60 MHz ULPI clock is provided by link processor), in Host or OTG application. Note this is just one example, it is of course possible to operate as HOST or OTG while also in ULPI output-clock mode.

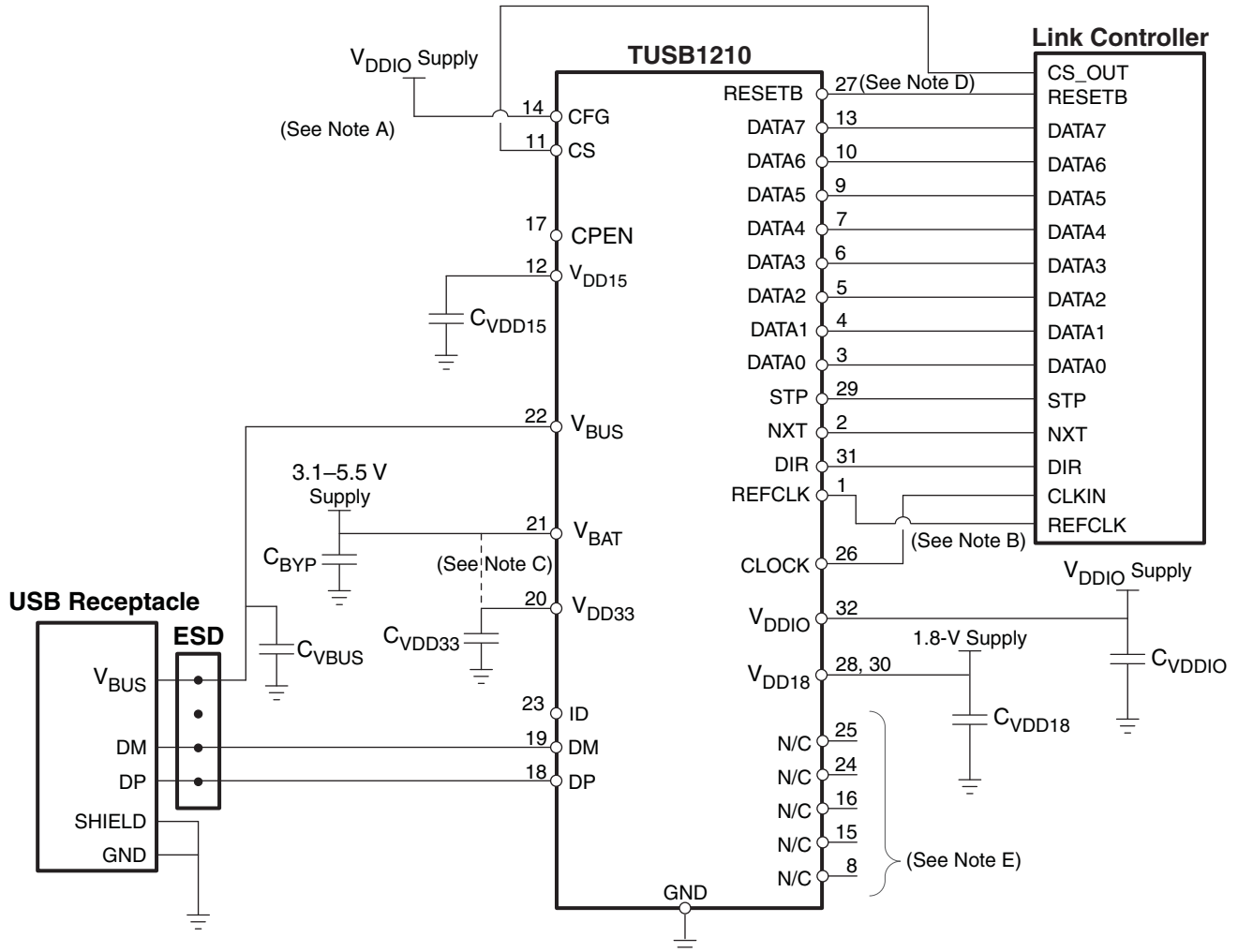


- A. Pin 11 (CS) : can be tied high to V_{IO} if CS_OUT pin unavailable; Pin 14 (CFG) : tie-high is Don't Care since ULPI clock is used in input mode
- B. Pin 1 (REFCLK) : must be tied low
- C. Ext 3 V supply supported
- D. Pin 27 (RESETB) can be tied to V_{DDIO} if unused.
- E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

Figure 10-1. Host or OTG, ULPI Input Clock Mode Application Diagram

10.2 Device, ULPI Output Clock Mode Application

Figure 10-2 shows a suggested application diagram for TUSB1210 in the case of ULPI output clock mode (60 MHz ULPI clock is provided by TUSB1210, while link processor or another external circuit provides REFCLK), in Device mode application. Note this is just one example, it is of course possible to operate as Device while also in ULPI input-clock mode. Refer also to Figure 10-1.



- A. Pin 11 (CS) : can be tied high to V_{IO} if CS_OUT pin unavailable; Pin 14 (CFG) : Tied to V_{DDIO} for 26MHz REFCLK mode here, tie to GND for 19.2MHz mode.
- B. Pin 1 (REFCLK) : connect to external 3.3V square-wave reference clock
- C. Ext 3 V supply supported
- D. Pin 27 (RESETB) can be tied to V_{DDIO} if unused.
- E. Pins labeled N/C (no-connect) are truly no-connect, and can be tied or left floating.

Figure 10-2. Device, ULPI Output Clock Mode Application Diagram

11 Glossary

| | |
|------------------|---|
| CMOS | Complimentary Metal Oxide Semiconductor |
| DM | Data manual |
| DSP | Digital signal processor |
| ESD | Electrostatic discharge |
| ESR | Equivalent series resistance |
| hiZ | High-impedance |
| HS | High speed |
| HW | Hardware |
| IC | Integrated circuit |
| ID | Identification |
| IDDQ | Direct drain quiescent current |
| IF | Interface |
| IO or I/O | Input/output |
| JTAG | Joint test action group, ieee 1149.1 standard |
| LDO | Low dropout regulator |
| LS | Low speed |
| NA | Not applicable |
| OTG | On the go |
| PBGA | Plastic ball grid array |
| PCB | Printed circuit board |
| PD | Pulldown |
| PLL | Phase locked loop |
| POL | Polarity |
| PSRR | Power supply rejection ratio |
| PU | Pullup |
| RX | Receive |
| SW | Software |

SYNC/SYNCHRO Synchronization

| | |
|-------------|---|
| SYS | System |
| TBD | To be defined |
| TRM | Technical reference manual |
| TX | Transmit |
| UART | Universal asynchronous receiver transmitter |
| ULPI | UTMI+ low pin interface |
| USB | Universal serial bus |
| UTMI | USB transceiver macrocell interface |

12 TUSB1210 Package

12.1 TUSB1210 Standard Package Symbolization

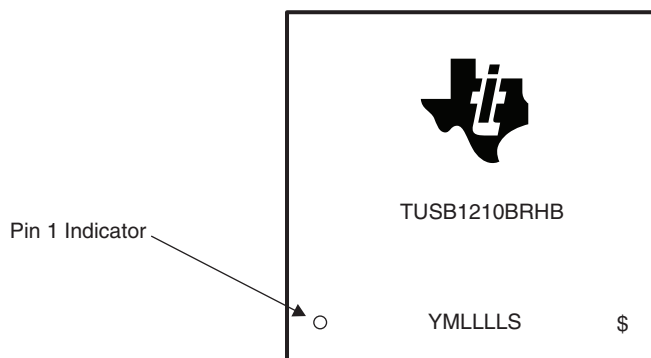


Figure 12-1. Printed Device Reference

Table 12-1. TUSB1210 Nomenclature Description

| FIELDS | MEANING |
|--------|---|
| P | Marking used to note prototype (X), preproduction (P), or qualified/production device (Blank)(1) |
| A | Mask set version descriptor (initial silicon = BLANK, first silicon revision = A, second silicon revision = B,...)(2) |
| YM | Year month |
| LLLLS | Lot code |
| \$ | Fab Planning Code |

12.2 Package Thermal Resistance Characteristics

Table 12-2 provides the thermal resistance characteristics for the recommended package type RHB (S-PQFP-N32) used for the TUSB1210 device. Refer to the application report *IC Package Thermal Metrics*, TI literature number [SPRA953](#), further details concerning parameter definitions and usage.

Table 12-2. TUSB1210 Thermal Resistance Characteristics

| PARAMETER | VALUE | UNIT | MEASUREMENT METHOD |
|--|-------|------|---|
| θ_{JA} Junction-to-ambient thermal resistance | 34.72 | °C/W | EIA/JESD 51-1 |
| θ_{JC} top Junction-to-case top thermal resistance ⁽¹⁾ | 37.3 | °C/W | No current JEDEC specification ⁽²⁾ |
| θ_{JC} bottom Junction-to-case bottom thermal resistance ⁽³⁾ | 3.6 | °C/W | No current JEDEC specification ⁽²⁾ |
| θ_{JB} Junction-to-board thermal resistance or junction-to-pin thermal resistance | 10.3 | °C/W | EIA/ JESD 51-8. |
| Ψ_{JT} Junction-to-top of package (not a true thermal resistance) | 0.5 | °C/W | EIA/JESD 51-2 |
| Ψ_{JB} Junction-to-board (not a true thermal resistance) | 10.5 | °C/W | EIA/JESD 51-6 |

(1) Top is surface of the package facing away from the PCB.

(2) Refer to measurement method in Chapter 2 of *IC Package Thermal Metrics*, TI literature number [SPRA953](#).

(3) Bottom surface is the surface of the package facing towards the PCB.

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/ Ball Finish | MSL Peak Temp ⁽³⁾ | Samples (Requires Login) |
|------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|-------------------|------------------------------|--------------------------|
| TUSB1210BRHBR | ACTIVE | QFN | RHB | 32 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |
| TUSB1210BRHBT | ACTIVE | QFN | RHB | 32 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR | |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



| | |
|----|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

TAPE AND REEL INFORMATION

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TUSB1210BRHBR | QFN | RHB | 32 | 3000 | 330.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TUSB1210BRHBT | QFN | RHB | 32 | 250 | 180.0 | 12.4 | 5.3 | 5.3 | 1.5 | 8.0 | 12.0 | Q2 |

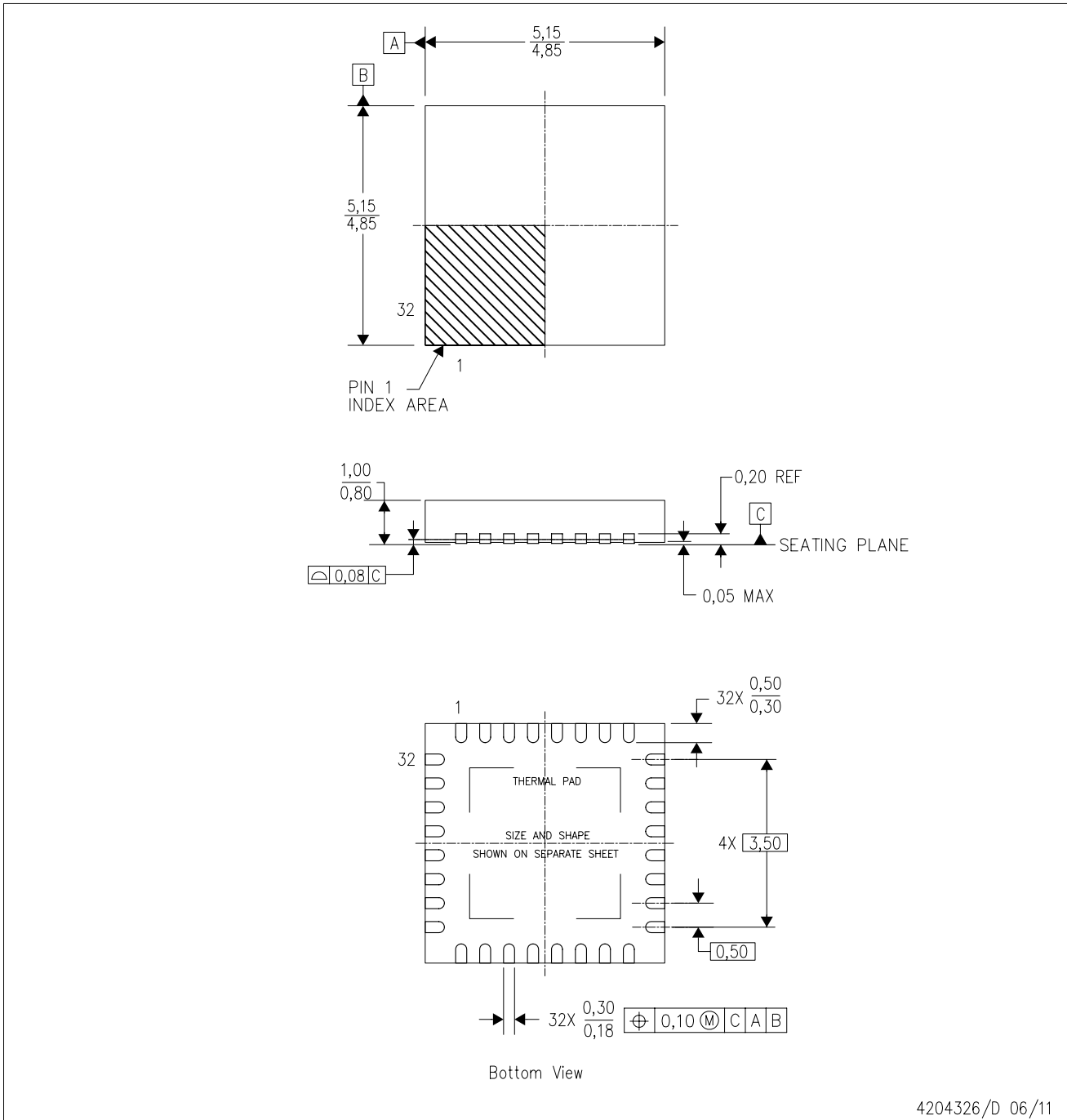
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TUSB1210BRHBR | QFN | RHB | 32 | 3000 | 367.0 | 367.0 | 35.0 |
| TUSB1210BRHBT | QFN | RHB | 32 | 250 | 210.0 | 185.0 | 35.0 |

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



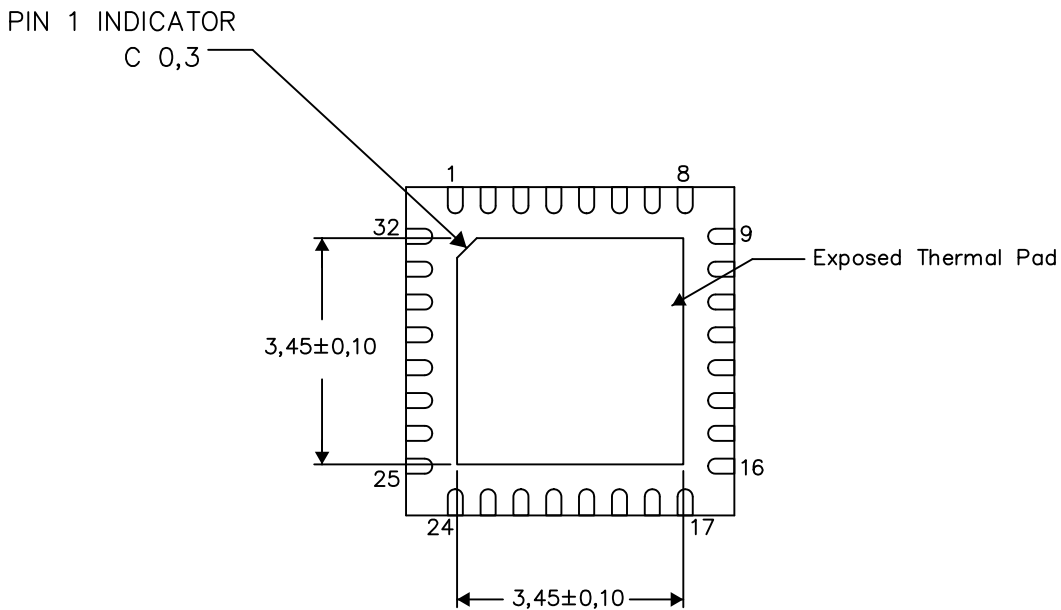
- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) Package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Falls within JEDEC MO-220.

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

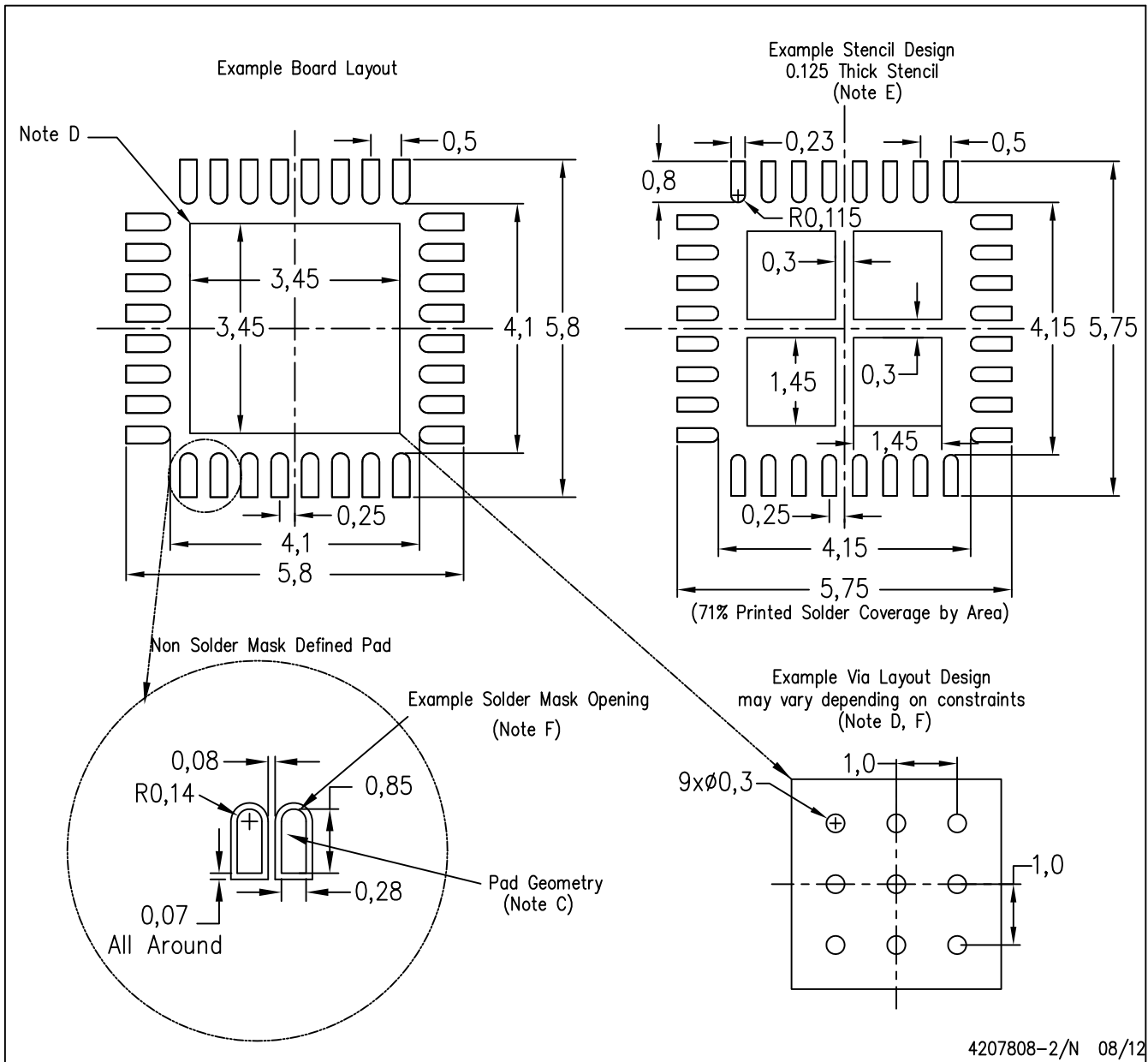
Exposed Thermal Pad Dimensions

4206356-2/W 09/12

NOTE: A. All linear dimensions are in millimeters

RHB (S-PVQFN-N32)

PLASTIC QUAD FLATPACK NO-LEAD



4207808-2/N 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as "components") are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI's terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers' products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers' products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI's goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or "enhanced plastic" are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have **not** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components which meet ISO/TS16949 requirements, mainly for automotive use. Components which have not been so designated are neither designed nor intended for automotive use; and TI will not be responsible for any failure of such components to meet such requirements.

Products

| | |
|------------------------------|--|
| Audio | www.ti.com/audio |
| Amplifiers | amplifier.ti.com |
| Data Converters | dataconverter.ti.com |
| DLP® Products | www.dlp.com |
| DSP | dsp.ti.com |
| Clocks and Timers | www.ti.com/clocks |
| Interface | interface.ti.com |
| Logic | logic.ti.com |
| Power Mgmt | power.ti.com |
| Microcontrollers | microcontroller.ti.com |
| RFID | www.ti-rfid.com |
| OMAP Applications Processors | www.ti.com/omap |
| Wireless Connectivity | www.ti.com/wirelessconnectivity |

Applications

| | |
|-------------------------------|--|
| Automotive and Transportation | www.ti.com/automotive |
| Communications and Telecom | www.ti.com/communications |
| Computers and Peripherals | www.ti.com/computers |
| Consumer Electronics | www.ti.com/consumer-apps |
| Energy and Lighting | www.ti.com/energy |
| Industrial | www.ti.com/industrial |
| Medical | www.ti.com/medical |
| Security | www.ti.com/security |
| Space, Avionics and Defense | www.ti.com/space-avionics-defense |
| Video and Imaging | www.ti.com/video |
| TI E2E Community | e2e.ti.com |

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2012, Texas Instruments Incorporated