![TEXAS INSTRUMENTS]

TPD4S014

COMPLETE PROTECTION SOLUTION FOR USB CHARGER PORT INCLUDING ESD PROTECTION FOR ALL LINES AND OVER-VOLTAGE PROTECTION ON VBUS

Check for Samples: TPD4S014

FEATURES

- **Input Voltage Protection at VBUS up to 28V**
- **Low Ron nFET Switch**
- **Supports >2A charging current**
- **Over Voltage and Under Voltage Lock Out Features**
- **Low Capacitance TVS ESD Clamp for USB2.0 High speed Data Rate**
- **Internal 16ms Startup Delay**
- **Integrated Input Enable and Status Output Signal**
- **Thermal Shutdown Feature**
- **ESD Performance D+/D–/ID/V_{BUS} Pins**
    - **±15-kV Contact Discharge (IEC 61000-4-2)**
    - **±15-kV Air Gap Discharge (IEC 61000-4-2)**
- **Space Saving QFN Package (2mm×2mm)**

APPLICATIONS

- **Cell Phones**
- **eBook**
- **Portable Media Players**
- **Digital Camera**

**DSQ PACKAGE
(TOP SIDE/SEE-THROUGH VIEW)**
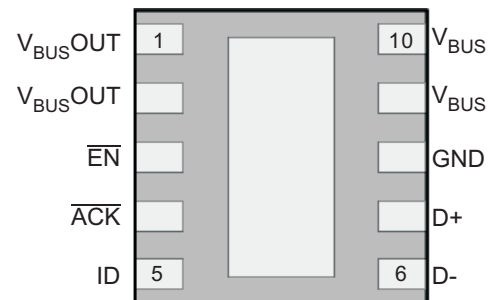
DESCRIPTION

The TPD4S014 is a single-chip solution for USB charger port protection. This device offers low capacitance TVS type ESD clamps for the D+, D- and standard Capacitance for the ID pin. On the VBUS pin, this device can handle over-voltage protection up to 28V. The over voltage lock-out feature ensures that if there is a fault condition at the VBUS line, the TPD4S014 is able to isolate the VBUS line and protects the internal circuitry from damage. There is a 16ms turn-on delay after VBUS crosses the under voltage lockout threshold, in order to let the voltage stabilize before closing the switch. This function acts as a deglitch and prevents unnecessary switching if there is any ringing on the line during connection.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.
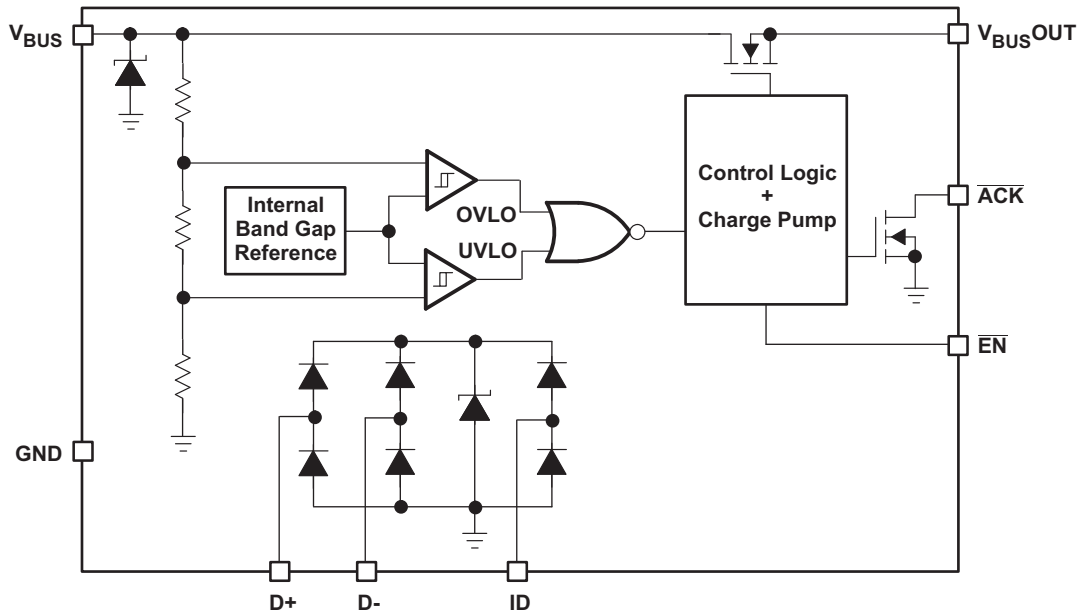
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

CIRCUIT SCHEMATIC DIAGRAM

DEVICE OPERATION

OTP	UVLO	OVLO	EN	SW	ACK
X	H	X	X	OFF	H
X	X	H	X	OFF	H
L	L	L	H	OFF	L
L	L	L	L	ON	L
H	X	X	X	OFF	H

OTP = Over temperature protection circuit active

UVLO = Under voltage lock-out circuit active

OVLO = Over voltage lock-out circuit active

SW = Load switch

CP = Charge pump

X = Don't Care

H = True

L = False

PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	NO.		
D–	6	I/O	USB data–
D+	7	I/O	USB data+
ID	5	I/O	USB ID signal
$\overline{ACK}$	4	O	Open-Drain Adapter-Voltage Indicator Output. ACOK is driven low after the VIN voltage is stable between UVLO and OVLO for 16ms (typ). Connect a pullup resistor from ACOK to the logic I/O voltage of the host system.
$\overline{EN}$	3	I	Enable Active-Low Input. Drive EN low to enable the switch. Drive EN high to disable the switch.
VBUS	9, 10	USB Input Power	USB connector VBUS
VBUS_OUT	1, 2	Power Output	Connect to PCB internal PCB plane
GND	8	Ground	Connect to PCB ground plane
Central PAD	Central PAD	Heat Sink	Electrically disconnected. Use as heat sink. Connect to GND plane via large PCB PAD

ABSOLUTE MAXIMUM RATINGS[(1)(2)]

over operating free-air temperature range (unless otherwise noted)

		VALUE		UNIT
		MIN	MAX	
Max Voltage on V_{BUS}		–0.5	30	V
Continuous current through NFET			2.6	A
Max Current through D+, D-, ID, VBUS ESD clamps			-50	mA
Continuous current through logic output		–50	50	mA
Maximum junction temperature		–40	150	°C
IEC 61000-4-2 Contact Discharge	D+, D–, ID, VBUS pins		±15	kV
IEC 61000-4-2 Air-gap Discharge	D+, D–, ID, VBUS pins		±15	kV
Human-Body Model	$\overline{EN}$, $\overline{ACK}$, VBUSOUT pins		±2	kV

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.

THERMAL INFORMATION

THERMAL METRIC[(1)]		TPD4S014	UNITS
		DSQ (10) PINS	
θ_{JA}	Junction-to-ambient thermal resistance	70.3	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	46.3	
θ_{JB}	Junction-to-board thermal resistance	33.8	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	33.5	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	16.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

ELECTRICAL CHARACTERISTICS, $\overline{EN}$, $\overline{ACK}$, D+, D–, ID Pins

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage $\overline{EN}$	Load current = 50 µA	1			V
V_{IL}	Low-level input voltage $\overline{EN}$	Load current = 50 µA			0.5	V
I_L	Input Leakage Current $\overline{EN}$, D+, D–, ID	V_I = 3.3 V			1.0	µA
V_{OL}	Low-level output voltage $\overline{ACK}$	I_{OL} = 2 mA			0.1	V
V_D	Diode forward Voltage D+, D–, ID pins; lower clamp diode	I_O = 8 mA			0.95	V
ΔC_{IO}	Differential Capacitance between the D+, D– lines			0.03		pF
C_{IO}	Capacitance to GND for the D+, D– lines			1.6		pF
$C_{IO\text{-}ID}$	Capacitance to GND for the ID line			19		pF
V_{RS}	Reverse stand-off voltage of D+, D- and ID pins			5		V
V_{BR}	Breakdown voltage D+, D–, ID pins	I_{br} = 1 mA	6			V
$V_{BR\ VBUS}$	Breakdown voltage on Vbus	I_{br} = 1 mA	28			V
R_{DYN}	Dynamic on resistance D+, D–, ID clamps	I_I = 1 Amps		1		Ω

ELECTRICAL CHARACTERISTICS OVP CIRCUITS

over operating free-air temperature range (unless otherwise noted)

	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT UNDERVOLTAGE LOCKOUT							
V_{UVLO+}	Under-voltage lock-out, input power detected threshold rising		VBUS increasing from 0V to 5V, No load on OUT pin	2.65	2.8	3	V
$V_{UVLO–}$	Under-voltage lock-out, input power detected threshold falling		VBUS decreasing from 5V to 0V, No load on OUT pin	2.25	2.44	2.7	V
$V_{HYS\text{-}UVLO}$	Hysteresis on UVLO		Δ of V_{UVLO+} and $V_{UVLO–}$	150	360	550	mV
INPUT TO OUTPUT CHARACTERISTICS							
$R_{DS\text{-}VBUSSWITCH}$	VBUS switch resistance		V_{BUS} = 5 V, I_{OUT} = 500 mA		151	200	mΩ
t_{ON}	Turn-ON time		R_L = 36 Ω, C_L = 10 uF	16	17.4	18	ms
t_{OFF}	Turn-OFF time		R_L = 36 Ω, C_L = 10 uF			8	µs
INPUT OVERVOLTAGE PROTECTION (OVP)							
V_{OVP+}	Input overvoltage protection threshold	VBUS	V_{BUS} increasing from 5 V to 7 V, No Load	5.9	6.15	6.45	V
V_{OVP-}	Input overvoltage protection threshold falling	VBUS	V_{BUS} decreasing from 7V to 5V, No Load	5.75	5.98	6.24	V
$V_{HYS\text{-}OVP}$	Hysteresis on OVP	VBUS	V_{BUS} decreasing from 7 V to 5 V, No Load	25	100	275	mV
$t_{d(OVP)}$	Max Overvoltage delay					11	µs
t_{REC}	Recovery time from input overvoltage condition	VBUS	Time measured from V_{BUS} 8 V ≥ 6 V, 1-µs fall-time		8	9	ms

SUPPLY CURRENT CONSUMPTION

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	TYP	MAX	UNIT
I_{VBUS}	VBUS Operating Current Consumption	No load on VBUS_OUT pin, V_{BUS} = 5 V, $\overline{EN}$ = 0 V	147.6	160	µA
I_{VBUS_OFF}	VBUS Operating Current Consumption	No load on VBUS_OUT pin, V_{BUS} = 5 V, $\overline{EN}$ = 5 V	111.8	120	µA
THERMAL SHUTDOWN FEATURE					
T_{SHDN}	Thermal Shutdown		144		°C
$T_{SHDN\text{-}HYS}$	Thermal-Shutdown Hysteresis		23		°C

GENERAL OPERATION

The TPD4S014 provides a single-chip protection solution for USB charger interfaces. The VBUS line is tolerant upto 28 V. A Low $R_{DS(on)}$ nFET switch is used to disconnect the downstream circuits in case of a fault condition. At power-up, when the voltage on VBUS is rising, the switch will close 16 ms after the input crosses the undervoltage threshold, thereby making power available to the downstream circuits. The TPD4S014 also has an $\overline{ACK}$ output, which deasserts to alert the system that a fault has occurred. The TPD4S014 offers 4 channel ESD clamps for D+, D-, ID, and VBUS pins that provide IEC61000-4-2 level 4 ESD protection. This eliminates the need for external TVS clamp circuits in the application.

The TPD4S014 has an internal oscillator and charge pump that controls the turn-on of the internal nFET switch. The internal oscillator controls the timers that enable the turn-on of the charge pump and sets the state of the open-drain $\overline{ACK}$ output. If $V_{BUS} < V_{UVLO}$ or if $V_{BUS} > V_{OVLO}$, the internal oscillator remains off, thus disabling the charge pump. The charge-pump at startup, after a 16ms internal delay, turns on the internal nFET switch and asserts $\overline{ACK}$. At any time, if V_{BUS} drops below V_{UVLO} or rises above V_{OVLO}, $\overline{ACK}$ is released and the nFET switch is disabled.

When the input voltage rises above $V_{OVP,}$ or drops below the V_{UVLO}, the internal V_{BUS} switch is turned off, removing power to the application. The $\overline{ACK}$ signal is asserted when a fault condition is detected. If the fault was an over voltage event, the V_{BUS} FET switch turns on 8ms after input voltage returns below $V_{OVP} - V_{HYS-OVP}$ and remains above VUVLO. If the fault was an under voltage event, the switch turns on 16ms after the voltage returns above V_{UVLO+} (similar to start up). When the switch turns on, the $\overline{ACK}$ is asserted once again.

A 16ms deglitch time has been introduced in to the turn on sequence to ensure that the input supply has stabilized before turning the switch ON. Noise on the Vbus line, could turn on the switch when the fault condition is still active. To avoid this, OVP glitch immunity allows noise on the VBUS line to be rejected. Such a glitch protection circuitry is also introduced in the turn off sequence in order to prevent the switch from turning off for voltage transients. The glitch protection circuitry integrates the glitch over time, allowing the OVP circuitry to trigger faster for larger voltage excursions above the OVP threshold and slower for shorter excursions. The protection circuitry has a maximum delay of 8 μs.

When the device is ON, current flowing through the device will cause the device to heat up. Over heating can lead to permanent damage to the device. To prevent this, an over temperature protection has been designed into the device. Whenever the junction temperature exceeds 145 °C, the switch will turn off, thereby limiting the temperature. The $\overline{ACK}$ signal will be asserted for an over temperature event. Once the device cools down to below 120 °C the $\overline{ACK}$ signal will be deasserted, and the switch will turn on if the $\overline{EN}$ is active and the VBUS voltage is within the UVLO and OVP thresholds. While the over temperature protection in the device will not kick-in unless the die temperature reaches 145 °C, It is generally recommended that care is taken to keep the junction temperature below 125 °C. Operation of the device above 125 °C for extended periods of time can affect the long-term reliability of the part.

The junction temperature of the device can be calculated using below formula:

$$T_j = T_a + P_D \theta_{JA}$$

(1)

T_j	=	Junction temperature
T_a	=	Ambient temperature
θ_{JA}	=	Thermal resistance
P_D	=	Power Dissipated in device

$$P_D = I^2 R_{on}$$

(2)

I	=	Current through device
R_{ON}	=	Max on resistance of device

Example

At 2A continuous current power dissipation is given by:

$$P_D = 2^2 \times 0.2 = 0.8W$$

If the ambient temperature is about 60oC the junction temperature will be:

$$T_j = 60 + (0.8 \times 70.3) = 116.24$$

This Implies that, at an ambient temperature of 60° Celcuis that TPD4S014 can pass a continuous of 2A with no problem. Conversely, the above calculation can also be used to calculate the total continuous current the TPD4S014 can handle at any given temperature.
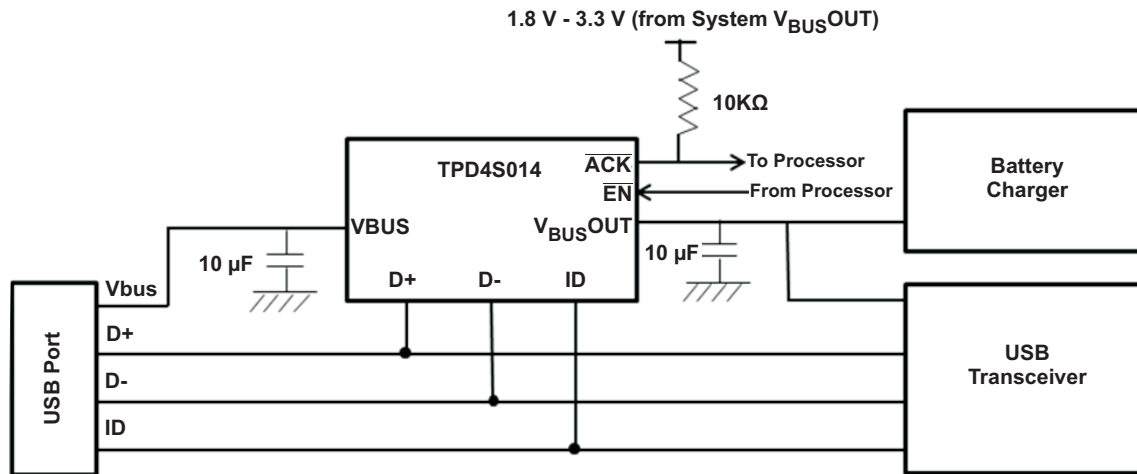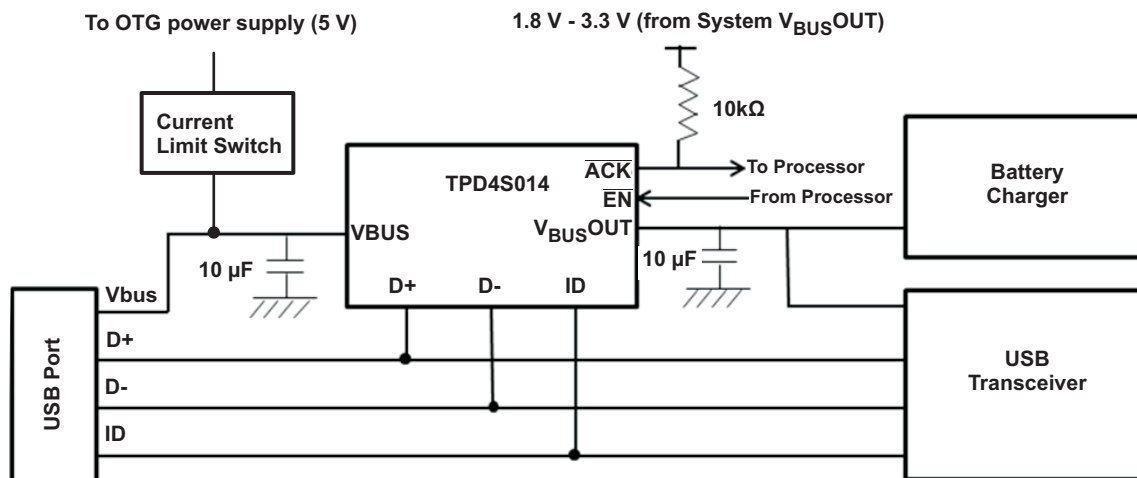
APPLICATION DIAGRAM

Figure 1. tandard Implementation for Non-OTG USB System

It is recommended the $C_{VBUS} >= C_{VBUS\_OUT}$. This is necessary to ensure that the VBUS voltage doesn't drop below the UVLO threshold when the device turns on at start up.

Figure 2. Implementation for System With OTG System Support

TYPICAL CHARACTERISTICS
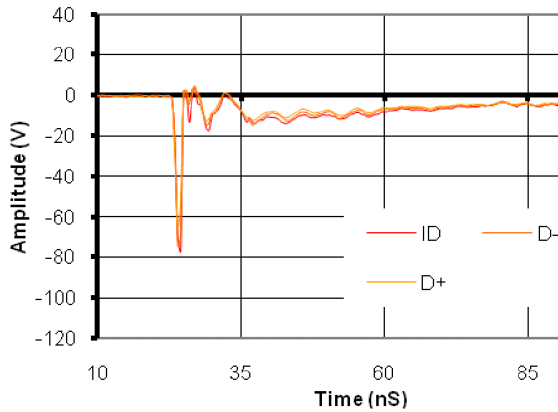
Figure 3. IEC61000-4-2 -8kV Contact Waveform
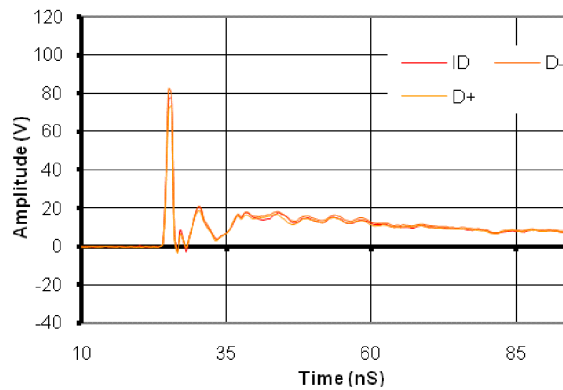
Figure 4. IEC61000-4-2 +8kV Contact Waveform
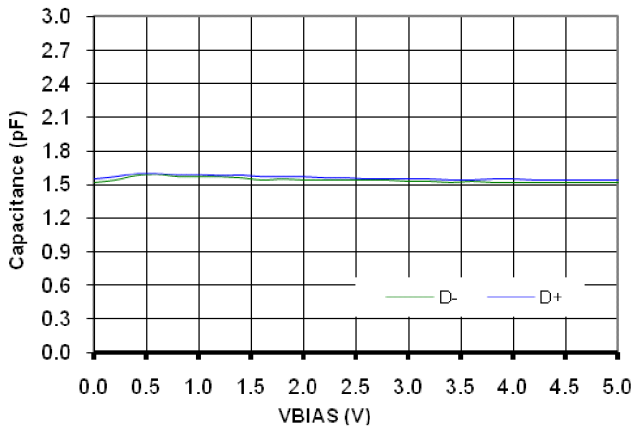
Figure 5. Capacitance Variation With Voltage
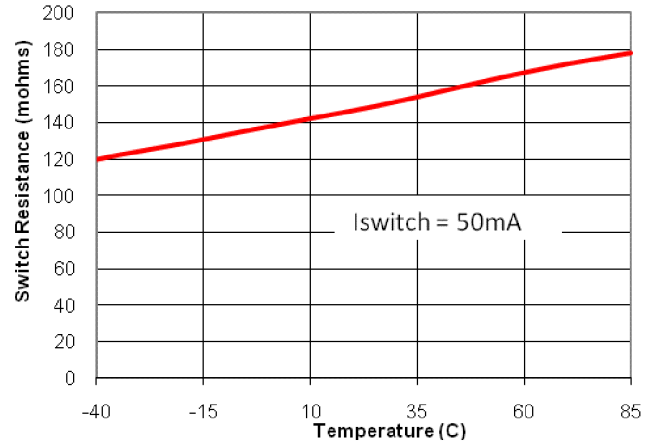

Figure 6. Variation of On Resistance with Ambient Temperature
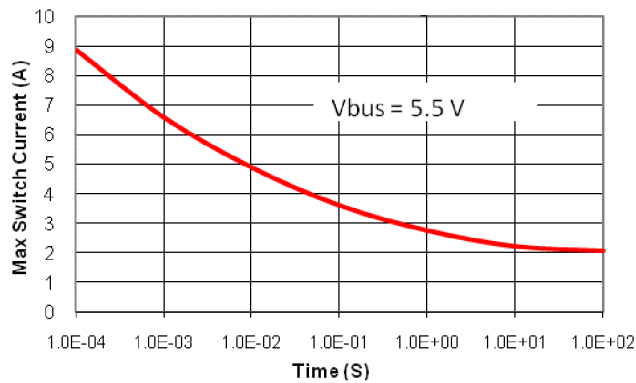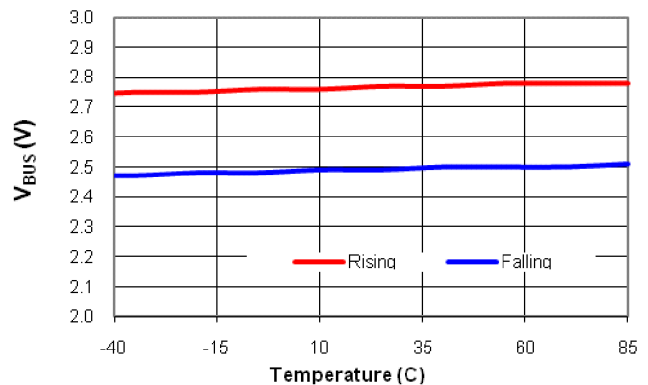

Figure 7. Max Pulse Current Through Switch vs Pulse Duration
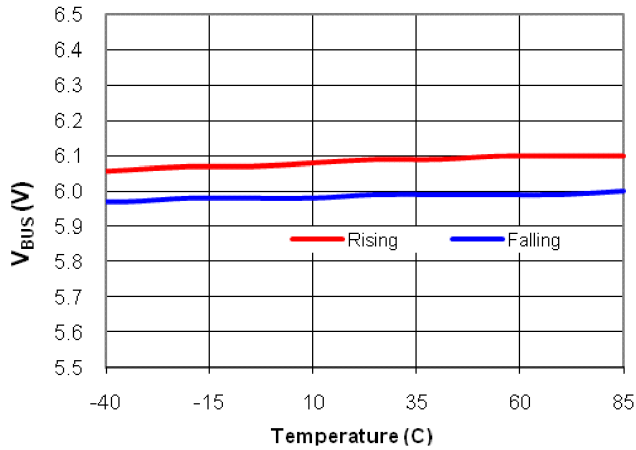

Figure 8. UVLO Threshold Variation With Temperature

Figure 9. OVP Threshold Variation With Temperature
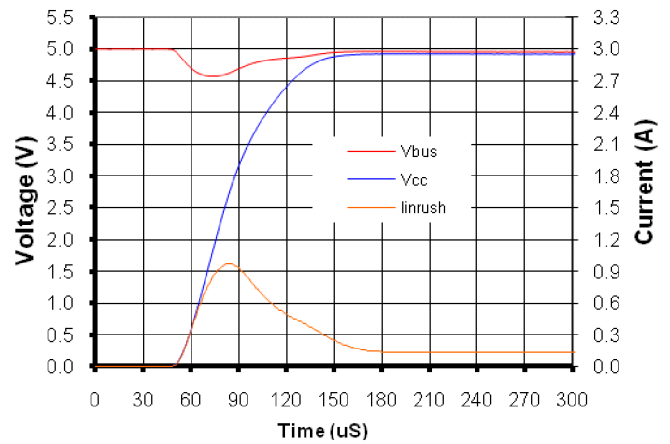

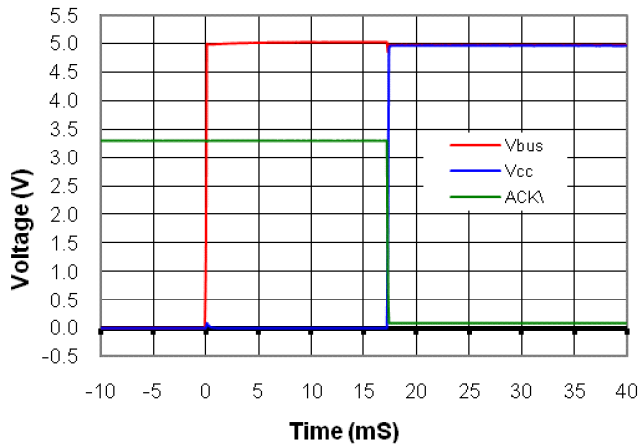**Figure 10. Start Up Inrush Current Characteristics**
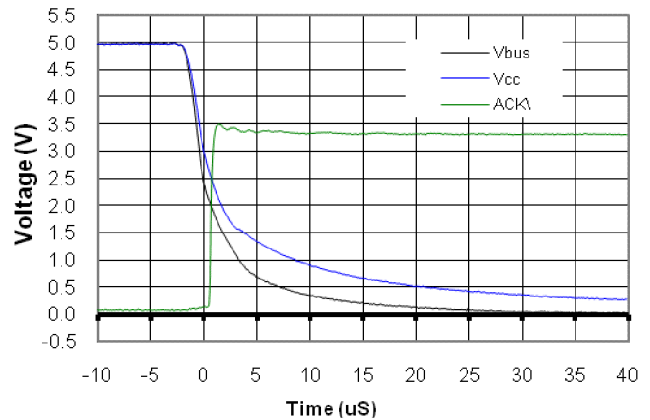

Figure 11. Device Turn on Characteristics

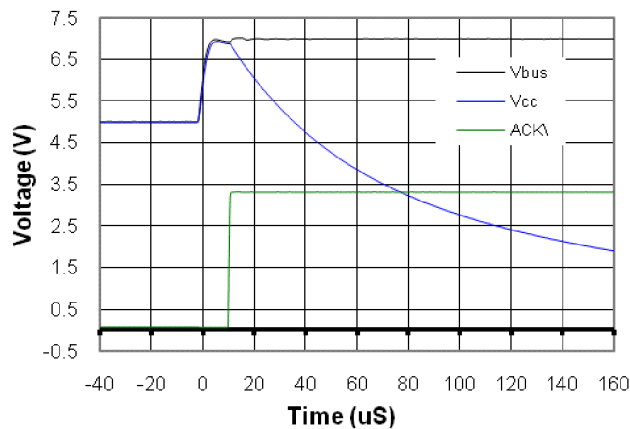**Figure 12. Device Turn OFF Characteristics (Undervoltage)**

Figure 13. Device Turn OFF Characteristics (Overvoltage)

8

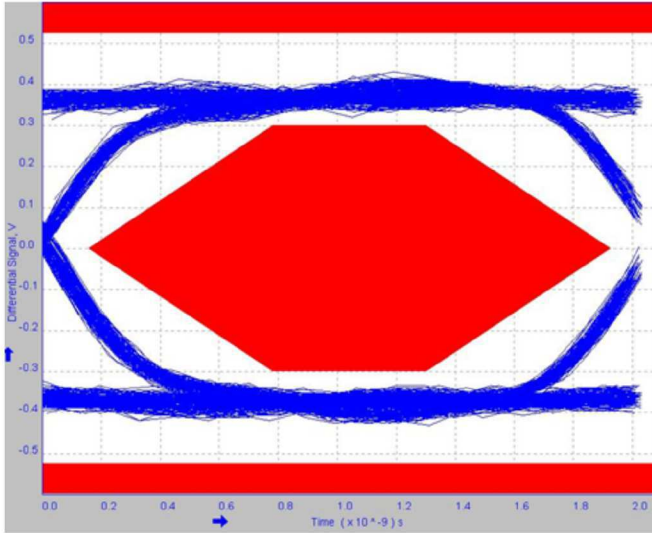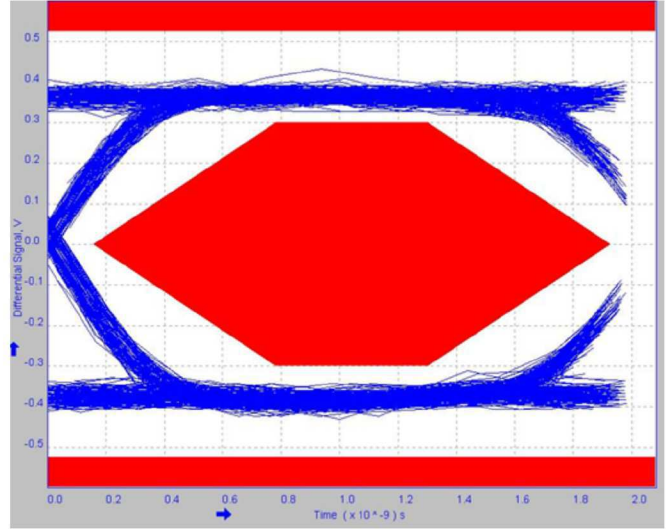**Figure 14. Eye Diagram With No EVM And No IC, Full USB2.0 Speed At 480Mbps**

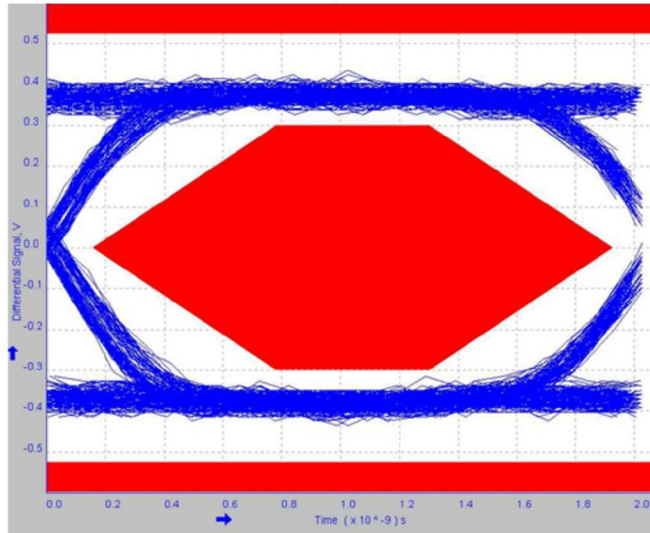**Figure 15. Eye Diagram With EVM, No IC, Full USB2.0 Speed At 480Mbps**

Figure 16. Eye Diagram With EVM and IC, Full USB2.0 Speed At 480Mbps

REVISION HISTORY

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TPD4S014DSQR	ACTIVE	SON	DSQ	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

[1] The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

REEL DIMENSIONS
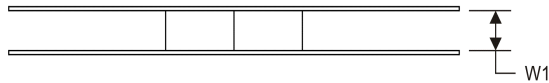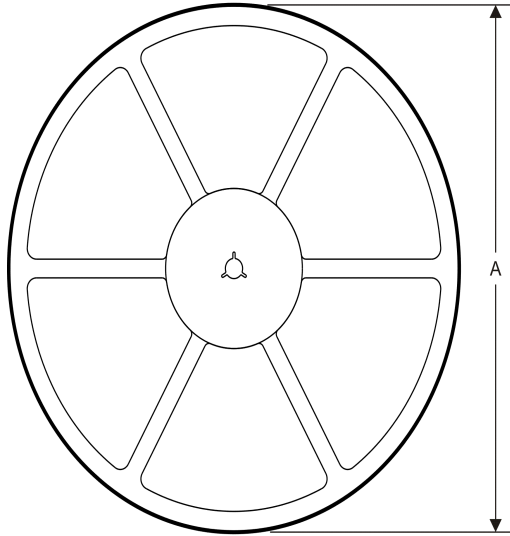
TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4S014DSQR	SON	DSQ	10	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

Pack Materials-Page 1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4S014DSQR	SON	DSQ	10	3000	195.0	200.0	45.0

DSQ (S−PWSON−N10)   PLASTIC SMALL OUTLINE NO−LEAD

A

$\frac{2,10}{1,90}$

B

$\frac{2,10}{1,90}$

PIN 1 INDEX AREA

$\frac{0,80}{0,70}$

0,20 REF.

C

0,08

SEATING PLANE

$\frac{0,05}{0,00}$

10X $\frac{0,35}{0,25}$

1

5

10X $\frac{0,25}{0,15}$

⊕ | 0,10 Ⓜ | C | A | B
0,05 Ⓜ | C

EXPOSED THERMAL PAD

D

10

6

0,40
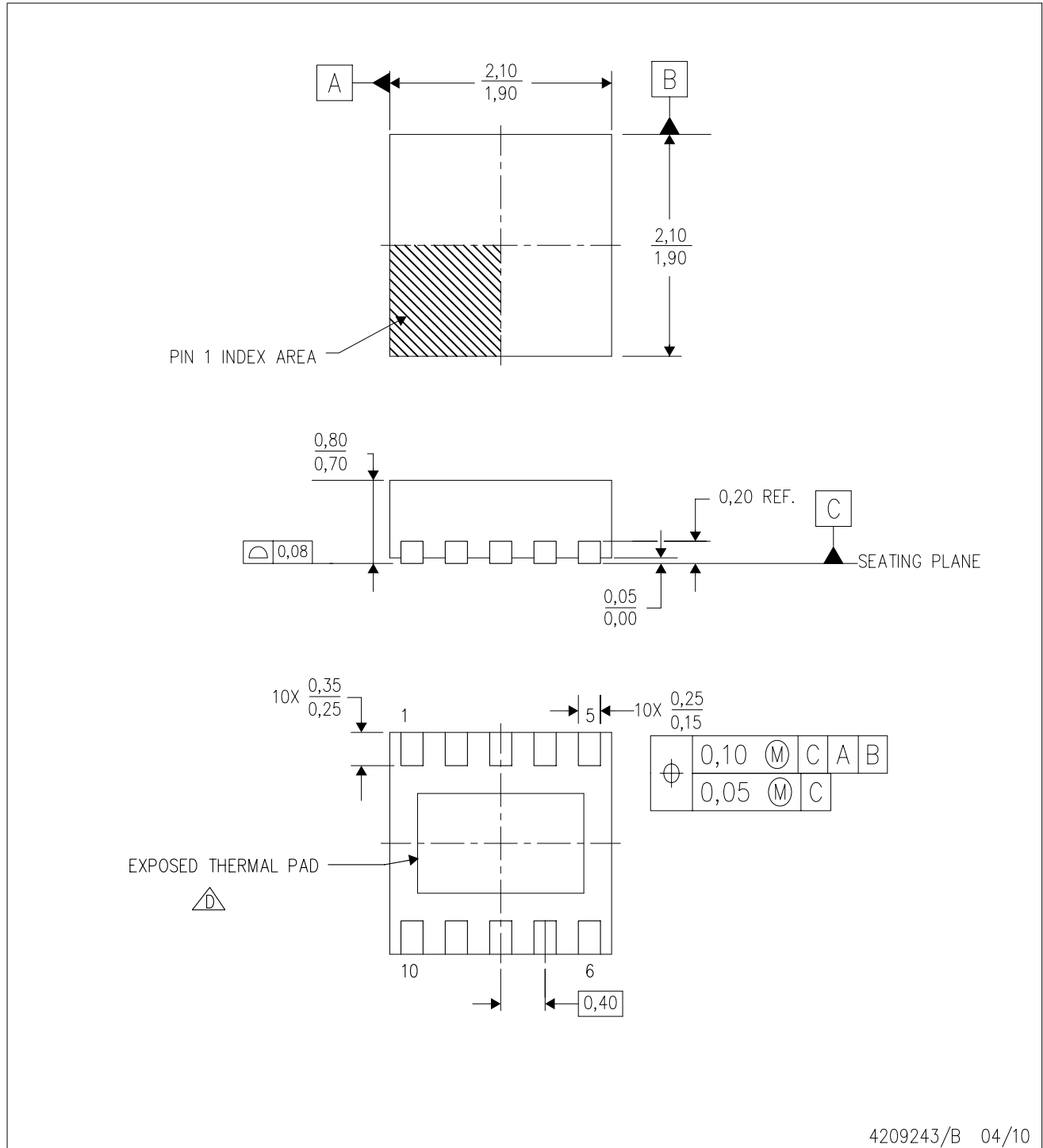
4209243/B 04/10

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M−1994.
        B. This drawing is subject to change without notice.
        C. Small Outline No−Lead (SON) package configuration.
        D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
            See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

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DSQ (R−PWSON−N10)   PLASTIC SMALL OUTLINE NO−LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No−Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

1   5

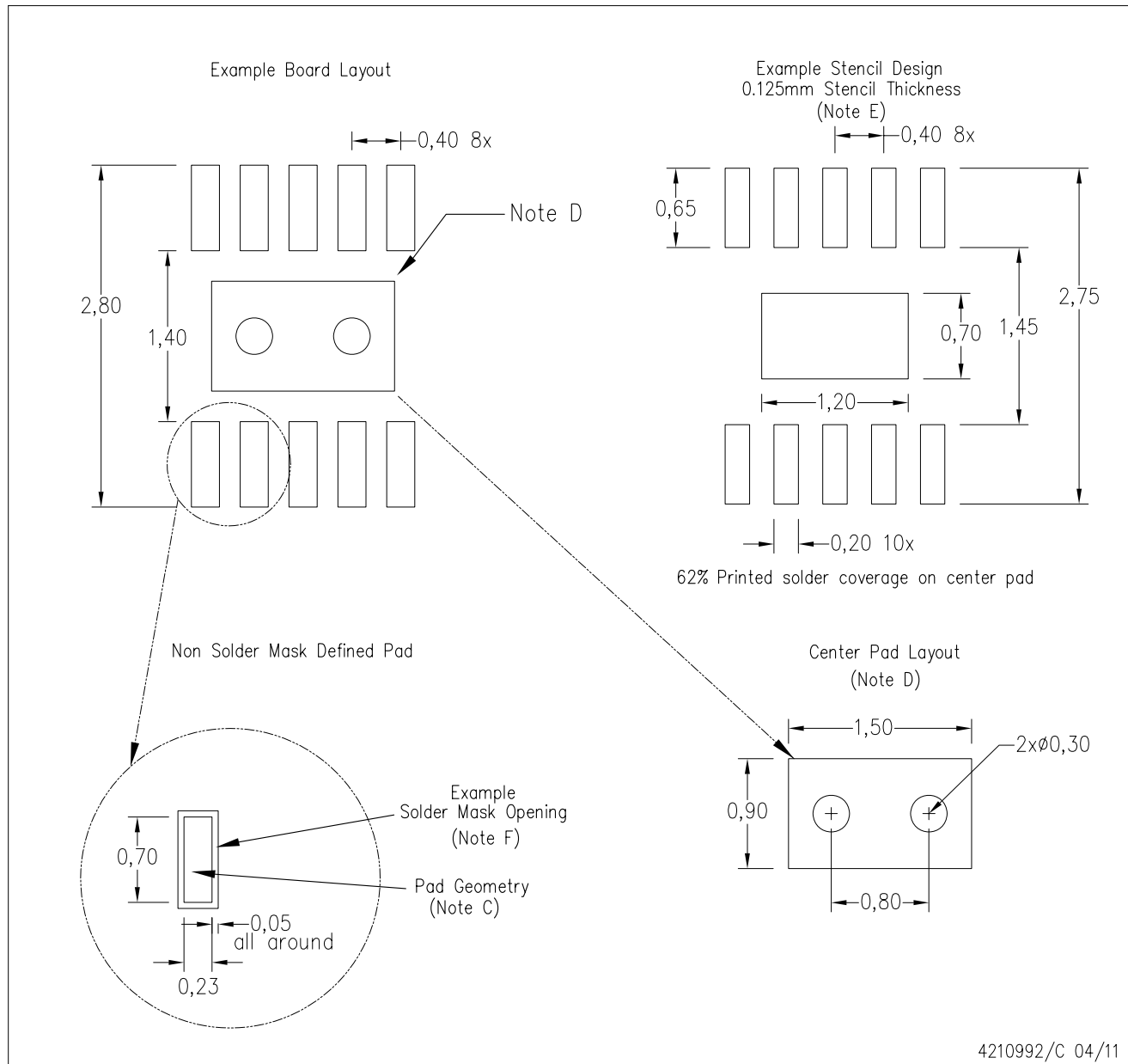0,90±0,10   Exposed
                              Thermal Pad

10   6

1,50±0,10
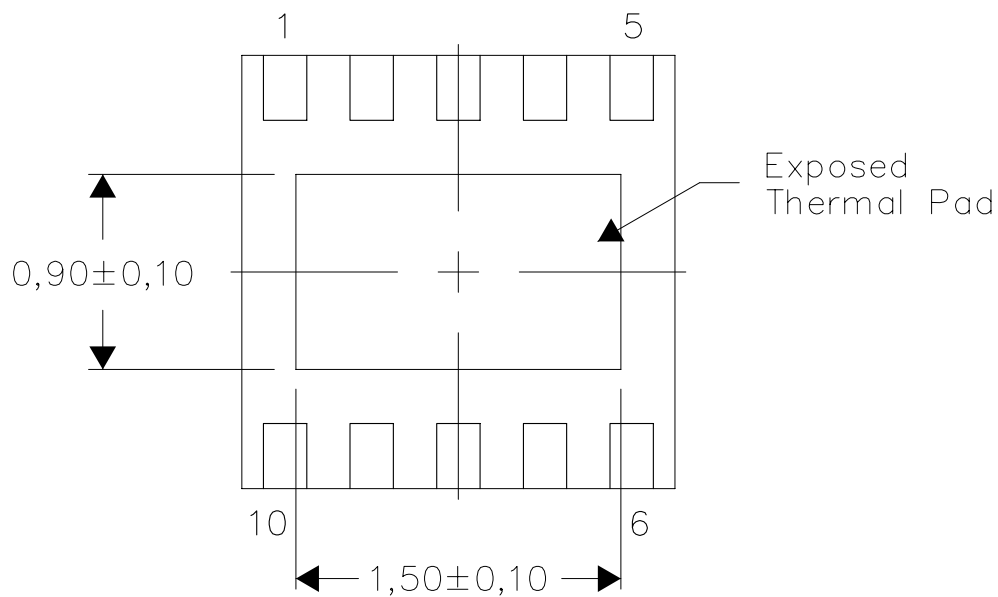
Bottom View

Exposed Thermal Pad Dimensions

4210993/C 04/11

NOTES: A. All linear dimensions are in millimeters

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DSQ (R−PWSON−N10)   PLASTIC SMALL OUTLINE NO−LEAD

Example Board Layout

←→ 0,40 8x

Note D

2,80

1,40

Non Solder Mask Defined Pad

Example
Solder Mask Opening
(Note F)

Pad Geometry
(Note C)

0,70

←0,05
all around

0,23

Example Stencil Design
0.125mm Stencil Thickness
(Note E)

←→ 0,40 8x

0,65

2,75

0,70   1,45

1,20

←0,20 10x

62% Printed solder coverage on center pad

Center Pad Layout
(Note D)

1,50

2xØ0,30

0,90

0,80

4210992/C 04/11

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC−7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note,
QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets
for specific thermal information, via requirements, and recommended board layout.
These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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