MIXED SIGNAL MICROCONTROLLER

FEATURES

- **Low Supply Voltage Range: 3.6 V Down to 1.8 V**
- **Ultra-Low Power Consumption**
  - **Active Mode (AM): All System Clocks Active 265 µA/MHz at 8 MHz, 3.0 V, Flash Program Execution (Typical) 140 µA/MHz at 8 MHz, 3.0 V, RAM Program Execution (Typical)**
  - **Standby Mode (LPM3): Real-Time Clock With Crystal, Watchdog, and Supply Supervisor Operational, Full RAM Retention, Fast Wake-Up: 1.7 µA at 2.2 V, 2.5 µA at 3.0 V (Typical)**
  - **Off Mode (LPM4): Full RAM Retention, Supply Supervisor Operational, Fast Wake-Up: 1.6 µA at 3.0 V (Typical)**
  - **Shutdown RTC Mode (LPM3.5): Shutdown Mode, Active Real-Time Clock (RTC) With Crystal: 1.24 µA at 3.0 V (Typical)**
  - **Shutdown Mode (LPM4.5): 0.78 µA at 3.0 V (Typical)**
- **Wake-Up From Standby Mode in 3 µs (Typical)**
- **16-Bit RISC Architecture, Extended Memory, up to 25-MHz System Clock**
- **Flexible Power Management System**
  - **Fully Integrated LDO With Programmable Regulated Core Supply Voltage**
  - **Supply Voltage Supervision, Monitoring, and Brownout**
  - **System Operation From up to Two Auxiliary Power Supplies**
- **Unified Clock System**
  - **FLL Control Loop for Frequency Stabilization**
  - **Low-Power Low-Frequency Internal Clock Source (VLO)**
  - **Low-Frequency Trimmed Internal Reference Source (REFO)**
  - **32-kHz Crystals (XT1)**
- **One 16-Bit Timer With Three Capture/Compare Registers**
- **Three 16-Bit Timers With Two Capture/Compare Registers Each**
- **Enhanced Universal Serial Communication Interfaces**
  - **eUSCI_A0, eUSCI_A1, and eUSCI_A2**
    - **Enhanced UART Supports Auto-Baudrate Detection**
    - **IrDA Encoder and Decoder**
    - **Synchronous SPI**
  - **eUSCI_B0**
    - **I^2C With Multi-Slave Addressing**
    - **Synchronous SPI**
- **Password-Protected RTC With Crystal Offset Calibration and Temperature Compensation**
- **Separate Voltage Supply for Backup Subsystem**
  - **32-kHz Low-Frequency Oscillator (XT1)**
  - **Real-Time Clock**
  - **Backup Memory (4 x 16 Bits)**
- **Three 24-Bit Sigma-Delta Analog-to-Digital (A/D) Converters With Differential PGA Inputs**
- **Integrated LCD Driver With Contrast Control for up to 320 Segments in 8-Mux Mode**
- **Hardware Multiplier Supports 32-Bit Operations**
- **10-Bit 200-ksps A/D Converter**
  - **Internal Reference**
  - **Sample-and-Hold, Autoscan Feature**
  - **Up to Six External Channels, Two Internal Channels, Including Temperature Sensor**
- **Three-Channel Internal DMA**
- **Serial Onboard Programming, No External Programming Voltage Needed**
- **Family Members are Summarized in Table 1**
- **Available in 100-Pin and 80-Pin LQFP Packages**
- **For Complete Module Descriptions, See the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208)**

DESCRIPTION

The Texas Instruments MSP430 family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in 3 µs (typical).

The MSP430F67xx series are microcontroller configurations with three high-performance 24-bit sigma-delta A/D converters, a 10-bit analog-to-digital (A/D) converter, four enhanced universal serial communication interfaces (three eUSCI_A and one eUSCI_B), four 16-bit timers, hardware multiplier, DMA, real-time clock module with alarm capabilities, LCD driver with integrated contrast control, auxiliary supply system, and up to 72 I/O pins in 100-pin devices and 52 I/O pins in 80-pin devices.

Typical applications for these devices are 2-wire and 3-wire single-phase metering, including tamper-resistant meter implementations.

Family members available are summarized in Table 1.

Table 1. Family Members

Device	Flash (KB)	SRAM (KB)	SD24_B Converters	ADC10_A Channels	Timer_A (1)	eUSCI Channel A: UART, IrDA, SPI	eUSCI Channel B: SPI, I^2C	I/O	Package Type
MSP430F6736IPZ	128	8	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6735IPZ	128	4	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6734IPZ	96	4	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6733IPZ	64	4	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6731IPZ	32	2	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6730IPZ	16	1	3	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6726IPZ	128	8	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6725IPZ	128	4	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6724IPZ	96	4	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6723IPZ	64	4	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6721IPZ	32	2	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6720IPZ	16	1	2	6 ext, 2 int	3, 2, 2, 2	3	1	72	100 PZ
MSP430F6736IPN	128	8	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6735IPN	128	4	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6734IPN	96	4	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6733IPN	64	4	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6731IPN	32	2	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6730IPN	16	1	3	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6726IPN	128	8	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6725IPN	128	4	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6724IPN	96	4	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6723IPN	64	4	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6721IPN	32	2	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN
MSP430F6720IPN	16	1	2	3 ext, 2 int	3, 2, 2, 2	3	1	52	80 PN

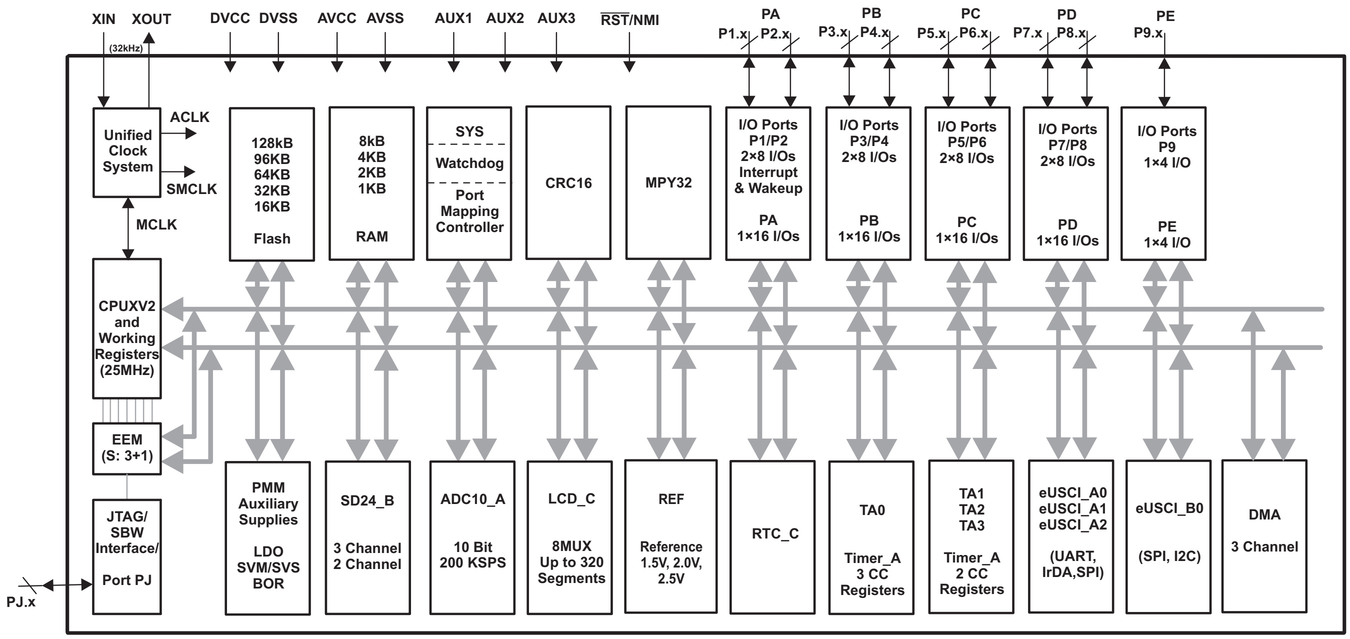
(1) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture compare registers and PWM output generators, respectively.

Table 2. Ordering Information(1)

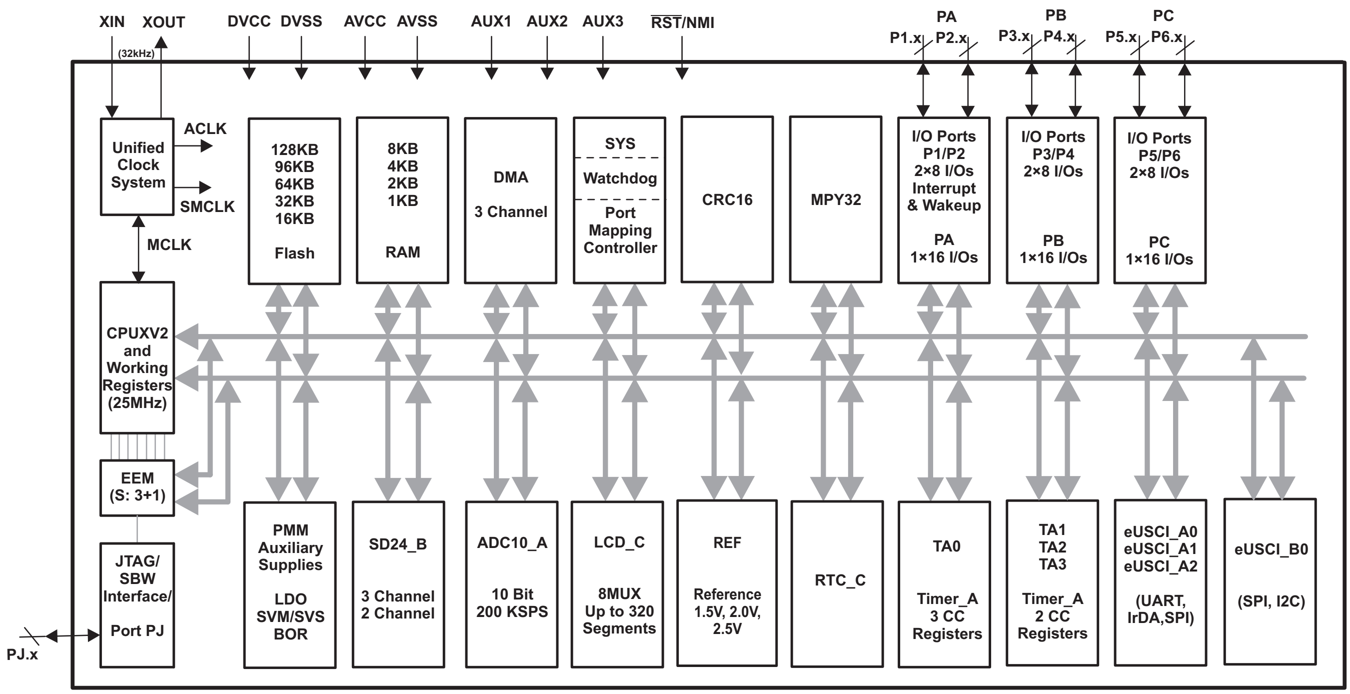
T_A	PACKAGED DEVICES(2)	
	PLASTIC 100-PIN LQFP (PZ)	PLASTIC 80-PIN LQFP (PN)
–40°C to 85°C	MSP430F6736IPZ	MSP430F6736IPN
	MSP430F6735IPZ	MSP430F6735IPN
	MSP430F6734IPZ	MSP430F6734IPN
	MSP430F6733IPZ	MSP430F6733IPN
	MSP430F6731IPZ	MSP430F6731IPN
	MSP430F6730IPZ	MSP430F6730IPN
	MSP430F6726IPZ	MSP430F6726IPN
	MSP430F6725IPZ	MSP430F6725IPN
	MSP430F6724IPZ	MSP430F6724IPN
	MSP430F6723IPZ	MSP430F6723IPN
	MSP430F6721IPZ	MSP430F6721IPN
	MSP430F6720IPZ	MSP430F6720IPN

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.

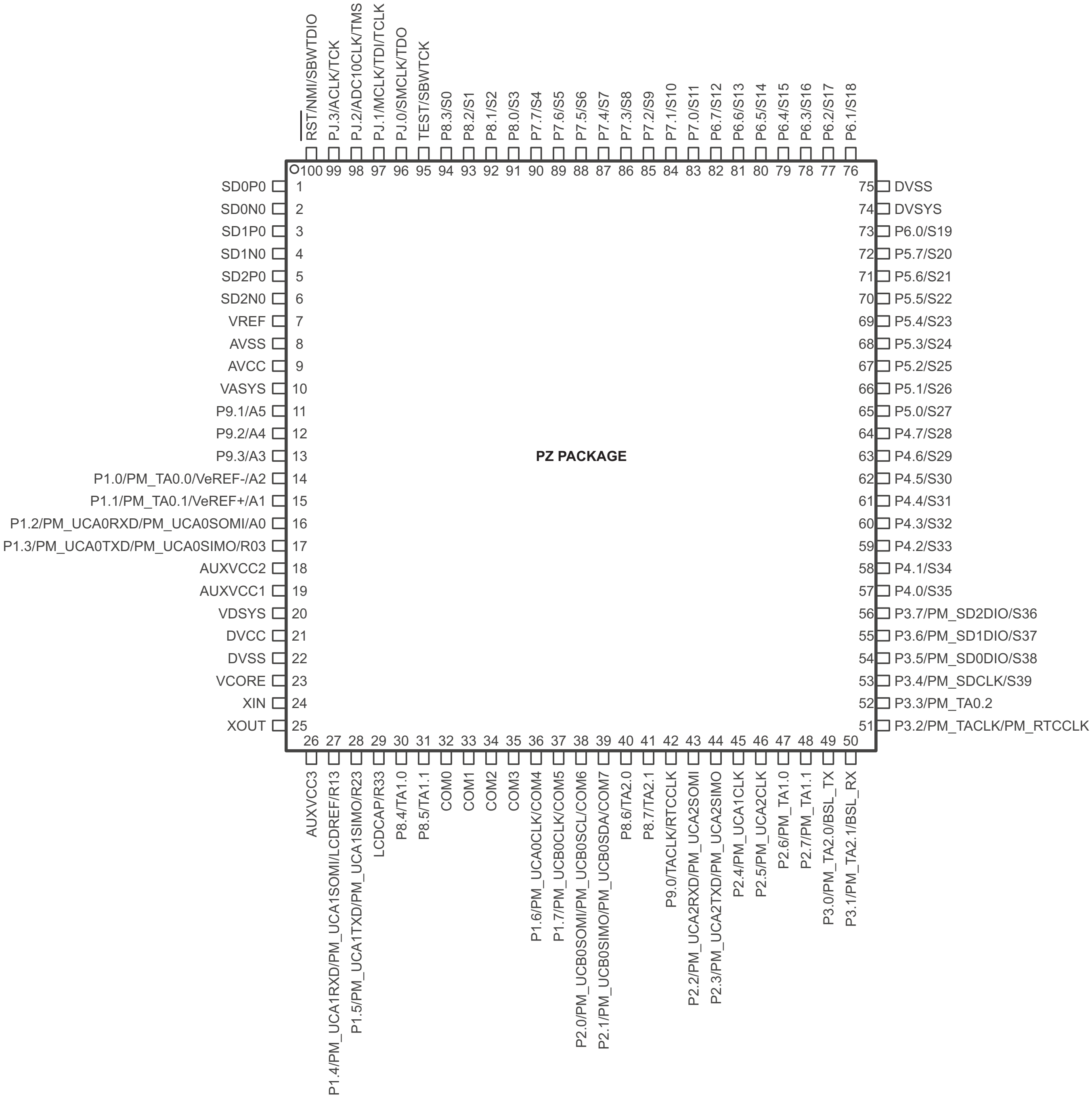
Functional Block Diagram, MSP430F673xIPZ, MSP430F672xIPZ



Functional Block Diagram, MSP430F673xIPN, MSP430F672xIPN



Pin Designation, MSP430F673xIPZ



NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. The pin designation shows the default mapping. See Table 14 for details.

NOTE: The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

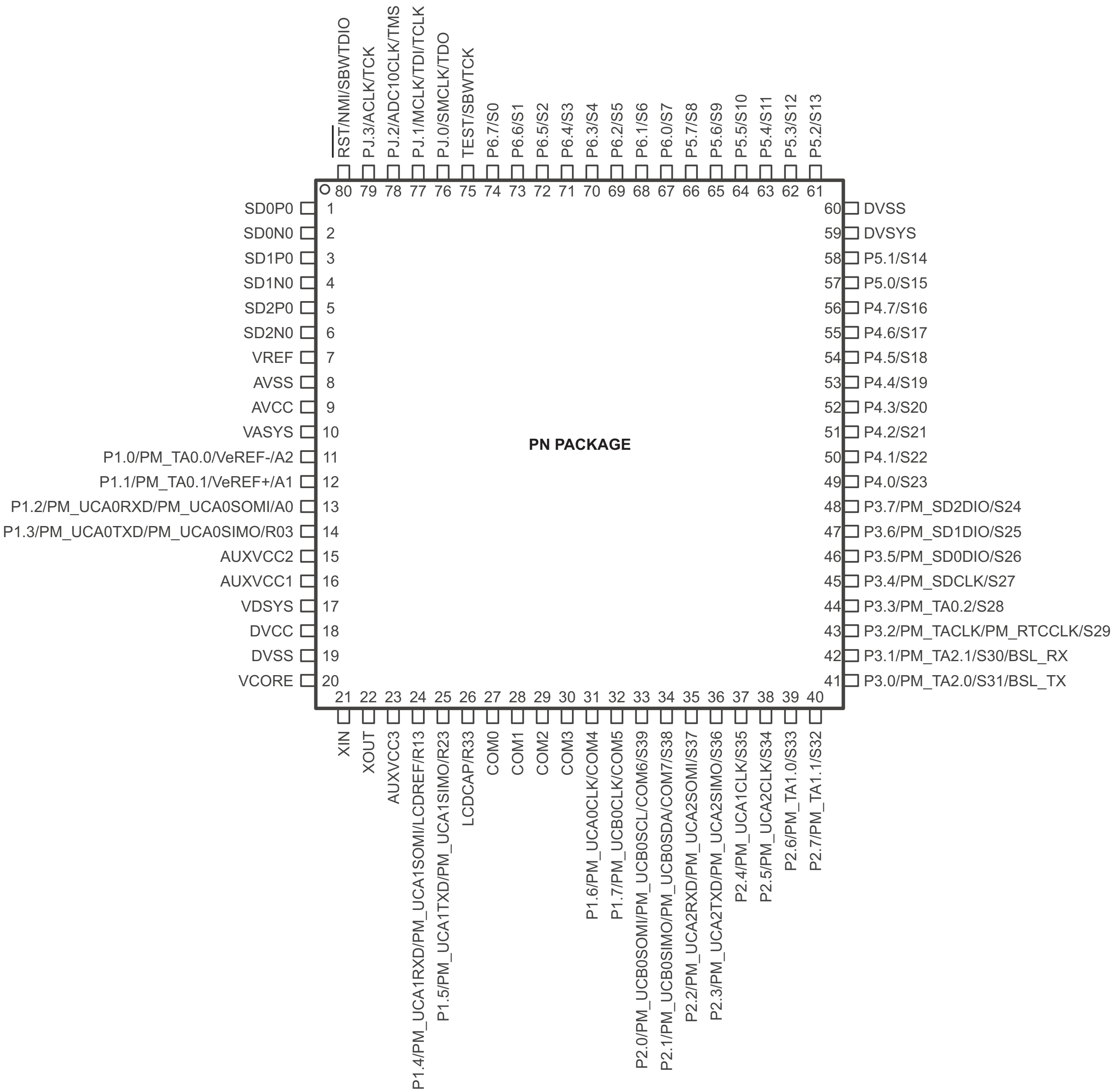
CAUTION: The LCDCAP/R33 pin must be connected to DVSS if not used.

Table 3. Pinout Differences Between MSP430F673xIPZ and MSP430F672xIPZ(1)

PIN NUMBER	PIN NAME	
	MSP430F673xIPZ	MSP430F672xIPZ
1	SD0P0	SD0P0
2	SD0N0	SD0N0
3	SD1P0	SD1P0
4	SD1N0	SD1N0
5	*SD2P0*	*NC*
6	*SD2N0*	*NC*
7	VREF	VREF
53	P3.4/PM_SDCLK/S39	P3.4/PM_SDCLK/S39
54	P3.5/PM_SD0DIO/S38	P3.5/PM_SD0DIO/S38
55	P3.6/PM_SD1DIO/S37	P3.6/PM_SD1DIO/S37
56	P3.7/*PM_SD2DIO*/S36	P3.7/*PM_NONE*/S36

(1) Signal names that differ between devices are indicated by *italic* typeface.

Pin Designation, MSP430F673xIPN



NOTE: The secondary digital functions on Ports P1, P2, and P3 are fully mappable. The pin designation shows the default mapping. See Table 14 for details.

NOTE: The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

CAUTION: The LCDCAP/R33 pin must be connected to DVSS if not used.

Table 4. Pinout Differences Between MSP430F673xIPN and MSP430F672xIPN(1)

PIN NUMBER	PIN NAME	
	MSP430F673xIPN	MSP430F672xIPN
1	SD0P0	SD0P0
2	SD0N0	SD0N0
3	SD1P0	SD1P0
4	SD1N0	SD1N0
5	*SD2P0*	*NC*
6	*SD2N0*	*NC*
7	VREF	VREF
45	P3.4/PM_SDCLK/S27	P3.4/PM_SDCLK/S27
46	P3.5/PM_SD0DIO/S26	P3.5/PM_SD0DIO/S26
47	P3.6/PM_SD1DIO/S25	P3.6/PM_SD1DIO/S25
48	P3.7/*PM_SD2DIO*/S24	P3.7/*PM_NONE*/S24

(1) Signal names that differ between devices are indicated by *italic* typeface.

Table 5. Terminal Functions, MSP430F67xxIPZ

TERMINAL NAME	NO. PZ	I/O [(1)]	DESCRIPTION
SD0P0	1	I	SD24_B positive analog input for converter 0 [(2)]
SD0N0	2	I	SD24_B negative analog input for converter 0 [(2)]
SD1P0	3	I	SD24_B positive analog input for converter 1 [(2)]
SD1N0	4	I	SD24_B negative analog input for converter 1 [(2)]
SD2P0	5	I	SD24_B positive analog input for converter 2 [(2)] (not available on F672x devices)
SD2N0	6	I	SD24_B negative analog input for converter 2 [(2)] (not available on F672x devices)
VREF	7	I	SD24_B external reference voltage
AVSS	8		Analog ground supply
AVCC	9		Analog power supply
VASYS	10		Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C_{VSYS} (see Auxiliary Supplies - Recommended Operating Conditions).
P9.1/A5	11	I/O	General-purpose digital I/O Analog input A5 - 10-bit ADC
P9.2/A4	12	I/O	General-purpose digital I/O Analog input A4 - 10-bit ADC
P9.3/A3	13	I/O	General-purpose digital I/O Analog input A3 - 10-bit ADC
P1.0/PM_TA0.0/VeREF-/A2	14	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output Negative terminal for the ADC's reference voltage for an external applied reference voltage Analog input A2 - 10-bit ADC
P1.1/PM_TA0.1/VeREF+/A1	15	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output Positive terminal for the ADC's reference voltage for an external applied reference voltage Analog input A1 - 10-bit ADC
P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0	16	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 UART receive data; eUSCI_A0 SPI slave out/master in Analog input A0 - 10-bit ADC
P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03	17	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 UART transmit data; eUSCI_A0 SPI slave in/master out Input/output port of lowest analog LCD voltage (V5)
AUXVCC2	18		Auxiliary power supply AUXVCC2
AUXVCC1	19		Auxiliary power supply AUXVCC1
VDSYS [(3)]	20		Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C_{VSYS} (see Auxiliary Supplies - Recommended Operating Conditions).
DVCC	21		Digital power supply
DVSS	22		Digital ground supply
VCORE [(4)]	23		Regulated core power supply (internal use only, no external current loading)
XIN	24	I	Input terminal for crystal oscillator

(1) I = input, O = output
(2) It is recommended to short unused analog input pairs and connect them to analog ground.
(3) The pins VDSYS and DVSYS must be connected externally on board for proper device operation.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 5. Terminal Functions, MSP430F67xxIPZ (continued)

TERMINAL		I/O(1)	DESCRIPTION
NAME	NO. PZ		
XOUT	25	O	Output terminal for crystal oscillator
AUXVCC3	26		Auxiliary power supply AUXVCC3 for back up subsystem
P1.4/PM_UCA1RXD/ PM_UCA1SOMI/LCDREF/R13	27	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 UART receive data; eUSCI_A1 SPI slave out/master in External reference voltage input for regulated LCD voltage Input/output port of third most positive analog LCD voltage (V3 or V4)
P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23	28	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 UART transmit data; eUSCI_A1 SPI slave in/master out Input/output port of second most positive analog LCD voltage (V2)
LCDCAP/R33	29	I/O	LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) **CAUTION**: This pin must be connected to DVSS if not used.
P8.4/TA1.0	30	I/O	General-purpose digital I/O Timer TA1 CCR0 capture: CCI0A input, compare: Out0 output
P8.5/TA1.1	31	I/O	General-purpose digital I/O Timer TA1 CCR1 capture: CCI1A input, compare: Out1 output
COM0	32	O	LCD common output COM0 for LCD backplane
COM1	33	O	LCD common output COM1 for LCD backplane
COM2	34	O	LCD common output COM2 for LCD backplane
COM3	35	O	LCD common output COM3 for LCD backplane
P1.6/PM_UCA0CLK/COM4	36	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 clock input/output LCD common output COM4 for LCD backplane
P1.7/PM_UCB0CLK/COM5	37	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 clock input/output LCD common output COM5 for LCD backplane
P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6	38	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave out/master in; eUSCI_B0 I2C clock LCD common output COM6 for LCD backplane
P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7	39	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave in/master out; eUSCI_B0 I2C data LCD common output COM7 for LCD backplane
P8.6/TA2.0	40	I/O	General-purpose digital I/O Timer TA2 CCR0 capture: CCI0A input, compare: Out0 output
P8.7/TA2.1	41	I/O	General-purpose digital I/O Timer TA2 CCR1 capture: CCI1A input, compare: Out1 output
P9.0/TACLK/RTCCLK	42	I/O	General-purpose digital I/O Timer clock input TACLK for TA0, TA1, TA2, TA3 RTCCLK clock output
P2.2/PM_UCA2RXD/ PM_UCA2SOMI	43	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 UART receive data; eUSCI_A2 SPI slave out/master in
P2.3/PM_UCA2TXD/ PM_UCA2SIMO	44	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 UART transmit data; eUSCI_A2 SPI slave in/master out

Table 5. Terminal Functions, MSP430F67xxIPZ (continued)

TERMINAL NAME	NO. PZ	I/O (1)	DESCRIPTION
P2.4/PM_UCA1CLK	45	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 clock input/output
P2.5/PM_UCA2CLK	46	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 clock input/output
P2.6/PM_TA1.0	47	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output
P2.7/PM_TA1.1	48	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output
P3.0/PM_TA2.0/BSL_TX	49	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output Bootstrap loader: Data transmit
P3.1/PM_TA2.1/BSL_RX	50	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output Bootstrap loader: Data receive
P3.2/PM_TACLK/PM_RTCCLK	51	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3; RTCCLK clock output
P3.3/PM_TA0.2	52	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output
P3.4/PM_SDCLK/S39	53	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B bit stream clock input/output LCD segment output S39
P3.5/PM_SD0DIO/S38	54	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-0 bit stream data input/output LCD segment output S38
P3.6/PM_SD1DIO/S37	55	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-1 bit stream data input/output LCD segment output S37
P3.7/PM_SD2DIO/S36	56	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-2 bit stream data input/output (not available on F672x devices) LCD segment output S36
P4.0/S35	57	I/O	General-purpose digital I/O LCD segment output S35
P4.1/S34	58	I/O	General-purpose digital I/O LCD segment output S34
P4.2/S33	59	I/O	General-purpose digital I/O LCD segment output S33
P4.3/S32	60	I/O	General-purpose digital I/O LCD segment output S32
P4.4/S31	61	I/O	General-purpose digital I/O LCD segment output S31
P4.5/S30	62	I/O	General-purpose digital I/O LCD segment output S30

Table 5. Terminal Functions, MSP430F67xxIPZ (continued)

TERMINAL		I/O (1)	DESCRIPTION
NAME	NO. PZ		
P4.6/S29	63	I/O	General-purpose digital I/O LCD segment output S29
P4.7/S28	64	I/O	General-purpose digital I/O LCD segment output S28
P5.0/S27	65	I/O	General-purpose digital I/O LCD segment output S27
P5.1/S26	66	I/O	General-purpose digital I/O LCD segment output S26
P5.2/S25	67	I/O	General-purpose digital I/O LCD segment output S25
P5.3/S24	68	I/O	General-purpose digital I/O LCD segment output S24
P5.4/S23	69	I/O	General-purpose digital I/O LCD segment output S23
P5.5/S22	70	I/O	General-purpose digital I/O LCD segment output S22
P5.6/S21	71	I/O	General-purpose digital I/O LCD segment output S21
P5.7/S20	72	I/O	General-purpose digital I/O LCD segment output S20
P6.0/S19	73	I/O	General-purpose digital I/O LCD segment output S19
DVSYS (5)	74		Digital power supply for I/Os
DVSS	75		Digital ground supply
P6.1/S18	76	I/O	General-purpose digital I/O LCD segment output S18
P6.2/S17	77	I/O	General-purpose digital I/O LCD segment output S17
P6.3/S16	78	I/O	General-purpose digital I/O LCD segment output S16
P6.4/S15	79	I/O	General-purpose digital I/O LCD segment output S15
P6.5/S14	80	I/O	General-purpose digital I/O LCD segment output S14
P6.6/S13	81	I/O	General-purpose digital I/O LCD segment output S13
P6.7/S12	82	I/O	General-purpose digital I/O LCD segment output S12
P7.0/S11	83	I/O	General-purpose digital I/O LCD segment output S11
P7.1/S10	84	I/O	General-purpose digital I/O LCD segment output S10

(5) The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

Table 5. Terminal Functions, MSP430F67xxIPZ (continued)

TERMINAL NAME	NO. PZ	I/O [(1)]	DESCRIPTION
P7.2/S9	85	I/O	General-purpose digital I/O LCD segment output S9
P7.3/S8	86	I/O	General-purpose digital I/O LCD segment output S8
P7.4/S7	87	I/O	General-purpose digital I/O LCD segment output S7
P7.5/S6	88	I/O	General-purpose digital I/O LCD segment output S6
P7.6/S5	89	I/O	General-purpose digital I/O LCD segment output S5
P7.7/S4	90	I/O	General-purpose digital I/O LCD segment output S4
P8.0/S3	91	I/O	General-purpose digital I/O LCD segment output S3
P8.1/S2	92	I/O	General-purpose digital I/O LCD segment output S2
P8.2/S1	93	I/O	General-purpose digital I/O LCD segment output S1
P8.3/S0	94	I/O	General-purpose digital I/O LCD segment output S0
TEST/SBWTCK	95	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
PJ.0/SMCLK/TDO	96	I/O	General-purpose digital I/O SMCLK clock output Test data output
PJ.1/MCLK/TDI/TCLK	97	I/O	General-purpose digital I/O MCLK clock output Test data input or Test clock input
PJ.2/ADC10CLK/TMS	98	I/O	General-purpose digital I/O ADC10_A clock output Test mode select
PJ.3/ACLK/TCK	99	I/O	General-purpose digital I/O ACLK clock output Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO	100	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output

Table 6. Terminal Functions, MSP430F67xxIPN

TERMINAL NAME	NO. PN	I/O (1)	DESCRIPTION
SD0P0	1	I	SD24_B positive analog input for converter 0 (2)
SD0N0	2	I	SD24_B negative analog input for converter 0 (2)
SD1P0	3	I	SD24_B positive analog input for converter 1 (2)
SD1N0	4	I	SD24_B negative analog input for converter 1 (2)
SD2P0	5	I	SD24_B positive analog input for converter 2 (2) (not available on F672x devices)
SD2N0	6	I	SD24_B negative analog input for converter 2 (2) (not available on F672x devices)
VREF	7	I	SD24_B external reference voltage
AVSS	8		Analog ground supply
AVCC	9		Analog power supply
VASYS	10		Analog power supply selected between AVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C_{VSYS} (see Auxiliary Supplies - Recommended Operating Conditions).
P1.0/PM_TA0.0/VeREF-/A2	11	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 CCR0 capture: CCI0A input, compare: Out0 output Negative terminal for the ADC's reference voltage for an external applied reference voltage Analog input A2 - 10-bit ADC
P1.1/PM_TA0.1/VeREF+/A1	12	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA0 CCR1 capture: CCI1A input, compare: Out1 output Positive terminal for the ADC reference voltage for an external applied reference voltage Analog input A1 - 10-bit ADC
P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0	13	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 UART receive data; eUSCI_A0 SPI slave out/master in Analog input A0 - 10-bit ADC
P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03	14	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 UART transmit data; eUSCI_A0 SPI slave in/master out Input/output port of lowest analog LCD voltage (V5)
AUXVCC2	15		Auxiliary power supply AUXVCC2
AUXVCC1	16		Auxiliary power supply AUXVCC1
VDSYS (3)	17		Digital power supply selected between DVCC, AUXVCC1, AUXVCC2. Connect recommended capacitor value of C_{VSYS} (see Auxiliary Supplies - Recommended Operating Conditions).
DVCC	18		Digital power supply
DVSS	19		Digital ground supply
VCORE (4)	20		Regulated core power supply (internal use only, no external current loading)
XIN	21	I	Input terminal for crystal oscillator
XOUT	22	O	Output terminal for crystal oscillator
AUXVCC3	23		Auxiliary power supply AUXVCC3 for back up subsystem
P1.4/PM_UCA1RXD/ PM_UCA1SOMI/LCDREF/R13	24	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 UART receive data; eUSCI_A1 SPI slave out/master in External reference voltage input for regulated LCD voltage Input/output port of third most positive analog LCD voltage (V3 or V4)

(1) I = input, O = output
(2) It is recommended to short unused analog input pairs and connect them to analog ground.
(3) The pins VDSYS and DVSYS must be connected externally on board for proper device operation.
(4) VCORE is for internal use only. No external current loading is possible. VCORE should only be connected to the recommended capacitor value, C_{VCORE}.

Table 6. Terminal Functions, MSP430F67xxIPN (continued)

TERMINAL NAME	NO. PN	I/O (1)	DESCRIPTION
P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23	25	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 UART transmit data; eUSCI_A1 SPI slave in/master out Input/output port of second most positive analog LCD voltage (V2)
LCDCAP/R33	26	I/O	LCD capacitor connection Input/output port of most positive analog LCD voltage (V1) **CAUTION**: This pin must be connected to DVSS if not used.
COM0	27	O	LCD common output COM0 for LCD backplane
COM1	28	O	LCD common output COM1 for LCD backplane
COM2	29	O	LCD common output COM2 for LCD backplane
COM3	30	O	LCD common output COM3 for LCD backplane
P1.6/PM_UCA0CLK/COM4	31	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A0 clock input/output LCD common output COM4 for LCD backplane
P1.7/PM_UCB0CLK/COM5	32	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 clock input/output LCD common output COM5 for LCD backplane
P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/S39	33	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave out/master in; eUSCI_B0 I2C clock LCD common output COM6 for LCD backplane LCD segment output S39
P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/S38	34	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_B0 SPI slave in/master out; eUSCI_B0 I2C data LCD common output COM7 for LCD backplane LCD segment output S38
P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37	35	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 UART receive data; eUSCI_A2 SPI slave out/master in LCD segment output S37
P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36	36	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 UART transmit data; eUSCI_A2 SPI slave in/master out LCD segment output S36
P2.4/PM_UCA1CLK/S35	37	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A1 clock input/output LCD segment output S35
P2.5/PM_UCA2CLK/S34	38	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: eUSCI_A2 clock input/output LCD segment output S34
P2.6/PM_TA1.0/S33	39	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA1 capture CCR0: CCI0A input, compare: Out0 output LCD segment output S33
P2.7/PM_TA1.1/S32	40	I/O	General-purpose digital I/O with port interrupt and mappable secondary function Default mapping: Timer TA1 capture CCR1: CCI1A input, compare: Out1 output LCD segment output S32

Table 6. Terminal Functions, MSP430F67xxIPN (continued)

TERMINAL NAME	NO. PN	I/O[1]	DESCRIPTION
P3.0/PM_TA2.0/S31/BSL_TX	41	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA2 capture CCR0: CCI0A input, compare: Out0 output LCD segment output S31 Bootstrap loader: Data transmit
P3.1/PM_TA2.1/S30/BSL_RX	42	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA2 capture CCR1: CCI1A input, compare: Out1 output LCD segment output S30 Bootstrap loader: Data receive
P3.2/PM_TACLK/PM_RTCCLK/ S29	43	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer clock input TACLK for TA0, TA1, TA2, TA3; RTCCLK clock output LCD segment output S29
P3.3/PM_TA0.2/S28	44	I/O	General-purpose digital I/O with mappable secondary function Default mapping: Timer TA0 capture CCR2: CCI2A input, compare: Out2 output LCD segment output S28
P3.4/PM_SDCLK/S27	45	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B bit stream clock input/output LCD segment output S27
P3.5/PM_SD0DIO/S26	46	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-0 bit stream data input/output LCD segment output S26
P3.6/PM_SD1DIO/S25	47	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-1 bit stream data input/output LCD segment output S25
P3.7/PM_SD2DIO/S24	48	I/O	General-purpose digital I/O with mappable secondary function Default mapping: SD24_B converter-2 bit stream data input/output (not available on F672x devices) LCD segment output S24
P4.0/S23	49	I/O	General-purpose digital I/O LCD segment output S23
P4.1/S22	50	I/O	General-purpose digital I/O LCD segment output S22
P4.2/S21	51	I/O	General-purpose digital I/O LCD segment output S21
P4.3/S20	52	I/O	General-purpose digital I/O LCD segment output S20
P4.4/S19	53	I/O	General-purpose digital I/O LCD segment output S19
P4.5/S18	54	I/O	General-purpose digital I/O LCD segment output S18
P4.6/S17	55	I/O	General-purpose digital I/O LCD segment output S17
P4.7/S16	56	I/O	General-purpose digital I/O LCD segment output S16

Table 6. Terminal Functions, MSP430F67xxIPN (continued)

TERMINAL NAME	NO. PN	I/O [1]	DESCRIPTION
P5.0/S15	57	I/O	General-purpose digital I/O LCD segment output S15
P5.1/S14	58	I/O	General-purpose digital I/O LCD segment output S14
DVSYS [5]	59		Digital power supply for I/Os
DVSS	60		Digital ground supply
P5.2/S13	61	I/O	General-purpose digital I/O LCD segment output S13
P5.3/S12	62	I/O	General-purpose digital I/O LCD segment output S12
P5.4/S11	63	I/O	General-purpose digital I/O LCD segment output S11
P5.5/S10	64	I/O	General-purpose digital I/O LCD segment output S10
P5.6/S9	65	I/O	General-purpose digital I/O LCD segment output S9
P5.7/S8	66	I/O	General-purpose digital I/O LCD segment output S8
P6.0/S7	67	I/O	General-purpose digital I/O LCD segment output S7
P6.1/S6	68	I/O	General-purpose digital I/O LCD segment output S6
P6.2/S5	69	I/O	General-purpose digital I/O LCD segment output S5
P6.3/S4	70	I/O	General-purpose digital I/O LCD segment output S4
P6.4/S3	71	I/O	General-purpose digital I/O LCD segment output S3
P6.5/S2	72	I/O	General-purpose digital I/O LCD segment output S2
P6.6/S1	73	I/O	General-purpose digital I/O LCD segment output S1
P6.7/S0	74	I/O	General-purpose digital I/O LCD segment output S0
TEST/SBWTCK	75	I	Test mode pin – select digital I/O on JTAG pins Spy-Bi-Wire input clock
PJ.0/SMCLK/TDO	76	I/O	General-purpose digital I/O SMCLK clock output Test data output
PJ.1/MCLK/TDI/TCLK	77	I/O	General-purpose digital I/O MCLK clock output Test data input or Test clock input

(5) The pins VDSYS and DVSYS must be connected externally on board for proper device operation.

Table 6. Terminal Functions, MSP430F67xxIPN (continued)

TERMINAL		I/O[(1)]	DESCRIPTION
NAME	NO. PN		
PJ.2/ADC10CLK/TMS	78	I/O	General-purpose digital I/O ADC10_A clock output Test mode select
PJ.3/ACLK/TCK	79	I/O	General-purpose digital I/O ACLK clock output Test clock
$\overline{\text{RST}}$/NMI/SBWTDIO	80	I/O	Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output

SHORT-FORM DESCRIPTION

CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

Program Counter	PC/R0
Stack Pointer	SP/R1
Status Register	SR/CG1/R2
Constant Generator	CG2/R3
General-Purpose Register	R4
General-Purpose Register	R5
General-Purpose Register	R6
General-Purpose Register	R7
General-Purpose Register	R8
General-Purpose Register	R9
General-Purpose Register	R10
General-Purpose Register	R11
General-Purpose Register	R12
General-Purpose Register	R13
General-Purpose Register	R14
General-Purpose Register	R15

Instruction Set

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data. Table 7 shows examples of the three types of instruction formats; Table 8 shows the address modes.

Table 7. Instruction Word Formats

INSTRUCTION WORD FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4,R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, un/conditional	JNE	Jump-on-equal bit = 0

Table 8. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	+	+	MOV Rs,Rd	MOV R10,R11	R10 → R11
Indexed	+	+	MOV X(Rn),Y(Rm)	MOV 2(R5),6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	+	+	MOV EDE,TONI		M(EDE) → M(TONI)
Absolute	+	+	MOV & MEM, & TCDAT		M(MEM) → M(TCDAT)
Indirect	+		MOV @Rn,Y(Rm)	MOV @R10,Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	+		MOV @Rn+,Rm	MOV @R10+,R11	M(R10) → R11 R10 + 2 → R10
Immediate	+		MOV #X,TONI	MOV #45,TONI	#45 → M(TONI)

(1) S = source, D = destination

Operating Modes

The MSP430 has one active mode and seven software selectable low-power modes of operation. An interrupt event can wake up the device from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following seven operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
  - FLL loop control remains active
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - FLL loop control is disabled
  - ACLK and SMCLK remain active, MCLK is disabled
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and FLL loop control and DCOCLK are disabled
  - DCO's dc-generator remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK, FLL loop control, and DCOCLK are disabled
  - DCO's dc-generator is disabled
  - Crystal oscillator is stopped
  - Complete data retention
- Low-power mode 3.5 (LPM3.5)
  - Internal regulator disabled
  - No RAM retention, Backup RAM retained
  - I/O pad state retention
  - RTC clocked by low-frequency oscillator
  - Wakeup from $\overline{RST}$/NMI, RTC_C events, Ports P1 and P2
- Low-power mode 4.5 (LPM4.5)
  - Internal regulator disabled
  - No RAM retention, Backup RAM retained
  - RTC is disabled
  - I/O pad state retention
  - Wakeup from $\overline{RST}$/NMI, Ports P1 and P2

Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 9. Interrupt Sources, Flags, and Vectors of MSP430F67xx Configurations

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power-Up External Reset Watchdog Timeout, Key Violation Flash Memory Key Violation	WDTIFG, KEYV (SYSRSTIV)(1)(2)	Reset	0FFFEh	63, highest
System NMI PMM Vacant Memory Access JTAG Mailbox	SVMLIFG, SVMHIFG, DLYLIFG, DLYHIFG, VLRLIFG, VLRHIFG, VMAIFG, JMBNIFG, JMBOUTIFG (SYSSNIV) (1)(3)	(Non)maskable	0FFFCh	62
User NMI NMI Oscillator Fault Flash Memory Access Violation Supply Switch	NMIIFG, OFIFG, ACCVIFG, AUXSWNMIFG (SYSUNIV)(1)(3)	(Non)maskable	0FFFAh	61
Watchdog Timer_A Interval Timer Mode	WDTIFG	Maskable	0FFF8h	60
eUSCI_A0 Receive or Transmit	UCA0RXIFG, UCA0TXIFG (UCA0IV)(1)(4)	Maskable	0FFF6h	59
eUSCI_B0 Receive or Transmit	UCB0RXIFG, UCB0TXIFG (UCB0IV)(1)(4)	Maskable	0FFF4h	58
ADC10_A	ADC10IFG0, ADC10INIFG, ADC10LOIFG, ADC10HIIFG, ADC10TOVIFG, ADC10OVIFG (ADC10IV)(1)(4)	Maskable	0FFF2h	57
SD24_B	SD24_B Interrupt Flags (SD24IV)(1)(4)	Maskable	0FFF0h	56
Timer TA0	TA0CCR0 CCIFG0(4)	Maskable	0FFEEh	55
Timer TA0	TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV)(1)(4)	Maskable	0FFECh	54
eUSCI_A1 Receive or Transmit	UCA1RXIFG, UCA1TXIFG (UCA1IV)(1)(4)	Maskable	0FFEAh	53
eUSCI_A2 Receive or Transmit	UCA2RXIFG, UCA2TXIFG (UCA2IV)(1)(4)	Maskable	0FFE8h	52
Auxiliary Supplies	Auxiliary Supplies Interrupt Flags (AUXIV)(1)(4)	Maskable	0FFE6h	51
DMA	DMA0IFG, DMA1IFG, DMA2IFG (DMAIV)(1)(4)	Maskable	0FFE4h	50
Timer TA1	TA1CCR0 CCIFG0(4)	Maskable	0FFE2h	49
Timer TA1	TA1CCR1 CCIFG1, TA1IFG (TA1IV)(1)(4)	Maskable	0FFE0h	48
I/O Port P1	P1IFG.0 to P1IFG.7 (P1IV)(1)(4)	Maskable	0FFDEh	47
Timer TA2	TA2CCR0 CCIFG0(4)	Maskable	0FFDCh	46
Timer TA2	TA2CCR1 CCIFG1, TA2IFG (TA2IV)(1)(4)	Maskable	0FFDAh	45
I/O Port P2	P2IFG.0 to P2IFG.7 (P2IV)(1)(4)	Maskable	0FFD8h	44
Timer TA3	TA3CCR0 CCIFG0(4)	Maskable	0FFD6h	43
Timer TA3	TA3CCR1 CCIFG1, TA3IFG (TA3IV)(1)(4)	Maskable	0FFD4h	42
LCD_C	LCD_C Interrupt Flags (LCDCIV)(1)(4)	Maskable	0FFD2h	41
RTC_C	RTCOFIFG, RTCRDYIFG, RTCTEVIFG, RTCAIFG, RT0PSIFG, RT1PSIFG (RTCIV)(1)(4)	Maskable	0FFD0h	40

(1) Multiple source flags
(2) A reset is generated if the CPU tries to fetch instructions from within peripheral space or vacant memory space.
(3) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable cannot disable it.
(4) Interrupt flags are located in the module.

Table 9. Interrupt Sources, Flags, and Vectors of MSP430F67xx Configurations (continued)

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Reserved	Reserved(5)		0FFCEh	39
			⋮	⋮
			0FF80h	0, lowest

(5) Reserved interrupt vectors at addresses are not used in this device and can be used for regular program code if necessary. To maintain compatibility with other devices, it is recommended to reserve these locations.

Memory Organization

Table 10. Memory Organization

		MSP430F6730 MSP430F6720	MSP430F6731 MSP430F6721	MSP430F6733 MSP430F6723
Main Memory (flash)	Total Size	16kB	32kB	64kB
Main: Interrupt vector		00FFFFh to 00FF80h	00FFFFh to 00FF80h	00FFFFh to 00FF80h
Main: code memory	Bank 3	not available	not available	not available
	Bank 2	not available	not available	not available
	Bank 1	not available	16kB 00FFFFh to 00C000h	32kB 013FFFh to 00C000h
	Bank 0	16kB 00FFFFh to 00C000h	16kB 00BFFFh to 008000h	32kB 00BFFFh to 004000h
RAM	Total Size	1kB	2kB	4kB
	Sector 3	not available	not available	not available
	Sector 2	not available	not available	not available
	Sector 1	not available	not available	2kB 002BFFh to 002400h
	Sector 0	1kB 001FFFh to 001C00h	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals		4 KB 000FFFh to 0h	4 KB 000FFFh to 0h	4 KB 000FFFh to 0h

		MSP430F6734 MSP430F6724	MSP430F6735 MSP430F6725	MSP430F6736 MSP430F6726
Main Memory (flash)	Total Size	96kB	128kB	128kB
Main: Interrupt vector		00FFFFh to 00FF80h	00FFFFh to 00FF80h	00FFFFh to 00FF80h
Main: code memory	Bank 3	not available	32kB 023FFFh to 01C000h	32kB 023FFFh to 01C000h
	Bank 2	32kB 01BFFFh to 014000h	32kB 01BFFFh to 014000h	32kB 01BFFFh to 014000h
	Bank 1	32kB 013FFFh to 00C000h	32kB 013FFFh to 00C000h	32kB 013FFFh to 00C000h
	Bank 0	32kB 00BFFFh to 004000h	32kB 00BFFFh to 004000h	32kB 00BFFFh to 004000h
RAM	Total Size	4kB	4kB	8kB
	Sector 3	not available	not available	2kB 003BFFh to 003400h
	Sector 2	not available	not available	2kB 0033FFh to 002C00h
	Sector 1	2kB 002BFFh to 002400h	2kB 002BFFh to 002400h	2kB 002BFFh to 002400h
	Sector 0	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h	2kB 0023FFh to 001C00h
Information memory (flash)	Info A	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h	128 B 0019FFh to 001980h
	Info B	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h	128 B 00197Fh to 001900h
	Info C	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h	128 B 0018FFh to 001880h
	Info D	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h	128 B 00187Fh to 001800h
Bootstrap loader (BSL) memory (flash)	BSL 3	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h	512 B 0017FFh to 001600h
	BSL 2	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h	512 B 0015FFh to 001400h
	BSL 1	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h	512 B 0013FFh to 001200h
	BSL 0	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h	512 B 0011FFh to 001000h
Peripherals		4 KB 000FFFh to 0h	4 KB 000FFFh to 0h	4 KB 000FFFh to 0h

Bootstrap Loader (BSL)

The BSL enables users to program the flash memory or RAM using various serial interfaces. Access to the device memory via the BSL is protected by an user-defined password. BSL entry requires a specific entry sequence on the RST/NMI/SBWTDIO and TEST/SBWTCK pins. For complete description of the features of the BSL and its implementation, see *MSP430 Programming via the Bootstrap Loader (BSL)* (SLAU319).

Table 11. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
RST/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P3.0	Data transmit
P3.1	Data receive
VCC	Power supply
VSS	Ground supply

JTAG Operation

JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the RST/NMI/SBWTDIO is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in Table 12. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278) and *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 12. JTAG Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
PJ.3/ACLK/TCK	IN	JTAG clock input
PJ.2/ADC10CLK/TMS	IN	JTAG state control
PJ.1/MCLK/TDI/TCLK	IN	JTAG data input/TCLK input
PJ.0/SMCLK/TDO	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
VCC		Power supply
VSS		Ground supply

Spy-Bi-Wire Interface

In addition to the standard JTAG interface, the MSP430 family supports the two-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. The Spy-Bi-Wire interface pin requirements are shown in Table 13. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* (SLAU278) and *MSP430 Programming Via the JTAG Interface* (SLAU320).

Table 13. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input/output
VCC		Power supply
VSS		Ground supply

Flash Memory

The flash memory can be programmed via the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. The CPU can perform single-byte, single-word, and long-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and four segments of information memory (A to D) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A to D can be erased individually, or as a group with segments 0 to n. Segments A to D are also called *information memory*.
- Segment A can be locked separately.

RAM Memory

The RAM memory is made up of n sectors. Each sector can be completely powered down to save leakage, however all data is lost. Features of the RAM memory include:

- RAM memory has n sectors of 2k bytes each.
- Each sector 0 to n can be complete disabled; however, data retention is lost.
- Each sector 0 to n automatically enters low-power retention mode when possible.

Backup RAM Memory

The Backup RAM provides a limited number of bytes of RAM that are retained during LPMx.5. This Backup RAM is part of Backup subsystem in MSP430F67xx that operates on dedicated power supply AUXVCC3.There are 8 bytes of Backup RAM available in this device. It can be wordwise accessed via the registers BAKMEM0, BAKMEM1, BAKMEM2, and BAKMEM3. The Backup RAM registers can not be accessed by CPU when the high side SVS is disabled by user.

Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

Oscillator and System Clock

The Unified Clock System (UCS) module includes support for a 32768-Hz watch crystal oscillator, an internal very-low-power low-frequency oscillator (VLO), an internal trimmed low-frequency oscillator (REFO), and an integrated internal digitally-controlled oscillator (DCO). The UCS module is designed to meet the requirements of both low system cost and low power consumption. The UCS module features digital frequency locked loop (FLL) hardware that, in conjunction with a digital modulator, stabilizes the DCO frequency to a programmable multiple of the selected FLL reference frequency. The internal DCO provides a fast turn-on clock source and stabilizes in 3 µs (typical). The UCS module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal, the internal low-frequency oscillator (VLO), or the trimmed low-frequency oscillator (REFO).
- Main clock (MCLK), the system clock used by the CPU. MCLK can be sourced by same sources made available to ACLK.
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules. SMCLK can be sourced by same sources made available to ACLK.
- ACLK/n, the buffered output of ACLK, ACLK/2, ACLK/4, ACLK/8, ACLK/16, ACLK/32.

Power Management Module (PMM)

The PMM includes an integrated voltage regulator that supplies the core voltage to the device and contains programmable output levels to provide for power optimization. The PMM also includes supply voltage supervisor (SVS) and supply voltage monitoring (SVM) circuitry, as well as brownout protection. The brownout circuit is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS/SVM circuitry detects if the supply voltage drops below a user-selectable level and supports both supply voltage supervision (the device is automatically reset) and supply voltage monitoring (the device is not automatically reset). SVS and SVM circuitry is available on the primary supply and core supply.

Auxiliary Supply System

The auxiliary supply system provides the possibility to operate the device from auxiliary supplies when the primary supply fails.There are two auxililary supplies AUXVCC1 and AUXVCC2 supported in MSP430F67xx. This module supports automatic and manual switching from primary supply to auxiliary suppllies while maintaining full functionality. It allows threshold based monitoring of primary and auxiliary supplies. The device can be started from primary supply or AUXVCC1, whichever is higher. Auxiliary supply system enables internal monitoring of voltage levels on primary and auxiliary supplies using ADC10_A. Also this module implements simple charger for backup supplies.

Backup Subsystem

The Backup subsystem operates on a dedicated power supply AUXVCC3. This subsystem includes low-frequency oscillator (XT1), Real-Time Clock module, and Backup RAM. The functionality of Backup subsystem is retained during LPM3.5. The Backup susb-system module registers can not be accessed by CPU when the high side SVS is disabled by user. It is necessary to keep the high side SVS enabled with SVSHMD = 1 and SVSMHACE = 0 to turn off the low-frequency oscillator (XT1) in LPM4.

Digital I/O

There are up to nine 8-bit I/O ports implemented. For 100 pin options, Ports P1 to P8 are complete. P9 is reduced to 4-bit I/O. For 80 pin options, Ports P1 to P6 are complete. P7, P8 and P9 are completely removed. Port PJ contains four individual I/O pins, common to all devices. All I/O bits are individually programmable.

- Any combination of input, output and interrupt conditions is possible.
- Pullup or pulldown on all ports is programmable.
- Programmable drive strength on all ports.
- Edge-selectable interrupt and LPM3.5, LPM4.5 wakeup input capability available for all bits of ports P1 and P2.
- Read-write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise (P1 through P9) or word-wise in pairs (PA through PE).

Port Mapping Controller

The port mapping controller allows flexible and reconfigurable mapping of digital functions to P1, P2, and P3.

Table 14. Port Mapping Mnemonics and Functions

VALUE	PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
0	PM_NONE	None	DVSS
1	PM_UCA0RXD	eUSCI_A0 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA0SOMI	eUSCI_A0 SPI slave out master in (direction controlled by eUSCI)	
2	PM_UCA0TXD	eUSCI_A0 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA0SIMO	eUSCI_A0 SPI slave in master out (direction controlled by eUSCI)	
3	PM_UCA0CLK	eUSCI_A0 clock input/output (direction controlled by eUSCI)	
4	PM_UCA0STE	eUSCI_A0 SPI slave transmit enable (direction controlled by eUSCI)	
5	PM_UCA1RXD	eUSCI_A1 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA1SOMI	eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
6	PM_UCA1TXD	eUSCI_A1 UART TXD (direction controlled by eUSCI – Output)	
	PM_UCA1SIMO	eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
7	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
8	PM_UCA1STE	eUSCI_A1 SPI slave transmit enable (direction controlled by eUSCI)	
9	PM_UCA2RXD	eUSCI_A2 UART RXD (direction controlled by eUSCI – Input)	
	PM_UCA2SOMI	eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
10	PM_UCA2TXD	eUSCI_A2 UART TXD (direction controlled by eUSCI – Output)	
	PM_ UCA2SIMO	eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
11	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
12	PM_UCA2STE	eUSCI_A2 SPI slave transmit enable (direction controlled by eUSCI)	
13	PM_UCB0SIMO	eUSCI_B0 SPI slave in master out (direction controlled by eUSCI)	
	PM_UCB0SDA	eUSCI_B0 I2C data (open drain and direction controlled by eUSCI)	
14	PM_UCB0SOMI	eUSCI_B0 SPI slave out master in (direction controlled by eUSCI)	
	PM_UCB0SCL	eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI)	
15	PM_UCB0CLK	eUSCI_B0 clock input/output (direction controlled by eUSCI)	
16	PM_UCB0STE	eUSCI_B0 SPI slave transmit enable (direction controlled by eUSCI)	
17	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
18	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
19	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
20	PM_TA1.0	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0
21	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
22	PM_TA2.0	TA2 CCR0 capture input CCI0A	TA2 CCR0 compare output Out0
23	PM_TA2.1	TA2 CCR1 capture input CCI1A	TA2 CCR1 compare output Out1
24	PM_TA3.0	TA3 CCR0 capture input CCI0A	TA3 CCR0 compare output Out0
25	PM_TA3.1	TA3 CCR1 capture input CCI1A	TA3 CCR1 compare output Out1
26	PM_TACLK	Timer_A clock input to TA0, TA1, TA2, TA3	None
	PM_RTCCLK	None	RTC_C clock output
27	PM_SDCLK	SD24_B bit stream clock input/output (direction controlled by SD24_B)	
28	PM_SD0DIO	SD24_B converter-0 bit stream data input/output (direction controlled by SD24_B)	
29	PM_SD1DIO	SD24_B converter-1 bit stream data input/output (direction controlled by SD24_B)	
30	PM_SD2DIO	SD24_B converter-2 bit stream data input/output (direction controlled by SD24_B)	
31(0FFh)[(1)]	PM_ANALOG	Disables the output driver as well as the input Schmitt-trigger to prevent parasitic cross currents when applying analog signals.	

(1) The value of the PM_ANALOG mnemonic is set to 0FFh. The port mapping registers are only 5 bits wide and the upper bits are ignored resulting in a read out value of 31.

Table 15. Default Mapping

PIN NAME		PxMAPy MNEMONIC	INPUT PIN FUNCTION	OUTPUT PIN FUNCTION
PZ	PN			
P1.0/PM_TA0.0/ VeREF-/A2	P1.0/PM_TA0.0/ VeREF-/A2	PM_TA0.0	TA0 CCR0 capture input CCI0A	TA0 CCR0 compare output Out0
P1.1/PM_TA0.1/ VeREF+/A1	P1.1/PM_TA0.1/ VeREF+/A1	PM_TA0.1	TA0 CCR1 capture input CCI1A	TA0 CCR1 compare output Out1
P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0	P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0	PM_UCA0RXD, PM_UCA0SOMI	eUSCI_A0 UART RXD (direction controlled by eUSCI – input), eUSCI_A0 SPI slave out master in (direction controlled by eUSCI)	
P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03	P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03	PM_UCA0TXD, PM_UCA0SIMO	eUSCI_A0 UART TXD (direction controlled by eUSCI – output), eUSCI_A0 SPI slave in master out (direction controlled by eUSCI)	
P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13	P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13	PM_UCA1RXD, PM_UCA1SOMI	eUSCI_A1 UART RXD (direction controlled by eUSCI – input), eUSCI_A1 SPI slave out master in (direction controlled by eUSCI)	
P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23	P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23	PM_UCA1TXD, PM_UCA1SIMO	eUSCI_A1 UART TXD (direction controlled by eUSCI – output), eUSCI_A1 SPI slave in master out (direction controlled by eUSCI)	
P1.6/PM_UCA0CLK/ COM4	P1.6/PM_UCA0CLK/ COM4	PM_UCA0CLK	eUSCI_A0 clock input/output (direction controlled by eUSCI)	
P1.7/PM_UCB0CLK/ COM5	P1.7/PM_UCB0CLK/ COM5	PM_UCB0CLK	eUSCI_B0 clock input/output (direction controlled by eUSCI)	
P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6	P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6/S39	PM_UCB0SOMI, PM_UCB0SCL	eUSCI_B0 SPI slave out master in (direction controlled by eUSCI), eUSCI_B0 I2C clock (open drain and direction controlled by eUSCI)	
P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7	P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7/S38	PM_UCB0SIMO, PM_UCB0SDA	eUSCI_B0 SPI slave in master out (direction controlled by eUSCI), eUSCI_B0 I2C data (open drain and direction controlled by eUSCI)	
P2.2/PM_UCA2RXD/ PM_UCA2SOMI	P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37	PM_UCA2RXD, PM_UCA2SOMI	eUSCI_A2 UART RXD (direction controlled by eUSCI – input), eUSCI_A2 SPI slave out master in (direction controlled by eUSCI)	
P2.3/PM_UCA2TXD/ PM_UCA2SIMO	P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36	PM_UCA2TXD, PM_UCA2SIMO	eUSCI_A2 UART TXD (direction controlled by eUSCI – output), eUSCI_A2 SPI slave in master out (direction controlled by eUSCI)	
P2.4/PM_UCA1CLK	P2.4/PM_UCA1CLK/S35	PM_UCA1CLK	eUSCI_A1 clock input/output (direction controlled by eUSCI)	
P2.5/PM_UCA2CLK	P2.5/PM_UCA2CLK/S34	PM_UCA2CLK	eUSCI_A2 clock input/output (direction controlled by eUSCI)	
P2.6/PM_TA1.0	P2.6/PM_TA1.0/S33	PM_TA1.0	TA1 CCR0 capture input CCI0A	TA1 CCR0 compare output Out0
P2.7/PM_TA1.1	P2.7/PM_TA1.1/S32	PM_TA1.1	TA1 CCR1 capture input CCI1A	TA1 CCR1 compare output Out1
P3.0/PM_TA2.0	P3.0/PM_TA2.0/S31	PM_TA2.0	TA2 CCR0 capture input CCI0A	TA2 CCR0 compare output Out0
P3.1/PM_TA2.1	P3.1/PM_TA2.1/S30	PM_TA2.1	TA2 CCR1 capture input CCI1A	TA2 CCR1 compare output Out1
P3.2/PM_TACLK/ PM_RTCCLK	P3.2/PM_TACLK/ PM_RTCCLK/S29	PM_TACLK, PM_RTCCLK	Timer_A clock input to TA0, TA1, TA2, TA3	RTC_C clock output
P3.3/PM_TA0.2	P3.3/PM_TA0.2/S28	PM_TA0.2	TA0 CCR2 capture input CCI2A	TA0 CCR2 compare output Out2
P3.4/PM_SDCLK/S39	P3.4/PM_SDCLK/S27	PM_SDCLK	SD24_B bit stream clock input/output (direction controlled by SD24_B)	
P3.5/PM_SD0DIO/S38	P3.5/PM_SD0DIO/S26	PM_SD0DIO	SD24_B converter-0 bit stream data input/output (direction controlled by SD24_B)	
P3.6/PM_SD1DIO/S37	P3.6/PM_SD1DIO/S25	PM_SD1DIO	SD24_B converter-1 bit stream data input/output (direction controlled by SD24_B)	
P3.7/PM_SD2DIO/S36	P3.7/PM_SD2DIO/S24	PM_SD2DIO	SD24_B converter-2 bit stream data input/output (direction controlled by SD24_B)	

System Module (SYS)

The SYS module handles many of the system functions within the device. These include power on reset (POR) and power up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, boot strap loader entry mechanisms, as well as, configuration management (device descriptors). It also includes a data exchange mechanism via JTAG called a JTAG mailbox that can be used in the application.

Table 16. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	INTERRUPT EVENT	WORD ADDRESS	OFFSET	PRIORITY
SYSRSTIV, System Reset	No interrupt pending	019Eh	00h	
	Brownout (BOR)		02h	Highest
	RST/NMI (POR)		04h	
	DoBOR (BOR)		06h	
	Wakeup from LPMx.5 (BOR)		08h	
	Security violation (BOR)		0Ah	
	SVSL (POR)		0Ch	
	SVSH (POR)		0Eh	
	SVML_OVP (POR)		10h	
	SVMH_OVP (POR)		12h	
	DoPOR (POR)		14h	
	WDT timeout (PUC)		16h	
	WDT key violation (PUC)		18h	
	KEYV flash key violation (PUC)		1Ah	
	Reserved		1Ch	
	Peripheral area fetch (PUC)		1Eh	
	PMM key violation (PUC)		20h	
	Reserved		22h to 3Eh	Lowest
SYSSNIV, System NMI	No interrupt pending	019Ch	00h	
	SVMLIFG		02h	Highest
	SVMHIFG		04h	
	DLYLIFG		06h	
	DLYHIFG		08h	
	VMAIFG		0Ah	
	JMBINIFG		0Ch	
	JMBOUTIFG		0Eh	
	VLRLIFG		10h	
	VLRHIFG		12h	
	Reserved		14h to 1Eh	Lowest
SYSUNIV, User NMI	No interrupt pending	019Ah	00h	
	NMIFG		02h	Highest
	OFIFG		04h	
	ACCVIFG		06h	
	AUXSWNMIFG		08h	
	Reserved		0Ah to 1Eh	Lowest

Watchdog Timer (WDT_A)

The primary function of the watchdog timer (WDT_A) module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the timer can be configured as an interval timer and can generate interrupts at selected time intervals.

DMA Controller

The DMA controller allows movement of data from one memory address to another without CPU intervention. For example, the DMA controller can be used to move data from the ADC10_A conversion memory to RAM. Using the DMA controller can increase the throughput of peripheral modules. The DMA controller reduces system power consumption by allowing the CPU to remain in sleep mode, without having to awaken to move data to or from a peripheral.

Table 17. DMA Trigger Assignments(1)

TRIGGER	CHANNEL		
	0	1	2
0	DMAREQ		
1	TA0CCR0 CCIFG		
2	TA0CCR2 CCIFG		
3	TA1CCR0 CCIFG		
4	Reserved		
5	TA2CCR0 CCIFG		
6	Reserved		
7	TA3CCR0 CCIFG		
8	Reserved		
9	Reserved		
10	Reserved		
11	Reserved		
12	Reserved		
13	SD24IFG		
14	Reserved		
15	Reserved		
16	UCA0RXIFG		
17	UCA0TXIFG		
18	UCA1RXIFG		
19	UCA1TXIFG		
20	UCA2RXIFG		
21	UCA2TXIFG		
22	UCB0RXIFG0		
23	UCB0TXIFG0		
24	ADC10IFG0		
25	Reserved		
26	Reserved		
27	Reserved		
28	Reserved		
29	MPY ready		
30	DMA2IFG	DMA0IFG	DMA1IFG
31	Reserved		

(1) Reserved DMA triggers may be used by other devices in the family. Reserved DMA triggers do not cause any DMA trigger event when selected.

CRC16

The CRC16 module produces a signature based on a sequence of entered data values and can be used for data checking purposes. The CRC16 module signature is based on the CRC-CCITT standard.

Hardware Multiplier

The multiplication operation is supported by a dedicated peripheral module. The module performs operations with 32-bit, 24-bit, 16-bit, and 8-bit operands. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations.

Enhanced Universal Serial Communication Interface (eUSCI)

The eUSCI module is used for serial data communication. The eUSCI module supports synchronous communication protocols such as SPI (3 or 4 pin) and I^2C, and asynchronous communication protocols such as UART, enhanced UART with automatic baudrate detection, and IrDA.

The eUSCI_An module supports for SPI (3 or 4 pin), UART, enhanced UART, or IrDA.

The eUSCI_Bn module supports for SPI (3 or 4 pin) or I2C.

Three eUSCI_A and one eUSCI_B module are implemented in MSP430F67xx devices.

ADC10_A

The ADC10_A module supports fast 10-bit analog-to-digital conversions. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion results buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

SD24_B

The SD24_B module integrates up to three independent 24-bit sigma-delta A/D converters. Each converter is designed with a fully differential analog input pair and programmable gain amplifier input stage. The converters are based on second-order over-sampling sigma-delta modulators and digital decimation filters. The decimation filters are comb type filters with selectable oversampling ratios of up to 1024.

TA0

TA0 is a 16-bit timer/counter (Timer_A type) with three capture/compare registers. TA0 can support multiple capture/compares, PWM outputs, and interval timing. TA0 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 18. TA0 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
PM_TACLK	TACLK	Timer	NA	NA
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
PM_TACLK	INCLK			
PM_TA0.0	CCI0A	CCR0	TA0	PM_TA0.0
DVSS	CCI0B			
DVSS	GND			
DVCC	VCC			
PM_TA0.1	CCI1A	CCR1	TA1	PM_TA0.1
ACLK (internal)	CCI1B			ADC10_A (internal) ADC10SHSx = {1}
DVSS	GND			SD24_B (internal) SD24SCSx = {1}
DVCC	VCC			
PM_TA0.2	CCI2A	CCR2	TA2	PM_TA0.2
DVSS	CCI2B			
DVSS	GND			
DVCC	VCC			

TA1

TA1 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA1 can support multiple capture/compares, PWM outputs, and interval timing. TA1 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 19. TA1 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
				PZ
PM_TACLK	TACLK	Timer	NA	NA
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
PM_TACLK	INCLK			
PM_TA1.0	CCI0A	CCR0	TA0	PM_TA1.0
DVSS	CCI0B			
DVSS	GND			
DVCC	VCC			
PM_TA1.1	CCI1A	CCR1	TA1	PM_TA1.1
ACLK (internal)	CCI1B			
DVSS	GND			
DVCC	VCC			

TA2

TA2 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA2 can support multiple capture/compares, PWM outputs, and interval timing. TA2 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 20. TA2 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
PM_TACLK	TACLK	Timer	NA	NA
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
PM_TACLK	INCLK			
PM_TA2.0	CCI0A	CCR0	TA0	PM_TA2.0
DVSS	CCI0B			
DVSS	GND			
DVCC	VCC			
PM_TA2.1	CCI1A	CCR1	TA1	PM_TA2.1
ACLK (internal)	CCI1B			SD24_B (internal) SD24SCSx = {2}
DVSS	GND			
DVCC	VCC			

TA3

TA3 is a 16-bit timer/counter (Timer_A type) with two capture/compare registers. TA3 can support multiple capture/compares, PWM outputs, and interval timing. TA3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 21. TA3 Signal Connections

DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
PM_TACLK	TACLK	Timer	NA	
ACLK (internal)	ACLK			
SMCLK (internal)	SMCLK			
PM_TACLK	INCLK			
PM_TA3.0	CCI0A	CCR0	TA0	PM_TA3.0
DVSS	CCI0B			ADC10_A (internal) ADC10SHSx = {2}
DVSS	GND			
DVCC	VCC			
PM_TA3.1	CCI1A	CCR1	TA1	PM_TA3.1
ACLK (internal)	CCI1B			SD24_B (internal) SD24SCSx = {3}
DVSS	GND			
DVCC	VCC			

SD24_B Triggers

Table 22 shows the input trigger connections to SD24_B converters from Timer_A modules and output trigger pulse connection from SD24_B to ADC10_A.

Table 22. SD24_B Input/Output Trigger Connections

DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
TA0.1 (internal)	SD24_B SD24SCSx = {1}	SD24_B	Trigger Pulse	ADC10_A (internal) ADC10SHSx = {3}
TA2.1 (internal)	SD24_B SD24SCSx = {2}			
TA3.1 (internal)	SD24_B SD24SCSx = {3}			

ADC10_A Triggers

Table 23 shows input trigger connections to ADC10_A from Timer_A modules and SD24_B.

Table 23. ADC10_A Input Trigger Connections

DEVICE INPUT SIGNAL	MODULE INPUT SIGNAL	MODULE BLOCK
TA0.1 (internal)	ADC10_A ADC10SHSx = {1}	ADC10_A
TA3.0 (internal)	ADC10_A ADC10SHSx = {2}	
SD24_B trigger pulse (internal)	ADC10_A ADC10SHSx = {3}	

Real-Time Clock (RTC_C)

The RTC_C module can be configured for real-time clock (RTC) or calendar mode providing seconds, hours, day of week, day of month, month, and year. The RTC_C control and configuration registers are password protected to ensure clock integrity against runaway code. Calendar mode integrates an internal calendar that compensates for months with less than 31 days and includes leap year correction. The RTC_C also supports flexible alarm functions, offset calibration, and temperature compensation. The RTC_C on this device operates on dedicated AUXVCC3 supply and supports operation in LPM3.5.

REF Voltage Reference

The reference module (REF) is responsible for generation of all critical reference voltages that can be used by the various analog peripherals in the device. These include the ADC10_A, LCD_C, and SD24_B modules.

LCD_C

The LCD_C driver generates the segment and common signals required to drive a liquid crystal display (LCD). The LCD_C controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, 4-mux, up to 8-mux LCDs are supported. The module can provide a LCD voltage independent of the supply voltage with its integrated charge pump. It is possible to control the level of the LCD voltage and thus contrast by software. The module also provides an automatic blinking capability for individual segments in static, 2-mux, 3-mux, and 4-mux modes.

Embedded Emulation Module (EEM) (S Version)

The Embedded Emulation Module (EEM) supports real-time in-system debugging. The S version of the EEM implemented on all devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

Peripheral File Map

Table 24. Peripherals

MODULE NAME	BASE ADDRESS	OFFSET ADDRESS RANGE
Special Functions (see Table 25)	0100h	000h-01Fh
PMM (see Table 26)	0120h	000h-01Fh
Flash Control (see Table 27)	0140h	000h-00Fh
CRC16 (see Table 28)	0150h	000h-007h
RAM Control (see Table 29)	0158h	000h-001h
Watchdog (see Table 30)	015Ch	000h-001h
UCS (see Table 31)	0160h	000h-01Fh
SYS (see Table 32)	0180h	000h-01Fh
Shared Reference (see Table 33)	01B0h	000h-001h
Port Mapping Control (see Table 34)	01C0h	000h-007h
Port Mapping Port P1 (see Table 35)	01C8h	000h-007h
Port Mapping Port P2 (see Table 36)	01D0h	000h-007h
Port Mapping Port P3 (see Table 37)	01D8h	000h-007h
Port P1/P2 (see Table 38)	0200h	000h-01Fh
Port P3/P4 (see Table 39)	0220h	000h-00Bh
Port P5/P6 (see Table 40)	0240h	000h-00Bh
Port P7/P8 (see Table 41) (Port P7/P8 not available in MSP430F67xxIPN)	0260h	000h-00Bh
Port P9 (Port P9 not available in MSP430F67xxIPN) (see Table 42)	0280h	000h-00Bh
Port PJ (refer toTable 43)	0320h	000h-01Fh
Timer TA0 (see Table 44)	0340h	000h-03Fh
Timer TA1 (see Table 45)	0380h	000h-03Fh
Timer TA2 (see Table 46)	0400h	000h-03Fh
Timer TA3 (see Table 47)	0440h	000h-03Fh
Backup Memory (see Table 48)	0480h	000h-00Fh
RTC_C (see Table 49)	04A0h	000h-01Fh
32-bit Hardware Multiplier (see Table 50)	04C0h	000h-02Fh
DMA General Control (see Table 51)	0500h	000h-00Fh
DMA Channel 0 (see Table 52)	0500h	010h-01Fh
DMA Channel 1 (see Table 53)	0500h	020h-02Fh
DMA Channel 2 (see Table 54)	0500h	030h-03Fh
eUSCI_A0 (see Table 55)	05C0h	000h-01Fh
eUSCI_A1 (see Table 56)	05E0h	000h-01Fh
eUSCI_A2 (see Table 57)	0600h	000h-01Fh
eUSCI_B0 (see Table 58)	0640h	000h-02Fh
ADC10_A (see Table 59)	0740h	000h-01Fh
SD24_B(see Table 60)	0800h	000h-06Fh
Auxiliary Supply (see Table 54)	09E0h	000h-01Fh
LCD_C (see Table 62)	0A00h	000h-05Fh

Table 25. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

Table 26. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM Control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
SVS high side control	SVSMHCTL	04h
SVS low side control	SVSMLCTL	06h
PMM interrupt flags	PMMIFG	0Ch
PMM interrupt enable	PMMIE	0Eh
PMM Power Mode 5 control register 0	PM5CTL0	10h

Table 27. Flash Control Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Flash control 1	FCTL1	00h
Flash control 3	FCTL3	04h
Flash control 4	FCTL4	06h

Table 28. CRC16 Registers (Base Address: 0150h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRC16DIRB	02h
CRC result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

Table 29. RAM Control Registers (Base Address: 0158h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RAM control 0	RCCTL0	00h

Table 30. Watchdog Registers (Base Address: 015Ch)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

Table 31. UCS Registers (Base Address: 0160h)

REGISTER DESCRIPTION	REGISTER	OFFSET
UCS control 0	UCSCTL0	00h
UCS control 1	UCSCTL1	02h
UCS control 2	UCSCTL2	04h
UCS control 3	UCSCTL3	06h
UCS control 4	UCSCTL4	08h
UCS control 5	UCSCTL5	0Ah
UCS control 6	UCSCTL6	0Ch
UCS control 7	UCSCTL7	0Eh
UCS control 8	UCSCTL8	10h

Table 32. SYS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootstrap loader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
Bus Error vector generator	SYSBERRIV	18h
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh

Table 33. Shared Reference Registers (Base Address: 01B0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Shared reference control	REFCTL	00h

Table 34. Port Mapping Controller (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port mapping password register	PMAPPWD	00h
Port mapping control register	PMAPCTL	02h

Table 35. Port Mapping for Port P1 (Base Address: 01C8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1.0 mapping register	P1MAP0	00h
Port P1.1 mapping register	P1MAP1	01h
Port P1.2 mapping register	P1MAP2	02h
Port P1.3 mapping register	P1MAP3	03h
Port P1.4 mapping register	P1MAP4	04h
Port P1.5 mapping register	P1MAP5	05h
Port P1.6 mapping register	P1MAP6	06h
Port P1.7 mapping register	P1MAP7	07h

Table 36. Port Mapping for Port P2 (Base Address: 01D0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P2.0 mapping register	P2MAP0	00h
Port P2.1 mapping register	P2MAP2	01h
Port P2.2 mapping register	P2MAP2	02h
Port P2.3 mapping register	P2MAP3	03h
Port P2.4 mapping register	P2MAP4	04h
Port P2.5 mapping register	P2MAP5	05h
Port P2.6 mapping register	P2MAP6	06h
Port P2.7 mapping register	P2MAP7	07h

Table 37. Port Mapping for Port P3 (Base Address: 01D8h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3.0 mapping register	P3MAP0	00h
Port P3.1 mapping register	P3MAP3	01h
Port P3.2 mapping register	P3MAP2	02h
Port P3.3 mapping register	P3MAP3	03h
Port P3.4 mapping register	P3MAP4	04h
Port P3.5 mapping register	P3MAP5	05h
Port P3.6 mapping register	P3MAP6	06h
Port P3.7 mapping register	P3MAP7	07h

Table 38. Port P1/P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pullup/pulldown enable	P1REN	06h
Port P1 drive strength	P1DS	08h
Port P1 selection	P1SEL	0Ah
Port P1 interrupt vector word	P1IV	0Eh
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pullup/pulldown enable	P2REN	07h
Port P2 drive strength	P2DS	09h
Port P2 selection	P2SEL	0Bh
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

Table 39. Port P3/P4 Registers (Base Address: 0220h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P3 input	P3IN	00h
Port P3 output	P3OUT	02h
Port P3 direction	P3DIR	04h
Port P3 pullup/pulldown enable	P3REN	06h
Port P3 drive strength	P3DS	08h
Port P3 selection	P3SEL	0Ah
Port P4 input	P4IN	01h
Port P4 output	P4OUT	03h
Port P4 direction	P4DIR	05h
Port P4 pullup/pulldown enable	P4REN	07h
Port P4 drive strength	P4DS	09h
Port P4 selection	P4SEL	0Bh

Table 40. Port P5/P6 Registers (Base Address: 0240h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P5 input	P5IN	00h
Port P5 output	P5OUT	02h
Port P5 direction	P5DIR	04h
Port P5 pullup/pulldown enable	P5REN	06h
Port P5 drive strength	P5DS	08h
Port P5 selection	P5SEL	0Ah
Port P6 input	P6IN	01h
Port P6 output	P6OUT	03h
Port P6 direction	P6DIR	05h
Port P6 pullup/pulldown enable	P6REN	07h
Port P6 drive strength	P6DS	09h
Port P6 selection	P6SEL	0Bh

Table 41. Port P7/P8 Registers (Base Address: 0260h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P7 input	P7IN	00h
Port P7 output	P7OUT	02h
Port P7 direction	P7DIR	04h
Port P7 pullup/pulldown enable	P7REN	06h
Port P7 drive strength	P7DS	08h
Port P7 selection	P7SEL	0Ah
Port P8 input	P8IN	01h
Port P8 output	P8OUT	03h
Port P8 direction	P8DIR	05h
Port P8 pullup/pulldown enable	P8REN	07h
Port P8 drive strength	P8DS	09h
Port P8 selection	P8SEL	0Bh

Table 42. Port P9 Registers (Base Address: 0280h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P9 input	P9IN	00h
Port P9 output	P9OUT	02h
Port P9 direction	P9DIR	04h
Port P9 pullup/pulldown enable	P9REN	06h
Port P9 drive strength	P9DS	08h
Port P9 selection	P9SEL	0Ah

Table 43. Port J Registers (Base Address: 0320h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port PJ input	PJIN	00h
Port PJ output	PJOUT	02h
Port PJ direction	PJDIR	04h
Port PJ pullup/pulldown enable	PJREN	06h
Port PJ drive strength	PJDS	08h
Port PJ selection	PJSEL	0Ah

Table 44. TA0 Registers (Base Address: 0340h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA0 control	TA0CTL	00h
Capture/compare control 0	TA0CCTL0	02h
Capture/compare control 1	TA0CCTL1	04h
Capture/compare control 2	TA0CCTL2	06h
TA0 counter register	TA0R	10h
Capture/compare register 0	TA0CCR0	12h
Capture/compare register 1	TA0CCR1	14h
Capture/compare register 2	TA0CCR2	16h
TA0 expansion register 0	TA0EX0	20h
TA0 interrupt vector	TA0IV	2Eh

Table 45. TA1 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA1 control	TA1CTL	00h
Capture/compare control 0	TA1CCTL0	02h
Capture/compare control 1	TA1CCTL1	04h
TA1 counter register	TA1R	10h
Capture/compare register 0	TA1CCR0	12h
Capture/compare register 1	TA1CCR1	14h
TA1 expansion register 0	TA1EX0	20h
TA1 interrupt vector	TA1IV	2Eh

Table 46. TA2 Registers (Base Address: 0400h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA2 control	TA2CTL	00h
Capture/compare control 0	TA2CCTL0	02h
Capture/compare control 1	TA2CCTL1	04h
TA2 counter register	TA2R	10h
Capture/compare register 0	TA2CCR0	12h
Capture/compare register 1	TA2CCR1	14h
TA2 expansion register 0	TA2EX0	20h
TA2 interrupt vector	TA2IV	2Eh

Table 47. TA3 Registers (Base Address: 0440h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TA3 control	TA3CTL	00h
Capture/compare control 0	TA3CCTL0	02h
Capture/compare control 1	TA3CCTL1	04h
TA3 counter register	TA3R	10h
Capture/compare register 0	TA3CCR0	12h
Capture/compare register 1	TA3CCR1	14h
TA3 expansion register 0	TA3EX0	20h
TA3 interrupt vector	TA3IV	2Eh

Table 48. Backup Memory Registers (Base Address: 0480h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Backup Memory 0	BAKMEM0	00h
Backup Memory 1	BAKMEM1	02h
Backup Memory 2	BAKMEM2	04h
Backup Memory 3	BAKMEM3	06h

Table 49. RTC_C Registers (Base Address: 04A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control 0	RTCCTL0	00h
RTC password	RTCPWD	01h
RTC control 1	RTCCTL1	02h
RTC control 3	RTCCTL3	03h
RTC offset calibration	RTCOCAL	04h
RTC temperature compensation	RTCTCMP	06h
RTC prescaler 0 control	RTCPS0CTL	08h
RTC prescaler 1 control	RTCPS1CTL	0Ah
RTC prescaler 0	RTCPS0	0Ch
RTC prescaler 1	RTCPS1	0Dh
RTC interrupt vector word	RTCIV	0Eh
RTC seconds	RTCSEC	10h
RTC minutes	RTCMIN	11h
RTC hours	RTCHOUR	12h
RTC day of week	RTCDOW	13h
RTC days	RTCDAY	14h
RTC month	RTCMON	15h
RTC year	RTCYEAR	16h
RTC alarm minutes	RTCAMIN	18h
RTC alarm hours	RTCAHOUR	19h
RTC alarm day of week	RTCADOW	1Ah
RTC alarm days	RTCADAY	1Bh
Binary-to-BCD conversion register	BIN2BCD	1Ch
BCD-to-Binary conversion register	BCD2BIN	1Eh

Table 50. 32-bit Hardware Multiplier Registers (Base Address: 04C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
16-bit operand 1 – multiply	MPY	00h
16-bit operand 1 – signed multiply	MPYS	02h
16-bit operand 1 – multiply accumulate	MAC	04h
16-bit operand 1 – signed multiply accumulate	MACS	06h
16-bit operand 2	OP2	08h
16 × 16 result low word	RESLO	0Ah
16 × 16 result high word	RESHI	0Ch
16 × 16 sum extension register	SUMEXT	0Eh
32-bit operand 1 – multiply low word	MPY32L	10h
32-bit operand 1 – multiply high word	MPY32H	12h
32-bit operand 1 – signed multiply low word	MPYS32L	14h
32-bit operand 1 – signed multiply high word	MPYS32H	16h
32-bit operand 1 – multiply accumulate low word	MAC32L	18h
32-bit operand 1 – multiply accumulate high word	MAC32H	1Ah
32-bit operand 1 – signed multiply accumulate low word	MACS32L	1Ch
32-bit operand 1 – signed multiply accumulate high word	MACS32H	1Eh
32-bit operand 2 – low word	OP2L	20h
32-bit operand 2 – high word	OP2H	22h
32 × 32 result 0 – least significant word	RES0	24h
32 × 32 result 1	RES1	26h
32 × 32 result 2	RES2	28h
32 × 32 result 3 – most significant word	RES3	2Ah
MPY32 control register 0	MPY32CTL0	2Ch

Table 51. DMA General Control Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA module control 0	DMACTL0	00h
DMA module control 1	DMACTL1	02h
DMA module control 2	DMACTL2	04h
DMA module control 3	DMACTL3	06h
DMA module control 4	DMACTL4	08h
DMA interrupt vector	DMAIV	0Eh

Table 52. DMA Channel 0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 0 control	DMA0CTL	10h
DMA channel 0 source address low	DMA0SAL	12h
DMA channel 0 source address high	DMA0SAH	14h
DMA channel 0 destination address low	DMA0DAL	16h
DMA channel 0 destination address high	DMA0DAH	18h
DMA channel 0 transfer size	DMA0SZ	1Ah

Table 53. DMA Channel 1 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 1 control	DMA1CTL	20h
DMA channel 1 source address low	DMA1SAL	22h
DMA channel 1 source address high	DMA1SAH	24h
DMA channel 1 destination address low	DMA1DAL	26h
DMA channel 1 destination address high	DMA1DAH	28h
DMA channel 1 transfer size	DMA1SZ	2Ah

Table 54. DMA Channel 2 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
DMA channel 2 control	DMA2CTL	30h
DMA channel 2 source address low	DMA2SAL	32h
DMA channel 2 source address high	DMA2SAH	34h
DMA channel 2 destination address low	DMA2DAL	36h
DMA channel 2 destination address high	DMA2DAH	38h
DMA channel 2 transfer size	DMA2SZ	3Ah

Table 55. eUSCI_A0 Registers (Base Address: 05C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI _A control word 1	UCA0CTLW1	02h
eUSCI_A baud rate 0	UCA0BR0	06h
eUSCI_A baud rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	UCA0IRTCTL	12h
eUSCI_A IrDA receive control	UCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

Table 56. eUSCI_A1 Registers (Base Address:05E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA1CTLW0	00h
eUSCI _A control word 1	UCA1CTLW1	02h
eUSCI_A baud rate 0	UCA1BR0	06h
eUSCI_A baud rate 1	UCA1BR1	07h
eUSCI_A modulation control	UCA1MCTLW	08h
eUSCI_A status	UCA1STAT	0Ah
eUSCI_A receive buffer	UCA1RXBUF	0Ch
eUSCI_A transmit buffer	UCA1TXBUF	0Eh
eUSCI_A LIN control	UCA1ABCTL	10h
eUSCI_A IrDA transmit control	UCA1IRTCTL	12h
eUSCI_A IrDA receive control	UCA1IRRCTL	13h
eUSCI_A interrupt enable	UCA1IE	1Ah

Table 56. eUSCI_A1 Registers (Base Address:05E0h) (continued)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A interrupt flags	UCA1IFG	1Ch
eUSCI_A interrupt vector word	UCA1IV	1Eh

Table 57. eUSCI_A2 Registers (Base Address:0600h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA2CTLW0	00h
eUSCI _A control word 1	UCA2CTLW1	02h
eUSCI_A baud rate 0	UCA2BR0	06h
eUSCI_A baud rate 1	UCA2BR1	07h
eUSCI_A modulation control	UCA2MCTLW	08h
eUSCI_A status	UCA2STAT	0Ah
eUSCI_A receive buffer	UCA2RXBUF	0Ch
eUSCI_A transmit buffer	UCA2TXBUF	0Eh
eUSCI_A LIN control	UCA2ABCTL	10h
eUSCI_A IrDA transmit control	UCA2IRTCTL	12h
eUSCI_A IrDA receive control	UCA2IRRCTL	13h
eUSCI_A interrupt enable	UCA2IE	1Ah
eUSCI_A interrupt flags	UCA2IFG	1Ch
eUSCI_A interrupt vector word	UCA2IV	1Eh

Table 58. eUSCI_B0 Registers (Base Address: 0640h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_B control word 0	UCB0CTLW0	00h
eUSCI_B control word 1	UCB0CTLW1	02h
eUSCI_B bit rate 0	UCB0BR0	06h
eUSCI_B bit rate 1	UCB0BR1	07h
eUSCI_B status word	UCB0STATW	08h
eUSCI_B byte counter threshold	UCB0TBCNT	0Ah
eUSCI_B receive buffer	UCB0RXBUF	0Ch
eUSCI_B transmit buffer	UCB0TXBUF	0Eh
eUSCI_B I2C own address 0	UCB0I2COA0	14h
eUSCI_B I2C own address 1	UCB0I2COA1	16h
eUSCI_B I2C own address 2	UCB0I2COA2	18h
eUSCI_B I2C own address 3	UCB0I2COA3	1Ah
eUSCI_B received address	UCB0ADDRX	1Ch
eUSCI_B address mask	UCB0ADDMASK	1Eh
eUSCI I2C slave address	UCB0I2CSA	20h
eUSCI interrupt enable	UCB0IE	2Ah
eUSCI interrupt flags	UCB0IFG	2Ch
eUSCI interrupt vector word	UCB0IV	2Eh

Table 59. ADC10_A Registers (Base Address: 0740h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC10_A Control register 0	ADC10CTL0	00h
ADC10_A Control register 1	ADC10CTL1	02h
ADC10_A Control register 2	ADC10CTL2	04h
ADC10_A Window Comparator Low Threshold	ADC10LO	06h
ADC10_A Window Comparator High Threshold	ADC10HI	08h
ADC10_A Memory Control Register 0	ADC10MCTL0	0Ah
ADC10_A Conversion Memory Register	ADC10MCTL0	12h
ADC10_A Interrupt Enable	ADC10IE	1Ah
ADC10_A Interrupt Flags	ADC10IGH	1Ch
ADC10_A Interrupt Vector Word	ADC10IV	1Eh

Table 60. SD24_B Registers (Base Address: 0800h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SD24_B Control 0 register	SD24BCTL0	00h
SD24_B Control 1 register	SD24BCTL1	02h
SD24_B Trigger Control register	SD24BTRGCTL	04h
SD24_B Trigger OSR Control register	SD24BTRGOSR	06h
SD24_B Trigger Preload register	SD24BTRGPRE	08h
SD24_B interrupt flag register	SD24BIFG	0Ah
SD24_B interrupt enable register	SD24BIE	0Ch
SD24_B Interrupt Vector register	SD24BIV	0Eh
SD24_B converter 0 Control register	SD24BCCTL0	10h
SD24_B converter 0 Input Control register	SD24BINCTL0	12h
SD24_B converter 0 OSR Control register	SD24BOSR0	14h
SD24_B converter 0 Preload register	SD24BPRE0	16h
SD24_B converter 1 Control register	SD24BCCTL1	18h
SD24_B Converter 1 Input Control register	SD24BINCTL1	1Ah
SD24_B Converter 1 OSR Control register	SD24BOSR1	1Ch
SD24_B Converter 1 Preload register	SD24BPRE1	1Eh
SD24_B Converter 2 Control register	SD24BCCTL2	20h
SD24_B Converter 2 Input Control register	SD24BINCTL2	22h
SD24_B Converter 2 OSR Control register	SD24BOSR2	24h
SD24_B Converter 2 Preload register	SD24BPRE2	26h
SD24_B Converter 0 Conversion Memory Low Word register	SD24BMEML0	50h
SD24_B Converter 0 Conversion Memory High Word regiser	SD24BMEMH0	52h
SD24_B Converter 1 Conversion Memory Low Word register	SD24BMEML1	54h
SD24_B Converter 1 Conversion Memory High Word regiser	SD24BMEMH1	56h
SD24_B Converter 2 Conversion Memory Low Word register	SD24BMEML2	58h
SD24_B Converter 2 Conversion Memory High Word regiser	SD24BMEMH2	5Ah

Table 61. Auxiliary Supplies Registers (Base Address: 09E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Auxiliary Supply Control 0 register	AUXCTL0	00h
Auxiliary Supply Control 1 register	AUXCTL1	02h
Auxiliary Supply Control 2 register	AUXCTL2	04h
AUX2 Charger Control	AUX2CHCTL	12h
AUX3 Charger Control	AUX3CHCTL	14h
AUX ADC Control	AUXADCCTL	16h
AUX Interrupt Flag	AUXIFG	1Ah
AUX Interrupt Enable	AUXIE	1Ch
AUX Interrupt Vector Word	AUXIV	1Eh

Table 62. LCD_C Registers (Base Address: 0A00h)

REGISTER DESCRIPTION	REGISTER	OFFSET
LCD_C control register 0	LCDCCTL0	000h
LCD_C control register 1	LCDCCTL1	002h
LCD_C blinking control register	LCDCBLKCTL	004h
LCD_C memory control register	LCDCMEMCTL	006h
LCD_C voltage control register	LCDCVCTL	008h
LCD_C port control 0	LCDCPCTL0	00Ah
LCD_C port control 1	LCDCPCTL1	00Ch
LCD_C port control 2	LCDCPCTL2	00Eh
LCD_C charge pump control register	LCDCCPCTL	012h
LCD_C interrupt vector	LCDCIV	01Eh
Static and 2 to 4 mux modes		
LCD_C memory 1	LCDM1	020h
LCD_C memory 2	LCDM2	021h
⋮	⋮	⋮
LCD_C memory 20	LCDM20	033h
LCD_C blinking memory 1	LCDBM1	040h
LCD_C blinking memory 2	LCDBM2	041h
⋮	⋮	⋮
LCD_C blinking memory 20	LCDBM20	053h
5 to 8 mux modes		
LCD_C memory 1	LCDM1	020h
LCD_C memory 2	LCDM2	021h
⋮	⋮	⋮
LCD_C memory 40	LCDM40	047h

Absolute Maximum Ratings[1]

over operating free-air temperature range (unless otherwise noted)

Voltage applied at DVCC to DVSS	-0.3 V to 4.1 V
Voltage applied to any pin (excluding VCORE)[2]	-0.3 V to V_{CC} + 0.3 V
Diode current at any device pin	±2 mA
Storage temperature range, T_{stg} [3]	–55°C to 150°C
Maximum junction temperature, T_J	95°C

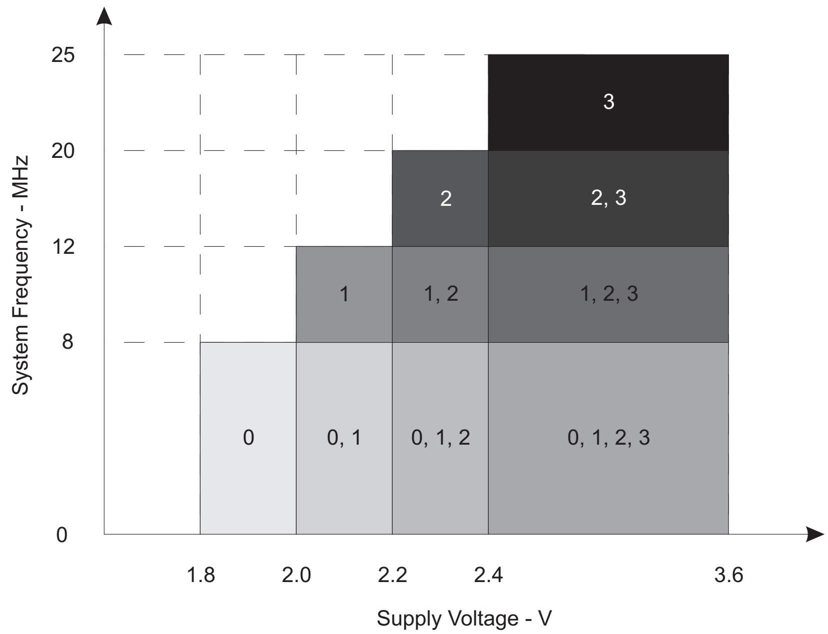
(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to V_{SS}. V_{CORE} is for internal device usage only. No external DC loading or voltage should be applied.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage during program execution and flash programming. V(AVCC) = V(DVCC) = V_{CC} [1][2]	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 0, 1	2.0		3.6	V
		PMMCOREVx = 0, 1, 2	2.2		3.6	V
		PMMCOREVx = 0, 1, 2, 3	2.4		3.6	V
V_{SS}	Supply voltage V(AVSS) = V(DVSS) = V_{SS}			0		V
T_A	Operating free-air temperature	I version	–40		85	°C
T_J	Operating junction temperature	I version	–40		85	°C
C_{VCORE}	Recommended capacitor at VCORE			470		nF
C_{DVCC}/ C_{VCORE}	Capacitor ratio of DVCC to VCORE		10			
f_{SYSTEM}	Processor frequency (maximum MCLK frequency)[3][4] (see Figure 1)	PMMCOREVx = 0, 1.8 V ≤ V_{CC} ≤ 3.6 V (default condition)	0		8.0	MHz
		PMMCOREVx = 1, 2.0 V ≤ V_{CC} ≤ 3.6 V	0		12.0	MHz
		PMMCOREVx = 2, 2.2 V ≤ V_{CC} ≤ 3.6 V	0		20.0	MHz
		PMMCOREVx = 3, 2.4 V ≤ V_{CC} ≤ 3.6 V	0		25.0	MHz
$I_{LOAD, DVCCD}$	Maximum load current that can be drawn from DVCC for core and IO (I_{LOAD} = I_{CORE} + I_{IO})				20	mA
$I_{LOAD, AUX1D}$	Maximum load current that can be drawn from AUXVCC1 for core and IO (I_{LOAD} = I_{CORE} + I_{IO})				20	mA
$I_{LOAD, AUX2D}$	Maximum load current that can be drawn from AUXVCC2 for core and IO (I_{LOAD} = I_{CORE} + I_{IO})				20	mA
$I_{LOAD, AVCCA}$	Maximum load current that can be drawn from AVCC for analog modules (I_{LOAD} = $I_{Modules}$)				10	mA
$I_{LOAD, AUX1A}$	Maximum load current that can be drawn from AUXVCC1 for analog modules (I_{LOAD} = $I_{Modules}$)				5	mA
$I_{LOAD, AUX2A}$	Maximum load current that can be drawn from AUXVCC2 for analog modules (I_{LOAD} = $I_{Modules}$)				5	mA

(1) It is recommended to power AVCC and DVCC from the same source. A maximum difference of 0.3 V between V(AVCC) and V(DVCC) can be tolerated during power up and operation.
(2) The minimum supply voltage is defined by the supervisor SVS levels when it is enabled. See the PMM, SVS High Side threshold parameters for the exact values and further details.
(3) The MSP430 CPU is clocked directly with MCLK. Both the high and low phase of MCLK must not exceed the pulse width of the specified maximum frequency.
(4) Modules may have a different maximum input clock specification. Refer to the specification of the respective module in this data sheet.



The numbers within the fields denote the supported PMMCOREVx settings.

Figure 1. Maximum System Frequency

Active Mode Supply Current Into V_{CC} Excluding External Current

over recommended operating free-air temperature (unless otherwise noted)[(1)] [(2)] [(3)]

PARAMETER	EXECUTION MEMORY	V_{CC}	PMMCOREVx	FREQUENCY ($f_{DCO} = f_{MCLK} = f_{SMCLK}$)										UNIT
				1 MHz		8 MHz		12 MHz		20 MHz		25 MHz		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, Flash}$ [(4)]	Flash	3.0 V	0	0.32	0.36	2.10	2.30							mA
			1	0.36		2.39		3.54	3.90					
			2	0.39		2.65		3.94		6.54	7.23			
			3	0.42		2.82		4.20		6.96		8.65	9.54	
$I_{AM, RAM}$ [(5)]	RAM	3.0 V	0	0.20	0.22	1.10	1.22							mA
			1	0.22		1.30		1.90	2.10					
			2	0.24		1.45		2.15		3.55	4.0			
			3	0.26		1.55		2.30		3.80		4.70	5.30	

(1) All inputs are tied to 0 or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Characterized with program executing typical data processing.
f_{ACLK} = 32786 Hz, $f_{DCO} = f_{MCLK} = f_{SMCLK}$ at specified frequency.
XTS = CPUOFF = SCG0 = SCG1 = OSCOFF = SMCLKOFF = 0.
(4) Active mode supply current when program executes in flash at a nominal supply voltage of 3.0V.
(5) Active mode supply current when program executes in RAM at a nominal supply voltage of 3 V.

Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)(2)

PARAMETER		V_{CC}	PMMCOREVx	TEMPERATURE (T_A)								UNIT
				-40°C		25°C		60°C		85°C		
				TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM0,1MHz}$	Low-power mode 0(3)(4)	2.2 V	0	75		78	87	81		84	96	µA
		3.0 V	3	85		89	99	93		98	110	
I_{LPM2}	Low-power mode 2(5)(4)	2.2 V	0	5.9		6.2	9	6.9		9.4	17	µA
		3.0 V	3	6.9		7.4	10	8.4		11	19	
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	2.2 V	0	1.4		1.7		2.5		4.9		µA
			1	1.5		1.9		2.7		5.2		
			2	1.7		2.0		2.9		5.5		
$I_{LPM3,XT1LF}$	Low-power mode 3, crystal mode(6)(4)	3.0 V	0	2.2		2.5	3.1	3.3		5.5	12.7	µA
			1	2.3		2.7		3.5		5.8		
			2	2.5		2.9		3.7		6.1		
			3	2.5		2.9	3.5	3.7		6.1	14.0	
$I_{LPM3,VLO}$	Low-power mode 3, VLO mode(7)(4)	3.0 V	0	1.4		1.7	2.2	2.4		4.5	11.5	µA
			1	1.5		1.8		2.5		4.7		
			2	1.6		1.9		2.7		4.9		
			3	1.6		1.9	2.4	2.7		5.0	12.7	
I_{LPM4}	Low-power mode 4(8)(4)	3.0 V	0	1.3		1.6	2.0	2.3		4.4	11.1	µA
			1	1.4		1.6		2.4		4.5		
			2	1.4		1.7		2.5		4.8		
			3	1.4		1.7	2.2	2.5		4.8	12.2	
$I_{LPM3.5}$	Low-power mode 3.5, RTC active on AUXVCC3(9)	2.2V		0.65		0.80		0.90		1.30		µA
		3.0V		1.16		1.24	2.05	1.43		1.87	2.71	
$I_{LPM4.5}$	Low-power mode 4.5(10)	3.0V		0.70		0.78	1.05	0.90		1.20	1.85	µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by SMCLK included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 0, OSCOFF = 0 (LPM0); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 1 MHz
(4) Current for brownout, high side supervisor (SVS_H) normal mode included. Low side supervisor and monitors disabled (SVS_L, SVM_L). High side monitor disabled (SVM_H). RAM retention enabled.
(5) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 0, SCG1 = 1, OSCOFF = 0 (LPM2); f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} = f_{DCO} = 0 MHz; DCO setting = 1 MHz operation, DCO bias generator enabled.
(6) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(7) Current for watchdog timer clocked by ACLK included. RTC is disabled (RTCHOLD=1). ACLK = VLO.
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = f_{VLO}, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
(8) CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 1 (LPM4); f_{DCO} = f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0 MHz
(9) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 32768 Hz, PMMREGOFF = 1, RTC active on AUXVCC3 supply
(10) f_{DCO} = f_{MCLK} = f_{SMCLK} = 0 MHz, f_{ACLK} = 0 Hz, PMMREGOFF = 1

Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)[1][2]

PARAMETER		V_{CC}	PMMCOREVx	Temperature (T_A) -40°C TYP	-40°C MAX	25°C TYP	25°C MAX	60°C TYP	60°C MAX	85°C TYP	85°C MAX	UNIT
I_{LPM3} LCD, int. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled[3][4]	2.2 V	0	2.4		2.9	3.6	3.8		5.8	12.2	µA
			1	2.5		3.1		4.0		6.0		
			2	2.6		3.3	3.9	4.2		6.3	13.4	
I_{LPM3} LCD, int. bias	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump disabled[3][4]	3.0 V	0	2.8		3.2	3.9	4.1		6.4	13.3	µA
			1	2.9		3.4		4.3		6.7		
			2	3.1		3.6		4.5		7.0		
			3	3.1		3.6	4.5	4.5		7.0	14.7	
I_{LPM3} LCD,CP	Low-power mode 3 (LPM3) current, LCD 4-mux mode, internal biasing, charge pump enabled[3][5]	2.2 V	0			3.8						µA
			1			3.9						
			2			4.0						
		3.0 V	0			4.0						µA
			1			4.1						
			2			4.2						
			3			4.2						

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) The currents are characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance of 12.5 pF. The internal and external load capacitance are chosen to closely match the required 12.5 pF.
(3) Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. ACLK = low-frequency crystal operation (XTS = 0, XT1DRIVEx = 0).
CPUOFF = 1, SCG0 = 1, SCG1 = 1, OSCOFF = 0 (LPM3); f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} = 0 MHz
Current for brownout, high-side supervisor (SVS_H) normal mode included. Low-side supervisor and monitors disabled (SVS_L, SVM_L). High-side monitor disabled (SVM_H). RAM retention enabled.
(4) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 0 (charge pump disabled), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.
(5) LCDMx = 11 (4-mux mode), LCDREXT = 0, LCDEXTBIAS = 0 (internal biasing), LCD2B = 0 (1/3 bias), LCDCPEN = 1 (charge pump enabled), VLCDx = 1000 (V_{LCD} = 3V,typ.), LCDSSEL = 0, LCDPREx = 101, LCDDIVx = 00011 (f_{LCD} = 32768 Hz / 32 / 4 = 256 Hz)
Even segments S0, S2, ... = 0 and odd segments S1, S3, ... = 1. No LCD panel load.

Schmitt-Trigger Inputs – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		1.8 V	0.80		1.40	V
			3 V	1.50		2.10	
V_{IT-}	Negative-going input threshold voltage		1.8 V	0.45		1.00	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis (V_{IT+} – V_{IT-})		1.8 V	0.3		0.85	V
			3 V	0.4		1.0	
R_{Pull}	Pullup/pulldown resistor	For pullup: V_{IN} = V_{SS} For pulldown: V_{IN} = V_{CC}		20	35	50	kΩ
C_I	Input capacitance	V_{IN} = V_{SS} or V_{CC}			5		pF

Inputs – Ports P1 and P2[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing[2]	Port P1, P2: P1.x to P2.x, External trigger pulse width to set interrupt flag	2.2 V/3 V	20		ns

(1) Some devices may contain additional ports with interrupts. See the block diagram and terminal function descriptions.
(2) An external signal sets the interrupt flag every time the minimum interrupt pulse width $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

Leakage Current – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(Px.y)}$	High-impedance leakage current	See [1][2]	1.8 V/3 V		±50	nA

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin(s), unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.

Outputs – General Purpose I/O (Full Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –3 mA[1]	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –10 mA[1]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –5 mA[1]	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –15 mA[1]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 3 mA[2]	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 10 mA[3]		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 5 mA[2]	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 15 mA[3]		V_{SS}	V_{SS} + 0.60	

(1) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Recommended Operating Conditions for more details.
(2) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined should not exceed ±100 mA to hold the maximum voltage drop specified.

Typical Characteristics – General Purpose I/O (Full Drive Strength)

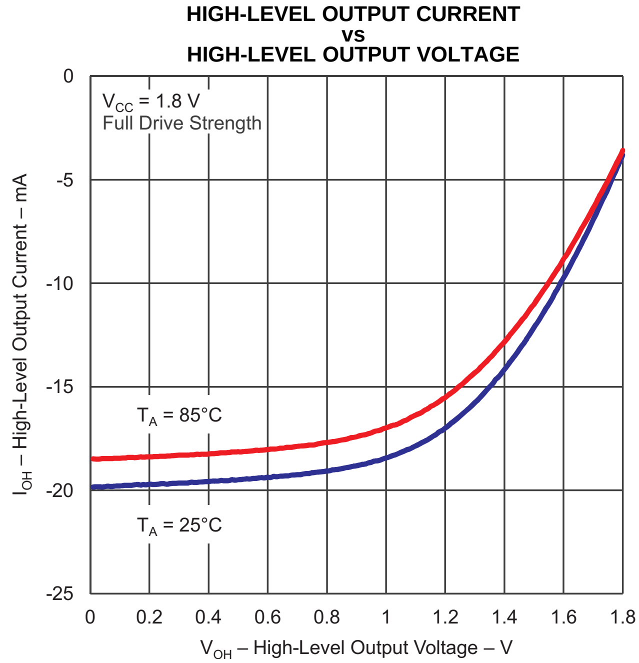


Figure 2.

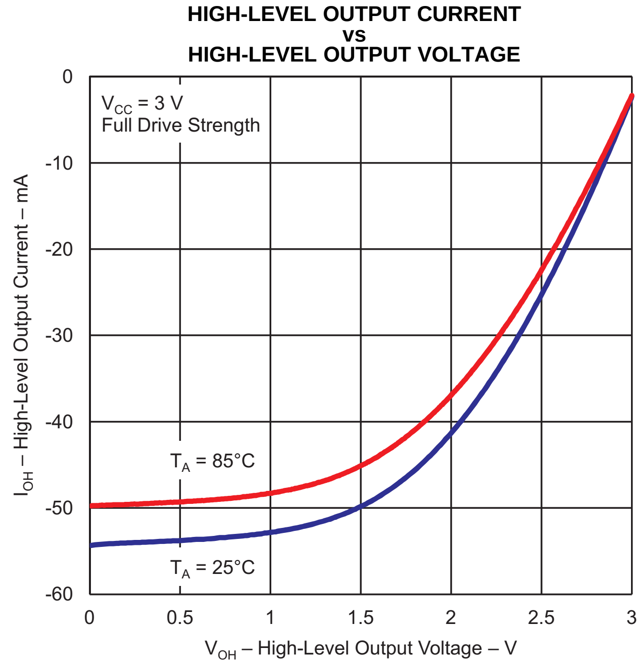


Figure 3.

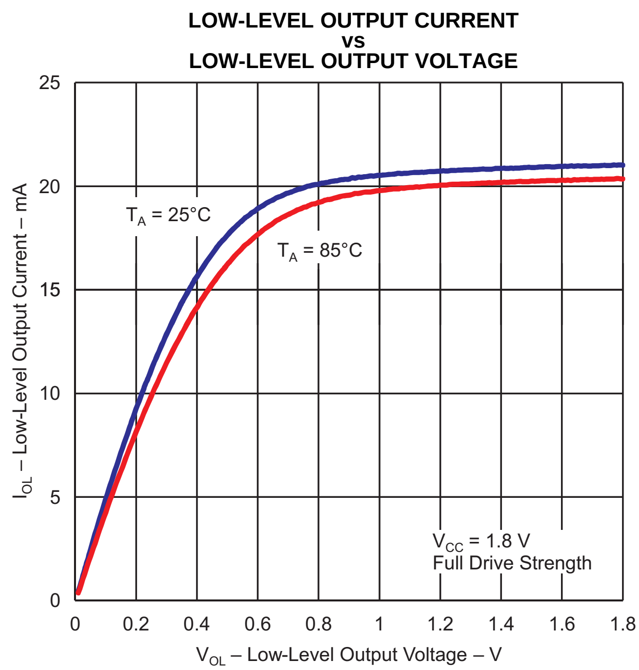


Figure 4.

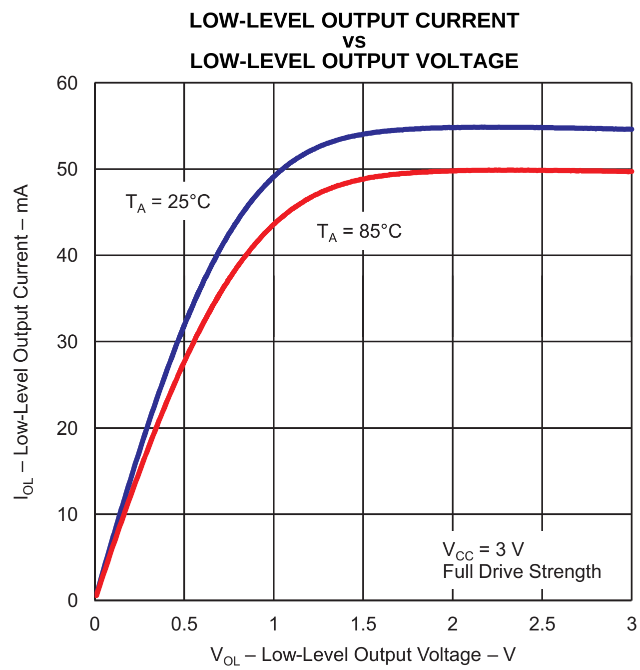


Figure 5.

Outputs – General Purpose I/O (Reduced Drive Strength)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA(2)	1.8 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –3 mA(2)		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = –2 mA(2)	3.0 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA(2)		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1 mA(3)	1.8 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 3 mA(4)		V_{SS}	V_{SS} + 0.60	
		$I_{(OLmax)}$ = 2 mA(3)	3.0 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA(4)		V_{SS}	V_{SS} + 0.60	

(1) Selecting reduced drive strength may reduce EMI.
(2) The maximum total current, $I_{(OHmax)}$, for all outputs combined should not exceed ±20 mA to hold the maximum voltage drop specified. See Recommended Operating Conditions for more details.
(3) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±48 mA to hold the maximum voltage drop specified.
(4) The maximum total current, $I_{(OLmax)}$, for all outputs combined, should not exceed ±100 mA to hold the maximum voltage drop specified.

Typical Characteristics – General Purpose I/O (Reduced Drive Strength)

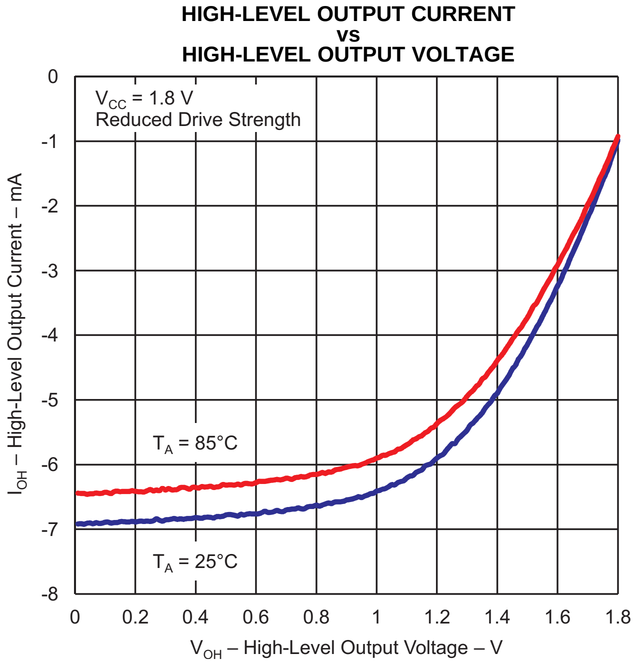


Figure 6.

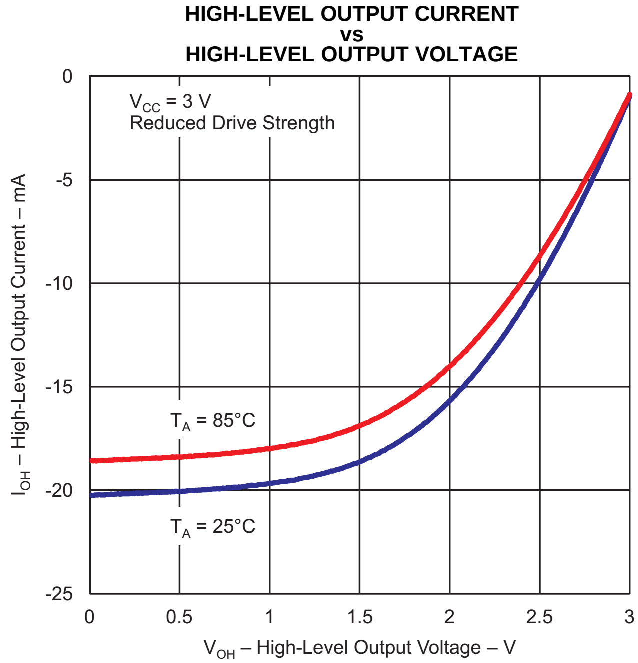


Figure 7.

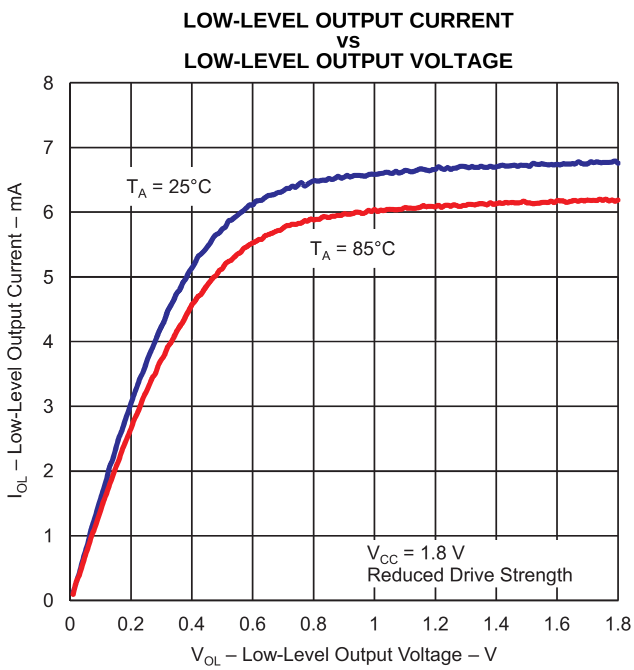


Figure 8.

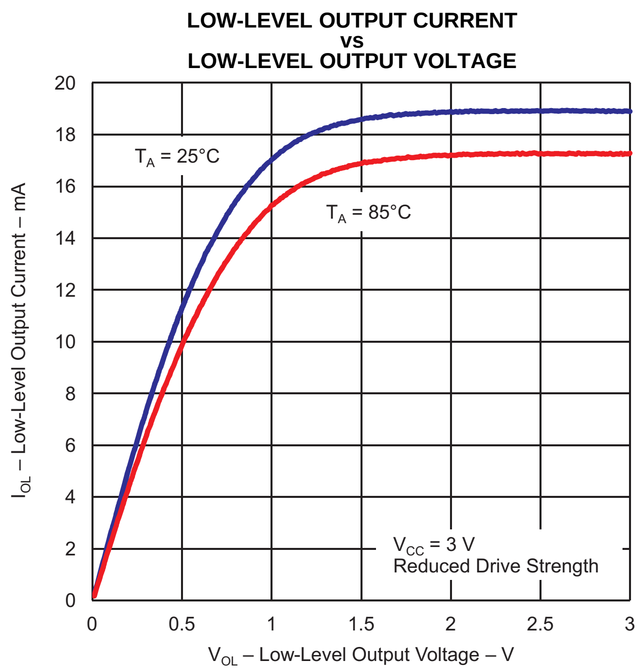


Figure 9.

Output Frequency – General Purpose I/O

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$f_{Px.y}$	Port output frequency (with load)	See [1][2]	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	
f_{Port_CLK}	Clock output frequency	ACLK, SMCLK, MCLK, C_L = 20 pF [2]	V_{CC} = 1.8 V, PMMCOREVx = 0		16	MHz
			V_{CC} = 3 V, PMMCOREVx = 3		25	

(1) A resistive divider with 2 × R1 between V_{CC} and V_{SS} is used as load. The output is connected to the center tap of the divider. For full drive strength, R1 = 550 Ω. For reduced drive strength, R1 = 1.6 kΩ. C_L = 20 pF is connected to the output to V_{SS}.
(2) The output voltage reaches at least 10% and 90% V_{CC} at the specified toggle frequency.

Crystal Oscillator, XT1, Low-Frequency Mode[1]

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$\Delta I_{DVCC.LF}$	Differential XT1 oscillator crystal current consumption from lowest drive setting, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, T_A = 25°C	3.0 V		0.075		µA
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 2, T_A = 25°C			0.170		
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C			0.290		
$f_{XT1,LF0}$	XT1 oscillator crystal frequency, LF mode	XTS = 0, XT1BYPASS = 0			32768		Hz
$f_{XT1,LF,SW}$	XT1 oscillator logic-level square-wave input frequency, LF mode	XTS = 0, XT1BYPASS = 1 [2] [3]		10	32.768	50	kHz
OA_{LF}	Oscillation allowance for LF crystals[4]	XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 6 pF			210		kΩ
		XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 1, $f_{XT1,LF}$ = 32768 Hz, $C_{L,eff}$ = 12 pF			300		
$C_{L,eff}$	Integrated effective load capacitance, LF mode[5]	XTS = 0, XCAPx = 0 [6]			2		pF
		XTS = 0, XCAPx = 1			5.5		
		XTS = 0, XCAPx = 2			8.5		
		XTS = 0, XCAPx = 3			12.0		

(1) To improve EMI on the XT1 oscillator, the following guidelines should be observed.
(a) Keep the trace between the device and the crystal as short as possible.
(b) Design a good ground plane around the oscillator pins.
(c) Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
(d) Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
(e) Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
(f) If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
(2) When XT1BYPASS is set, XT1 circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger Inputs section of this datasheet.
(3) Maximum frequency of operation of the entire device cannot be exceeded.
(4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the XT1DRIVEx settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
(a) For XT1DRIVEx = 0, $C_{L,eff} \leq 6$ pF.
(b) For XT1DRIVEx = 1, 6 pF $\leq C_{L,eff} \leq$ 9 pF.
(c) For XT1DRIVEx = 2, 6 pF $\leq C_{L,eff} \leq$ 10 pF.
(d) For XT1DRIVEx = 3, $C_{L,eff} \geq 6$ pF.
(5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
Since the PCB adds additional capacitance, it is recommended to verify the correct load by measuring the ACLK frequency. For a correct setup, the effective load capacitance should always match the specification of the used crystal.
(6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.

Crystal Oscillator, XT1, Low-Frequency Mode[1] (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
Duty cycle	LF mode	XTS = 0, Measured at ACLK, $f_{XT1,LF}$ = 32768 Hz		30		70	%
$f_{Fault,LF}$	Oscillator fault frequency, LF mode[7]	XTS = 0[8]		10		10000	Hz
$t_{START,LF}$	Startup time, LF mode	f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 0, T_A = 25°C, $C_{L,eff}$ = 6 pF	3.0 V		1000		ms
		f_{OSC} = 32768 Hz, XTS = 0, XT1BYPASS = 0, XT1DRIVEx = 3, T_A = 25°C, $C_{L,eff}$ = 12 pF			500		

(7) Frequencies below the MIN specification set the fault flag. Frequencies above the MAX specification do not set the fault flag. Frequencies in between might set the flag.
(8) Measured with logic-level input frequency but also applies to operation with crystals.

Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at ACLK	1.8 V to 3.6 V	6	9.4	15	kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at ACLK[1]	1.8 V to 3.6 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at ACLK[2]	1.8 V to 3.6 V		4		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	30		70	%

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Internal Reference, Low-Frequency Oscillator (REFO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	1.8 V to 3.6 V		3		µA
f_{REFO}	REFO frequency calibrated	Measured at ACLK	1.8 V to 3.6 V		32768		Hz
	REFO absolute tolerance calibrated	Full temperature range	1.8 V to 3.6 V			±3.5	%
		T_A = 25°C	3 V			±1.5	%
df_{REFO}/d_T	REFO frequency temperature drift	Measured at ACLK[1]	1.8 V to 3.6 V		0.01		%/°C
df_{REFO}/dV_{CC}	REFO frequency supply voltage drift	Measured at ACLK[2]	1.8 V to 3.6 V		1.0		%/V
	Duty cycle	Measured at ACLK	1.8 V to 3.6 V	40	50	60	%
t_{START}	REFO startup time	40%/60% duty cycle	1.8 V to 3.6 V		25		µs

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

DCO Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{DCO(0,0)}$	DCO frequency (0, 0)(1)	DCORSELx = 0, DCOx = 0, MODx = 0	0.07		0.20	MHz
$f_{DCO(0,31)}$	DCO frequency (0, 31)(1)	DCORSELx = 0, DCOx = 31, MODx = 0	0.70		1.70	MHz
$f_{DCO(1,0)}$	DCO frequency (1, 0)(1)	DCORSELx = 1, DCOx = 0, MODx = 0	0.15		0.36	MHz
$f_{DCO(1,31)}$	DCO frequency (1, 31)(1)	DCORSELx = 1, DCOx = 31, MODx = 0	1.47		3.45	MHz
$f_{DCO(2,0)}$	DCO frequency (2, 0)(1)	DCORSELx = 2, DCOx = 0, MODx = 0	0.32		0.75	MHz
$f_{DCO(2,31)}$	DCO frequency (2, 31)(1)	DCORSELx = 2, DCOx = 31, MODx = 0	3.17		7.38	MHz
$f_{DCO(3,0)}$	DCO frequency (3, 0)(1)	DCORSELx = 3, DCOx = 0, MODx = 0	0.64		1.51	MHz
$f_{DCO(3,31)}$	DCO frequency (3, 31)(1)	DCORSELx = 3, DCOx = 31, MODx = 0	6.07		14.0	MHz
$f_{DCO(4,0)}$	DCO frequency (4, 0)(1)	DCORSELx = 4, DCOx = 0, MODx = 0	1.3		3.2	MHz
$f_{DCO(4,31)}$	DCO frequency (4, 31)(1)	DCORSELx = 4, DCOx = 31, MODx = 0	12.3		28.2	MHz
$f_{DCO(5,0)}$	DCO frequency (5, 0)(1)	DCORSELx = 5, DCOx = 0, MODx = 0	2.5		6.0	MHz
$f_{DCO(5,31)}$	DCO frequency (5, 31)(1)	DCORSELx = 5, DCOx = 31, MODx = 0	23.7		54.1	MHz
$f_{DCO(6,0)}$	DCO frequency (6, 0)(1)	DCORSELx = 6, DCOx = 0, MODx = 0	4.6		10.7	MHz
$f_{DCO(6,31)}$	DCO frequency (6, 31)(1)	DCORSELx = 6, DCOx = 31, MODx = 0	39.0		88.0	MHz
$f_{DCO(7,0)}$	DCO frequency (7, 0)(1)	DCORSELx = 7, DCOx = 0, MODx = 0	8.5		19.6	MHz
$f_{DCO(7,31)}$	DCO frequency (7, 31)(1)	DCORSELx = 7, DCOx = 31, MODx = 0	60		135	MHz
$S_{DCORSEL}$	Frequency step between range DCORSEL and DCORSEL + 1	$S_{RSEL} = f_{DCO(DCORSEL+1,DCO)}/f_{DCO(DCORSEL,DCO)}$	1.2		2.3	ratio
S_{DCO}	Frequency step between tap DCO and DCO + 1	$S_{DCO} = f_{DCO(DCORSEL,DCO+1)}/f_{DCO(DCORSEL,DCO)}$	1.02		1.12	ratio
	Duty cycle	Measured at SMCLK	40	50	60	%
df_{DCO}/dT	DCO frequency temperature drift	f_{DCO} = 1 MHz		0.1		%/°C
df_{DCO}/dV_{CORE}	DCO frequency voltage drift	f_{DCO} = 1 MHz		1.9		%/V

(1) When selecting the proper DCO frequency range (DCORSELx), the target DCO frequency, f_{DCO}, should be set to reside within the range of $f_{DCO(n,\ 0),MAX} \leq f_{DCO} \leq f_{DCO(n,\ 31),MIN}$, where $f_{DCO(n,\ 0),MAX}$ represents the maximum frequency specified for the DCO frequency, range n, tap 0 (DCOx = 0) and $f_{DCO(n,31),MIN}$ represents the minimum frequency specified for the DCO frequency, range n, tap 31 (DCOx = 31). This ensures that the target DCO frequency resides within the range selected. It should also be noted that if the actual f_{DCO} frequency for the selected range causes the FLL or the application to select tap 0 or 31, the DCO fault flag is set to report that the selected range is at its minimum or maximum tap setting.

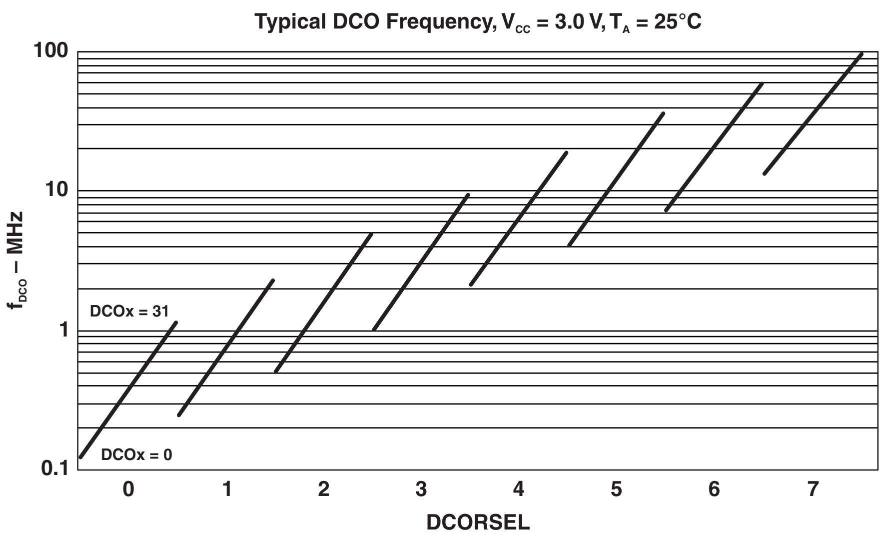


Figure 10. Typical DCO Frequency

PMM, Brown-Out Reset (BOR)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V(DV_{CC}\_BOR\_IT-)$	BOR_H on voltage, DV_{CC} falling level	$\| dDV_{CC}/d_t \| < 3$ V/s			1.45	V
$V(DV_{CC}\_BOR\_IT+)$	BOR_H off voltage, DV_{CC} rising level	$\| dDV_{CC}/d_t \| < 3$ V/s	0.80	1.30	1.50	V
$V(DV_{CC}\_BOR\_hys)$	BOR_H hysteresis		60		250	mV
t_{RESET} (1)	Pulse length required at $\overline{RST}$/NMI pin to accept a reset		2			µs

(1) Pulse much shorter than 2 µs might trigger reset.

PMM, Core Voltage

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CORE3}(AM)	Core voltage, active mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.93		V
V_{CORE2}(AM)	Core voltage, active mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.83		V
V_{CORE1}(AM)	Core voltage, active mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.62		V
V_{CORE0}(AM)	Core voltage, active mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.42		V
V_{CORE3}(LPM)	Core voltage, low-current mode, PMMCOREV = 3	2.4 V ≤ DV_{CC} ≤ 3.6 V		1.96		V
V_{CORE2}(LPM)	Core voltage, low-current mode, PMMCOREV = 2	2.2 V ≤ DV_{CC} ≤ 3.6 V		1.94		V
V_{CORE1}(LPM)	Core voltage, low-current mode, PMMCOREV = 1	2.0 V ≤ DV_{CC} ≤ 3.6 V		1.74		V
V_{CORE0}(LPM)	Core voltage, low-current mode, PMMCOREV = 0	1.8 V ≤ DV_{CC} ≤ 3.6 V		1.54		V

PMM, SVS High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSH)}$	SVS current consumption	SVSHE = 0, DV_{CC} = 3.6 V		0		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 0		200		nA
		SVSHE = 1, DV_{CC} = 3.6 V, SVSHFP = 1		1.5		µA
$V_{(SVSH\_IT-)}$	SVS_H on voltage level (1)	SVSHE = 1, SVSHRVL = 0	1.60	1.65	1.70	V
		SVSHE = 1, SVSHRVL = 1	1.77	1.84	1.90	
		SVSHE = 1, SVSHRVL = 2	1.97	2.04	2.10	
		SVSHE = 1, SVSHRVL = 3	2.09	2.16	2.23	
$V_{(SVSH\_IT+)}$	SVS_H off voltage level (1)	SVSHE = 1, SVSMHRRL = 0	1.68	1.74	1.80	V
		SVSHE = 1, SVSMHRRL = 1	1.89	1.95	2.01	
		SVSHE = 1, SVSMHRRL = 2	2.08	2.14	2.21	
		SVSHE = 1, SVSMHRRL = 3	2.21	2.27	2.34	
		SVSHE = 1, SVSMHRRL = 4	2.35	2.41	2.49	
		SVSHE = 1, SVSMHRRL = 5	2.65	2.72	2.80	
		SVSHE = 1, SVSMHRRL = 6	2.96	3.04	3.13	
		SVSHE = 1, SVSMHRRL = 7	2.96	3.04	3.13	
$t_{pd(SVSH)}$	SVS_H propagation delay	SVSHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVSHFP = 1		2.5		µs
		SVSHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVSHFP = 0		20		
$t_{(SVSH)}$	SVS_H on/off delay time	SVSHE = 0 → 1, SVSHFP = 1		12.5		µs
		SVSHE = 0 → 1, SVSHFP = 0		100		
dV_{DVCC}/dt	DV_{CC} rise time		0		1000	V/s

(1) The SVS_H settings available depend on the VCORE (PMMCOREVx) setting. Please refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208) on recommended settings and usage.

PMM, SVM High Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVMH)}$	SVM_H current consumption	SVMHE = 0, DV_{CC} = 3.6 V		0		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 0		200		nA
		SVMHE = 1, DV_{CC} = 3.6 V, SVMHFP = 1		1.5		µA
$V_{(SVMH)}$	SVM_H on/off voltage level (1)	SVMHE = 1, SVSMHRRL = 0	1.68	1.74	1.80	V
		SVMHE = 1, SVSMHRRL = 1	1.89	1.95	2.01	
		SVMHE = 1, SVSMHRRL = 2	2.08	2.14	2.21	
		SVMHE = 1, SVSMHRRL = 3	2.21	2.27	2.34	
		SVMHE = 1, SVSMHRRL = 4	2.35	2.41	2.49	
		SVMHE = 1, SVSMHRRL = 5	2.65	2.72	2.80	
		SVMHE = 1, SVSMHRRL = 6	2.96	3.04	3.13	
		SVMHE = 1, SVSMHRRL = 7	2.96	3.04	3.13	
		SVMHE = 1, SVMHOVPE = 1		3.79		
$t_{pd(SVMH)}$	SVM_H propagation delay	SVMHE = 1, dV_{DVCC}/dt = 10 mV/µs, SVMHFP = 1		2.5		µs
		SVMHE = 1, dV_{DVCC}/dt = 1 mV/µs, SVMHFP = 0		20		
$t_{(SVMH)}$	SVM_H on/off delay time	SVMHE = 0 → 1, SVMHFP = 1		12.5		µs
		SVMHE = 0 → 1, SVMHFP = 0		100		

(1) The SVM_H settings available depend on the VCORE (PMMCOREVx) setting. Refer to the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208) on recommended settings and usage.

PMM, SVS Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVSL)}$	SVS_L current consumption	SVSLE = 0, PMMCOREV = 2		0		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 0		200		nA
		SVSLE = 1, PMMCOREV = 2, SVSLFP = 1		1.5		µA
$t_{pd(SVSL)}$	SVS_L propagation delay	SVSLE = 1, dV_{CORE}/dt = 10 mV/µs, SVSLFP = 1		2.5		µs
		SVSLE = 1, dV_{CORE}/dt = 1 mV/µs, SVSLFP = 0		20		
$t_{(SVSL)}$	SVS_L on/off delay time	SVSLE = 0 → 1, SVSLFP = 1		12.5		µs
		SVSLE = 0 → 1, SVSLFP = 0		100		

PMM, SVM Low Side

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(SVML)}$	SVM_L current consumption	SVMLE = 0, PMMCOREV = 2		0		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 0		200		nA
		SVMLE = 1, PMMCOREV = 2, SVMLFP = 1		1.5		µA
$t_{pd(SVML)}$	SVM_L propagation delay	SVMLE = 1, dV_{CORE}/dt = 10 mV/µs, SVMLFP = 1		2.5		µs
		SVMLE = 1, dV_{CORE}/dt = 1 mV/µs, SVMLFP = 0		20		
$t_{(SVML)}$	SVM_L on/off delay time	SVMLE = 0 → 1, SVMLFP = 1		12.5		µs
		SVMLE = 0 → 1, SVMLFP = 0		100		

Wake-Up from Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{WAKE-UP-FAST}$	Wake-up time from LPM2, LPM3, or LPM4 to active mode(1)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 1	$f_{MCLK} \geq$ 4 MHz		3	5	µs
			1 MHz < f_{MCLK} < 4 MHz		4	6	
$t_{WAKE-UP-SLOW}$	Wake-up time from LPM2, LPM3 or LPM4 to active mode(2)	PMMCOREV = SVSMLRRL = n (where n = 0, 1, 2, or 3), SVSLFP = 0			150	160	µs
$t_{WAKE-UP-LPM4.5}$	Wake-up time from LPM4.5 to active mode(3)				2	3	ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode(3)				2	3	ms

(1) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). Fastest wakeup times are possible with SVS_L and SVM_L in full performance mode or disabled when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208).
(2) This value represents the time from the wakeup event to the first active edge of MCLK. The wakeup time depends on the performance mode of the low side supervisor (SVS_L) and low side monitor (SVM_L). In this case, the SVS_L and SVM_L are in normal mode (low current) mode when operating in AM, LPM0, and LPM1. Various options are available for SVS_L and SVM_L while operating in LPM2, LPM3, and LPM4. See the *Power Management Module and Supply Voltage Supervisor* chapter in the *MSP430x5xx Family User's Guide* (SLAU208).
(3) This value represents the time from the wakeup event to the reset vector execution.

Auxiliary Supplies - Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage range for all supplies at pins DVCC, AVCC, AUX1, AUX2, AUX3		1.8		3.6	V
V_{DSYS}	Digital system supply voltage range, $V_{DSYS} = V_{CC} - R_{ON} \times I_{LOAD}$	PMMCOREVx = 0	1.8		3.6	V
		PMMCOREVx = 1	2.0		3.6	
		PMMCOREVx = 2	2.2		3.6	
		PMMCOREVx = 3	2.4		3.6	
V_{ASYS}	Analog system supply voltage range, $V_{ASYS} = V_{CC} - R_{ON} \times I_{LOAD}$		Refer to modules			V
C_{VCC},$C_{AUX1/2}$	Recommended capacitor at pins DVCC, AVCC, AUX1, AUX2			4.7		µF
C_{VSYS}	Recommended capacitor at pins VDSYS and VASYS			4.7		µF
C_{VCORE}	Recommended capacitance at pin VCORE			0.47		µF
C_{AUX3}	Recommended capacitor at pin AUX3			0.47		µF

Auxiliary Supplies - AUX3 (Backup-Sub-System) Currents

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A	MIN	TYP	MAX	UNIT
$I_{AUX3,RTCon}$	AUX3 current with RTC enabled	RTC and 32-kHz oscillator in backup-subsystem enabled	3 V	25°C			0.83	µA
				85°C			0.95	
$I_{AUX3,RTCoff}$	AUX3 current with RTC disabled	RTC and 32-kHz oscillator in backup-subsystem disabled	3 V	25°C			110	nA
				85°C			165	

Auxiliary Supplies - Auxiliary Supply Monitor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{CC,Monitor}$	Average supply current for monitoring circuitry drawn from VDSYS	LOCKAUX = 0, AUXMRx = 0, AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, Current measured at VDSYS pin	3 V			0.70	µA
$I_{Meas,Monitor}$	Average current drawn from monitored supply during measurement cycle	LOCKAUX = 0, AUXMRx = 0, AUX0MD = 0, AUX1MD = 0, AUX2MD = 1, VDSYS = DVCC, VASYS = AVCC, AUXVCC1 = 3 V, Current measured at AUXVCC1 pin				0.11	µA
$V_{Monitor}$	Auxiliary supply threshold level	AUXLVLx = 0		1.67	1.74	1.80	V
		AUXLVLx = 1		1.87	1.95	2.01	
		AUXLVLx = 2		2.06	2.14	2.21	
		AUXLVLx = 3		2.19	2.27	2.33	
		AUXLVLx = 4		2.33	2.41	2.48	
		AUXLVLx = 5		2.63	2.72	2.79	
		AUXLVLx = 6		2.91	3.02	3.10	
		AUXLVLx = 7		2.91	3.02	3.10	

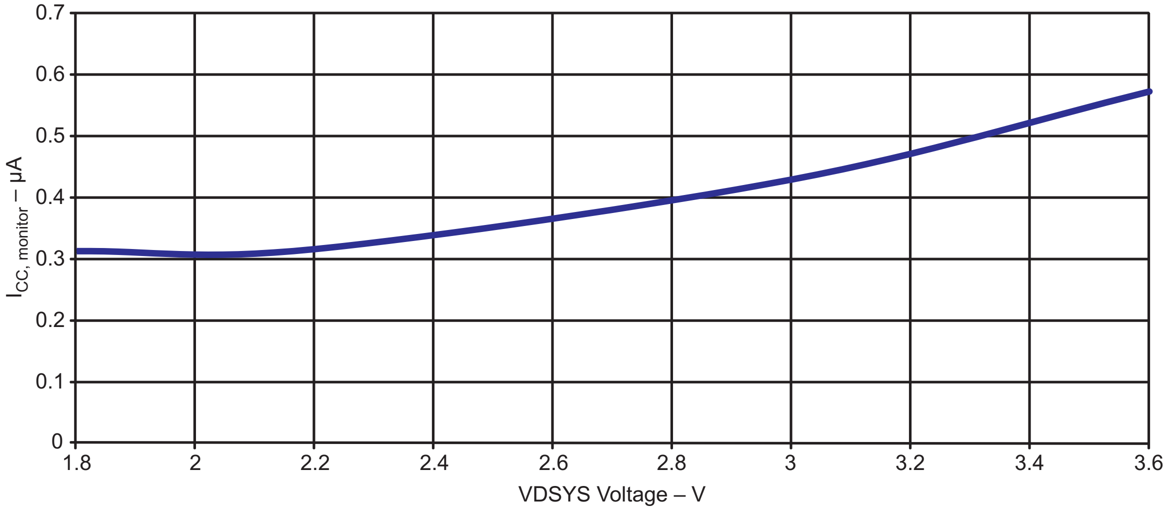


Figure 11. VDSYS Voltage vs $I_{CC,Monitor}$

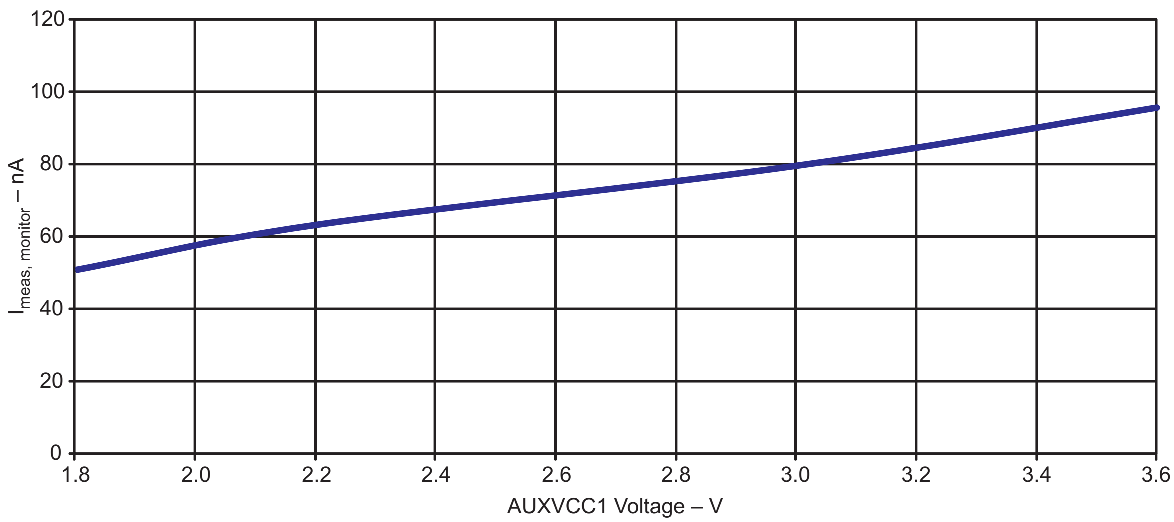


Figure 12. AUXVCC1 Voltage vs $I_{Meas,Monitor}$

Auxiliary Supplies - Switch On-Resistance

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$R_{ON,DVCC}$	On-resistance of switch between DVCC and VDSYS	$I_{LOAD} = I_{CORE} + I_{IO}$ = 10mA + 10mA = 20mA				5	Ω
$R_{ON,DAUX1}$	On-resistance of switch between AUX1 and VDSYS	$I_{LOAD} = I_{CORE} + I_{IO}$ = 10mA + 10mA = 20mA				5	Ω
$R_{ON,DAUX2}$	On-resistance of switch between AUX2 and VDSYS	$I_{LOAD} = I_{CORE} + I_{IO}$ = 10mA + 10mA = 20mA				5	Ω
$R_{ON,AVCC}$	On-resistance of switch between AVCC and V_{ASYS}	$I_{LOAD} = I_{Modules}$ = 10mA				5	Ω
$R_{ON,AAUX1}$	On-resistance of switch between AUX1 and V_{ASYS}	$I_{LOAD} = I_{Modules}$ = 5mA				20	Ω
$R_{ON,AAUX2}$	On-resistance of switch between AUX2 and V_{ASYS}	$I_{LOAD} = I_{Modules}$ = 5mA				20	Ω

Auxiliary Supplies - Switching Time

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_{Switch}	Time from occurence of trigger (SVM or software) to "new" supply connected to system supplies					100	ns
$t_{Recover}$	"Recovery time" after a switch over took place. During that time no further switching takes place.			200		450	µs

Auxiliary Supplies - Switch Leakage

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{SW,Lkg}$	Current into DVCC, AVCC, AUX1 or AUX2 if not selected	Per supply (but not the highest supply)			50	100	nA
I_{Vmax}	Current drawn from highest supply				450	730	nA

Auxiliary Supplies - Auxiliary Supplies to ADC10_A

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_3	Supply voltage divider $V_3 = V_{Supply}/3$			1.8 V	0.58	0.60	0.62	V
				3.0 V	0.98	1.00	1.02	
				3.6 V	1.18	1.20	1.22	
R_{V3}	Load resistance		AUXADCRx = 0				18	kΩ
			AUXADCRx = 1				1.5	kΩ
			AUXADCRx = 2				0.6	kΩ
$t_{Sample,V3}$	Sampling time required if V_3 selected.	AUXADC = 1, ADC10ON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB	AUXADCRx = 0		1000			ns
			AUXADCRx = 1		1000			ns
			AUXADCRx = 2		1000			ns

Auxiliary Supplies - Charge Limiting Resistor

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
R_{CHARGE}	Charge limiting resistor	CHCx = 1	3 V			5	kΩ
		CHCx = 2	3 V			10	
		CHCx = 3	3 V			20	

Timer_A

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{TA}	Timer_A input clock frequency	Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10%	1.8 V/ 3.0 V			25	MHz
$t_{TA,cap}$	Timer_A capture timing	All capture inputs. Minimum pulse width required for capture.	1.8 V/ 3.0 V	20			ns

eUSCI (UART Mode) - Recommended Operating Conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in MBaud)					5	MHz

eUSCI (UART Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2.0 V/3.0 V	10	15	25	ns
		UCGLITx = 1		30	50	85	
		UCGLITx = 2		50	80	150	
		UCGLITx = 3		70	120	200	

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

eUSCI (SPI Master Mode) - Recommended Operating Conditions

PARAMETER		CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz

eUSCI (SPI Master Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 0, UCMODEx = 01 or 10	2.0 V/3.0 V	150			ns
		UCSTEM = 1, UCMODEx = 01 or 10	2.0 V/3.0 V	150			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 0, UCMODEx = 01 or 10	2.0 V/3.0 V	200			ns
		UCSTEM = 1, UCMODEx = 01 or 10	2.0 V/3.0 V	200			
$t_{STE,ACC}$	STE access time, STE active to SIMO data out	UCSTEM = 0, UCMODEx = 01 or 10	2.0 V			50	ns
			3.0 V			30	
		UCSTEM = 1, UCMODEx = 01 or 10	2.0 V			50	
			3.0 V			30	
$t_{STE,DIS}$	STE disable time, STE inactive to SIMO high impedance	UCSTEM = 0, UCMODEx = 01 or 10	2.0 V			40	ns
			3.0 V			25	
		UCSTEM = 1, UCMODEx = 01 or 10	2.0 V			40	
			3.0 V			25	
$t_{SU,MI}$	SOMI input data setup time		2.0 V	50			ns
			3.0 V	30			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $tL_{O/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.

eUSCI (SPI Master Mode) (continued)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{HD,MI}$	SOMI input data hold time		2.0 V	0			ns
			3.0 V	0			
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.0 V			9	ns
			3.0 V			5	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.0 V	0			ns
			3.0 V	0			

(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in Figure 15 and Figure 16.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in Figure 15 and Figure 16.

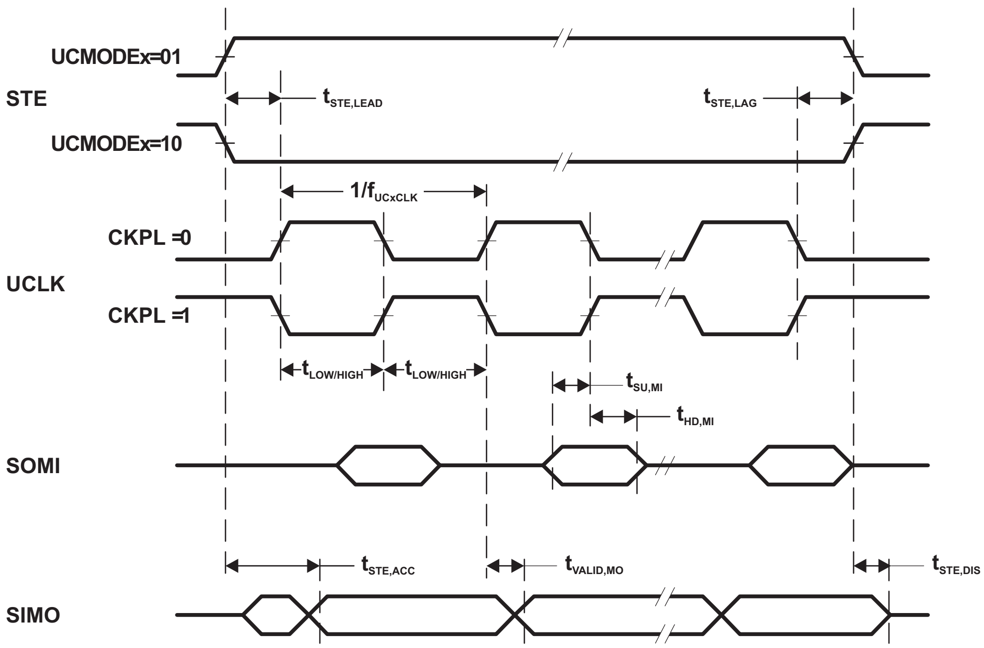


Figure 13. SPI Master Mode, CKPH = 0

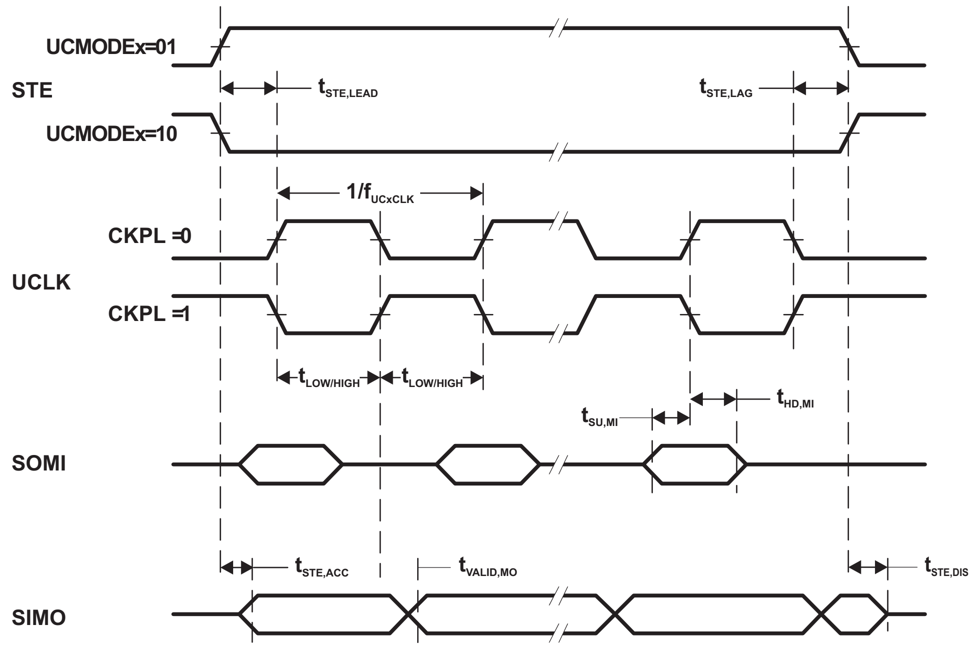


Figure 14. SPI Master Mode, CKPH = 1

eUSCI (SPI Slave Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.0 V	4			ns
			3.0 V	3			
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive		2.0 V	0			ns
			3.0 V	0			
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.0 V			46	ns
			3.0 V			24	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.0 V			38	ns
			3.0 V			25	
$t_{SU,SI}$	SIMO input data setup time		2.0 V	2			ns
			3.0 V	1			
$t_{HD,SI}$	SIMO input data hold time		2.0 V	2			ns
			3.0 V	2			
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.0 V			55	ns
			3.0 V			32	
$t_{HD,SO}$	SOMI output data hold time(3)	C_L = 20 pF	2.0 V	24			ns
			3.0 V	16			

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.
For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in Figure 15 and Figure 16.
(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams inFigure 15 and Figure 16.

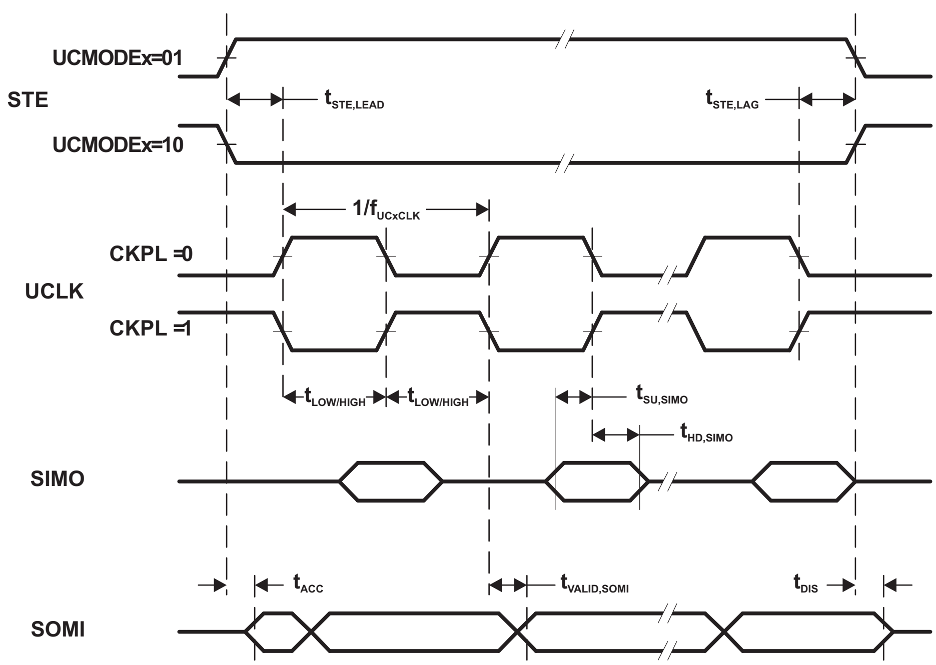


Figure 15. SPI Slave Mode, CKPH = 0

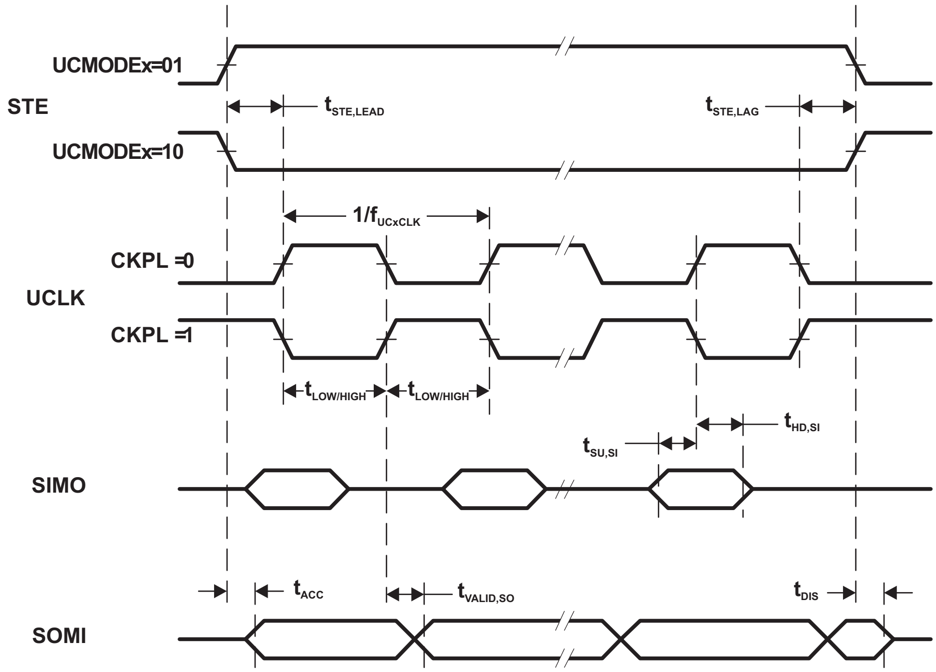


Figure 16. SPI Slave Mode, CKPH = 1

eUSCI (I2C Mode)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 17)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK, ACLK External: UCLK Duty cycle = 50% ± 10%				f_{SYSTEM}	MHz
f_{SCL}	SCL clock frequency		2 V/3 V	0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100 kHz	2 V/3 V	5.1			µs
		f_{SCL} > 100 kHz		1.5			
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100 kHz	2 V/3 V	5.1			µs
		f_{SCL} > 100 kHz		1.4			
$t_{HD,DAT}$	Data hold time		2 V/3 V	0.4			µs
$t_{SU,DAT}$	Data setup time	f_{SCL} = 100 kHz	2 V/3 V	5.0			µs
		f_{SCL} > 100 kHz	2 V/3 V	1.3			
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100 kHz	2 V/3 V	5.2			µs
		f_{SCL} > 100 kHz		1.7			
t_{SP}	Pulse duration of spikes suppressed by input filter	UCGLITx = 0	2 V/3 V	75		220	ns
		UCGLITx = 1		35		120	ns
		UCGLITx = 2		30		60	ns
		UCGLITx = 3		20		35	ns
$t_{TIMEOUT}$	Clock low timeout	UCCLTOx = 1	2 V/3 V		30		ms
		UCCLTOx = 2			33		ms
		UCCLTOx = 3			37		ms

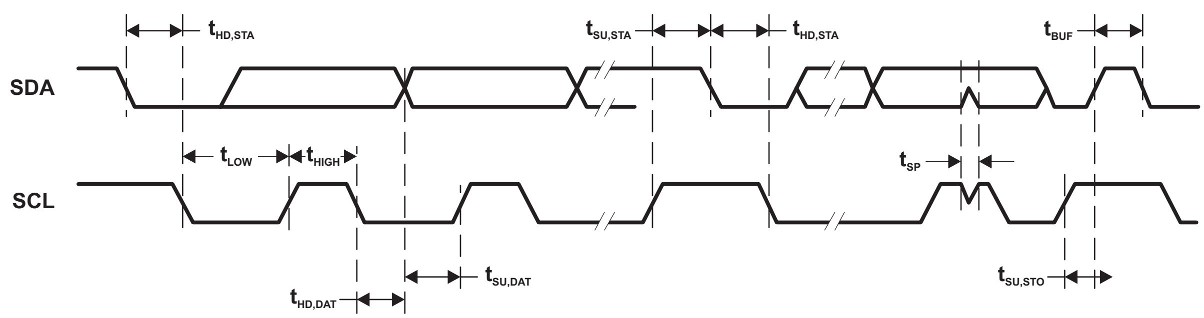


Figure 17. I2C Mode Timing

LCD_C - Recommended Operating Conditions

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
$V_{CC,LCD\_C,CP\ en,3.6}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.6 V	LCDCPEN = 1, 0000 < VLCDx ≤ 1111 (charge pump enabled, V_{LCD} ≤ 3.6 V)	2.2		3.6	V
$V_{CC,LCD\_C,CP\ en,3.3}$	Supply voltage range, charge pump enabled, V_{LCD} ≤ 3.3 V	LCDCPEN = 1, 0000 < VLCDx ≤ 1100 (charge pump enabled, V_{LCD} ≤ 3.3 V)	2.0		3.6	V
$V_{CC,LCD\_C,int.\ bias}$	Supply voltage range, internal biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD\_C,ext.\ bias}$	Supply voltage range, external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 0	2.4		3.6	V
$V_{CC,LCD\_C,VLCDEXT}$	Supply voltage range, external LCD voltage, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.0		3.6	V
$V_{LCDCAP/R33}$	External LCD voltage at LCDCAP/R33, internal or external biasing, charge pump disabled	LCDCPEN = 0, VLCDEXT = 1	2.4		3.6	V

LCD_C - Recommended Operating Conditions (continued)

PARAMETER		CONDITIONS	MIN	NOM	MAX	UNIT
C_{LCDCAP}	Capacitor on LCDCAP when charge pump enabled	LCDCPEN = 1, VLCDx > 0000 (charge pump enabled)		4.7	10	µF
f_{Frame}	LCD frame frequency range	$f_{LCD} = 2 \times mux \times f_{FRAME}$ with mux = 1 (static), 2, 3, 4 up to 8	0		100	Hz
$f_{ACLK,in}$	ACLK input frequency range		30	32	40	kHz
C_{Panel}	Panel capacitance	100-Hz frame frequency			10000	pF
V_{R33}	Analog input voltage at R33	LCDCPEN = 0, VLCDEXT = 1	2.4		V_{CC}+0.2	V
$V_{R23,1/3bias}$	Analog input voltage at R23	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R13}	V_{R03} + 2/3×(V_{R33}-V_{R03})	V_{R33}	V
$V_{R13,1/3bias}$	Analog input voltage at R13 with 1/3 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 0	V_{R03}	V_{R03} + 1/3×(V_{R33}-V_{R03})	V_{R23}	V
$V_{R13,1/2bias}$	Analog input voltage at R13 with 1/2 biasing	LCDREXT = 1, LCDEXTBIAS = 1, LCD2B = 1	V_{R03}	V_{R03} + 1/2×(V_{R33}-V_{R03})	V_{R33}	V
V_{R03}	Analog input voltage at R03	R0EXT = 1	V_{SS}			V
V_{LCD}-V_{R03}	Voltage difference between V_{LCD} and R03	LCDCPEN = 0, R0EXT = 1	2.4		V_{CC}+0.2	V
$V_{LCDREF/R13}$	External LCD reference voltage applied at LCDREF/R13	VLCDREFx = 01	0.8	1.2	1.5	V

LCD_C Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{LCD}	LCD voltage	VLCDx = 0000, VLCDEXT = 0	2.4 V to 3.6 V		V_{CC}		V
		LCDCPEN = 1, VLCDx = 0001	2 V to 3.6 V		2.58		
		LCDCPEN = 1, VLCDx = 0010	2 V to 3.6 V		2.64		
		LCDCPEN = 1, VLCDx = 0011	2 V to 3.6 V		2.71		
		LCDCPEN = 1, VLCDx = 0100	2 V to 3.6 V		2.78		
		LCDCPEN = 1, VLCDx = 0101	2 V to 3.6 V		2.83		
		LCDCPEN = 1, VLCDx = 0110	2 V to 3.6 V		2.90		
		LCDCPEN = 1, VLCDx = 0111	2 V to 3.6 V		2.96		
		LCDCPEN = 1, VLCDx = 1000	2 V to 3.6 V		3.02		
		LCDCPEN = 1, VLCDx = 1001	2 V to 3.6 V		3.07		
		LCDCPEN = 1, VLCDx = 1010	2 V to 3.6 V		3.14		
		LCDCPEN = 1, VLCDx = 1011	2 V to 3.6 V		3.21		
		LCDCPEN = 1, VLCDx = 1100	2 V to 3.6 V		3.27		
		LCDCPEN = 1, VLCDx = 1101	2.2 V to 3.6 V		3.32		
		LCDCPEN = 1, VLCDx = 1110	2.2 V to 3.6 V		3.38		
		LCDCPEN = 1, VLCDx = 1111	2.2 V to 3.6 V		3.44	3.6	
$I_{CC,Peak,CP}$	Peak supply currents due to charge pump activities	LCDCPEN = 1, VLCDx = 1111	2.2 V		400		µA
$t_{LCD,CP,on}$	Time to charge C_{LCD} when discharged	C_{LCD} = 4.7µF, LCDCPEN = 0→1, VLCDx = 1111	2.2 V		150	500	ms
$I_{CP,Load}$	Maximum charge pump load current	LCDCPEN = 1, VLCDx = 1111	2.2 V	50			µA
$R_{LCD,Seg}$	LCD driver output impedance, segment lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10µA	2.2 V			10	kΩ
$R_{LCD,COM}$	LCD driver output impedance, common lines	LCDCPEN = 1, VLCDx = 1000, I_{LOAD} = ±10µA	2.2 V			10	kΩ

SD24_B, Power Supply and Recommended Operating Conditions

				MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	$AV_{CC} = DV_{CC}$, $AV_{SS} = DV_{SS} = 0$ V		2.4		3.6	V
f_{SD}	Modulator clock frequency (1)			0.03		2.3	MHz
V_I	Absolute input voltage range			AV_{SS} - 1V		AV_{CC}	V
V_{IC}	Common-mode input voltage range			AV_{SS} - 1V		AV_{CC}	V
$V_{ID,FS}$	Differential full scale input voltage	$V_{ID} = V_{I,A+} - V_{I,A-}$		$-V_{REF}$/GAIN		$+V_{REF}$/GAIN	mV
V_{ID}	Differential input voltage for specified performance (2)	SD24REFS = 1	SD24GAINx = 1	±910	±920		mV
			SD24GAINx = 2	±455	±460		
			SD24GAINx = 4	±227	±230		
			SD24GAINx = 8	±113	±115		
			SD24GAINx = 16	±57	±58		
			SD24GAINx = 32	±28	±29		
			SD24GAINx = 64	±14	±14.5		
			SD24GAINx = 128	±7	±7.2		
C_{REF}	VREF load capacitance (3)	SD24REFS = 1			100		nF

(1) Modulator clock frequency: MIN = 32.768 kHz - 10% ≈ 30 kHz. MAX = 32.768 kHz × 64 + 10% ≈ 2.3 MHz
(2) The full-scale range (FSR) is defined by $V_{FS+} = +V_{REF}$/GAIN and $V_{FS-} = -V_{REF}$/GAIN: FSR = $V_{FS+} - V_{FS-} = 2*V_{REF}$/GAIN. If V_{REF} is sourced externally, the analog input range should not exceed 80% of V_{FS+} or V_{FS-}; i.e., V_{ID} = 0.8 V_{FS-} to 0.8 V_{FS+}. If V_{REF} is sourced internally, the given V_{ID} ranges apply.
(3) There is no capacitance required on VREF. However, a capacitance of 100nF is recommended to reduce any reference voltage noise.

SD24_B, Analog Input (1)

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
C_I	Input capacitance	SD24GAINx = 1				5		pF
		SD24GAINx = 2				5		
		SD24GAINx = 4				5		
		SD24GAINx = 8				5		
		SD24GAINx = 16				5		
		SD24GAINx = 32, 64, 128				5		
Z_I	Input impedance (Pin A+ or A- to AV_{SS})	f_{SD24} = 1MHz	SD24GAINx = 1	3 V		200		kΩ
			SD24GAINx = 8	3 V		200		
			SD24GAINx = 32	3 V		200		
Z_{ID}	Differential input impedance (Pin A+ to pin A-)	f_{SD24} = 1MHz	SD24GAINx = 1	3 V	300	400		kΩ
			SD24GAINx = 8	3 V		400		
			SD24GAINx = 32	3 V	300	400		

(1) All parameters pertain to each SD24_B converter.

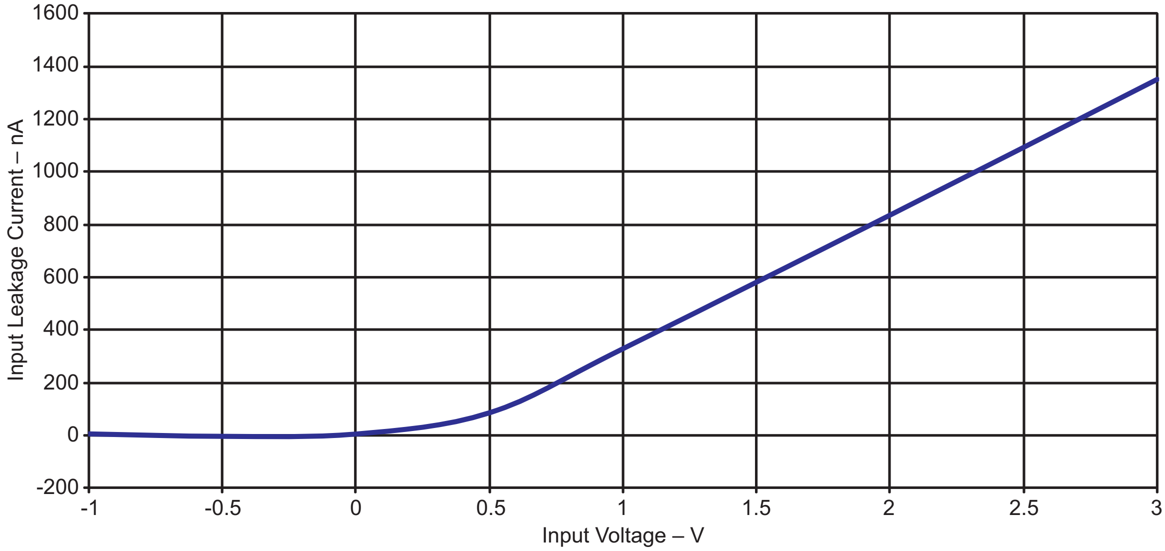


Figure 18. Input Leakage Current vs Input Voltage (Modulator OFF)

SD24_B, Supply Currents

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
$I_{SD,256}$	Analog plus digital supply current per converter (reference not included)	f_{SD24} = 1 MHz, SD24OSR = 256	SD24GAIN: 1	3 V		600	675	µA
			SD24GAIN: 2	3 V		600	675	
			SD24GAIN: 4	3 V		600	675	
			SD24GAIN: 8	3 V		700	750	
			SD24GAIN: 16	3 V		700	750	
			SD24GAIN: 32	3 V		775	850	
			SD24GAIN: 64	3 V		775	850	
			SD24GAIN: 128	3 V		775	850	
$I_{SD,512}$	Analog plus digital supply current per converter (reference not included)	f_{SD24} = 2 MHz, SD24OSR = 512	SD24GAIN: 1	3 V		750	800	µA
			SD24GAIN: 8	3 V		825	900	
			SD24GAIN: 32	3 V		900	1000	

SD24_B, Performance

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFS = 1

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
INL	Integral nonlinearity, end-point fit	SD24GAIN: 1	3 V	-0.01		0.01	% of FSR
		SD24GAIN: 8	3 V	-0.01		0.01	
		SD24GAIN: 32	3 V	-0.01		0.01	
G_{nom}	Nominal gain	SD24GAIN: 1	3 V		1		
		SD24GAIN: 2	3 V		2		
		SD24GAIN: 4	3 V		4		
		SD24GAIN: 8	3 V		8		
		SD24GAIN: 16	3 V		16		
		SD24GAIN: 32	3 V		31.7		
		SD24GAIN: 64	3 V		63.4		
		SD24GAIN: 128	3 V		126.8		

SD24_B, Performance (continued)

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFS = 1

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_G	Gain error(1)	SD24GAIN: 1, with external reference (1.2 V)	3 V	-1		+1	%
		SD24GAIN: 8, with external reference (1.2 V)	3 V	-2		+2	
		SD24GAIN: 32, with external reference (1.2 V)	3 V	-2		+2	
$\Delta E_G/\Delta T$	Gain error temperature coefficient(2), internal reference	SD24GAIN: 1/8/32 (with internal reference)	3 V			50	ppm/°C
$\Delta E_G/\Delta V_{CC}$	Gain error vs V_{CC} (3)	SD24GAIN: 1			0.15		%/V
		SD24GAIN: 8			0.15		
		SD24GAIN: 32			0.4		
E_{OS}[V]	Offset error(4)	SD24GAIN: 1 (with Vdiff = 0V)	3 V			2.3	mV
		SD24GAIN: 8	3 V			0.73	
		SD24GAIN: 32	3 V			0.18	
E_{OS}[FS]	Offset error(4)	SD24GAIN: 1 (with Vdiff = 0V)	3 V	-0.2		0.2	% FS
		SD24GAIN: 8	3 V	-0.5		0.5	
		SD24GAIN: 32	3 V	-0.5		0.5	
$\Delta E_{OS}/\Delta T$	Offset error temperature coefficient(5)	SD24GAIN: 1	3 V		1		uV/°C
		SD24GAIN: 8	3 V		0.15		
		SD24GAIN: 32	3 V		0.1		
$\Delta E_{OS}/\Delta V_{CC}$	Offset error vs V_{CC} (6)	SD24GAIN: 1			600		uV/V
		SD24GAIN: 8			100		
		SD24GAIN: 32			50		
CMRR,DC	Common mode rejection at DC(7)	SD24GAIN: 1	3 V		-110		dB
		SD24GAIN: 8	3 V		-110		
		SD24GAIN: 32	3 V		-110		

(1) The gain error E_G specifies the deviation of the actual gain G_{act} from the nominal gain G_{nom}: $E_G = (G_{act} - G_{nom})/G_{nom}$. It covers process, temperature and supply voltage variations.
(2) The gain error temperature coefficient $\Delta E_G / \Delta T$ specifies the variation of the gain error E_G over temperature ($E_G(T) = (G_{act}(T) - G_{nom})/G_{nom}$) using the box method (i.e. min. and max. values):
$\Delta E_G / \Delta T = (MAX(E_G(T)) - MIN(E_G(T)) / (MAX(T) - MIN(T)) = (MAX(G_{act}(T)) - MIN(G_{act}(T)) / G_{nom} / (MAX(T) - MIN(T))$
with T ranging from -40°C to +85°C.
(3) The gain error vs V_{CC} coefficient $\Delta E_G / \Delta V_{CC}$ specifies the variation of the gain error E_G over supply voltage ($E_G(V_{CC}) = (G_{act}(V_{CC}) - G_{nom})/G_{nom}$) using the box method (i.e. min. and max. values):
$\Delta E_G / \Delta V_{CC} = (MAX(E_G(V_{CC})) - MIN(E_G(V_{CC})) / (MAX(V_{CC}) - MIN(V_{CC})) = (MAX(G_{act}(V_{CC})) - MIN(G_{act}(V_{CC})) / G_{nom} / (MAX(V_{CC}) - MIN(V_{CC}))$
with V_{CC} ranging from 2.4V to 3.6V.
(4) The offset error E_{OS} is measured with shorted inputs in 2's complement mode with +100% FS = V_{REF}/G and -100% FS = -V_{REF}/G.
Conversion between E_{OS} [FS] and E_{OS} [V] is as follows: E_{OS} [FS] = E_{OS} [V]×G/V_{REF}; E_{OS} [V] = E_{OS} [FS]×V_{REF}/G.
(5) The offset error temperature coefficient $\Delta E_{OS} / \Delta T$ specifies the variation of the offset error E_{OS} over temperature using the box method (i.e. min. and max. values):
$\Delta E_{OS} / \Delta T = (MAX(E_{OS}(T)) - MIN(E_{OS}(T)) / (MAX(T) - MIN(T))$
with T ranging from -40°C to +85°C.
(6) The offset error vs V_{CC} $\Delta E_{OS} / \Delta V_{CC}$ specifies the variation of the offset error E_{OS} over supply voltage using the box method (i.e. min. and max. values):
$\Delta E_{OS} / \Delta V_{CC} = (MAX(E_{OS}(V_{CC})) - MIN(E_{OS}(V_{CC})) / (MAX(V_{CC}) - MIN(V_{CC}))$
with V_{CC} ranging from 2.4V to 3.6V.
(7) The DC CMRR specifies the change in the measured differential input voltage value when the common mode voltage varies:
DC CMRR = -20log(Δ_{MAX}/FSR) with Δ_{MAX} being the difference between the minium value and the maximum value measured when sweeping the common mode voltage (for example, calculating with 16-bits FSR = 65536 a maximum change by 1 LSB results in -20log(1/65536) ≈ -96 dB) .
The DC CMRR is measured with both inputs connected to the common mode voltage (i.e. no differential input signal is applied), and the common mode voltage is swept from -1V to V_{CC}.

SD24_B, Performance (continued)

f_{SD24} = 1 MHz, SD24OSRx = 256, SD24REFS = 1

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
CMRR,50Hz	Common mode rejection at 50 Hz(8)	SD24GAIN: 1, f_{CM} = 50 Hz, V_{CM} = 930 mV	3 V		-110		dB
		SD24GAIN: 8, f_{CM} = 50 Hz, V_{CM} = 120 mV	3 V		-110		
		SD24GAIN: 32, f_{CM} = 50 Hz, V_{CM} = 30 mV	3 V		-110		
AC PSRR,ext	AC power supply rejection ratio, external reference(9)	SD24GAIN: 1, V_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-61		dB
		SD24GAIN: 8, V_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-77		
		SD24GAIN: 32, V_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-79		
AC PSRR,int	AC power supply rejection ratio, internal reference(9)	SD24GAIN: 1, V_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-61		dB
		SD24GAIN: 8, VV_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-77		
		SD24GAIN: 32, V_{CC} = 3 V + 50 mV × sin(2π × f_{Vcc} × t), f_{Vcc} = 50 Hz			-79		
XT	Crosstalk between converters(10)	Crosstalk source: SD24GAIN: 1, Sine-wave with max. possible Vpp. f_{IN} = 50 Hz, 100 Hz, Converter under test: SD24GAIN: 1	3 V		-120		dB
		Crosstalk source: SD24GAIN: 1, Sine-wave with max. possible Vpp. f_{IN} = 50 Hz, 100 Hz, Converter under test: SD24GAIN: 8	3 V		-115		
		Crosstalk source: SD24GAIN: 1, Sine-wave with max. possible Vpp. f_{IN} = 50 Hz, 100 Hz, Converter under test: SD24GAIN: 32	3 V		-100		

(8) The AC CMRR is the difference between a hypothetical signal with the amplitude and frequency of the applied common mode ripple applied to the inputs of the ADC and the actual common mode signal spur visible in the FFT spectrum:
AC CMRR = Error Spur [dBFS] - 20log(V_{CM}/1.2V/G) [dBFS] with a common mode signal of V_{CM} × sin(2π × f_{CM} × t) applied to the analog inputs.
The AC CMRR is measured with the both inputs connected to the common mode signal i.e. no differential input signal is applied.
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).

(9) The AC PSRR is the difference between a hypothetical signal with the amplitude and frequency of the applied supply voltage ripple applied to the inputs of the ADC and the actual supply ripple spur visible in the FFT spectrum:
AC PSRR = Error Spur [dBFS] - 20log(50 mV / 1.2 V / G) [dBFS] with a signal of 50 mV × sin(2π × f_{Vcc} × t) added to V_{CC}.
The AC PSRR is measured with the inputs grounded; that is, no analog input signal is applied.
With the specified typical values the error spur is within the noise floor (as specified by the SINAD values).
SD24GAIN: 1 → Hypothetical signal: 20log(50 mV / 1.2 V / 1) = -27.6 dBFS
SD24GAIN: 8 → Hypothetical signal: 20log(50 mV / 1.2 V / 8) = -9.5 dBFS
SD24GAIN: 32 → Hypothetical signal: 20log(50 mV / 1.2 V / 32) = 2.5 dBFS

(10) The crosstalk XT is specified as the tone level of the signal applied to the crosstalk source seen in the spectrum of the converter under test. It is measured with the inputs of the converter under test being grounded.

SD24_B, AC Performance

f_{SD24} = 1MHz, SD24OSRx = 256, SD24REFS = 1

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAIN: 1	f_{IN} = 50Hz (1)	3 V	85	87		dB
		SD24GAIN: 2		3 V		86		
		SD24GAIN: 4		3 V		85		
		SD24GAIN: 8		3 V	82	84		
		SD24GAIN: 16		3 V		80		
		SD24GAIN: 32		3 V	73	74		
		SD24GAIN: 64		3 V		68		
		SD24GAIN: 128		3 V		62		
THD	Total Harmonic distiortion	SD24GAIN: 1	f_{IN} = 50Hz (1)	3 V		100		dB
		SD24GAIN: 8		3 V		90		
		SD24GAIN: 32		3 V		80		

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

SD24_B, AC Performance

f_{SD24} = 2MHz, SD24OSRx = 512, SD24REFS = 1

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAIN: 1	f_{IN} = 50Hz (1)	3 V		87		dB
		SD24GAIN: 2		3 V		86		
		SD24GAIN: 4		3 V		85		
		SD24GAIN: 8		3 V		84		
		SD24GAIN: 16		3 V		81		
		SD24GAIN: 32		3 V		76		
		SD24GAIN: 64		3 V		71		
		SD24GAIN: 128		3 V		65		

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times fIN \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

SD24_B, AC Performance

f_{SD24} = 32 kHz, SD24OSRx = 512, SD24REFS = 1

PARAMETER		TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise + distortion ratio	SD24GAIN: 1	f_{IN} = 12Hz (1)	3 V		89		dB
		SD24GAIN: 2		3 V		85		
		SD24GAIN: 4		3 V		84		
		SD24GAIN: 8		3 V		86		
		SD24GAIN: 16		3 V		80		
		SD24GAIN: 32		3 V		76		
		SD24GAIN: 64		3 V		67		
		SD24GAIN: 128		3 V		61		

(1) The following voltages were applied to the SD24_B inputs:
$V_{I,A+}(t) = 0\ V + V_{PP}/2 \times \sin(2\pi \times fIN \times t)$
$V_{I,A-}(t) = 0\ V - V_{PP}/2 \times \sin(2\pi \times f_{IN} \times t)$
resulting in a differential voltage of $V_{ID} = V_{I,A+}(t) - V_{I,A-}(t) = V_{PP} \times \sin(2\pi \times f_{IN} \times t)$ with V_{PP} being selected as the maximum value allowed for a given range (according to SD24_B recommended operating conditions).

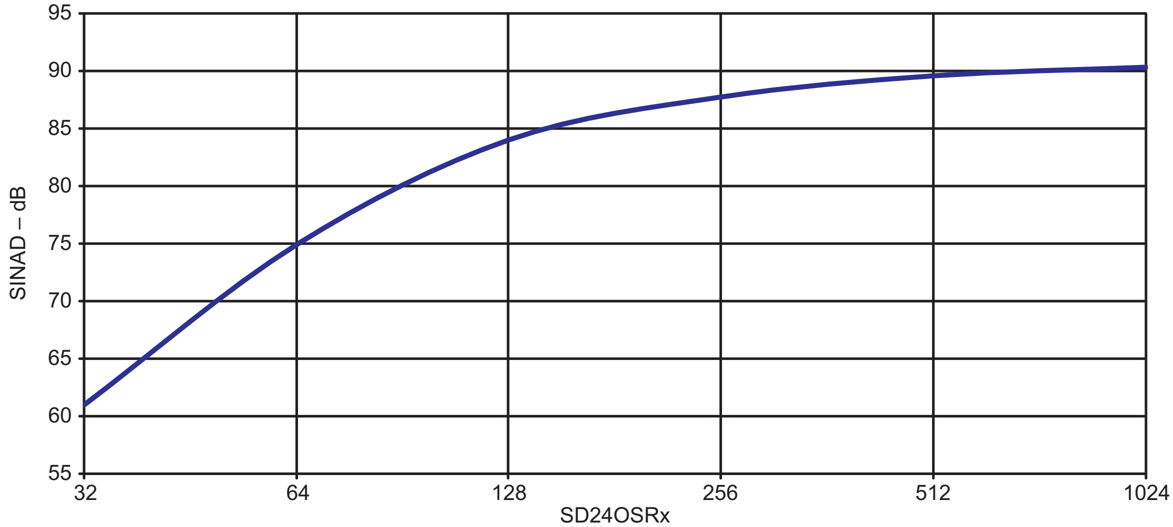


Figure 19. SINAD vs OSR
(f_{SD24} = 1 MHz, SD24REFS = 1, SD24GAIN = 1)

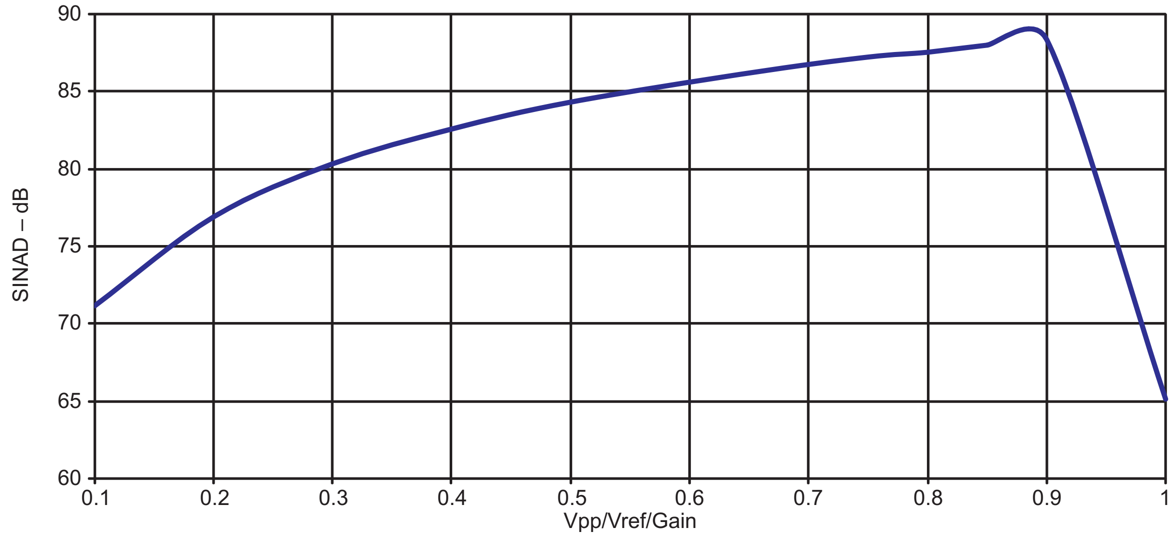


Figure 20. SINAD vs V_{PP}

SD24_B, External Reference Input

ensure correct input voltage range according to V_{REF}

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$V_{REF(I)}$	Input voltage	SD24REFS = 0	3 V	1.0	1.20	1.5	V
$I_{REF(I)}$	Input current	SD24REFS = 0	3 V			50	nA

10-Bit ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		1.8		3.6	V
$V_{(Ax)}$	Analog input voltage range(1)	All ADC10_A pins		0		AV_{CC}	V
I_{ADC10_A}	Operating supply current into AVCC terminal, REF module and reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON =1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 00	2.2 V		70	105	µA
			3 V		80	115	µA
	Operating supply current into AVCC terminal, REF module on, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 1, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 01	3 V		130	185	µA
	Operating supply current into AVCC terminal, REF module off, reference buffer on	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 10, VEREF = 2.5 V	3 V		108	160	µA
	Operating supply current into AVCC terminal, REF module off, reference buffer off	$f_{ADC10CLK}$ = 5 MHz, ADC10ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC10DIV = 0, ADC10SREF = 11, VEREF = 2.5 V	3 V		74	105	µA
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC10_A capacitor array including wiring and pad.	2.2 V		3.5		pF
R_I	Input MUX ON resistance	$AV_{CC} > 2$ V, $0 \text{ V} \le V_{Ax} \le AV_{CC}$				36	kΩ
		$1.8 \text{ V} < AV_{CC} < 2$ V, $0 \text{ V} \le V_{Ax} \le AV_{CC}$				96	kΩ

(1) The analog input voltage range must be within the selected reference voltage range V_{R+} to V_{R-} for valid conversion results. The external reference voltage requires decoupling capacitors. Two decoupling capacitors, 10 µF and 100 nF, should be connected to VREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

10-Bit ADC, Timing Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC10CLK}$		For specified performance of ADC10_A linearity parameters	2.2 V, 3 V	0.45	5	5.5	MHz
$f_{ADC10OSC}$	Internal ADC10_A oscillator(1)	ADC10DIV = 0, $f_{ADC10CLK}$ = $f_{ADC10OSC}$	2.2 V, 3 V	4.4	5.0	5.6	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 12 ADC10CLK cycles, 10-bit mode $f_{ADC10OSC}$ = 4 MHz to 5 MHz	2.2 V, 3 V	2.4		3.0	µs
		External $f_{ADC10CLK}$ from ACLK, MCLK or SMCLK, ADC10SSEL ≠ 0			(2)		µs
$t_{ADC10ON}$	Turn on settling time of the ADC	See (3)				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I = 96 kΩ, C_I = 3.5 pF(4)	1.8 V	3			µs
		R_S = 1000 Ω, R_I = 36 kΩ, C_I = 3.5 pF(4)	3 V	1			µs

(1) The ADC10OSC is sourced directly from MODOSC inside the UCS.
(2) 12 × ADC10DIV × 1/$f_{ADC10CLK}$
(3) The condition is that the error in a conversion started after $t_{ADC10ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(4) Approximately eight Tau (t) are needed to get an error of less than ±0.5 LSB

10-Bit ADC, Linearity Parameters

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ (V_{eREF+} – $V_{eREF–}$)min ≤ 1.6 V	2.2 V, 3 V			±1.0	LSB
		1.6 V < (V_{eREF+} – $V_{eREF–}$)min ≤ V_{AVCC}				±1.0	
E_D	Differential linearity error	(V_{eREF+} – $V_{eREF–}$)min ≤ (V_{eREF+} – $V_{eREF–}$), C_{VeREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E_O	Offset error	(V_{eREF+} – $V_{eREF–}$)min ≤ (V_{eREF+} – $V_{eREF–}$), Internal impedance of source R_S < 100 Ω, C_{VREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E_G	Gain error	(V_{eREF+} – $V_{eREF–}$)min ≤ (V_{eREF+} – $V_{eREF–}$), C_{VeREF+} = 20 pF	2.2 V, 3 V			±1.0	LSB
E_T	Total unadjusted error	(V_{eREF+} – $V_{eREF–}$)min ≤ (V_{eREF+} – $V_{eREF–}$), C_{VeREF+} = 20 pF	2.2 V, 3 V		±1.0	±2.0	LSB

10-Bit ADC, External Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{eREF+}	Positive external reference voltage input	V_{eREF+} > $V_{eREF–}$ (2)		1.4		AV_{CC}	V
$V_{eREF–}$	Negative external reference voltage input	V_{eREF+} > $V_{eREF–}$ (3)		0		1.2	V
(V_{eREF+} – $V_{eREF–}$)	Differential external reference voltage input	V_{eREF+} > $V_{eREF–}$ (4)		1.4		AV_{CC}	V
I_{VeREF+} $I_{VeREF–}$	Static input current	1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , $V_{eREF–}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTx = 0x0001, Conversion rate 200 ksps	2.2 V, 3 V		±8.5	±26	µA
		1.4 V ≤ V_{eREF+} ≤ V_{AVCC} , $V_{eREF–}$ = 0 V, $f_{ADC10CLK}$ = 5 MHz, ADC10SHTX = 0x1000, Conversion rate 20 ksps	2.2 V, 3 V			±1	µA
$C_{VeREF+/-}$	Capacitance at VeREF+ or VeREF- terminal	See (5)		10			µF

(1) The external reference is used during ADC conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 10-bit accuracy.
(2) The accuracy limits the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements.
(3) The accuracy limits the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy limits minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.
(5) Two decoupling capacitors, 10 µF and 100 nF, should be connected to VeREF to decouple the dynamic current required for an external reference source if it is used for the ADC10_A. Also see the *MSP430x5xx and MSP430x6xx Family User's Guide* (SLAU208).

REF, Built-In Reference

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage	REFVSEL = {2} for 2.5 V, REFON = 1	3 V	2.47	2.51	2.55	V
		REFVSEL = {1} for 2.0 V, REFON = 1	3 V	1.95	1.99	2.03	
		REFVSEL = {0} for 1.5 V, REFON = 1	2.2 V, 3 V	1.46	1.50	1.54	
$AV_{CC(min)}$	AVCC minimum voltage, Positive built-in reference active	REFVSEL = {0} for 1.5 V		1.8			V
		REFVSEL = {1} for 2.0 V		2.2			
		REFVSEL = {2} for 2.5 V		2.7			
I_{REF+}	Operating supply current into AVCC terminal(1)	$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {2} for 2.5 V	3 V		23	30	µA
		$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {1} for 2.0 V	3 V		21	27	µA
		$f_{ADC10CLK}$ = 5 MHz, REFON = 1, REFBURST = 0, REFVSEL = {0} for 1.5 V	3 V		19	25	µA
TC_{REF+}	Temperature coefficient of built-in reference(2)	REFVSEL = {0, 1, 2}, REFON = 1			10	50	ppm/°C
I_{SENSOR}	Operating supply current into AVCC terminal	REFON = 1, ADC10ON = 1, INCH = 0Ah, T_A = 30°C	2.2 V		145	220	µA
			3 V		170	245	
V_{SENSOR}	See (3)	REFON = 1, ADC10ON = 1, INCH = 0Ah, T_A = 30°C	2.2 V		780		mV
			3 V		780		
V_{MID}	AV_{CC} divider at channel 11	ADC10ON = 1, INCH = 0Bh, V_{MID} is ~0.5 × V_{AVCC}	2.2 V	1.08	1.1	1.12	V
			3 V	1.48	1.5	1.52	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(4)	REFON = 1, ADC10ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB		30			µs
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(5)	ADC10ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB		1			µs
PSRR_DC	Power supply rejection ratio (dc)	$AV_{CC} = AV_{CC\ (min)} - AV_{CC(max)}$ T_A = 25 °C REFVSEL = {0, 1, 2}, REFON = 1			120	300	µV/V
PSRR_AC	Power supply rejection ratio (ac)	$AV_{CC} = AV_{CC\ (min)} - AV_{CC(max)}$ T_A = 25 °C f = 1 kHz, ΔVpp = 100 mV REFVSEL = {0, 1, 2}, REFON = 1			1		mV/V
t_{SETTLE}	Settling time of reference voltage(6)	$AV_{CC} = AV_{CC\ (min)} - AV_{CC(max)}$ REFVSEL = {0, 1, 2}, REFON = 0 → 1			75		µs
$V_{SD24REF}$	SD24_B internal reference voltage	SD24REFS = 1	3 V	1.137	1.151	1.165	V
t_{ON}	SD24_B internal reference turn-on time(7)	SD24REFS = 0->1, C_{REF} = 100 nF	3 V		200		µs

(1) The internal reference current is supplied via terminal AV_{CC}. Consumption is independent of the ADC10ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting an A/D conversion.
(2) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C)/(85°C – (–40°C)).
(3) The temperature sensor offset can be as much as ±20°C. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
(4) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor-on time $t_{SENSOR(on)}$.
(5) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.
(6) The condition is that the error in a conversion started after t_{REFON} is ≤ 1 LSB.
(7) The condition is that SD24_B conversion started after t_{ON} should guarantee specified SINAD values for the selected Gain, OSR and f_{SD24}.

Flash Memory

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$DV_{CC(PGM/ERASE)}$	Program and erase supply voltage		1.8		3.6	V
I_{PGM}	Average supply current from DVCC during program			3	5	mA
I_{ERASE}	Average supply current from DVCC during erase			6	11	mA
I_{MERASE}, I_{BANK}	Average supply current from DVCC during mass erase or bank erase			6	11	mA
t_{CPT}	Cumulative program time	See (1)			16	ms
	Program and erase endurance		10^4	10^5		cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
t_{Word}	Word or byte program time	See (2)	64		85	µs
$t_{Block,\ 0}$	Block program time for first byte or word	See (2)	49		65	µs
$t_{Block,\ 1–(N–1)}$	Block program time for each additional byte or word, except for last byte or word	See (2)	37		49	µs
$t_{Block,\ N}$	Block program time for last byte or word	See (2)	55		73	µs
t_{Erase}	Erase time for segment erase, mass erase, and bank erase when available	See (2)	23		32	ms
$f_{MCLK,MGR}$	MCLK frequency in marginal read mode (FCTL4.MGR0 = 1 or FCTL4. MGR1 = 1)		0		1	MHz

(1) The cumulative program time must not be exceeded when writing to a 128-byte flash block. This parameter applies to all programming methods: individual word- or byte-write and block-write modes.
(2) These values are hardwired into the flash controller's state machine.

JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.2 V, 3 V	0		20	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.2 V, 3 V	0.025		15	µs
$t_{SBW,\ En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.2 V, 3 V			1	µs
$t_{SBW,Rst}$	Spy-Bi-Wire return to normal operation time		15		100	µs
f_{TCK}	TCK input frequency for 4-wire JTAG (2)	2.2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pulldown resistance on TEST	2.2 V, 3 V	45	60	80	kΩ

(1) Tools accessing the Spy-Bi-Wire interface need to wait for the minimum $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
(2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

INPUT/OUTPUT SCHEMATICS

Port P1, P1.0 and P1.1, Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

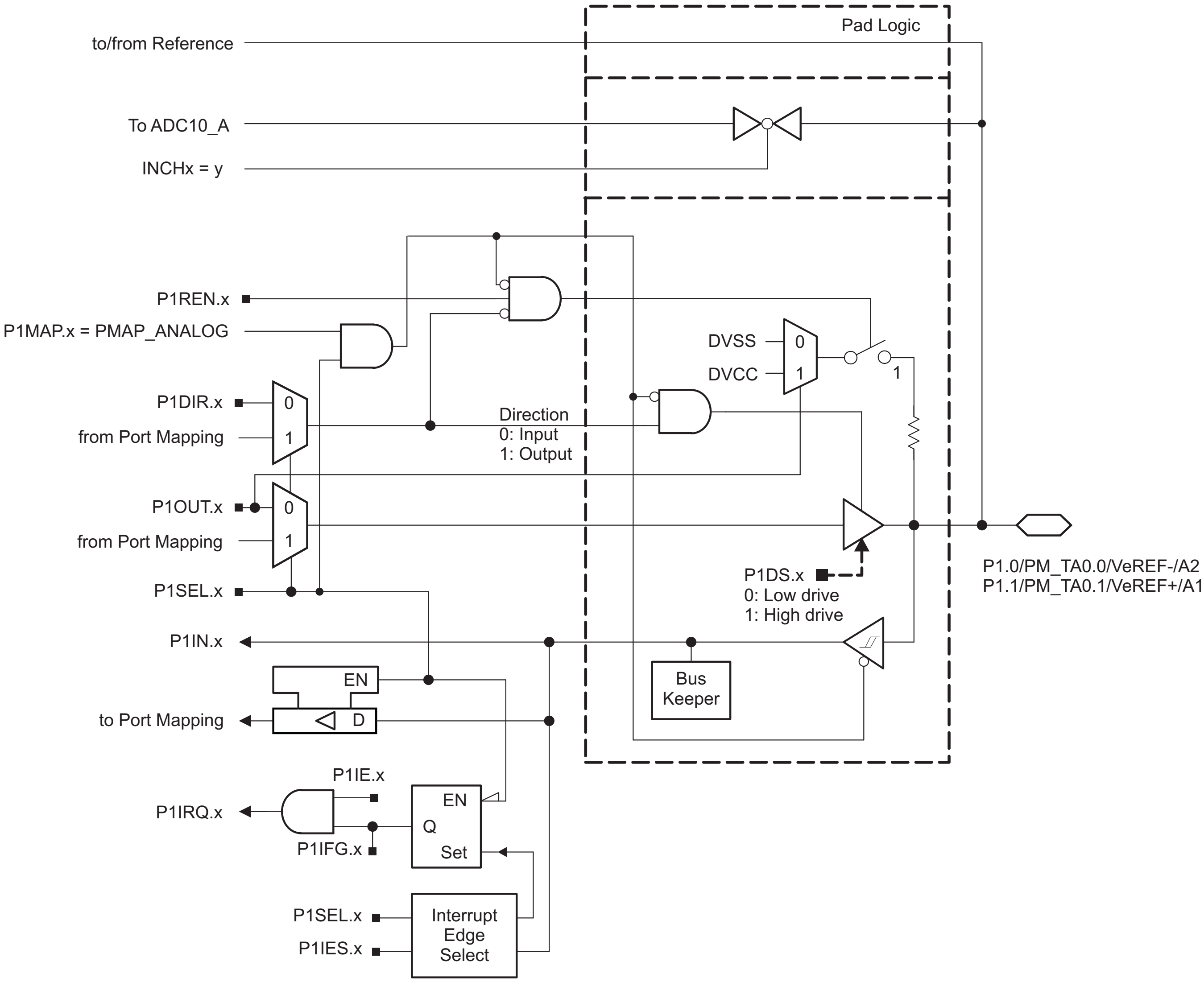


Table 63. Port P1 (P1.0 and P1.1) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P1DIR.x	P1SEL.x	P1MAPx
P1.0/PM_TA0.0/ VeREF-/A2	0	P1.0 (I/O)	I: 0; O: 1	0	X
		TA0.CCI0A	0	1	default
		TA0.TA0	1	1	default
		VeREF-/A2(2)	X	1	= 31
P1.1/PM_TA0.1/ VeREF+/A1	1	P1.1 (I/O)	I: 0; O: 1	0	X
		TA0.CCI1A	0	1	default
		TA0.TA1	1	1	default
		VeREF+/A1(2)	X	1	= 31

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver as well as the input Schmitt trigger.

Port P1, P1.2, Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

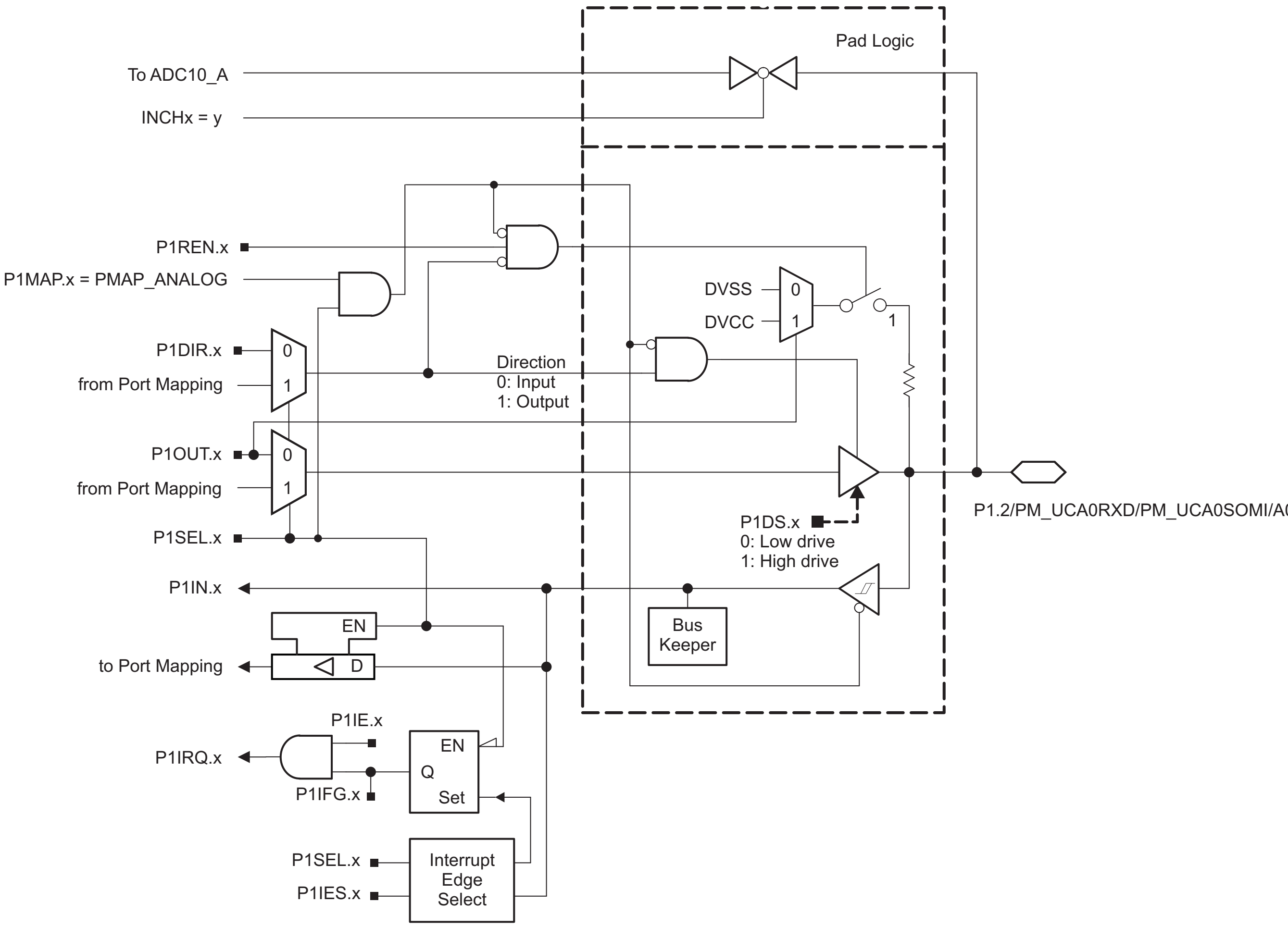


Table 64. Port P1 (P1.2) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P1DIR.x	P1SEL.x	P1MAPx
P1.2/PM_UCA0RXD/ PM_UCA0SOMI/A0	2	P1.2 (I/O)	I: 0; O: 1	0	X
		UCA0RXD/UCA0SOMI	X	1	default
		A0 (2)	X	1	= 31

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver as well as the input Schmitt trigger.

Port P1, P1.3 to P1.5, Input/Output With Schmitt Trigger (MSP430F67xxIPZ and MSP430F67xxIPN)

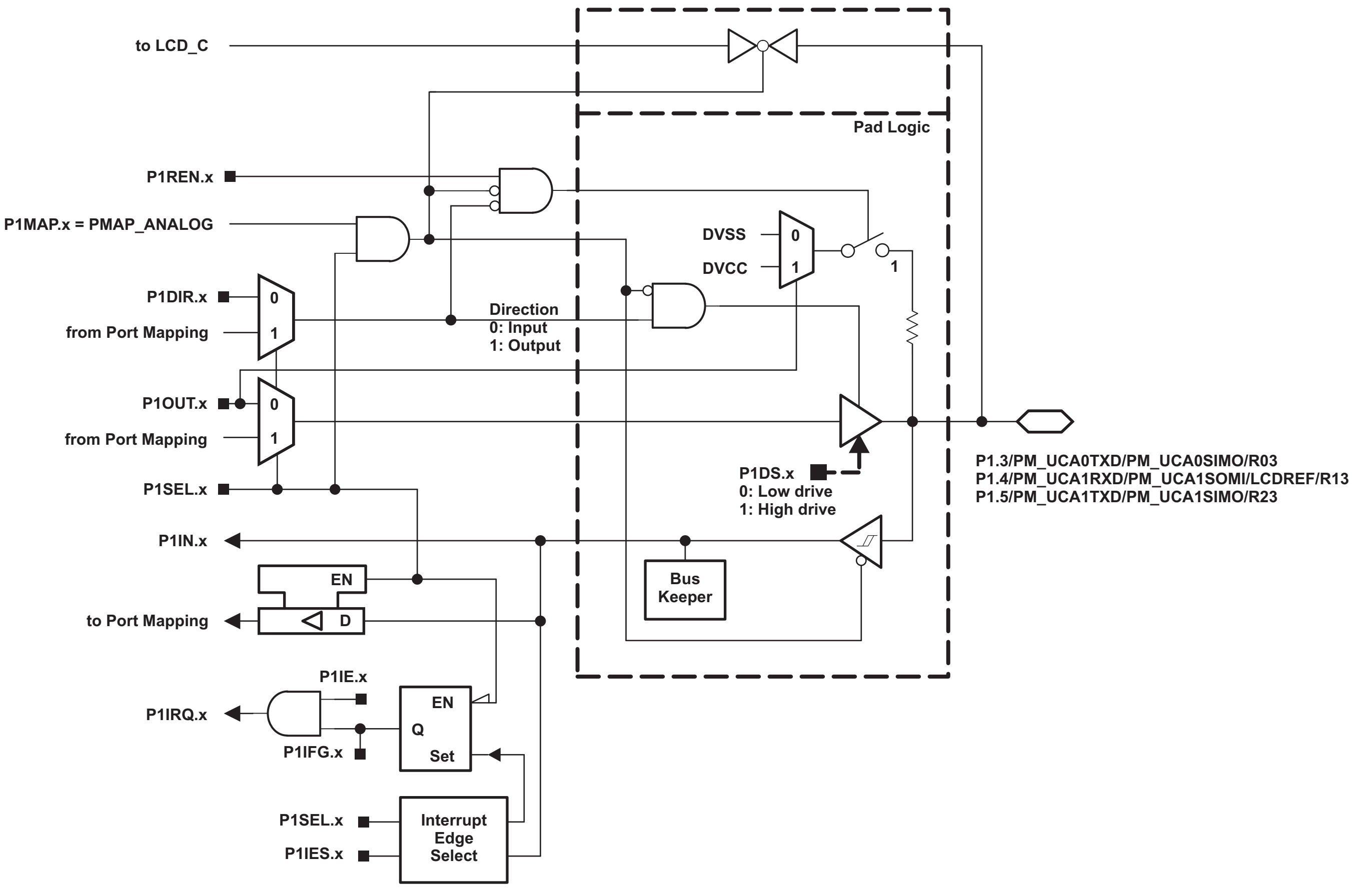


Table 65. Port P1 (P1.3 to P1.5) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P1DIR.x	P1SEL.x	P1MAPx
P1.3/PM_UCA0TXD/ PM_UCA0SIMO/R03	3	P1.3 (I/O)	I: 0; O: 1	0	X
		UCA0TXD/UCA0SIMO	X	1	default
		R03(2)	X	1	= 31
P1.4/PM_UCA1RXD/ PM_UCA1SOMI/ LCDREF/R13	4	P1.4 (I/O)	I: 0; O: 1	0	X
		UCA1RXD/UCA1SOMI	X	1	default
		LCDREF/R13(2)	X	1	= 31
P1.5/PM_UCA1TXD/ PM_UCA1SIMO/R23	5	P1.5 (I/O)	I: 0; O: 1	0	X
		UCA1TXD/UCA1SIMO	X	1	default
		R23(2)	X	1	= 31

(1) X = Don't care
(2) Setting P1SEL.x bit together with P1MAPx = PM_ANALOG disables the output driver as well as the input Schmitt trigger.

Port P1, P1.6 and P1.7 (MSP430F67xxIPZ and MSP430F67xxIPN), Port P2, P2.0 and P2.1 (MSP430F67xxIPZ Only) Input/Output With Schmitt Trigger

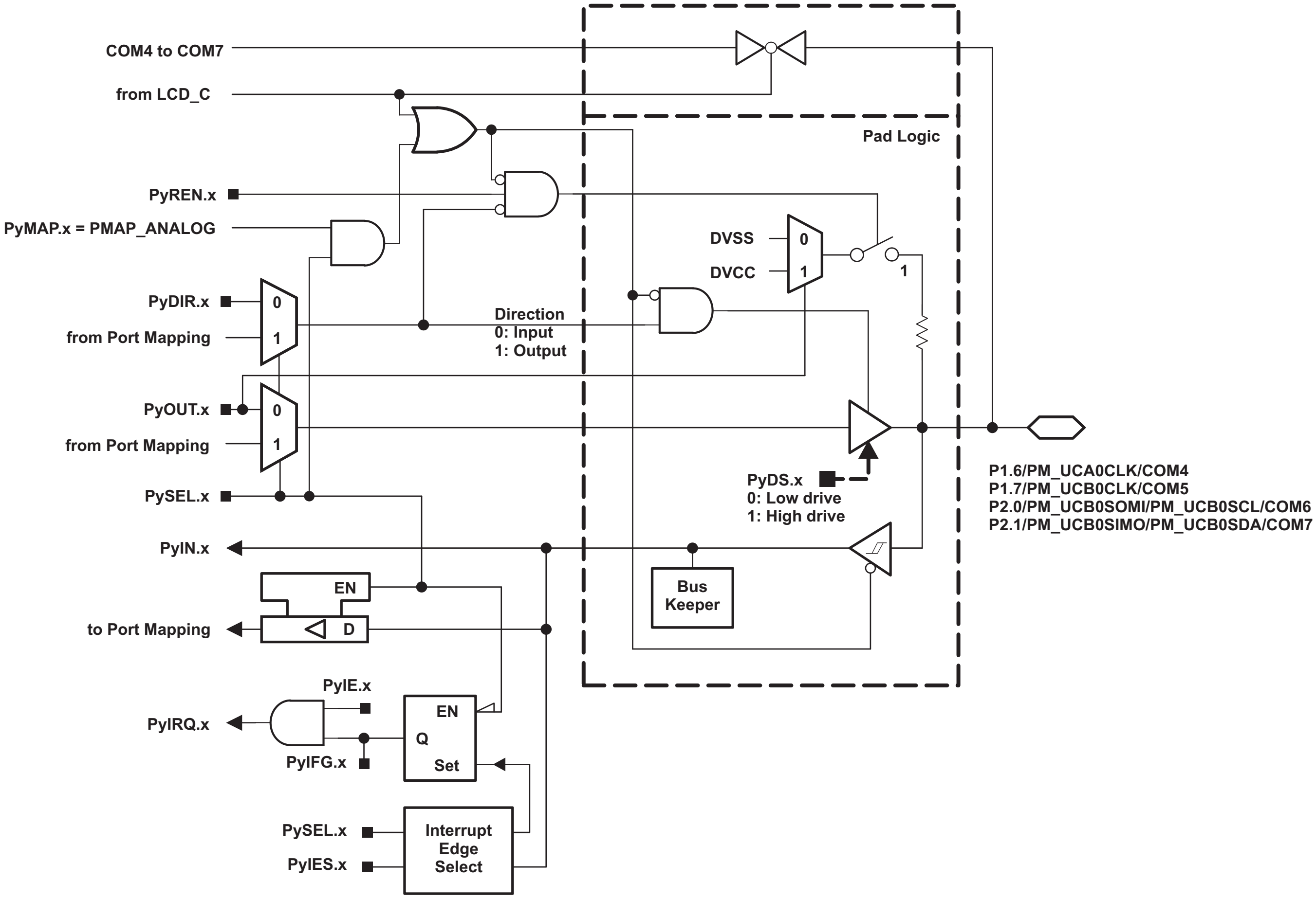


Table 66. Port P1 (P1.6 and P1.7) Pin Functions (MSP430F67xxIPZ and MSP430F67xxIPN)

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]			
			P1DIR.x	P1SEL.x	P1MAPx	COM4,5 Enable Signal
P1.6/PM_UCA0CLK/COM4	6	P1.6 (I/O)	I: 0; O: 1	0	X	0
		UCA0CLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		COM4	X	X	X	1
P1.7/PM_UCB0CLK/COM5	7	P1.7 (I/O)	I: 0; O: 1	0	X	0
		UCB0CLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		COM5	X	X	X	1

(1) X = Don't care

Table 67. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]			
			P2DIR.x	P2SEL.x	P2MAPx	COM6,7 Enable Signal
P2.0/PM_UCB0SOMI/ PM_UCB0SCL/COM6	0	P2.0 (I/O)	I: 0; O: 1	0	X	0
		UCB0SOMI/UCB0SCL	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		COM6	X	X	X	1
P2.1/PM_UCB0SIMO/ PM_UCB0SDA/COM7	1	P2.1 (I/O)	I: 0; O: 1	0	X	0
		UCB0SIMO/UCB0SDA	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		COM7	X	X	X	1

(1) X = Don't care

Port P2, P2.2 to P2.7, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

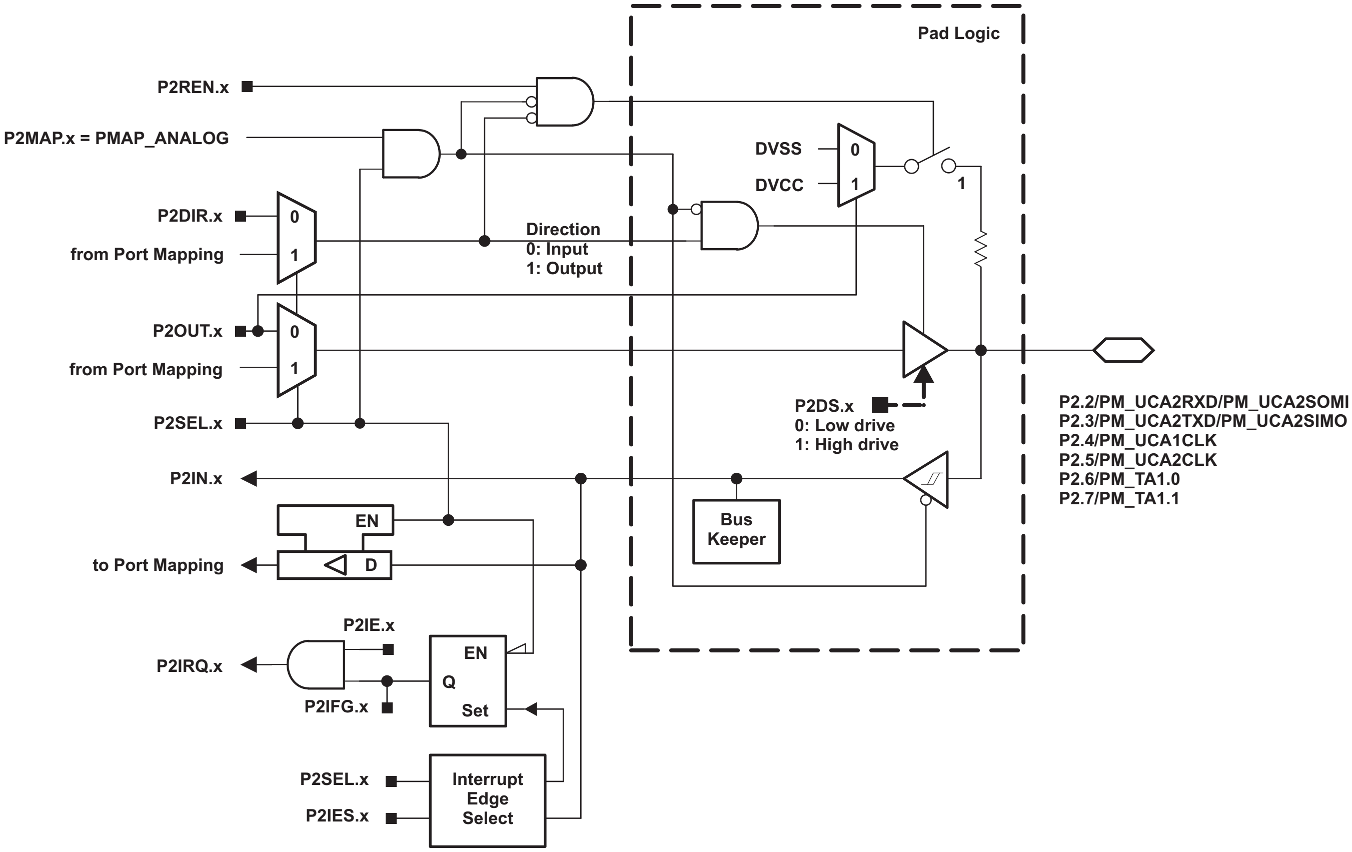


Table 68. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]		
			P2DIR.x	P2SEL.x	P2MAPx
P2.2/PM_UCA2RXD/ PM_UCA2SOMI	2	P2.2 (I/O)	I: 0; O: 1	0	X
		UCA2RXD/UCA2SOMI	X	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P2.3/PM_UCA2TXD/ PM_UCA2SIMO	3	P2.3 (I/O)	I: 0; O: 1	0	X
		UCA2TXD/UCA2SIMO	X	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P2.4/PM_UCA1CLK	4	P2.4 (I/O)	I: 0; O: 1	0	X
		UCA1CLK	X	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P2.5/PM_UCA2CLK	5	P2.5 (I/O)	I: 0; O: 1	0	X
		UCA2CLK	X	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P2.6/PM_TA1.0	6	P2.6 (I/O)	I: 0; O: 1	0	X
		TA1.CC10A	0	1	default
		TA1.TA0	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P2.7/PM_TA1.1	7	P2.7 (I/O)	I: 0; O: 1	0	X
		TA1.CCI1A	0	1	default
		TA1.TA1	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31

(1) X = Don't care

Port P3, P3.0 to P3.3, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

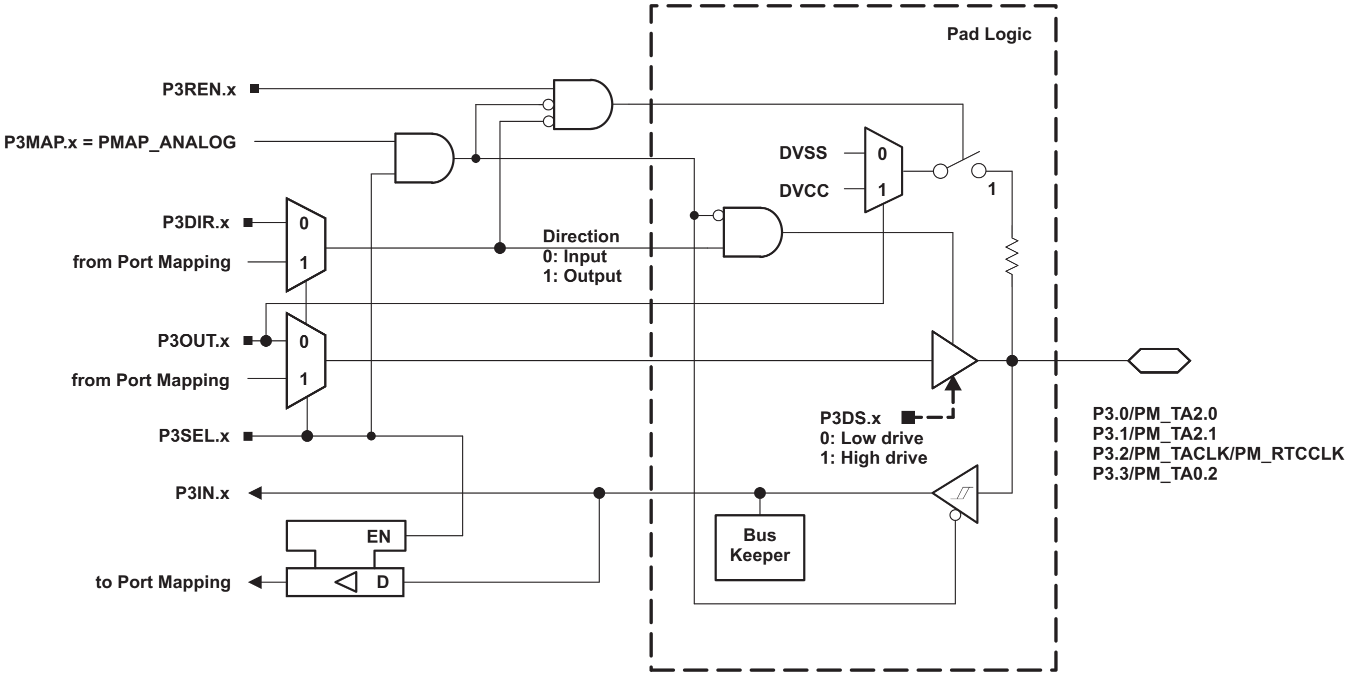


Table 69. Port P3 (P3.0 to P3.3) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P3DIR.x	P3SEL.x	P3MAPx
P3.0/PM_TA2.0	0	P3.0 (I/O)	I: 0; O: 1	0	X
		TA2.CC10A	0	1	default
		TA2.TA0	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P3.1/PM_TA2.1	1	P3.1 (I/O)	I: 0; O: 1	0	X
		TA2.CCI1A	0	1	default
		TA2.TA1	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P3.2/PM_TACLK/ PM_RTCCLK	2	P3.2 (I/O)	I: 0; O: 1	0	X
		TACLK	0	1	default
		RTCCLK	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31
P3.3/PM_TA0.2	3	P3.3 (I/O)	I: 0; O: 1	0	X
		TA0.CCI2A	0	1	default
		TA0.TA2	1	1	default
		Output driver and input Schmitt trigger disabled	X	1	= 31

(1) X = Don't care

Port P3, P3.4 to P3.7 , Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

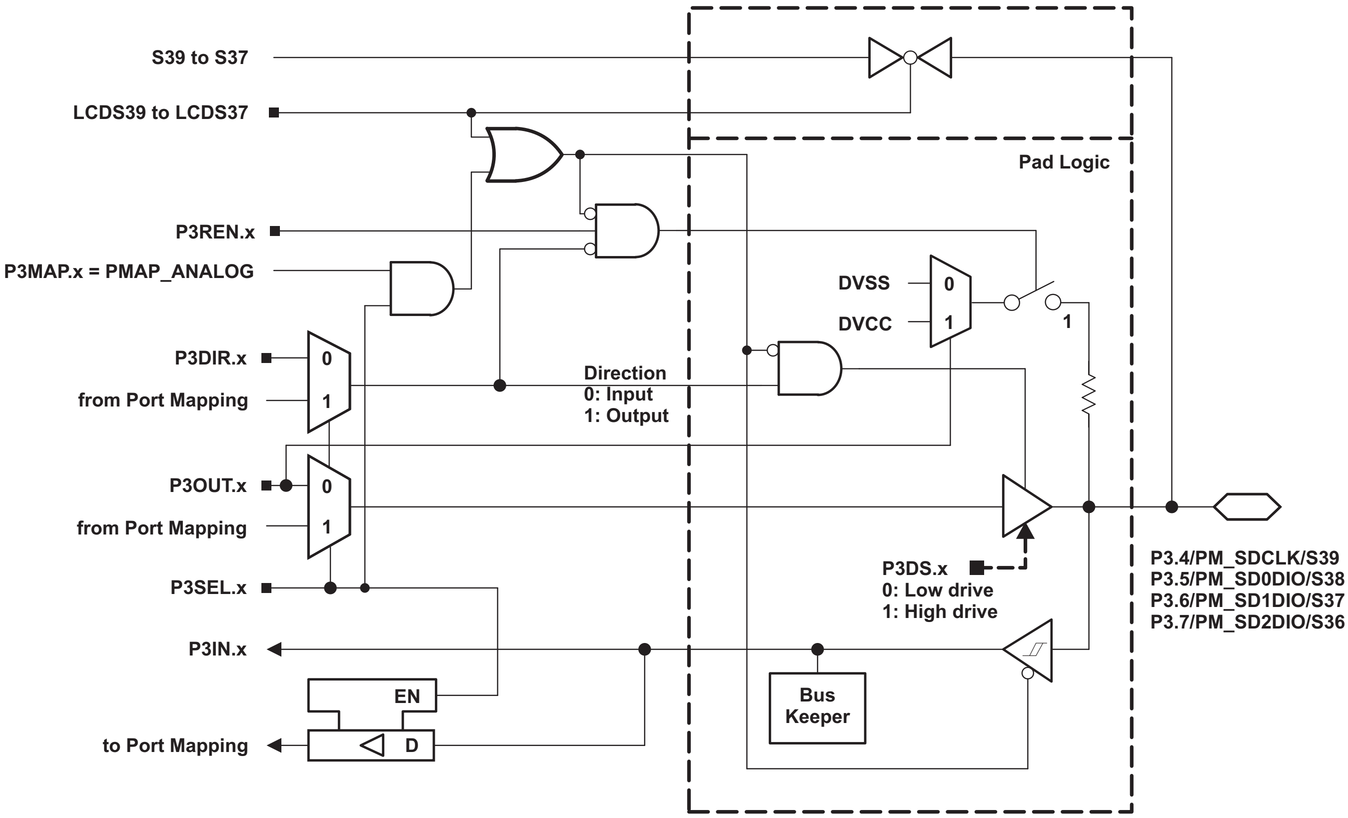


Table 70. Port P3 (P3.4 to P3.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]			
			P3DIR.x	P3SEL.x	P3MAPx	LCDS39...36
P3.4/PM_SDCLK/S39	4	P3.4 (I/O)	I: 0; O: 1	0	X	0
		SDCLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S39	X	X	X	1
P3.5/PM_SD0DIO/S38	5	P3.5 (I/O)	I: 0; O: 1	0	X	0
		SD0DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S38	X	X	X	1
P3.6/PM_SD1DIO/S37	6	P3.6 (I/O)	I: 0; O: 1	0	X	0
		SD1DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S37	X	X	X	1
P3.7/PM_SD2DIO/S36	7	P3.7 (I/O)	I: 0; O: 1	0	X	0
		SD2DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S36	X	X	X	1

(1) X = Don't care

Port P4, Port P5, Port P6, Port P7, Port P8, P8.0 to P8.3 Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

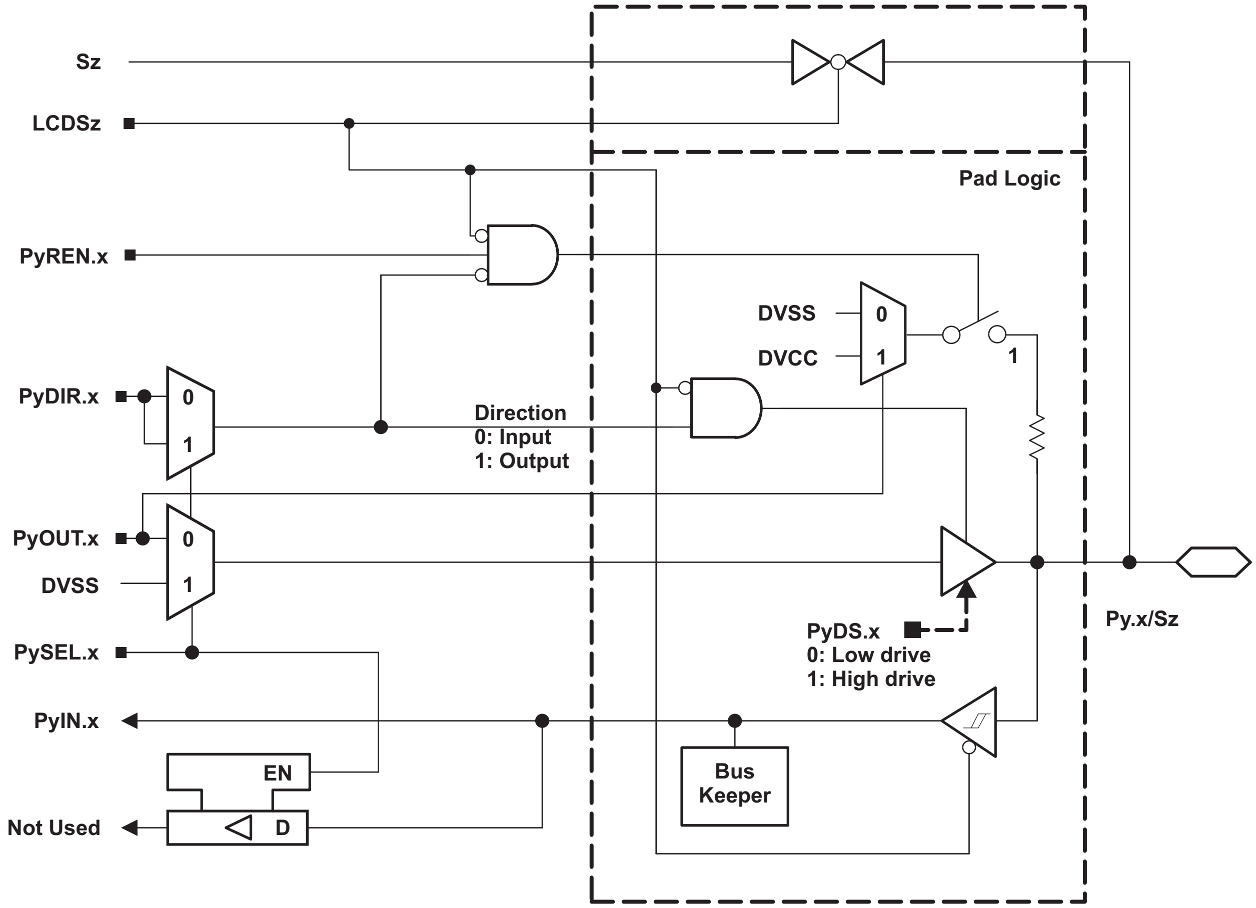


Table 71. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]		
			P4DIR.x	P4SEL.x	LCDS35...28
P4.0/S35	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S35	X	X	1
P4.1/S34	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S34	X	X	1
P4.2/S33	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S33	X	X	1
P4.3/S32	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S32	X	X	1
P4.4/S31	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S31	X	X	1
P4.5/S30	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S30	X	X	1
P4.6/S29	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S29	X	X	1
P4.7/S28	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S28	X	X	1

(1) X = Don't care

Table 72. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]		
			P5DIR.x	P5SEL.x	LCDS27...20
P5.0/S27	0	P5.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S27	X	X	1
P5.1/S26	1	P5.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S26	X	X	1
P5.2/S25	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S25	X	X	1
P5.3/S24	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S24	X	X	1
P5.4/S23	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S23	X	X	1
P5.5/S22	5	P5.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S22	X	X	1
P5.6/S21	6	P5.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S21	X	X	1
P5.7/S20	7	P5.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S20	X	X	1

(1) X = Don't care

Table 73. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)		
			P6DIR.x	P6SEL.x	LCDS19...12
P6.0/S19	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S19	X	X	1
P6.1/S18	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S18	X	X	1
P6.2/S17	2	P6.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S17	X	X	1
P6.3/S16	3	P6.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S16	X	X	1
P6.4/S15	4	P6.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S15	X	X	1
P6.5/S14	5	P6.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S14	X	X	1
P6.6/S13	6	P6.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S13	X	X	1
P6.7/S12	7	P6.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S12	X	X	1

(1) X = Don't care

Table 74. Port P7 (P7.0 to P7.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P7.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P7DIR.x	P7SEL.x	LCDS11...4
P7.0/S11	0	P7.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S11	X	X	1
P7.1/S10	1	P7.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S10	X	X	1
P7.2/S9	2	P7.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1
P7.3/S8	3	P7.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1
P7.4/S7	4	P7.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P7.5/S6	5	P7.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1
P7.6/S5	6	P7.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S5	X	X	1
P7.7/S4	7	P7.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S4	X	X	1

(1) X = Don't care

Table 75. Port P8 (P8.0 to P8.3) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P8DIR.x	P8SEL.x	LCDS3...0
P8.0/S3	0	P8.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S3	X	X	1
P8.1/S2	1	P8.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S2	X	X	1
P8.2/S1	2	P8.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S1	X	X	1
P8.3/S0	3	P8.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1

(1) X = Don't care

Port P8, P8.4 to P8.7, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

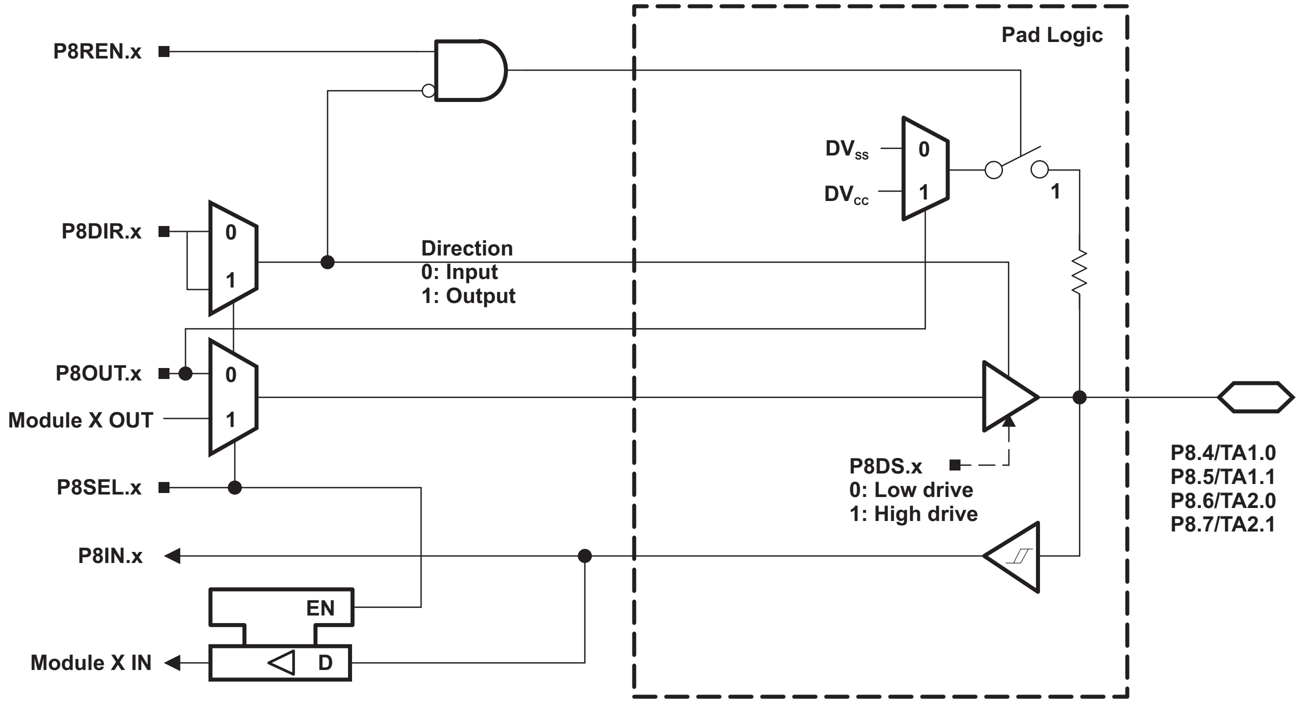


Table 76. Port P8 (P8.4 to P8.7) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P8.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P8DIR.x	P8SEL.x
P8.4/TA1.0	4	P8.4 (I/O)	I: 0; O: 1	0
		TA1.CCI0A	0	1
		TA1.TA0	1	1
P8.5/TA1.1	5	P8.5 (I/O)	I: 0; O: 1	0
		TA1.CCI1A	0	1
		TA1.TA1	1	1
P8.6/TA2.0	6	P8.6 (I/O)	I: 0; O: 1	0
		TA2.CCI0A	0	1
		TA2.TA0	1	1
P8.7/TA2.1	7	P8.7 (I/O)	I: 0; O: 1	0
		TA2.CCI1A	0	1
		TA2.TA1	1	1

Port P9, P9.0, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

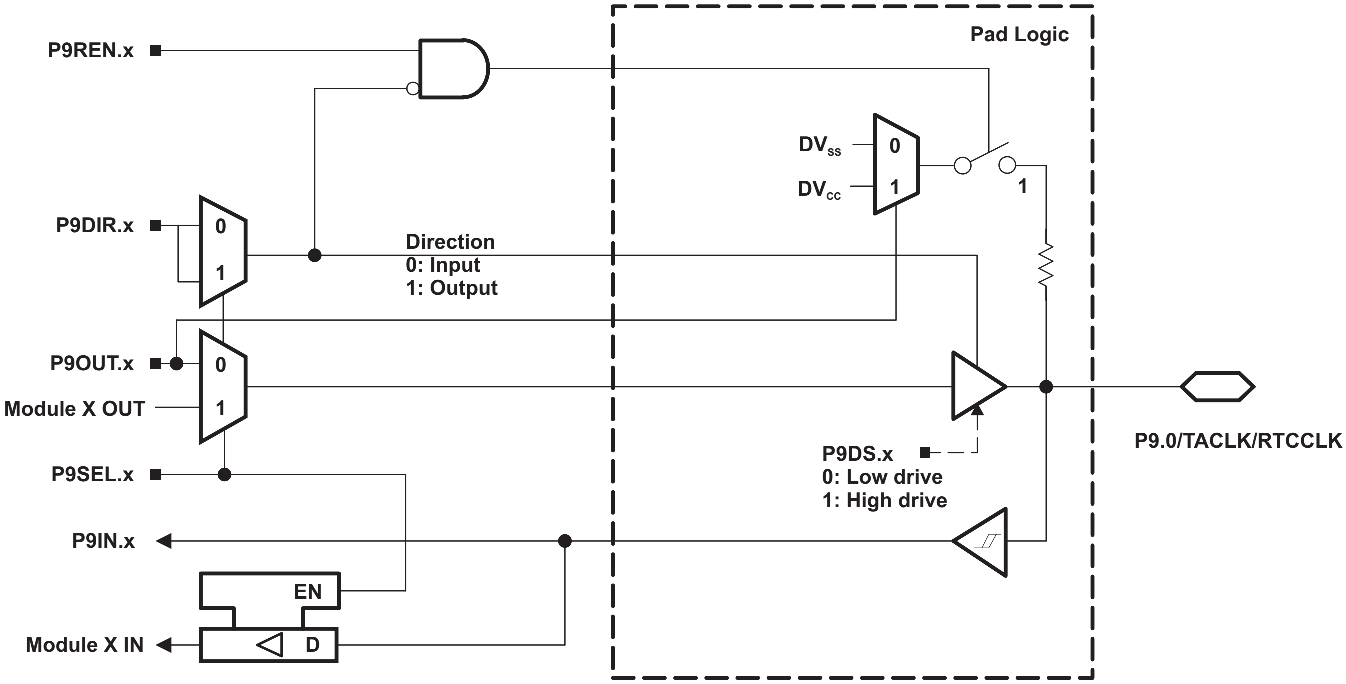


Table 77. Port P9 (P9.0) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS	
			P9DIR.x	P9SEL.x
P9.0/TACLK/RTCCLK	0	P9.0 (I/O)	I: 0; O: 1	0
		TACLK	0	1
		RTCCLK	1	1

Port P9, P9.1 to P9.3, Input/Output With Schmitt Trigger (MSP430F67xxIPZ Only)

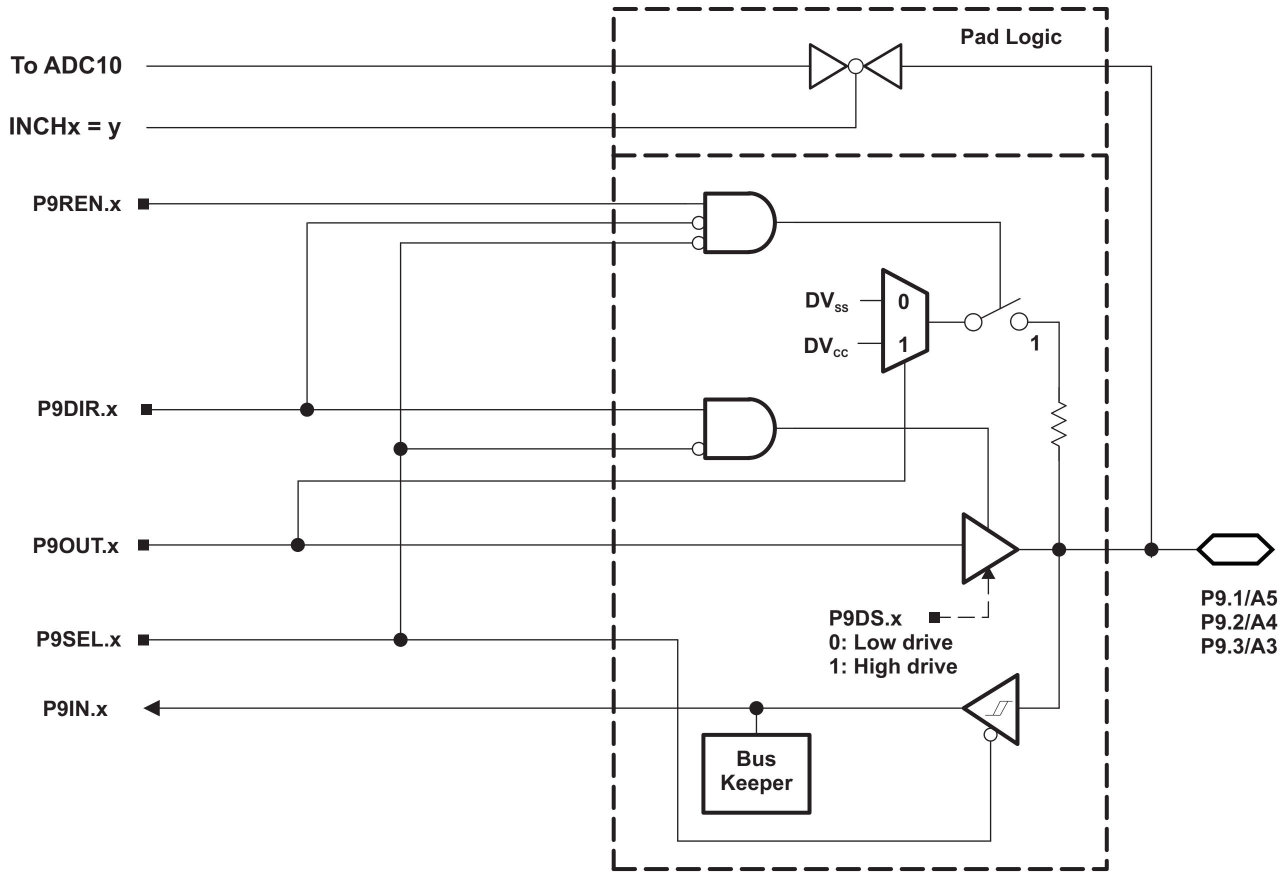


Table 78. Port P9 (P9.1 to P9.3) Pin Functions (MSP430F67xxIPZ Only)

PIN NAME (P9.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)	
			P9DIR.x	P9SEL.x
P9.1/A5	1	P9.1 (I/O)	I: 0; O: 1	0
		A5(2)	X	1
P9.2/A4	2	P9.2 (I/O)	I: 0; O: 1	0
		A4(2)	X	1
P9.3/A3	3	P9.3 (I/O)	I: 0; O: 1	0
		A3(2)	X	1

(1) X = Don't care
(2) Setting P9SEL.x bit disables the output driver as well as the input Schmitt trigger.

Port P2, P2.0 and P2.1, Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

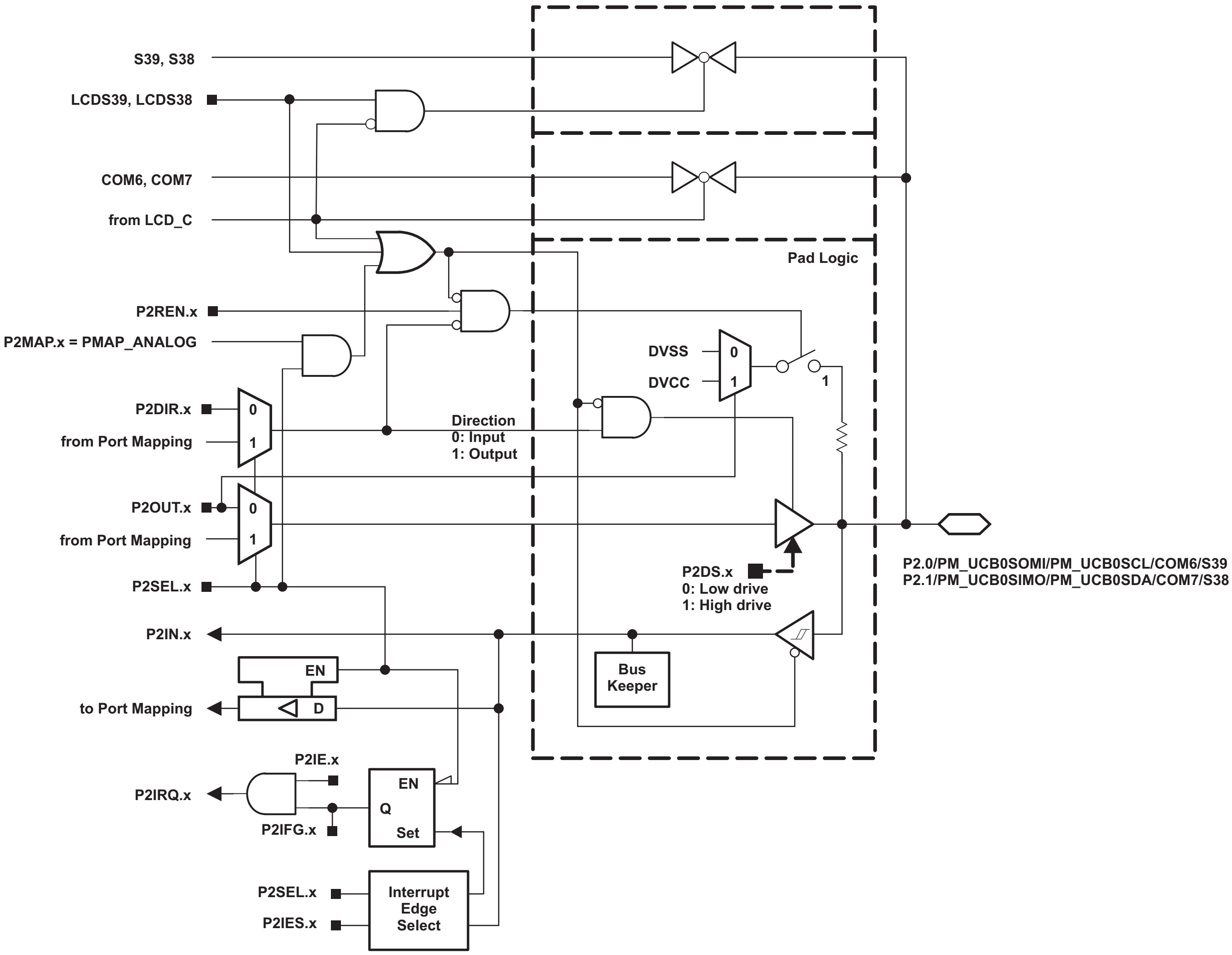


Table 79. Port P2 (P2.0 and P2.1) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS[(1)]				
			P2DIR.x	P2SEL.x	P2MAPx	LCDS39, LCDS38	COM6,7 Enable Signal
P2.0/PM_UCB0SOMI/PM_UCB0SCL/COM6/S39	0	P2.0 (I/O)	I: 0; O: 1	0	X	0	0
		UCB0SOMI/UCB0SCL	X	1	default	0	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0	0
		COM6	X	X	X	X	1
		S39	X	X	X	1	0
P2.1/PM_UCB0SIMO/PM_UCB0SDA/COM7/S38	1	P2.1 (I/O)	I: 0; O: 1	0	X	0	0
		UCB0SIMO/UCB0SDA	X	1	default	0	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0	0
		COM7	X	X	X	X	1
		S38	X	X	X	1	0

(1) X = Don't care

Port P2, P2.2 to P2.7 , Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

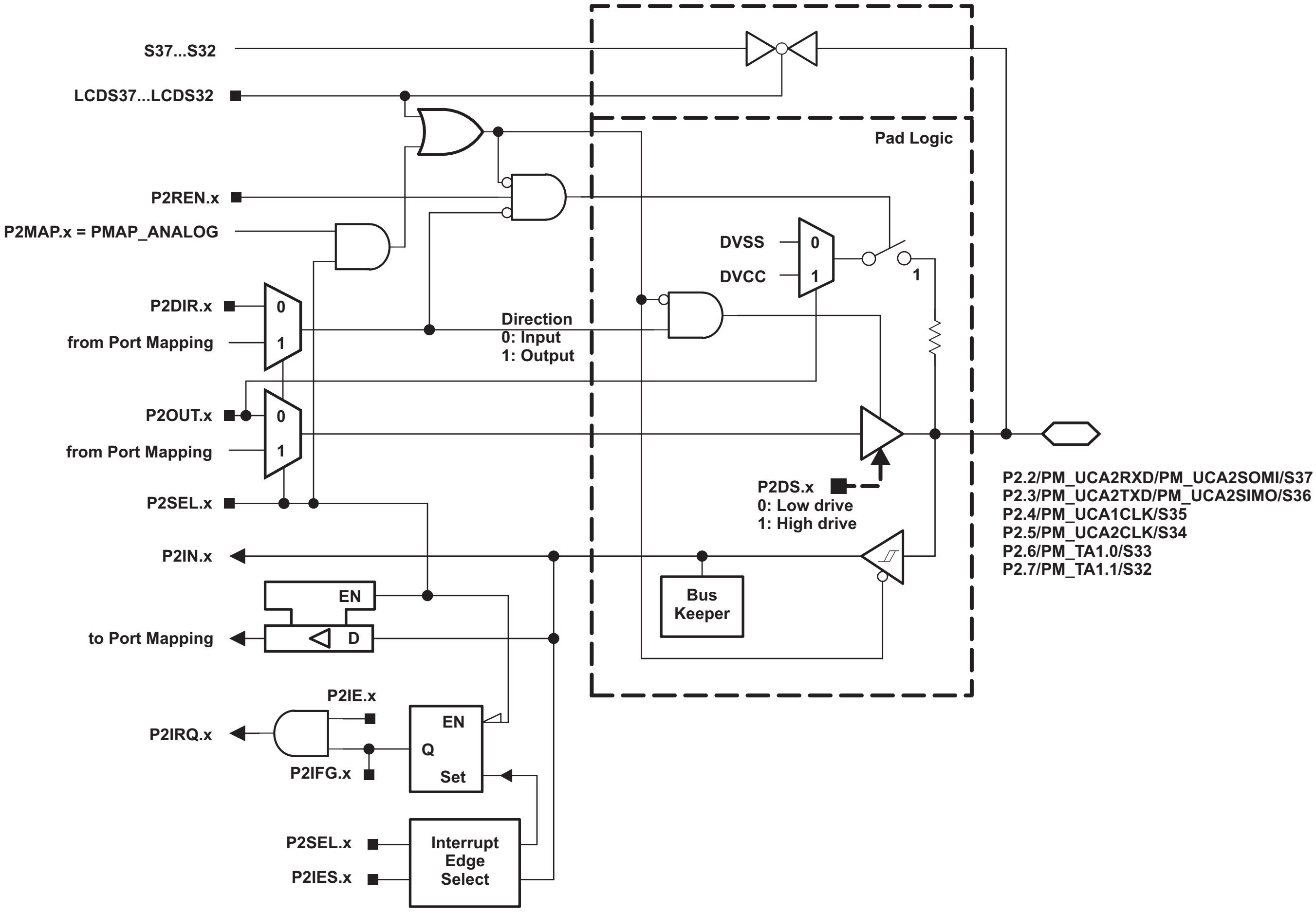


Table 80. Port P2 (P2.2 to P2.7) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P2DIR.x	P2SEL.x	P2MAPx	LCDS37...32
P2.2/PM_UCA2RXD/ PM_UCA2SOMI/S37	2	P2.2 (I/O)	I: 0; O: 1	0	X	0
		UCA2RXD/UCA2SOMI	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S37	X	X	X	1
P2.3/PM_UCA2TXD/ PM_UCA2SIMO/S36	3	P2.3 (I/O)	I: 0; O: 1	0	X	0
		UCA2TXD/UCA2SIMO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S36	X	X	X	1
P2.4/PM_UCA1CLK/S35	4	P2.4 (I/O)	I: 0; O: 1	0	X	0
		UCA1CLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S35	X	X	X	1
P2.5/PM_UCA2CLK/S34	5	P2.5 (I/O)	I: 0; O: 1	0	X	0
		UCA2CLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S34	X	X	X	1
P2.6/PM_TA1.0/S33	6	P2.6 (I/O)	I: 0; O: 1	0	X	0
		TA1.CCI0A	0	1	default	0
		TA1.TA0	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S33	X	X	X	1
P2.7/PM_TA1.1/S32	7	P2.7 (I/O)	I: 0; O: 1	0	X	0
		TA1.CCI1A	0	1	default	0
		TA1.TA1	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S32	X	X	X	1

(1) X = Don't care

Port P3, P3.0 to P3.7 , Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

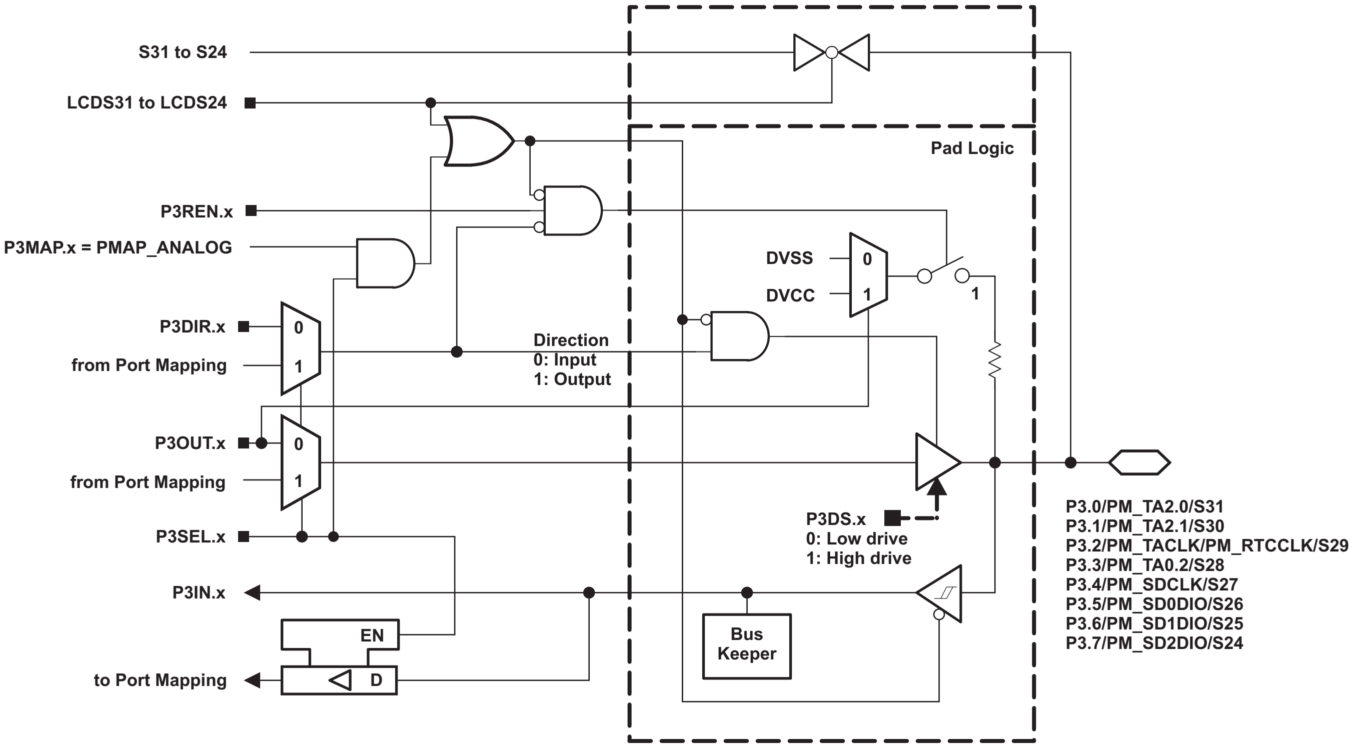


Table 81. Port P3 (P3.0 to P3.7) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P3.x)	x	FUNCTION	CONTROL BITS/SIGNALS (1)			
			P3DIR.x	P3SEL.x	P3MAPx	LCDS31...24
P3.0/PM_TA2.0/S31	0	P3.0 (I/O)	I: 0; O: 1	0	X	0
		TA2.CCI0A	0	1	default	0
		TA2.TA0	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S31	X	X	X	1
P3.1/PM_TA2.1/S30	1	P3.1 (I/O)	I: 0; O: 1	0	X	0
		TA2.CCI1A	0	1	default	0
		TA2.TA1	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S30	X	X	X	1
P3.2/PM_TACLK/ PM_RTCCLK/S29	2	P3.2 (I/O)	I: 0; O: 1	0	X	0
		TACLK	0	1	default	0
		RTCCLK	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S29	X	X	X	1
P3.3/PM_TA0.2/S28	3	P3.3 (I/O)	I: 0; O: 1	0	X	0
		TA0.CCI2A	0	1	default	0
		TA0.TA2	1	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S28	X	X	X	1
P3.4/PM_SDCLK/S27	4	P3.4 (I/O)	I: 0; O: 1	0	X	0
		SDCLK	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S27	X	X	X	1
P3.5/PM_SD0DIO/S26	5	P3.5 (I/O)	I: 0; O: 1	0	X	0
		SD0DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S26	X	X	X	1
P3.6/PM_SD1DIO/S25	6	P3.6 (I/O)	I: 0; O: 1	0	X	0
		SD1DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S25	X	X	X	1
P3.7/PM_SD2DIO/S24	7	P3.7 (I/O)	I: 0; O: 1	0	X	0
		SD2DIO	X	1	default	0
		Output driver and input Schmitt trigger disabled	X	1	= 31	0
		S24	X	X	X	1

(1) X = Don't care

Port P4, Port P5, Port P6, Input/Output With Schmitt Trigger (MSP430F67xxIPN Only)

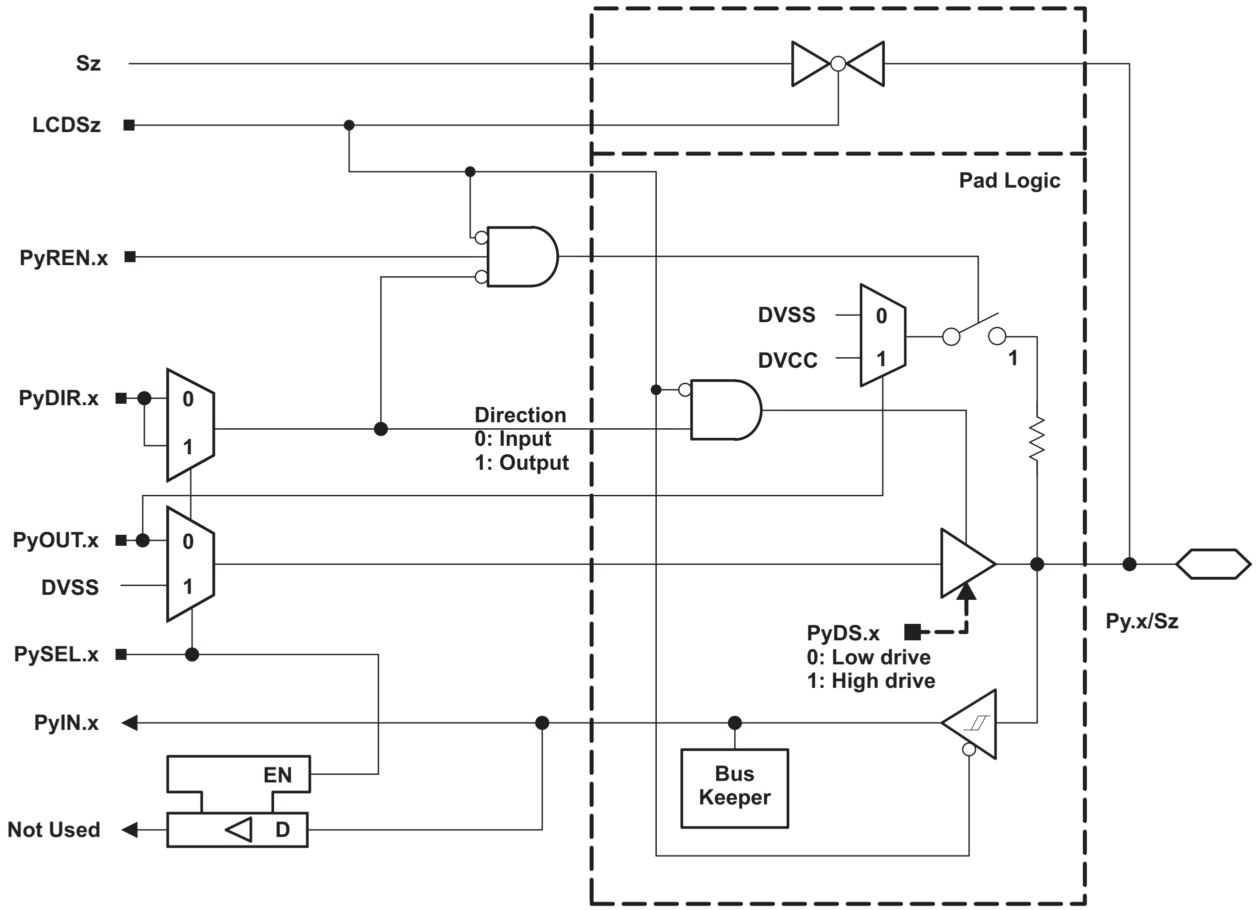


Table 82. Port P4 (P4.0 to P4.7) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P4.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P4DIR.x	P4SEL.x	LCDS23...16
P4.0/S23	0	P4.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S23	X	X	1
P4.1/S22	1	P4.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S22	X	X	1
P4.2/S21	2	P4.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S21	X	X	1
P4.3/S20	3	P4.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S20	X	X	1
P4.4/S19	4	P4.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S19	X	X	1
P4.5/S18	5	P4.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S18	X	X	1
P4.6/S17	6	P4.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S17	X	X	1
P4.7/S16	7	P4.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S16	X	X	1

(1) X = Don't care

Table 83. Port P5 (P5.0 to P5.7) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P5.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P5DIR.x	P5SEL.x	LCDS15...8
P5.0/S15	0	P5.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S15	X	X	1
P5.1/S14	1	P5.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S14	X	X	1
P5.2/S13	2	P5.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S13	X	X	1
P5.3/S12	3	P5.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S12	X	X	1
P5.4/S11	4	P5.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S11	X	X	1
P5.5/S10	5	P5.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S10	X	X	1
P5.6/S9	6	P5.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S9	X	X	1
P5.7/S8	7	P5.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S8	X	X	1

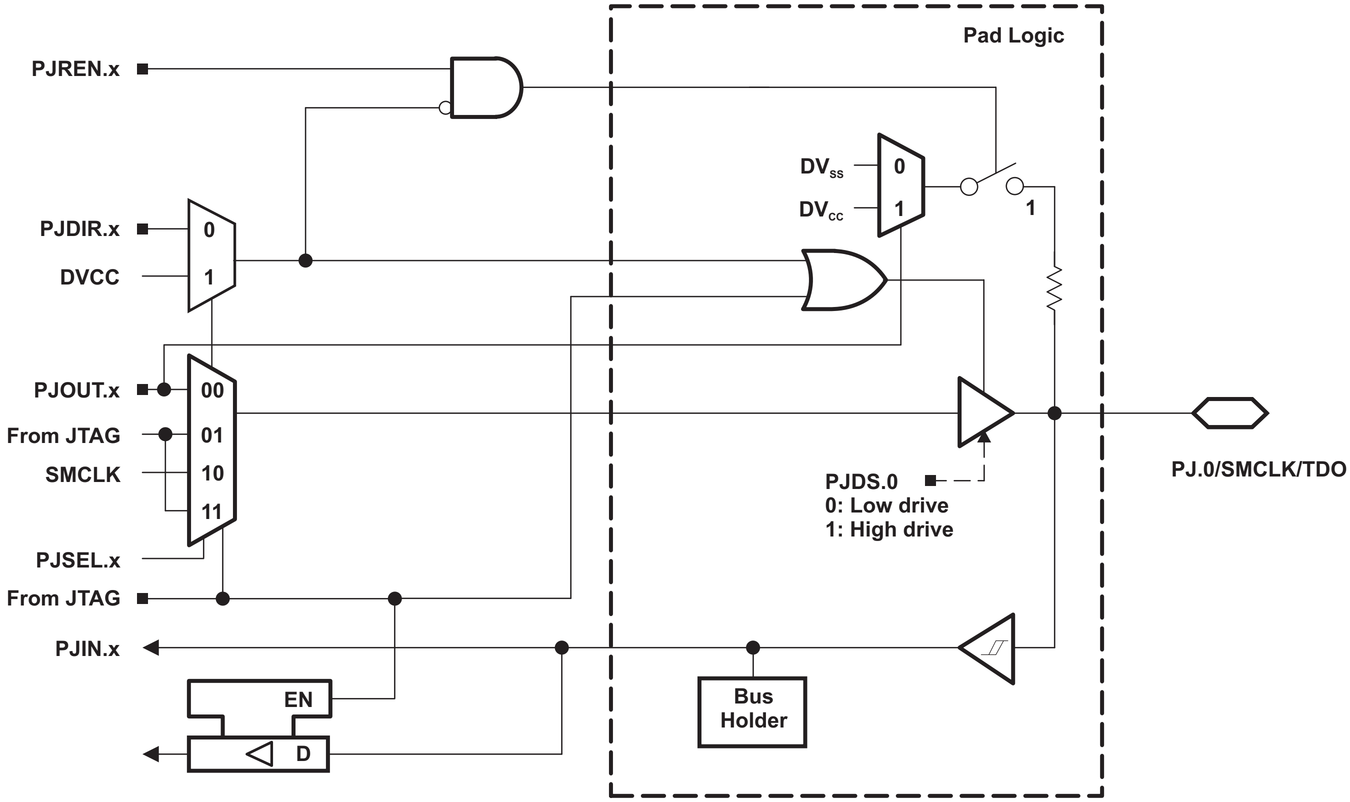
(1) X = Don't care

Table 84. Port P6 (P6.0 to P6.7) Pin Functions (MSP430F67xxIPN Only)

PIN NAME (P6.x)	x	FUNCTION	CONTROL BITS/SIGNALS(1)		
			P6DIR.x	P6SEL.x	LCDS7...0
P6.0/S7	0	P6.0 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S7	X	X	1
P6.1/S6	1	P6.1 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S6	X	X	1
P6.2/S5	2	P6.2 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S5	X	X	1
P6.3/S4	3	P6.3 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S4	X	X	1
P6.4/S3	4	P6.4 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S3	X	X	1
P6.5/S2	5	P6.5 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S2	X	X	1
P6.6/S1	6	P6.6 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S1	X	X	1
P6.7/S0	7	P6.7 (I/O)	I: 0; O: 1	0	0
		N/A	0	1	0
		DVSS	1	1	0
		S0	X	X	1

(1) X = Don't care

Port J, J.0, JTAG pin TDO, Input/Output With Schmitt Trigger or Output



Port J, J.1 to J.3, JTAG pins TMS, TCK, TDI/TCLK, Input/Output With Schmitt Trigger or Output

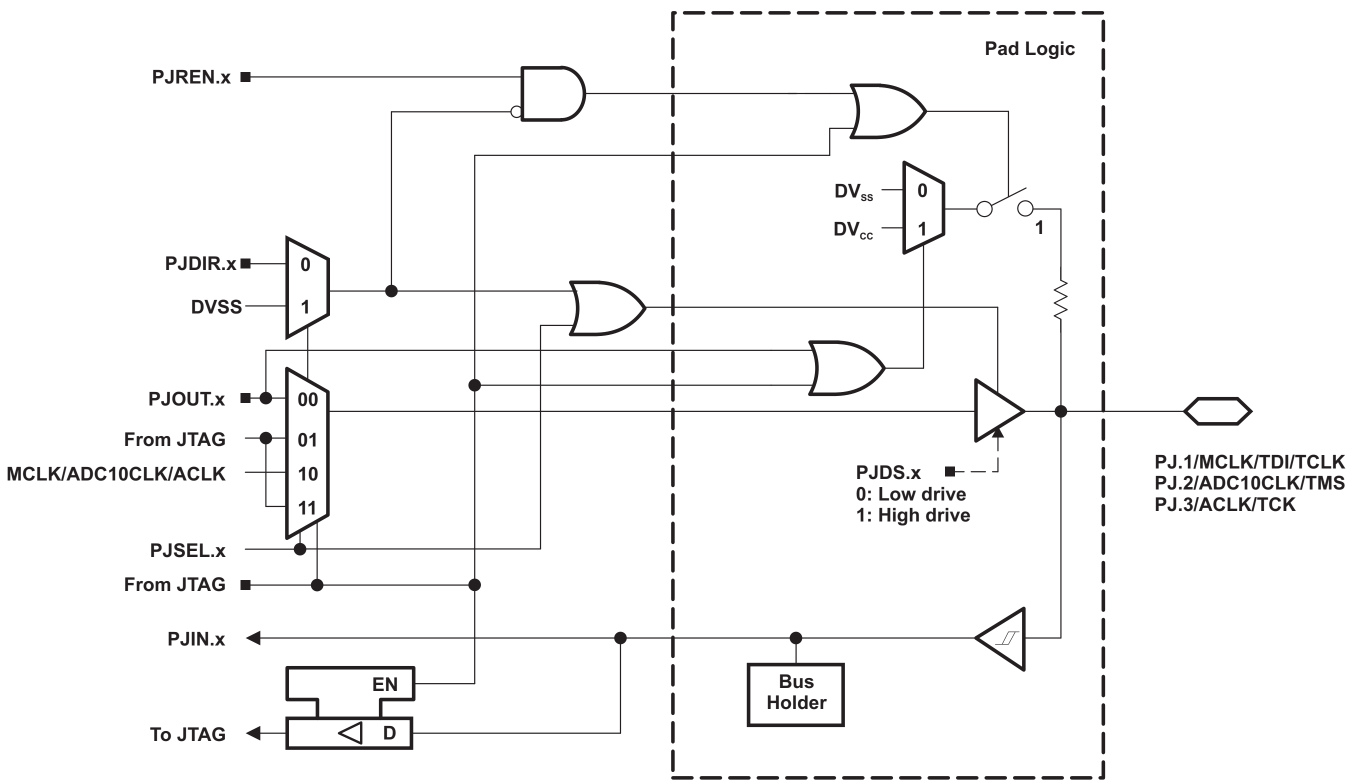


Table 85. Port PJ (PJ.0 to PJ.3) Pin Functions

PIN NAME (PJ.x)	x	FUNCTION	CONTROL BITS/ SIGNALS[(1)]		
			PJDIR.x	PJSEL.x	JTAG Mode Signal
PJ.0/SMCLK/TDO	0	PJ.0 (I/O)[(2)]	I: 0; O: 1	0	0
		SMCLK	1	1	0
		TDO[(3)]	X	X	1
PJ.1/MCLK/TDI/TCLK	1	PJ.1 (I/O)[(2)]	I: 0; O: 1	0	0
		MCLK	1	1	0
		TDI/TCLK [(3)(4)]	X	X	1
PJ.2/ADC10CLK/TMS	2	PJ.2 (I/O)[(2)]	I: 0; O: 1	0	0
		ADC10CLK	1	1	0
		TMS [(3)(4)]	X	X	1
PJ.3/ACLK/TCK	3	PJ.3 (I/O)[(2)]	I: 0; O: 1	0	0
		ACLK	1	1	0
		TCK [(3)(4)]	X	X	1

(1) X = Don't care
(2) Default condition
(3) The pin direction is controlled by the JTAG module.
(4) In JTAG mode, pullups are activated automatically on TMS, TCK, and TDI/TCLK. PJREN.x are don't care.

DEVICE DESCRIPTORS (TLV)

Table 86 and Table 87 list the complete contents of the device descriptor tag-length-value (TLV) structure for each device type.

Table 86. MSP430F673x Device Descriptor Table

	Description	Address	Size bytes	F6736PZ F6736PN	F6735PZ F6735PN	F6734PZ F6734PN	F6733PZ F6733PN	F6731PZ F6731PN	F6730PZ F6730PN
				Value	Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	6Ch	6Bh	6Ah	65h	63h	62h
	Device ID	01A05h	1	81h	81h	81h	80h	80h	80h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit
ADC10 Calibration	ADC10 Calibration Tag	01A14h	1	13h	13h	13h	13h	13h	13h
	ADC10 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit	per unit

Table 87. MSP430F672x Device Descriptor Table

	Description	Address	Size bytes	F6726PZ F6726PN	F6725PZ F6725PN	F6724PZ F6724PN	F6723PZ F6723PN	F6721PZ F6721PN	F6720PZ F6720PN
				Value	Value	Value	Value	Value	Value
Info Block	Info length	01A00h	1	06h	06h	06h	06h	06h	06h
	CRC length	01A01h	1	06h	06h	06h	06h	06h	06h
	CRC value	01A02h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Device ID	01A04h	1	6Fh	6Eh	6Dh	61h	59h	58h
	Device ID	01A05h	1	81h	81h	81h	80h	80h	80h
	Hardware revision	01A06h	1	per unit	per unit	per unit	per unit	per unit	per unit
	Firmware revision	01A07h	1	per unit	per unit	per unit	per unit	per unit	per unit
Die Record	Die Record Tag	01A08h	1	08h	08h	08h	08h	08h	08h
	Die Record length	01A09h	1	0Ah	0Ah	0Ah	0Ah	0Ah	0Ah
	Lot/Wafer ID	01A0Ah	4	per unit	per unit	per unit	per unit	per unit	per unit
	Die X position	01A0Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	Die Y position	01A10h	2	per unit	per unit	per unit	per unit	per unit	per unit
	Test results	01A12h	2	per unit	per unit	per unit	per unit	per unit	per unit
ADC10 Calibration	ADC10 Calibration Tag	01A14h	1	13h	13h	13h	13h	13h	13h
	ADC10 Calibration length	01A15h	1	10h	10h	10h	10h	10h	10h
	ADC Gain Factor	01A16h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC Offset	01A18h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 30°C	01A1Ah	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 1.5-V Reference Temp. Sensor 85°C	01A1Ch	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 30°C	01A1Eh	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.0-V Reference Temp. Sensor 85°C	01A20h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 30°C	01A22h	2	per unit	per unit	per unit	per unit	per unit	per unit
	ADC 2.5-V Reference Temp. Sensor 85°C	01A24h	2	per unit	per unit	per unit	per unit	per unit	per unit

REVISION HISTORY

REVISION	COMMENTS
SLAS731	Production Data release
SLAS731A	Changed the SYSRSTIV, System Reset Interrupt Event at offset 1Ch to Reserved in Table 16. Changed LPM3 current in Features. Changed limits for $I_{LPM0,1MHz}$, I_{LPM2}, and $I_{LPM3,XT1LF}$ in Low-Power Mode Supply Currents (Into V_{CC}) Excluding External Current. Changed limits for $I_{LPM3,LCD,int.\ bias}$ in Low-Power Mode With LCD Supply Currents (Into V_{CC}) Excluding External Current. Corrected values in "x" column in Table 70.
SLAS731B	Added "reverse byte" registers to Table 28. Added note to Recommended Operating Conditions regarding interaction between minimum VCC and SVSH.
SLAS731C	Recommended Operating Conditions, Added test conditions for typical characteristics. DCO Frequency, Added note (1). 10-Bit ADC, External Reference, Changed note (1): "12-bit accuracy" to "10-bit accuracy". Flash Memory, Changed I_{ERASE} and I_{MERASE} values.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F6720IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6720	Samples
MSP430F6720IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6720	Samples
MSP430F6720IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6720	Samples
MSP430F6720IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6720	Samples
MSP430F6721IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6721	Samples
MSP430F6721IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6721	Samples
MSP430F6721IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6721	Samples
MSP430F6721IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6721	Samples
MSP430F6723IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6723	Samples
MSP430F6723IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6723	Samples
MSP430F6723IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6723	Samples
MSP430F6723IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6723	Samples
MSP430F6724IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6724	Samples
MSP430F6724IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6724	Samples
MSP430F6724IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6724	Samples
MSP430F6724IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6724	Samples
MSP430F6725IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6725	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F6725IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6725	Samples
MSP430F6725IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6725	Samples
MSP430F6725IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6725	Samples
MSP430F6726IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6726	Samples
MSP430F6726IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6726	Samples
MSP430F6726IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6726	Samples
MSP430F6726IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6726	Samples
MSP430F6730IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6730	Samples
MSP430F6730IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6730	Samples
MSP430F6730IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6730	Samples
MSP430F6730IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6730	Samples
MSP430F6731IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6731	Samples
MSP430F6731IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6731	Samples
MSP430F6731IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6731	Samples
MSP430F6731IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6731	Samples
MSP430F6733IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6733	Samples
MSP430F6733IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6733	Samples
MSP430F6733IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6733	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
MSP430F6733IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6733	Samples
MSP430F6734IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6734	Samples
MSP430F6734IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6734	Samples
MSP430F6734IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6734	Samples
MSP430F6734IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6734	Samples
MSP430F6735IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6735	Samples
MSP430F6735IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6735	Samples
MSP430F6735IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6735	Samples
MSP430F6735IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6735	Samples
MSP430F6736IPN	ACTIVE	LQFP	PN	80	119	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6736	Samples
MSP430F6736IPNR	ACTIVE	LQFP	PN	80	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6736	Samples
MSP430F6736IPZ	ACTIVE	LQFP	PZ	100	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6736	Samples
MSP430F6736IPZR	ACTIVE	LQFP	PZ	100	1000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		F6736	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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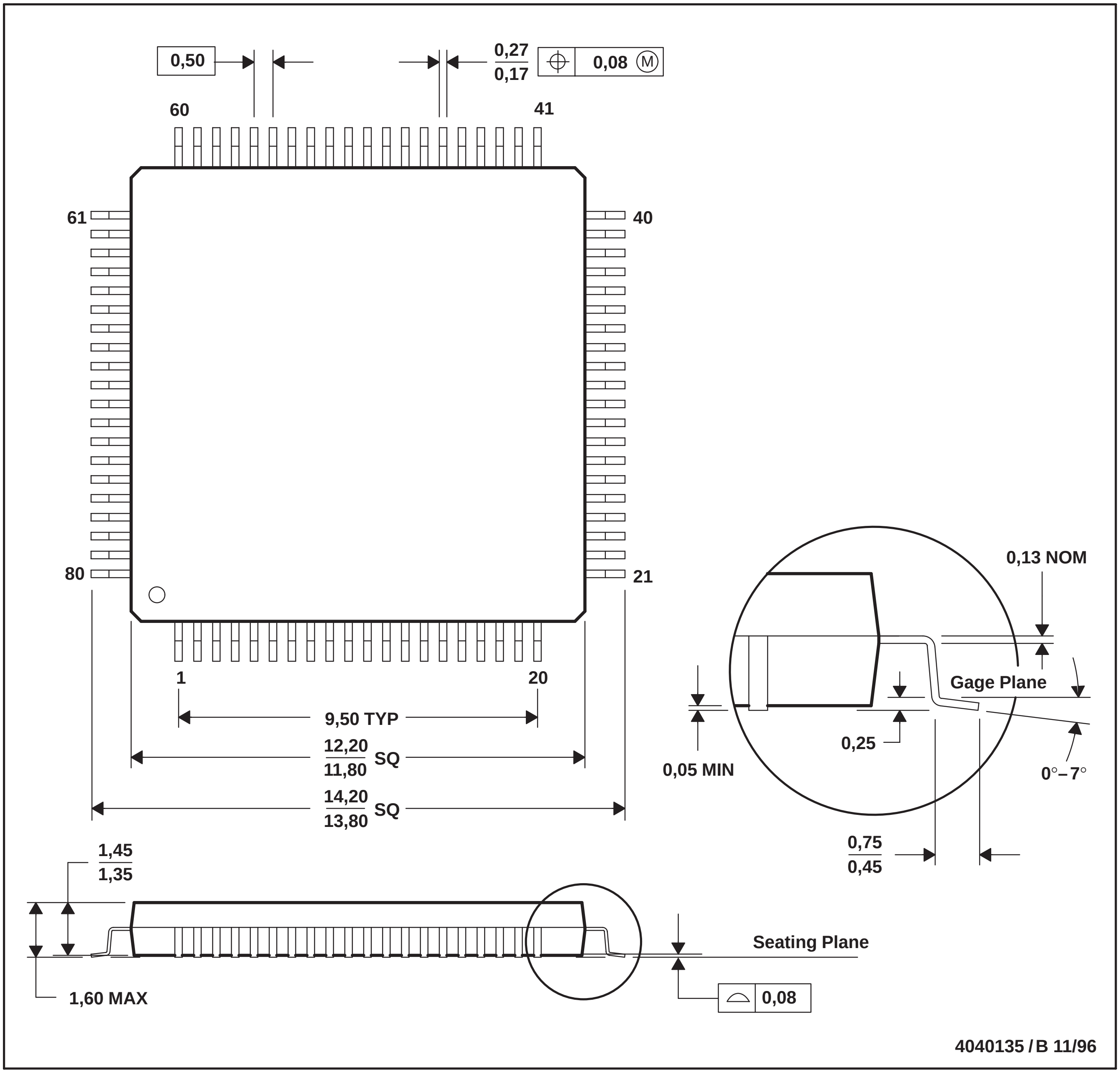
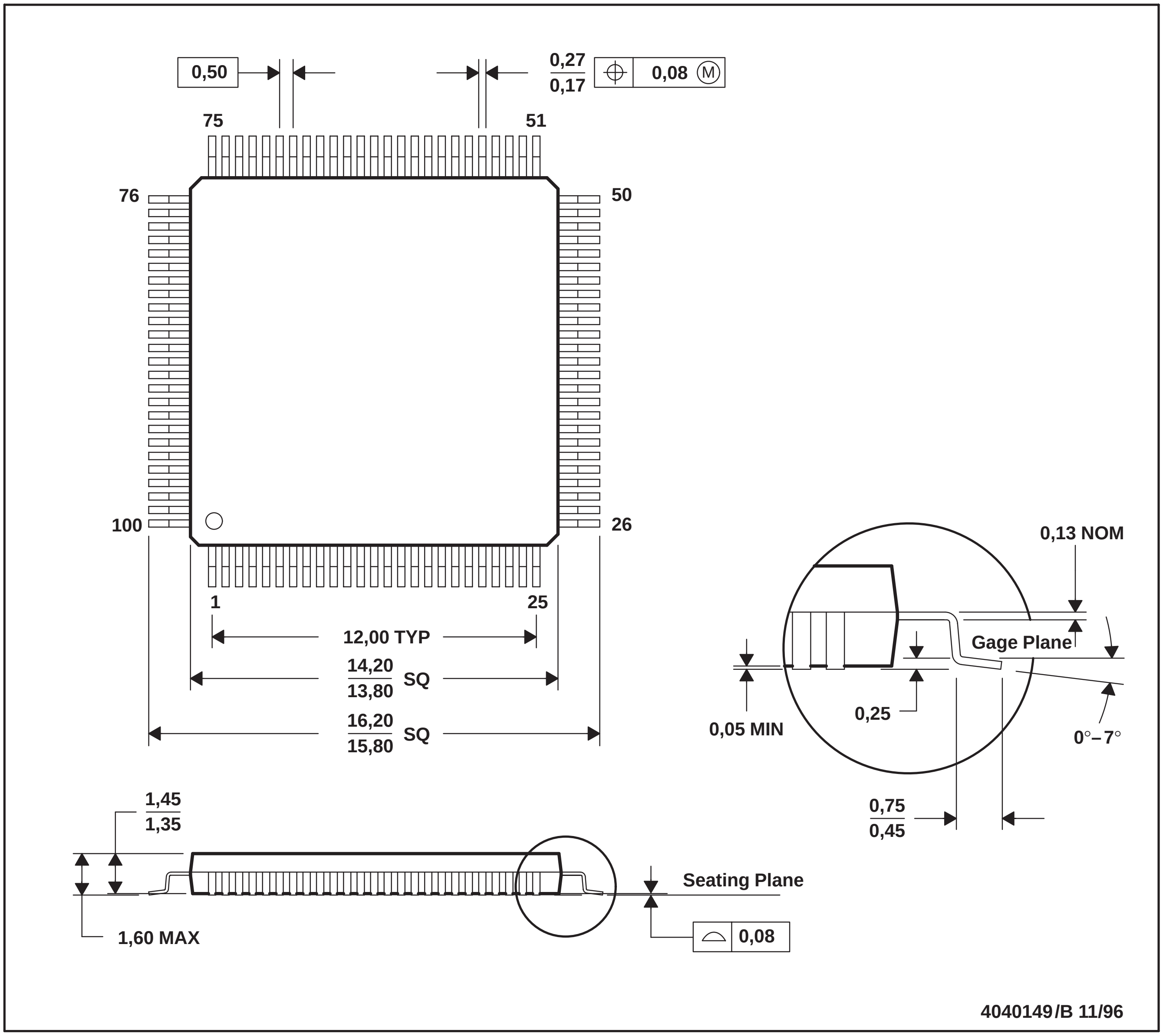
PN (S-PQFP-G80) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PZ (S-PQFP-G100) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026