Dual Linear Regulator with 300 mA and 150 mA Outputs and Power-On-Reset

Check for Samples: LP3996-Q1

FEATURES

- **2 LDO Outputs with Independent Enable**
- **1.5% Accuracy at Room Temperature, 3% Over Temperature**
- **Power-On-Reset Function with Adjustable Delay**
- **Thermal Shutdown Protection**
- **Stable with Ceramic Capacitors**
- **Qualified for Automotive Applications**
- **AEC-Q100 Test Guidance with the Following Results:**
  - **Device Temperature Grade 1: –40℃ to 125℃**
  - **Device HBM ESD Classification Level H2**
  - **Device CDM ESD Classification Level C4B**

APPLICATIONS

- **Cellular Handsets**
- **PDAs**
- **Wireless Network Adaptors**
- **Automotive**

DESCRIPTION

The LP3996-Q1 is a dual low dropout regulator with power-on-reset circuit. The first regulator can source 150 mA, while the second is capable of sourcing 300 mA and has a power-on-reset function included.

The LP3996-Q1 provides 1.5% accuracy requiring an ultra low quiescent current of 35 µA. Separate enable pins allow each output of the LP3996-Q1 to be shut down, drawing virtually zero current.

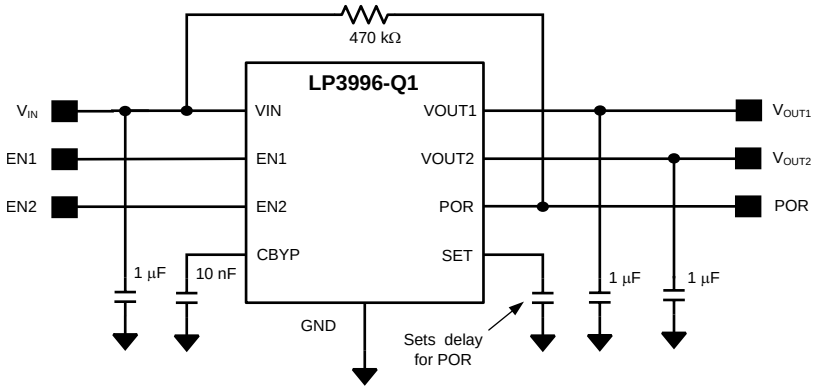
The device is designed to be stable with small footprint ceramic capacitors down to 1 µF. An external capacitor may be used to set the POR delay time as required.

The LP3996-Q1 is available in fixed output voltages and comes in a 10-pin, 3 mm x 3 mm package.

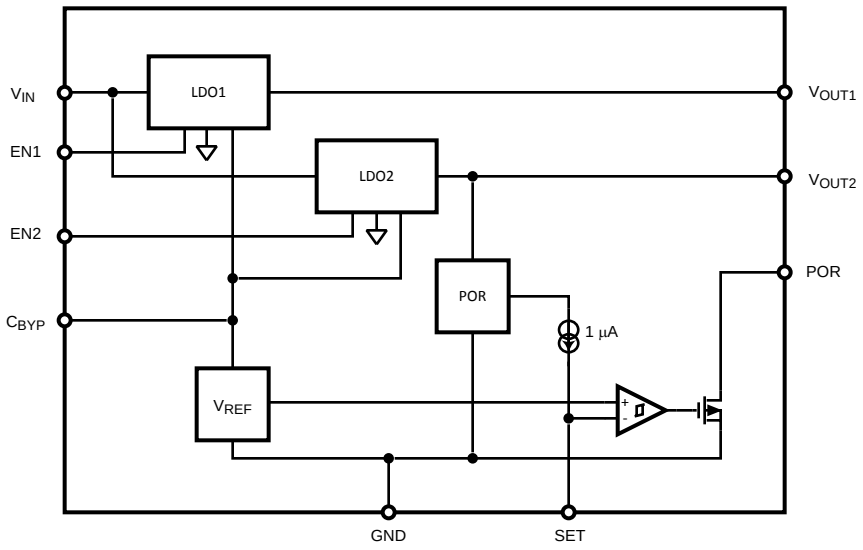
KEY SPECIFICATIONS

- **Input Voltage Range 2.0V to 6.0V**
- **Low Dropout Voltage 210 mV at 300 mA**
- **Ultra-Low I_Q (Enabled) 35 µA**
- **Virtually Zero I_Q (Disabled) <10 nA**
- **Package Available in Lead-Free Option 10-pin 3 mm x 3 mm**

Typical Application Circuit



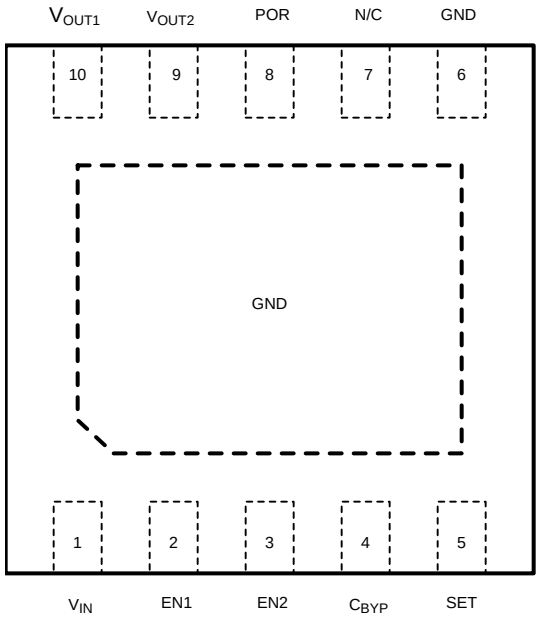
Functional Block Diagram



Pin Functions

Pin No	Symbol	Name and Function
1	VIN	Voltage Supply Input. Connect a 1 µF capacitor between this pin and GND.
2	EN1	Enable Input to Regulator 1. Active high input. High = On. Low = OFF.
3	EN2	Enable Input to Regulator 2. Active high input. High = On. Low = OFF.
4	CBYP	Internal Voltage Reference Bypass. Connect a 10 nF capacitor from this pin to GND to reduce output noise and improve line transient and PSRR. This pin may be left open.
5	SET	Set Delay Input. Connect a capacitor between this pin and GND to set the POR delay time. If left open, there will be no delay.
6	GND	Common Ground pin. Connect externally to exposed pad.
7	N/C	No Connection. Do not connect to any other pin.
8	POR	Power-On Reset Output. Open drain output. Active low indicates under-voltage output on Regulator 2. A pull-up resistor is required for correct operation.
9	VOUT2	Output of Regulator 2. 300 mA maximum current output. Connect a 1 µF capacitor between this pin and GND.
10	VOUT1	Output of Regulator 1. 150 mA maximum current output. Connect a 1 µF capacitor between this pin and GND.
Pad	GND	Common Ground. Connect to Pin 6.

Connection Diagram



Top View

Figure 1. WSON-10 Package
See Package Number DSC0010A

Table 1. Additional Device Information(1)

VOUT1/VOUT2 (V)	ORDER NUMBER	SUPPLIED AS
1.8/3.3	LP3996QSD-1833/NOPB	1000 Units, Tape-and-Reel
	LP3996QSDX-1833/NOPB	4500 Units, Tape-and-Reel

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS(1)(2)

Input Voltage to GND		–0.3V to 6.5V
VOUT1, VOUT2, EN1 and EN2 Voltage to GND		–0.3V to (V_{IN} + 0.3V) with 6.5V (max)
POR to GND		–0.3V to 6.5V
Junction Temperature (T_{J-MAX})		150℃
Lead/Pad Temp(3)		235℃
Storage Temperature		–65℃ to 150℃
Continuous Power Dissipation Internally Limited(4)		
ESD Rating(5)	Human Body Model	2.0kV
	Machine Model	200V

(1) All Voltages are with respect to the potential at the GND pin.
(2) Absolute Maximum Ratings are limits beyond which damage can occur. Recommended Operating Conditions are conditions under which operation of the device is ensured. Recommended Operating Conditions do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(3) For detailed soldering specifications and information, please refer to Texas Instruments Application Note AN-1187, Leadless Leadframe Package.
(4) Internal thermal shutdown circuitry protects the device from permanent damage.
(5) The human body model is 100 pF discharged through a 1.5 kΩ resistor into each pin. The machine model is a 200 pF capacitor discharged directly into each pin.

RECOMMENDED OPERATING CONDITIONS(1)(2)

Input Voltage	2.0V to 6.0V
EN1, EN2, POR Voltage	0 to (V_{IN} + 0.3V) to 6.0V (max)
Junction Temperature	–40℃ to 125℃
Ambient Temperature T_A Range(3)	–40℃ to 85℃

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Recommended Operating Conditions are conditions under which operation of the device is ensured. Recommended Operating Conditions do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) All Voltages are with respect to the potential at the GND pin.
(3) The maximum ambient temperature ($T_{A(max)}$) is dependant on the maximum operating junction temperature ($T_{J(max-op)}$ = 125℃), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A(max)} = T_{J(max-op)} - (\theta_{JA} \times P_{D(max)})$.

THERMAL PROPERTIES(1)

Junction-To-Ambient Thermal Resistance(2)	
θ_{JA} WSON-10 Package	55℃/W

(1) Absolute Maximum Ratings are limits beyond which damage can occur. Recommended Operating Conditions are conditions under which operation of the device is ensured. Recommended Operating Conditions do not imply ensured performance limits. For ensured performance limits and associated test conditions, see the Electrical Characteristics tables.
(2) Junction-to-ambient thermal resistance is dependant on the application and board layout. In applications where high maximum power dissipation is possible; special care must be paid to thermal dissipation issues in board design.

ELECTRICAL CHARACTERISTICS[1][2]

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT1} = C_{OUT2} = 1.0 µF.
Typical values and limits appearing in normal type apply for T_A = 25℃. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125℃.

SYMBOL	PARAMETER	CONDITIONS		TYP	LIMIT		UNITS
					MIN	MAX	
V_{IN}	Input Voltage	See[3]			2	6	V
ΔV_{OUT}	Output Voltage Tolerance	I_{OUT} = 1mA	1.5V < V_{OUT} ≤ 3.3V		–2.5 **–3.75**	+2.5 **+3.75**	%
			V_{OUT} ≤ 1.5V		–2.75 **–4**	+2.75 **+4**	
	Line Regulation Error	V_{IN} = ($V_{OUT(NOM)}$ + 1.0V) to 6.0V		0.03		**0.3**	%/V
	Load Regulation Error	I_{OUT} = 1 mA to 150 mA (LDO 1)		85		**155**	µV/mA
		I_{OUT} = 1 mA to 300 mA (LDO 2)		26		**85**	
V_{DO}	Dropout Voltage[4]	I_{OUT} = 1 mA to 150 mA (LDO 1)		110		**220**	mV
		I_{OUT} = 1 mA to 300 mA (LDO 2)		210		**550**	
I_Q	Quiescent Current	LDO 1 ON, LDO 2 ON I_{OUT1}= I_{OUT2} = 0 mA		35		**100**	µA
		LDO 1 ON, LDO 2 OFF I_{OUT1} = 150 mA		45		**110**	
		LDO 1 OFF, LDO 2 ON I_{OUT2} = 300 mA		45		**110**	
		LDO 1 ON, LDO 2 ON I_{OUT1} = 150 mA, I_{OUT2} = 300 mA		70		**170**	
		V_{EN1} = V_{EN2} = 0.4V		0.5		**10**	nA

(1) All Voltages are with respect to the potential at the GND pin.
(2) Min and Max limits are specified by design, test or statistical analysis. Typical numbers are not ensured, but do represent the most likely norm.
(3) $V_{IN(MIN)}$ = $V_{OUT(NOM)}$ +0.5V, or 2.0V, whichever is higher.
(4) Dropout voltage is voltage difference between input and output at which the output voltage drops to 100 mV below its nominal value. This parameter only for output voltages above 2.0V

ELECTRICAL CHARACTERISTICS[1][2] (continued)

Unless otherwise noted, V_{EN} = 950 mV, V_{IN} = V_{OUT} + 1.0V, or 2.0V, whichever is higher, where V_{OUT} is the higher of V_{OUT1} and V_{OUT2}. C_{IN} = 1 µF, I_{OUT} = 1 mA, C_{OUT1} = C_{OUT2} = 1.0 µF.
Typical values and limits appearing in normal type apply for T_A = 25℃. Limits appearing in **boldface** type apply over the full junction temperature range for operation, −40 to +125℃.

SYMBOL	PARAMETER	CONDITIONS		TYP	LIMIT		UNITS
					MIN	MAX	
I_{SC}	Short Circuit Current Limit	LDO 1		420		**750**	mA
		LDO 2		550		**840**	
I_{OUT}	Maximum Output Current	LDO 1			**150**		mA
		LDO 2			**300**		
PSRR	Power Supply Rejection Ratio[5]	f = 1kHz, I_{OUT} = 1mA to 150 mA C_{BYP} = 10 nF	LDO1	58			dB
			LDO2	70			
		f = 20 kHz, I_{OUT} = 1mA to 150 mA C_{BYP} = 10 nF	LDO1	45			
			LDO2	60			
e_n	Output noise Voltage[5]	BW = 10 Hz to 100kHz C_{BYP} = 10 nF	V_{OUT} = 0.8V	36			μV_{RMS}
			V_{OUT} = 3.3V	75			
$T_{SHUTDOWN}$	Thermal Shutdown	Temperature		160			℃
		Hysteresis		20			
Enable Control Characteristics							
I_{EN}	Input Current at V_{EN1} or V_{EN2}	V_{EN} = 0.0V		0.005		**0.1**	µA
		V_{EN} = 6V		2		**5**	
V_{IL}	Low Input Threshold at V_{EN1} or V_{EN2}					**0.4**	V
V_{IH}	High Input Threshold at V_{EN1} or V_{EN2}				**0.95**		V
POR Output Characteristics							
V_{TH}	Low Threshold % 0f $V_{OUT2\ (NOM)}$	Flag ON			88		%
	High Threshold % 0f $V_{OUT2\ (NOM)}$	Flag OFF				96	
I_{POR}	Leakage Current	Flag OFF, V_{POR} = 6.5V		30			nA
V_{OL}	Flag Output Low Voltage	I_{SINK} = 250 µA		20			mV
Timing Characteristics							
T_{ON}	Turn On Time[5]	To 95% Level C_{BYP} = 10 nF		300			µs
Transient Response	Line Transient Response $\lvert\delta V_{OUT}\rvert$[5]	T_{rise} = T_{fall} = 10 µs δV_{IN} = 1VC_{BYP} = 10 nF		20			mV (pk - pk)
	Load Transient Response $\lvert\delta V_{OUT}\rvert$[5]	T_{rise} = T_{fall} = 1 µs	LDO 1 I_{OUT} = 1 mA to 150 mA	175			
			LDO 2 I_{OUT} = 1 mA to 300 mA	150			
SET Input Characteristics							
I_{SET}	SET Pin Current Source	V_{SET} = 0V		1.3			µA
$V_{TH(SET)}$	SET Pin Threshold Voltage	POR = High		1.25			V

(5) This electrical specification is specified by design.

OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

SYMBOL	PARAMETER	CONDITIONS	NOM	LIMIT		UNITS
				MIN	MAX	
C_{OUT}	Output Capacitance	Capacitance(1)	1.0	**0.7**		µF
		ESR		5	500	mΩ

(1) The Capacitor tolerance should be 30% or better over temperature. The full operating conditions for the application should be considered when selecting a suitable capacitor to ensure that the minimum value of capacitance is always met. Recommended capacitor is X7R. However, depending on the application, X5R, Y5V and Z5U can also be used. (See Capacitor sections in APPLICATION HINTS.)

Transient Test Conditions

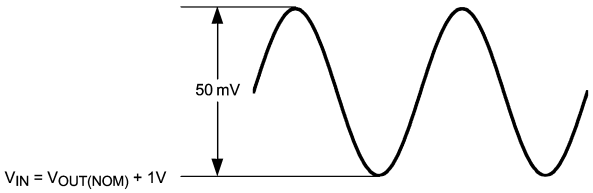


Figure 2. PSRR Input Signal

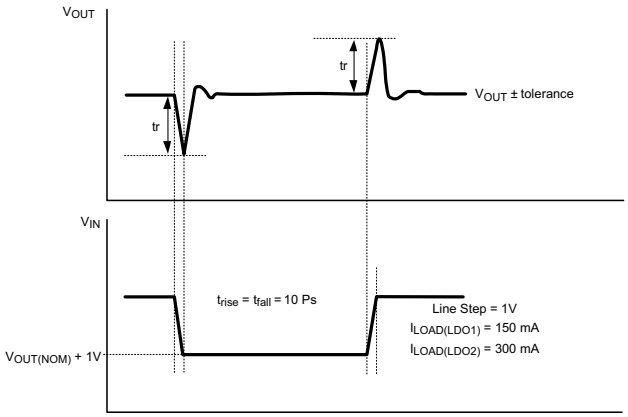


Figure 3. Line Transient Input Test Signal

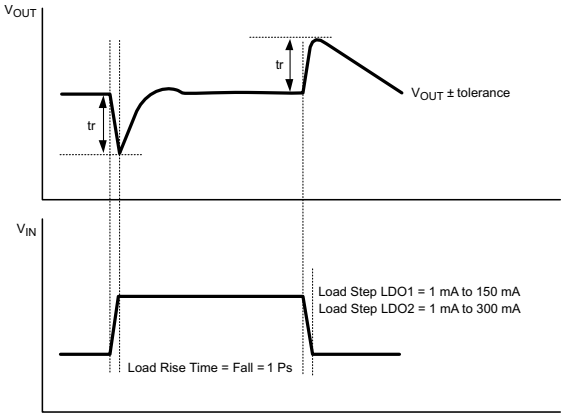


Figure 4. Load Transient Input Signal

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise specified, C_{IN} = 1.0 µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0 µF Ceramic, C_{BYP} = 10 nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25℃, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}. Typical Performance Characteristics are identical to the commercial grade product and are reproduced here as information only.

Output Voltage Change vs Temperature

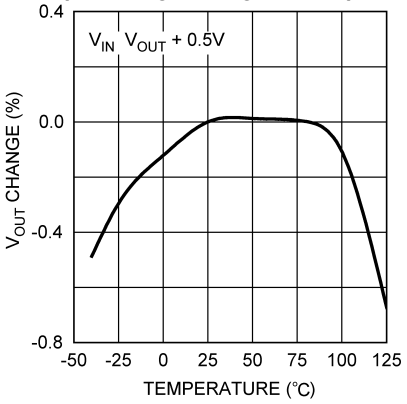


Figure 5.

Ground Current vs Load Current, LDO1

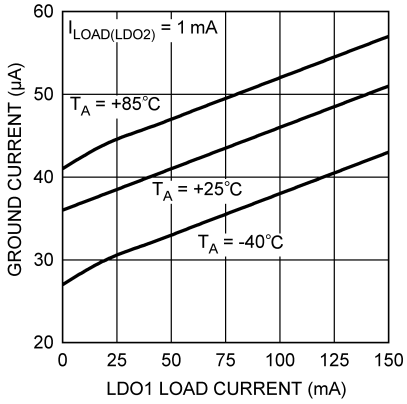


Figure 6.

Ground Current vs Load Current, LDO2

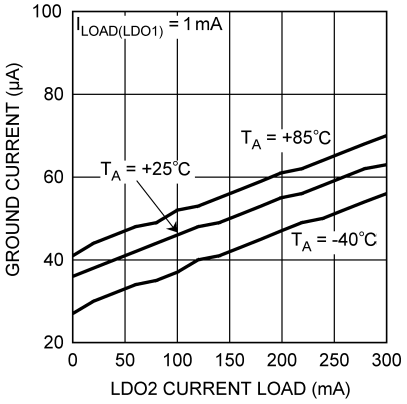


Figure 7.

Ground Current vs V_{IN}. I_{LOAD} = 1mA

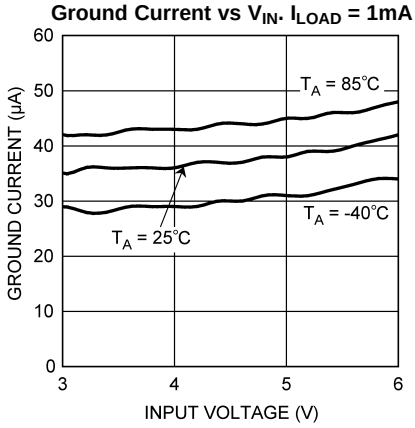


Figure 8.

Dropout Voltage vs I_{LOAD}, LDO1

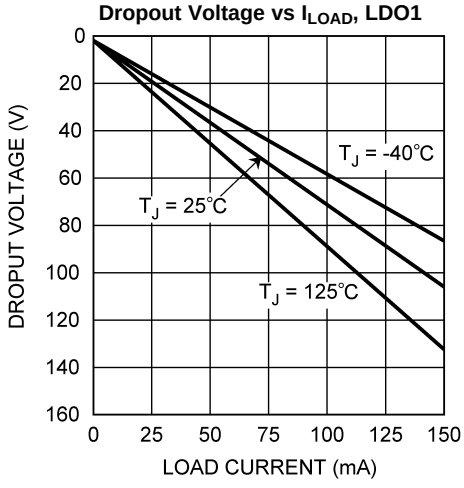


Figure 9.

Dropout Voltage vs I_{LOAD}, LDO2

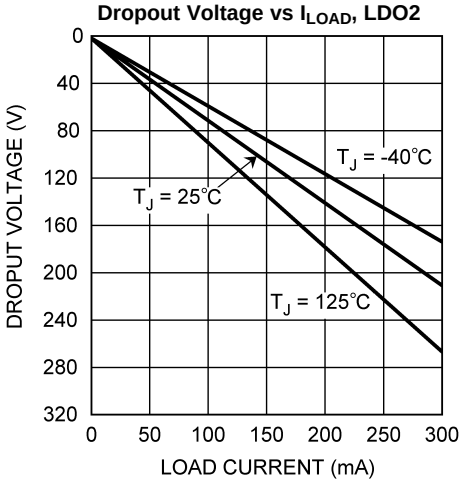


Figure 10.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, C_{IN} = 1.0 µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0 µF Ceramic, C_{BYP} = 10 nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25℃, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}. Typical Performance Characteristics are identical to the commercial grade product and are reproduced here as information only.

Short Circuit Current, LDO1

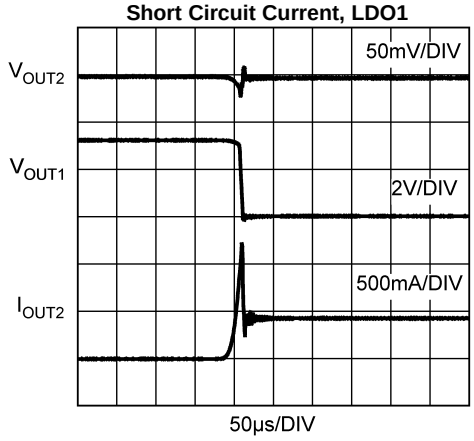


Figure 11.

Short Circuit Current, LDO2

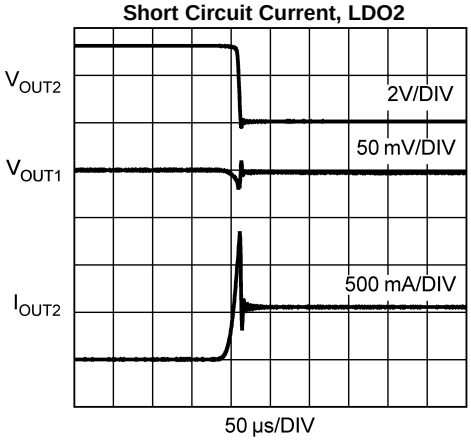


Figure 12.

Power Supply Rejection Ratio, LDO1

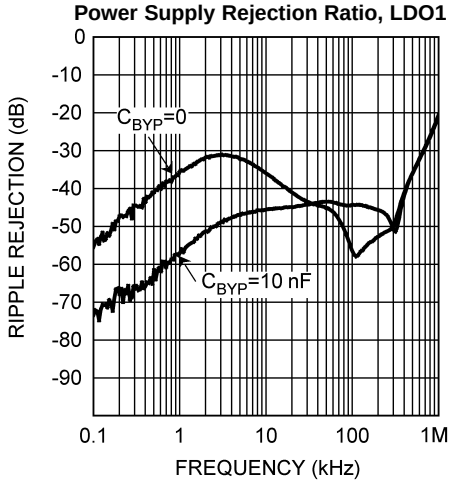


Figure 13.

Power Supply Rejection Ratio, LDO2

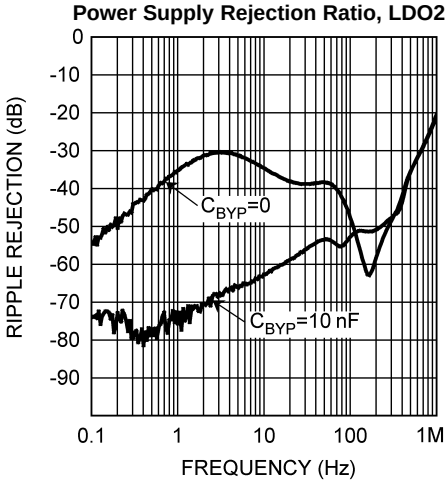


Figure 14.

Enable Start-up Time, C_{BYP}=0

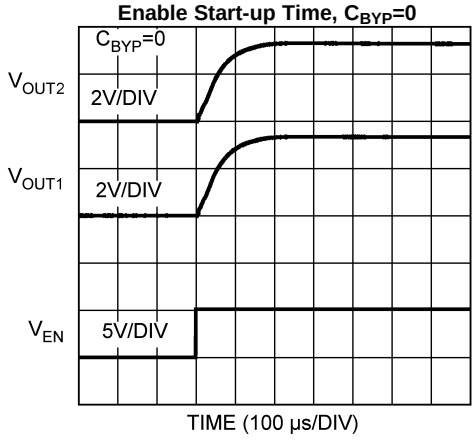


Figure 15.

Enable Start-up Time, C_{BYP}=10nF

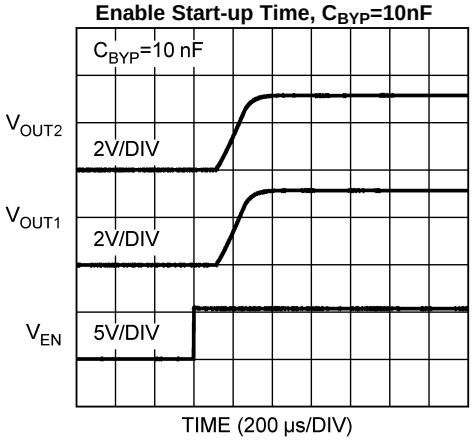


Figure 16.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, C_{IN} = 1.0 µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0 µF Ceramic, C_{BYP} = 10 nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25℃, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}. Typical Performance Characteristics are identical to the commercial grade product and are reproduced here as information only.

Line Transient, C_{BYP}=10nF

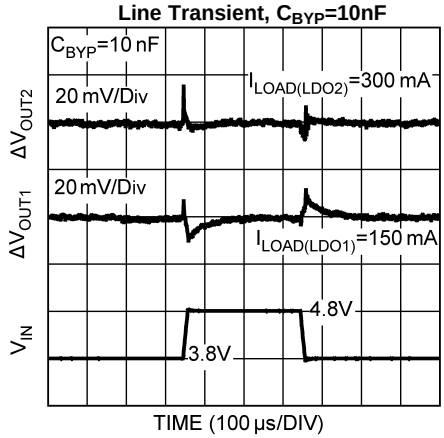


Figure 17.

Line Transient, C_{BYP}=0

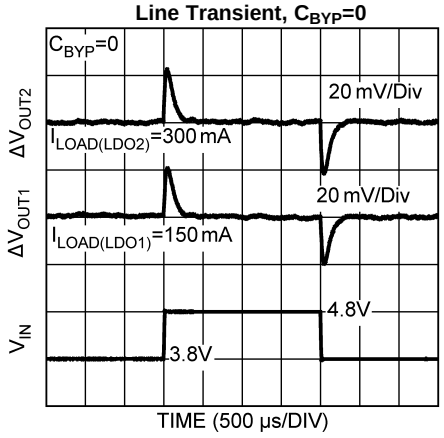


Figure 18.

Load Transient, LDO1

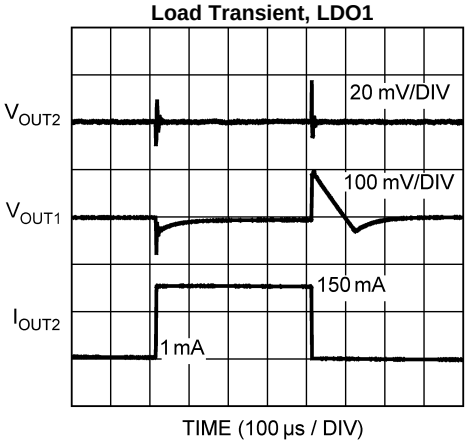


Figure 19.

Load Transient, LDO2

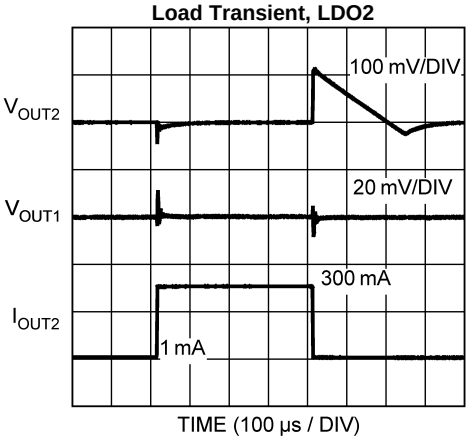


Figure 20.

Noise Density LDO1

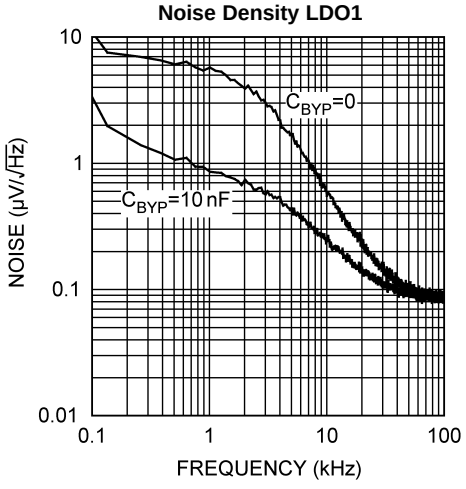


Figure 21.

Noise Density, LDO2

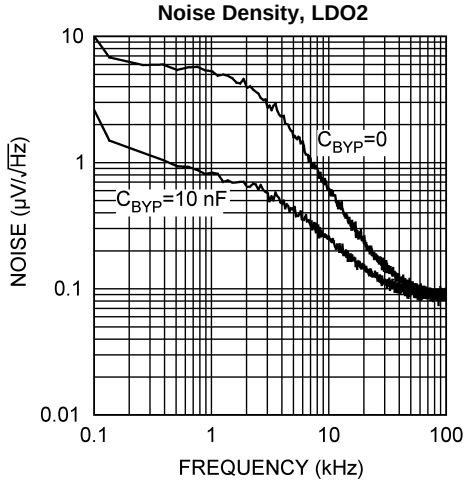


Figure 22.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Unless otherwise specified, C_{IN} = 1.0 µF Ceramic, C_{OUT1} = C_{OUT2} = 1.0 µF Ceramic, C_{BYP} = 10 nF, V_{IN} = $V_{OUT2(NOM)}$ + 1.0V, T_A = 25℃, $V_{OUT1(NOM)}$ = 3.3V, $V_{OUT2(NOM)}$ = 3.3V, Enable pins are tied to V_{IN}. Typical Performance Characteristics are identical to the commercial grade product and are reproduced here as information only.

Power-on-Reset Start-up Operation

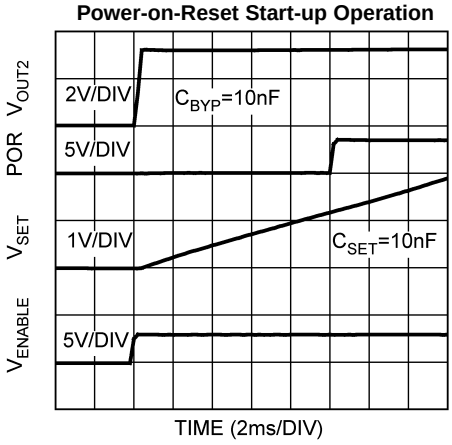


Figure 23.

Power-on-Reset Shutdown Operation

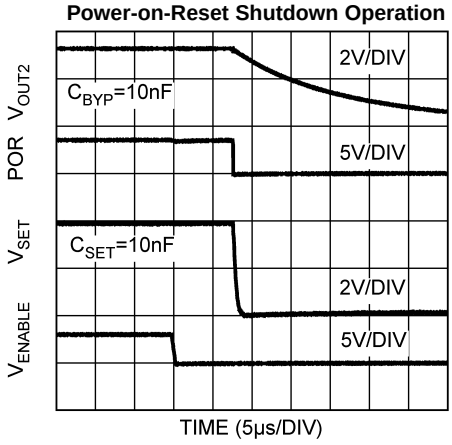


Figure 24.

POR Delay Time

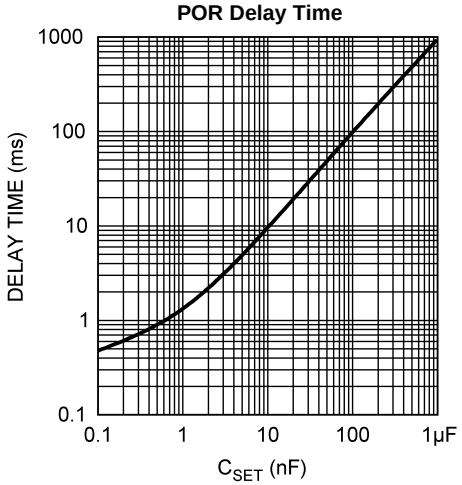


Figure 25.

APPLICATION HINTS

Operation Description

The LP3996-Q1 is a low quiescent current, power management IC, designed specifically for portable applications requiring minimum board space and smallest components. The LP3996-Q1 contains two independently selectable LDOs. The first is capable of sourcing 150 mA at factory-programmed outputs between 0.8V and 3.3V. The second can source 300 mA at factory-programmed output voltages of 0.8V to 3.3V. In addition, LDO2 contains a power-good flag circuit which monitors the output voltage and indicates when it is within 8% of its nominal value. The flag will also act as a power-on-reset signal and, by adding an external capacitor, a delay may be programmed for the POR output.

Input Capacitor

An input capacitor is required for stability. It is recommended that a 1.0 µF capacitor be connected between the LP3996-Q1 input pin and ground (this capacitance value may be increased without limit).

This capacitor must be located a distance of not more than 1 cm from the input pin and returned to a clean analog ground. Any good quality ceramic, tantalum, or film capacitor may be used at the input.

Important: Tantalum capacitors can suffer catastrophic failures due to surge current when connected to a low-impedance source of power (like a battery or a very large capacitor). If a tantalum capacitor is used at the input, it must be ensured by the manufacturer to have a surge current rating sufficient for the application.

There are no requirements for the ESR (Equivalent Series Resistance) on the input capacitor, but tolerance and temperature coefficient must be considered when selecting the capacitor to ensure the capacitance will remain approximately 1.0 µF over the entire operating temperature range.

Output Capacitor

The LP3996-Q1 is designed specifically to work with very small ceramic output capacitors. A 1.0 µF ceramic capacitor (temperature types Z5U, Y5V or X7R) with ESR between 5 mΩ to 500 mΩ, is suitable in the LP3996-Q1 application circuit.

For this device the output capacitor should be connected between the VOUT pin and ground.

It is also possible to use tantalum or film capacitors at the device output, C_{OUT} (or V_{OUT}), but these are not as attractive for reasons of size and cost (see Capacitor Characteristics).

The output capacitor must meet the requirement for the minimum value of capacitance and also have an ESR value that is within the range 5 mΩ to 500 mΩ for stability.

No-Load Stability

The LP3996-Q1 will remain stable and in regulation with no external load. This is an important consideration in some circuits, for example CMOS RAM keep-alive applications.

Capacitor Characteristics

The LP3996-Q1 is designed to work with ceramic capacitors on the output to take advantage of the benefits they offer. For capacitance values in the range of 0.47 µF to 4.7 µF, ceramic capacitors are the smallest and least expensive, and have the lowest ESR values, thus making them best for eliminating high frequency noise. The ESR of a typical 1.0 µF ceramic capacitor is in the range of 20 mΩ to 40 mΩ, which easily meets the ESR requirement for stability for the LP3996-Q1.

For both input and output capacitors, careful interpretation of the capacitor specification is required to ensure correct device operation. The capacitor value can change greatly, depending on the operating conditions and capacitor type.

In particular, the output capacitor selection should take account of all the capacitor parameters, to ensure that the specification is met within the application. The capacitance can vary with DC bias conditions as well as temperature and frequency of operation. Capacitor values will also show some decrease over time due to aging. The capacitor parameters are also dependant on the particular case size, with smaller sizes giving poorer performance figures in general. As an example, Figure 26 shows a typical graph comparing different capacitor case sizes in a Capacitance vs. DC Bias plot. As shown in the graph, increasing the DC Bias condition can result in the capacitance value falling below the minimum value given in the recommended capacitor specifications table (0.7 µF in this case). Note that the graph shows the capacitance out of spec for the 0402 case size capacitor at higher bias voltages. It is therefore recommended that the capacitor manufacturers' specifications for the nominal value capacitor are consulted for all conditions, as some capacitor sizes (that is, 0402) may not be suitable in the actual application.

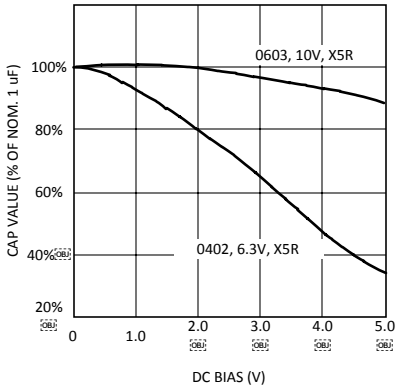


Figure 26. Graph Showing a Typical Variation in Capacitance vs DC Bias

The ceramic capacitor's capacitance can vary with temperature. The capacitor type X7R, which operates over a temperature range of –55℃ to +125℃, will only vary the capacitance to within ±15%. The capacitor type X5R has a similar tolerance over a reduced temperature range of –55℃ to +85°C. Many large value ceramic capacitors larger than 1 µF are manufactured with Z5U or Y5V temperature characteristics. Their capacitance can drop by more than 50% as the temperature varies from 25℃ to 85℃. Therefore X7R is recommended over Z5U and Y5V in applications where the ambient temperature will change significantly above or below 25℃.

Tantalum capacitors are less desirable than ceramic for use as output capacitors because they are more expensive when comparing equivalent capacitance and voltage ratings in the 0.47 µF to 4.7 µF range.

Another important consideration is that tantalum capacitors have higher ESR values than equivalent size ceramics. This means that while it may be possible to find a tantalum capacitor with an ESR value within the stable range, it would have to be larger in capacitance (which means bigger and more costly) than a ceramic capacitor with the same ESR value. It should also be noted that the ESR of a typical tantalum will increase about 2:1 as the temperature goes from 25℃ down to –40℃, so some guard band must be allowed.

Enable Control

The LP3996-Q1 features active high enable pins for each regulator, EN1 and EN2, which turns the corresponding LDO off when pulled low. The device outputs are enabled when the enable lines are set to high. When not enabled the regulator output is off and the device typically consumes 2 nA.

If the application does not require the Enable switching feature, one or both enable pins should be tied to V_{IN} to keep the regulator output permanently on.

To ensure proper operation, the signal source used to drive the enable inputs must be able to swing above and below the specified turn-on / off voltage thresholds listed in the Electrical Characteristics section under V_{IL} and V_{IH}.

Power-On-Reset

The POR pin is an open-drain output which will be set to Low whenever the output of LDO2 falls out of regulation to approximately 90% of its nominal value. An external pull-up resistor, connected to V_{OUT} or V_{IN}, is required on this pin. During start-up, or whenever a fault condition is removed, the POR flag will return to the High state after the output reaches approximately 96% of its nominal value. By connecting a capacitor from the SET pin to GND, a delay to the rising condition of the POR flag may be introduced. The delayed signal may then be used as a Power-on-Reset for a microprocessor within the user's application.

The duration of the delay is determined by the time to charge the delay capacitor to a threshold voltage of 1.25V at 1.2 µA from the SET pin as in the formula below.

$$t_{DELAY} = \frac{V_{TH(SET)} \times C_{SET}}{I_{SET}} \quad (1)$$

A 0.1 µF capacitor will introduce a delay of approximately 100 ms.

Bypass Capacitor

The internal voltage reference circuit of the LP3996-Q1 is connected to the CBYP pin via a high value internal resistor. An external capacitor, connected to this pin, forms a low-pass filter which reduces the noise level on both outputs of the device. There is also some improvement in PSSR and line transient performance. Internal circuitry ensures rapid charging of the CBYP capacitor during start-up. A 10 nF, high quality ceramic capacitor with either NPO or COG dielectric is recommended due to their low leakage characteristics and low noise performance.

Safe Area of Operation

Due consideration should be given to operating conditions to avoid excessive thermal dissipation of the LP3996-Q1 or triggering its thermal shutdown circuit. When both outputs are enabled, the total power dissipation will be $P_{D(LDO1)} + P_{D(LDO2)}$ Where $P_D = (V_{IN} - V_{OUT}) \times I_{OUT}$ for each LDO.

In general, device options which have a large difference in output voltage will dissipate more power when both outputs are enabled, due to the input voltage required for the higher output voltage LDO. In such cases, especially at elevated ambient temperature, it may not be possible to operate both outputs at maximum current at the same time.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3996QSD-1833/NOPB	ACTIVE	WSON	DSC	10	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L275B	Samples
LP3996QSDX-1833/NOPB	ACTIVE	WSON	DSC	10	4500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L275B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF LP3996-Q1 :

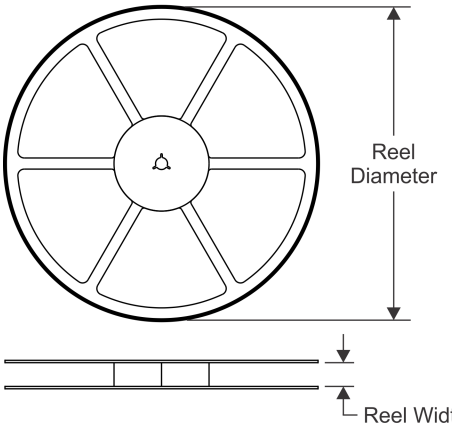
- Catalog: LP3996

NOTE: Qualified Version Definitions:

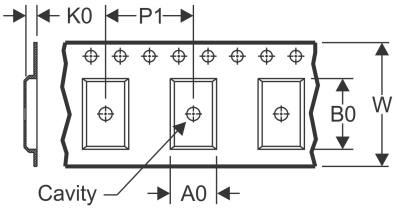
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

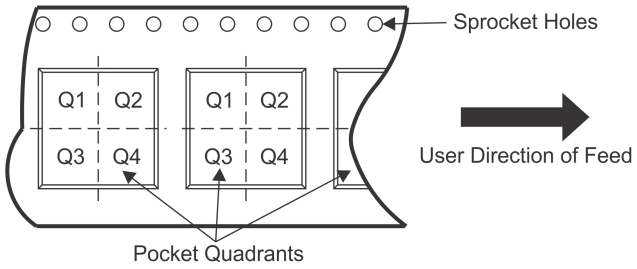


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

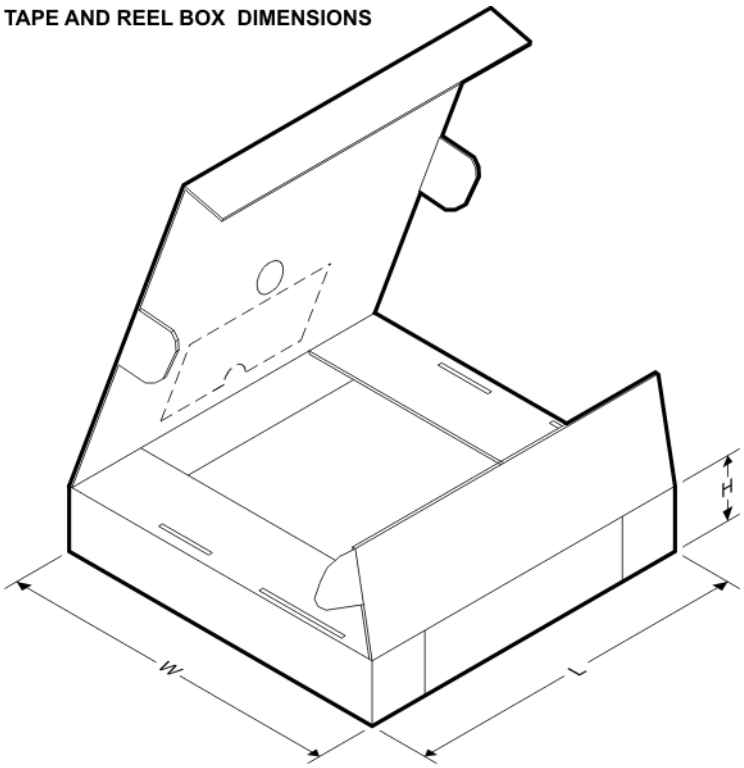
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3996QSD-1833/NOPB	WSON	DSC	10	1000	178.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1
LP3996QSDX-1833/NOPB	WSON	DSC	10	4500	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q1

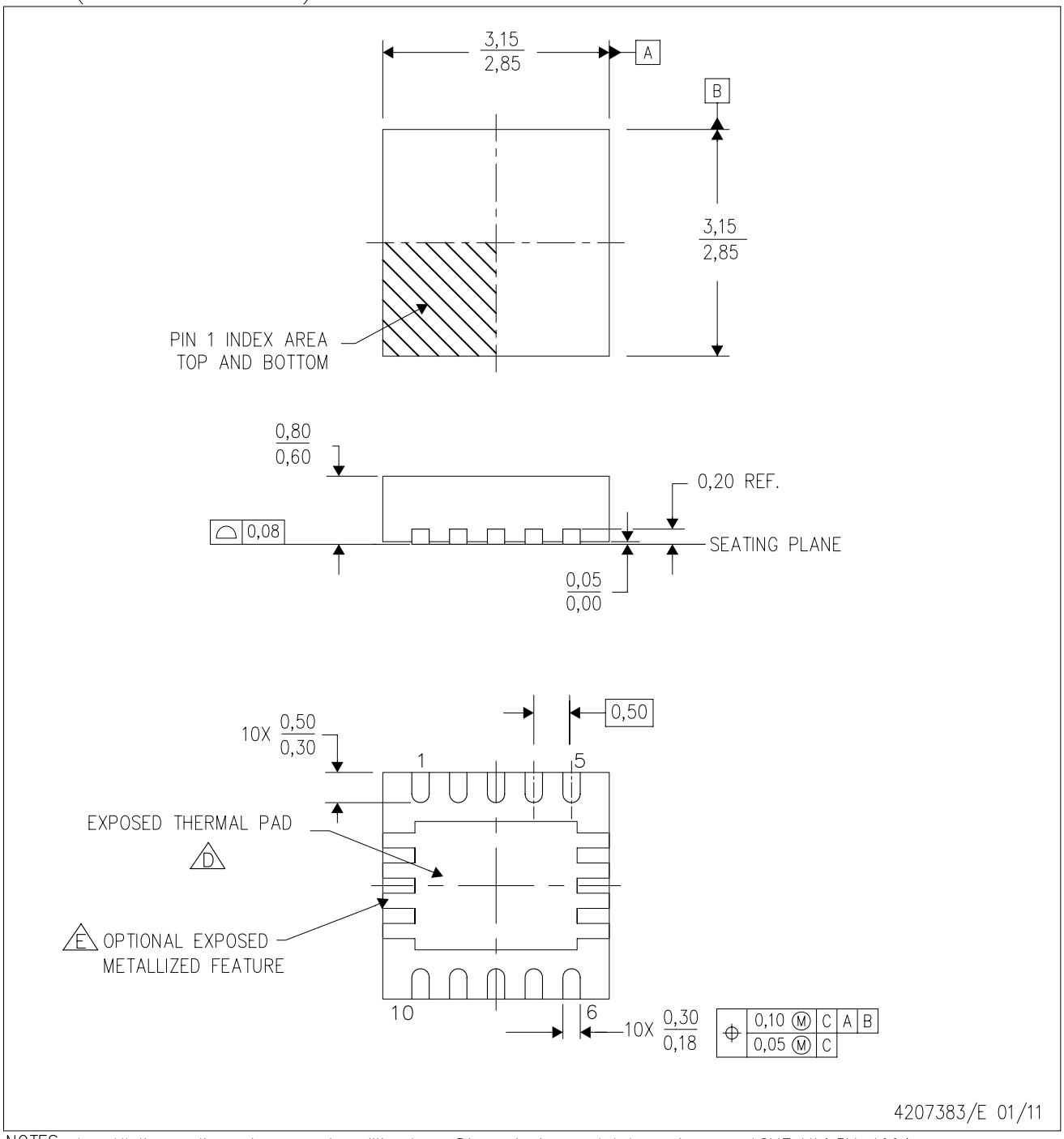
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3996QSD-1833/NOPB	WSON	DSC	10	1000	210.0	185.0	35.0
LP3996QSDX-1833/NOPB	WSON	DSC	10	4500	210.0	185.0	35.0

DSC (S–PWSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

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