

Pentium® Pro Controller

FEATURES

- Combined DAC/Voltage Monitor and PWM Functions
- 4-Bit Digital-to-Analog Converter (DAC)
- 1.0% DAC/Reference
- Low Offset X20 Current Sense Amplifier
- 100kHz, 200kHz, 400kHz Oscillator Frequency Options
- Foldback Current Limiting
- Overvoltage and Undervoltage Fault Windows
- Undervoltage Lockout
- 2Ω Totem Pole Output
- Chip Disable Function

DESCRIPTION

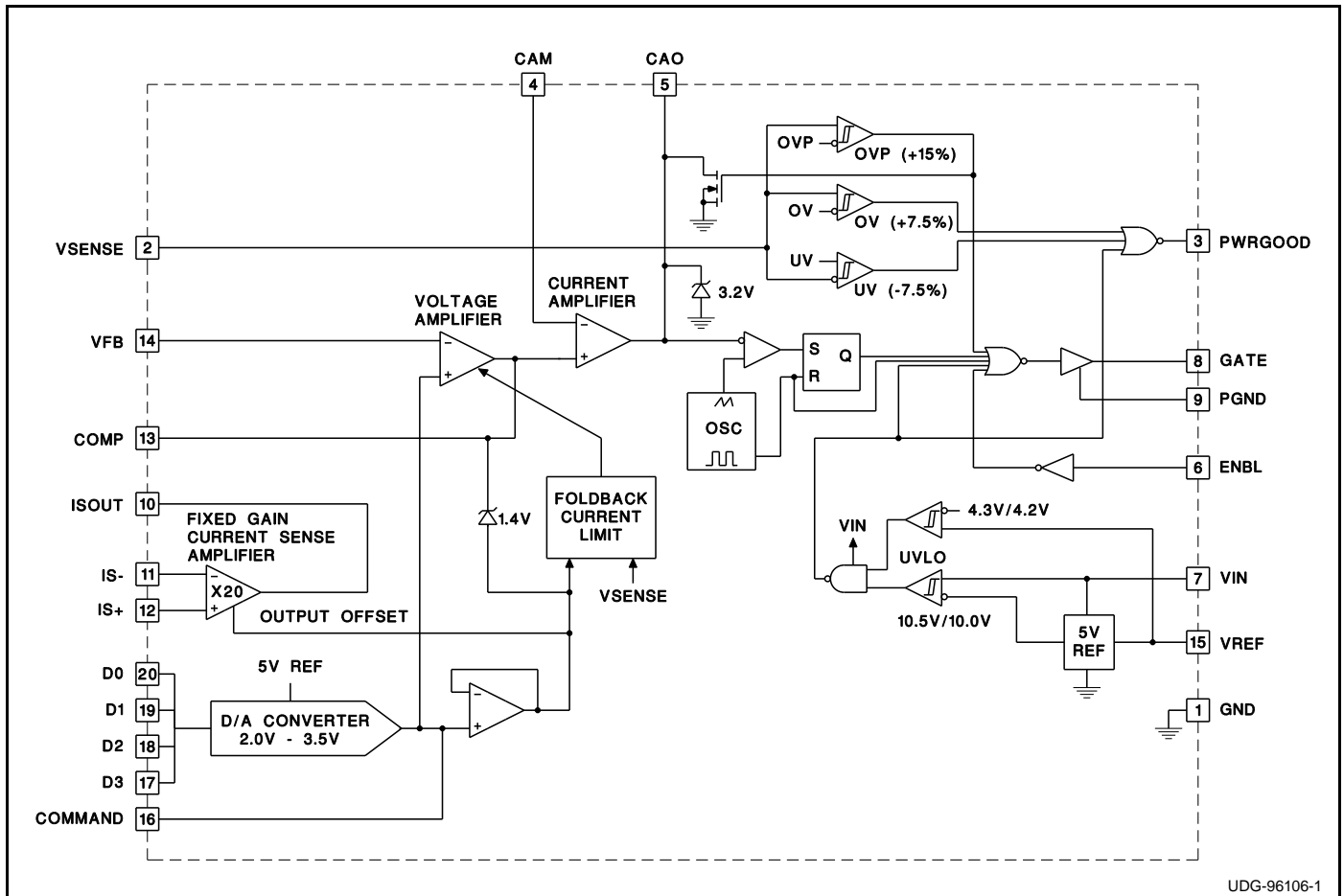
The UCC3880-4/-5/-6 combines high precision reference and voltage monitoring circuitry with average current mode PWM controller circuitry to power Intel Pentium Pro and other high-end microprocessors with a minimum of external components. The UCC3880-x converts 5VDC to an adjustable output, ranging from 2.0VDC to 3.5VDC in 100mV steps with 1% DC system accuracy.

The chip includes a precision 5V reference which is capable of sourcing current to an external load. The output voltage of the DAC is derived from this reference, and is programmed directly by Intel's VID pins (Table 1).

The accuracy of the DAC/reference combination is 1.0%. The overvoltage and undervoltage comparators monitor the system output voltage and indicate when it rises above or falls below its programmed value by more than 7.5%. A second overvoltage protection comparator pulls the current amplifier output voltage low to force zero duty cycle when the system output voltage exceeds its designed value by more than 15%. This comparator also terminates the cycle. Undervoltage lockout circuitry assures the correct logic states at the outputs during powerup and powerdown. Grounding the ENABLE pin forces the GATE output low.

(continued)

BLOCK DIAGRAM



UDG-96106-1

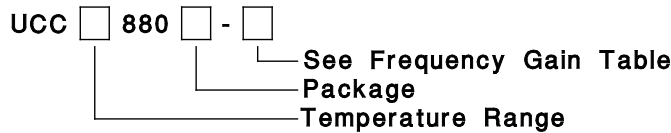
DESCRIPTION (cont.)

The voltage and current amplifiers have a 4MHz gain bandwidth product to satisfy high performance system requirements. The internal current sense amplifier permits the use of a low value current sense resistor, minimizing power loss. The oscillator frequency is fixed internally at 100kHz, 200kHz, or 400kHz, depending upon the option selected. The foldback circuit reduces the converter short circuit current limit to 50% of its nominal value when the converter is short circuited. The gate driver is a 2Ω totem pole output stage capable of driving an external MOSFET.

This device is available in 20-pin dual in-line and surface mount packages. The UCC2880-x is specified for operation from -25°C to 85°C, and the UCC3880-x is specified for operation from 0°C to 70°C.

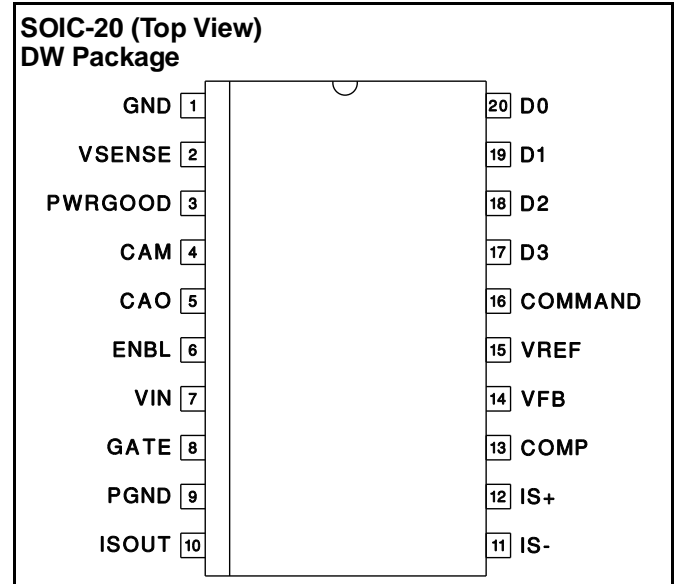
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ORDERING INFORMATION



Consult factory for temperature range or package options not shown.

CONNECTION DIAGRAM



Frequency Gain Table

	Frequency		
	100kHz	200kHz	400kHz
UCC3880-4	X		
UCC3880-5		X	
UCC3880-6			X

ELECTRICAL CHARACTERISTICS: Unless otherwise specified, VIN = 12V, VSENSE = 3.5V, VENBL = 5V, VD0 = VD1 = VD2 = VD3 = 0V, 0°C < TA < 70°C, TA = TJ.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Undervoltage Lockout					
VIN UVLO Turn-on Threshold			10.5	10.8	V
VIN UVLO Turn-off Threshold		9.5	10		V
UVLO Threshold Hysteresis			500		mV
Supply Current					
IIN			3.5		mA
DAC/Reference					
COMMAND Voltage Accuracy	10.8V < VIN < 13.2V, IVREF = 0mA	-1		1	%
D0-D3 Voltage High	DX Pin Floating		5		V
D0-D3 Input Bias Current	DX Pin Tied to GND		-70	-20	μA
VREF Output Voltage		4.975	5	5.025	V
VREF Load Regulation	IVREF = 0mA to 5mA	-10	0		mV
VREF Sourcing Current	VREF = 0V		10		mA
OVP Comparator					
Trip Point	% Over COMMAND Voltage	10	15	20	%
Hysteresis			20	30	mV
VSENSE Input Bias Current	OV, OVP, UV Combined		-0.1		μA
Propagation Delay			1		μs

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, $V_{IN} = 12V$, $V_{SENSE} = 3.5V$, $V_{ENBL} = 5V$, $V_{D0} = V_{D1} = V_{D2} = V_{D3} = 0V$, $0^{\circ}C < T_A < 70^{\circ}C$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)		7.6	10	%
Return Point	% Over COMMAND Voltage (Note 1)	5	7.4		%
Hysteresis			20	30	mV
PWRGOOD Equivalent Resistance	$V_{SENSE} = 2.0V$			470	Ω
Propagation Delay			1		μs
UV Comparator					
Trip Point	% Over COMMAND Voltage (Note 1)	-10	-7.6		%
Return Point	% Over COMMAND Voltage (Note 1)		-7.4	-5	%
Hysteresis			20	30	mV
Propagation Delay			1		μs
Enable Pin					
Pull-up Current	$V_{ENBL} = 2.5V$		-50	-20	μA
Voltage Error Amplifier					
Input Offset Voltage	$V_{COMP} = 3.5V$		0.0		mV
Input Bias Current	$V_{CM} = 3.0V$		-0.02	0	μA
Open Loop Gain	$1V < V_{COMP} < 4V$		90		dB
Common Mode Rejection Ratio	$2V < V_{COMP} < 3.5V$		90		dB
Power Supply Rejection Ratio	$10.8V < V_{IN} < 15V$		85		dB
Output Sourcing Current	$V_{VFB} = 2V$, $V_{COMMAND} = V_{COMP} = 2.5V$		-0.5		mA
Output Sinking Current	$V_{VFB} = 3V$, $V_{COMMAND} = V_{COMP} = 2.5V$		2.0		mA
Gain Bandwidth Product	$F = 100kHz$		3		MHz
Current Sense Amplifier					
Gain			20		V/V
Input Resistance			5		$k\Omega$
Common Mode Rejection Ratio	$0V < V_{CM} < 4.5V$		60		dB
Power Supply Rejection Ratio	$10.8V < V_{IN} < 15V$		80		dB
Output Sourcing Current	$V_{IS-} = 2V$, $V_{ISOUT} = V_{IS+} = 2.5V$		-0.5		mA
Output Sinking Current	$V_{IS-} = 3V$, $V_{ISOUT} = V_{IS+} = 2.5V$		6.0		mA
-3dB Frequency	At GAIN = 20		1.75		MHz
Current Amplifier					
Input Offset Voltage	$V_{CM} = 3.0V$			10	mV
Input Bias Current	$V_{CM} = 3.0V$		0.15		μA
Open Loop Gain	$1V < V_{CAO} < 3V$		90		dB
Output Voltage High	$V_{COMP} = 3V$, $V_{CAM} = 2.5V$		3.2		V
Common Mode Rejection Ratio	$1.5V < V_{CM} < 4.9V$		80		dB
Power Supply Rejection Ratio	$10.8V < V_{IN} < 15V$		80		dB
Output Sourcing Current	$V_{CAM} = 2V$, $V_{CAO} = V_{COMP} = 2.5V$		-0.5		mA
Output Sinking Current	$V_{CAM} = 3V$, $V_{CAO} = V_{COMP} = 2.5V$		2.0		mA
Gain Bandwidth Product	$F = 100kHz$		3.5		MHz

ELECTRICAL CHARACTERISTICS (cont.): Unless otherwise specified, $V_{IN} = 12V$, $V_{SENSE} = 3.5V$, $V_{ENBL} = 5V$, $VD0 = VD1 = VD2 = VD3 = 0V$, $0^{\circ}C < T_A < 70^{\circ}C$, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Oscillator					
Frequency (-4)		85	100	115	kHz
Frequency (-5)			200		kHz
Frequency (-6)			400		kHz
Frequency Change With Voltage	$10.8V < V_{IN} < 15V$		1		%
Output Section					
Maximum Duty Cycle		90	95	99	%
Output Low Voltage	$I_{GATE} = -100mA$		0.20		V
Output High Voltage	$I_{GATE} = 100mA$		11.8		V
Rise Time	$C_{GATE} = 3.3nF$		20	80	ns
Fall Time	$C_{GATE} = 3.3nF$		15	80	ns
Output Impedance	$I_{GATE} = 100mA$		2		Ω
	$I_{GATE} = -100mA$		2		Ω
Foldback Current Limit					
Clamp Level	Measured at Voltage EA Output; $V_{SENSE} = V_{COMMAND} = 3V$		4.4		V
	$V_{COMMAND} = 3V$, $V_{SENSE} = 0$		3.7		V

Note 1: This percentage is measured with respect to the ideal COMMAND voltage programmed by the D0 - D3 pins.

PIN DESCRIPTIONS (cont.)

CAM (Current Amplifier Inverting Input): The average load current feedback from ISOUT is applied through a resistor to this pin. The current loop compensation network is also connected to this pin (see CAO below).

CAO (Current Amplifier Output): The current loop compensation network is connected between this pin and CAM. The voltage on this pin is the input to the PWM comparator and regulates the output voltage of the system. The GATE output is disabled (held low) unless the voltage on this pin exceeds 1V, allowing the PWM to force zero duty cycle when necessary. The PWM forces maximum duty cycle when the voltage on CAO exceeds the oscillator peak voltage (3V). A 3.2V clamp circuit prevents the CAO voltage from rising excessively past the oscillator peak voltage for excellent transient response.

COMMAND (Digital-to-Analog Converter Output Voltage): This pin is the output of the 4-bit digital-to-analog converter (DAC) and the noninverting input of the voltage amplifier. The voltage on this pin sets the switching regulator output voltage. Setting all input control codes low produces 3.5V at COMMAND; setting all codes high produces 2.0V at COMMAND. The DAC LSB step size (i.e. resolution) is 100mV (See Table 1). The COMMAND source impedance is typically 1.2k Ω and must therefore drive only high impedance inputs if accuracy is to be maintained. Bypass COMMAND with a 0.01 μF , low ESR, low ESL capacitor for best circuit noise immunity.

Decimal Code	D3	D2	D1	D0	COMMAND Voltage
15	1	1	1	1	2.0
14	1	1	1	0	2.1
13	1	1	0	1	2.2
12	1	1	0	0	2.3
11	1	0	1	1	2.4
10	1	0	1	0	2.5
9	1	0	0	1	2.6
8	1	0	0	0	2.7
7	0	1	1	1	2.8
6	0	1	1	0	2.9
5	0	1	0	1	3.0
4	0	1	0	0	3.1
3	0	0	1	1	3.2
2	0	0	1	0	3.3
1	0	0	0	1	3.4
0	0	0	0	0	3.5

Table 1. Programming the COMMAND Voltage

COMP (Voltage Amplifier Output): The system voltage compensation network is applied between COMP and VFB.

D0 - D3 (DAC Digital Input Control Codes): These are the DAC digital input control codes, with D0 representing the least significant bit (LSB) and D3, the most significant bit (MSB). A bit is set low by being connected to GND. A

PIN DESCRIPTIONS (cont.)

bit is set high by floating it, or connecting it to a 5V source. Each control pin is pulled up to approximately 5V by an internal 70µA current source.

ENBL (Chip Enable Pin): This input is used to disable the GATE and PWRGOOD outputs. Grounding this pin causes the GATE output to be held low; floating the pin or pulling it up to 5V ensures normal operation. ENBL is pulled up to 5V internally.

GATE (PWM Output, MOSFET Driver): This output provides a 2Ω totem pole driver. Use a series resistor of at least 5Ω between this pin and the gate of the external MOSFET to prevent excessive overshoot.

GND (Signal Ground): All voltages are measured with respect to GND. Bypass capacitors on the VCC and VREF pins should be connected directly to the ground plane near the GND pin.

IS- (Current Sense Amplifier Inverting Input): This pin is the inverting input to the current sense amplifier and is connected to the low side of the average current sense resistor.

IS+ (Current Sense Amplifier Noninverting Input): This pin is the noninverting input to the current sense amplifier and is connected to the high side of the average current sense resistor.

ISOUT (Current Sense Amplifier Output): This pin is the output of the current sense amplifier. The voltage on this pin is $(\text{COMMAND} + \text{GCSA} \cdot I \cdot \text{RSENSE})$, where COMMAND is the voltage on the COMMAND pin, GCSA is the fixed gain of the current sense amplifier, equal to 20, I is the current through the sense resistor, and RSENSE is the value of the average current sensing resistor.

PGND (Power Ground): This pin provides a dedicated ground for the output gate driver. The GND and PGND pins should be connected externally using a short printed

circuit board trace close to the IC. Decouple VIN to PGND with a low ESR capacitor $\geq 0.10\mu\text{F}$.

PWRGOOD (Undervoltage/Lower Overvoltage Output): This pin is an open drain output which is driven low to reset the microprocessor when VSENSE rises above or falls below its nominal value by 7.5%. The on resistance of the open drain switch will be no higher than 470Ω. The OV and UV comparators' hysteresis is fixed at 20mV independent of the COMMAND voltage.

VIN (Positive Supply Voltage): This pin supplies power to the chip. Connect VIN to a stable voltage source of at least 10.8V. The GATE and PWRGOOD outputs will be held low until VCC exceeds the upper undervoltage lock-out threshold. This pin should be bypassed directly to the GND pin.

VFB (Voltage Amplifier Inverting Input): This input is connected to COMP through a feedback network and to the power supply output through a resistor or a divider network.

VREF (Voltage Reference Output): This pin provides an accurate 5V reference and is internally short circuit current limited. VREF powers the D/A converter and also provides a threshold voltage for the UVLO comparator. For best reference stability, bypass VREF directly to GND with a low ESR, low ESL capacitor of at least 0.01µF.

VSENSE (Output Voltage Sensing Input): This pin is connected to the system output voltage through a low pass filter. When the voltage on VSENSE rises above or falls below the COMMAND voltage by 7.5%, the PWRGOOD output is driven low to reset the microprocessor. When the voltage on VSENSE rises above the COMMAND voltage by 15%, the OVP comparator pulls the current amplifier output voltage below the oscillator valley voltage to force zero duty cycle at the GATE output. This pin is also used by the foldback current limiting circuitry.

APPLICATION INFORMATION

Current Limit

The short circuit current limit, I_{SC} , is set according to:

$$I_{SC} = \frac{1.4V}{R_{SENSE} \cdot GCSA}$$

where RSENSE is the average current sense resistor and GCSA is the current sense amplifier gain, where GCSA equals 20. Example: Choose RSENSE to set the short circuit current limit at 16A using the UCC3880-5

$$R_{SENSE} = \frac{1.4V}{16A \cdot 20} = 4.4m\Omega$$

A lower resistance value may be needed if the AC ripple current in the inductor is more than 20% of the full load current.

Related Publications

U-156 and U-157 are Unitrode Application Notes describing the operation of the UC3886 and the UC3886/UC3910 together in a Pentium® Pro application.

PARTS LIST

REF.	DESCRIPTION	PACKAGE
U1	Unitrode UCC3830DWP-5 DAC/PWM	SOIC-20 Wide
C1	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C2	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C3	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C4	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C5	Sprague/Vishay 595D475X0016A2B, 4.7 μ F 16V Tantalum	SPRAGUE Size A
C6	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C7	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C8	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C9	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C10	Sanyo 6MV1500GX, 1500 μ F, 6.3V, Aluminum Electrolytic	10x20mm Radial Can
C11	Sprague 593D107X9010D2, 100 μ F, 6.3V Tantalum	EIA Size D SMD
C12	0.10 μ F Ceramic	1206 SMD
C13	0.01 μ F Ceramic	0603 SMD
C14	0.01 μ F Ceramic	0603 SMD
C15	0.01 μ F Ceramic	0603 SMD
C16	1000pF Ceramic	0603 SMD
C17	0.10 μ F Ceramic	1206 SMD
C18	33pF NPO Ceramic	0603 SMD
C19	1500pF Ceramic	0603 SMD
C20	82pF NPO Ceramic	0603 SMD
C21	0.10 μ F Ceramic	1206 SMD
C22	0.10 μ F Ceramic	1206 SMD
CR1	International Rectifier 32CTQ030 30V, 30A Schottky Diode	TO-220AB
L1	Micrometals T50-52B, 10 Turns #16AWG, 4.5 μ H	Toroid
Q1	International Rectifier IRL3103, 30V, 56A	TO-220AB
R1	Dale/Vishay WSR-2 0.005 Ω 1%	SMD Power Package
R2	10 Ω , 5%, 1/16 Watt	0603 SMD
R3	8.2k Ω , 5%, 1/16 Watt	0603 SMD
R4	6.81k Ω , 1%, 1/16 Watt	0603 SMD
R5	3.92k Ω , 1%, 1/16 Watt	0603 SMD
R6	261k Ω , 1%, 1/16 Watt	0603 SMD
R7	100k Ω , 1%, 1/16 Watt	0603 SMD
R8	3.92k Ω , 1%, 1/16 Watt	0603 SMD
R9	10.5k Ω , 1%, 1/16 Watt	0603 SMD
Q1-HS	AAVID 576802 TO-220 Heat Sink	TO-220AB
CR1-HS	AAVID 577002 TO-220 Heat Sink	TO-220AB

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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
UCC3880DW-4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI
UCC3880DWTR-4	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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