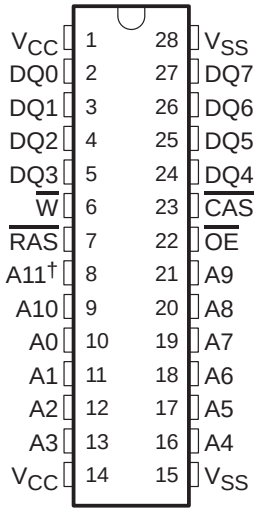
- **Organization . . . 2097152 × 8**
- **Single 5 V Power Supply (±10% Tolerance)**
- **Performance Ranges:**

	ACCESS TIME t_{RAC} MAX	ACCESS TIME t_{CAC} MAX	ACCESS TIME t_{AA} MAX	READ OR WRITE CYCLE MIN
’41x800-60	60 ns	15 ns	30 ns	110 ns
’41x800-70	70 ns	18 ns	35 ns	130 ns
’41x800-80	80 ns	20 ns	40 ns	150 ns

- **Enhanced Page-Mode Operation With $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) Refresh**
- **High-Impedance State Unlatched Output**
- **High-Reliability Plastic 28-Lead 400-Mil-Wide Surface-Mount Small-Outline J-Lead (SOJ) Package**
- **Operating Free-Air Temperature Range 0°C to 70°C**
- **Fabricated Using Enhanced Performance Implanted CMOS (EPIC™) Technology by Texas Instruments (TI™)**

DZ PACKAGE
(TOP VIEW)



PIN NOMENCLATURE	
A0–A11†	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ0–DQ7	Data In/Data Out
$\overline{OE}$	Output Enable
$\overline{RAS}$	Row-Address Strobe
V_{CC}	5 V
V_{SS}	Ground
$\overline{W}$	Write Enable

† A11 is NC (no internal connection) for TMS417800.

description

The TMS41x800 series is a set of high-speed, 16777216-bit dynamic random-access memories (DRAMs) organized as 2097152 words of eight bits each. It employs TI’s state-of-the-art EPIC technology for high performance, reliability, and low power.

These devices feature maximum $\overline{RAS}$ access times of 60 ns, 70 ns, and 80 ns. All addresses and data-in lines are latched on-chip to simplify system design. Data out is unlatched to allow greater system flexibility.

The TMS416800 and TMS417800 are offered in a 28-lead plastic surface-mount SOJ package (DZ suffix). This package is characterized for operation from 0°C to 70°C.

operation

enhanced page mode

Enhanced page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is eliminated. The maximum number of columns that can be accessed is determined by t_{RASP}, the maximum row-address strobe ($\overline{RAS}$) low time.

Unlike conventional page-mode DRAMs, the column-address buffers in these devices are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while column-address strobe ($\overline{CAS}$) is high. The falling edge of $\overline{CAS}$ latches the column addresses and enables the output. This feature allows the devices to operate at a higher data bandwidth than conventional page-mode parts because data retrieval begins as soon as the column address is valid rather than when $\overline{CAS}$ goes low. This performance improvement is referred to as enhanced page mode. A valid column address can be presented immediately after row-address hold time has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after t_{CAC} max (access time from $\overline{CAS}$ low) if t_{AA} max (access time from column address) and t_{RAC} (access time from $\overline{RAS}$) have been satisfied. In the event that column address for the next cycle is valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of t_{CPA} (access time from $\overline{CAS}$ precharge) or t_{CAC}.

address: A0 – A11 (TMS416800) and A0 – A10 (TMS417800)

Twenty-one address bits are required to decode one of 2097152 storage cell locations. For the TMS416800, 12 row-address bits are set up on A0 through A11 and latched on the chip by the $\overline{RAS}$. Nine column-address bits are set up on A0 through A8. For the TMS417800, 11 row-address bits are set up on inputs A0 through A10 and latched on the chip by $\overline{RAS}$. Ten column-address bits are set up on A0 through A9. All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable because it activates the sense amplifiers as well as the row decoder. $\overline{CAS}$ is used as a chip select, activating the output buffers and latching the address bits into the column-address buffers.

write enable ($\overline{W}$)

The read or write mode is selected through $\overline{W}$. A logic high on $\overline{W}$ selects the read mode, and a logic low selects the write mode. The data inputs are disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out remains in the high-impedance state for the entire cycle, permitting a write operation with $\overline{OE}$ grounded.

data in (DQ0 – DQ7)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early-write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$, and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{CAS}$ is already low, and the data is strobed in by $\overline{W}$ with setup and hold time referenced to this signal. In a delayed-write or read-modify-write cycle, $\overline{OE}$ must be high to bring the output buffers to the high-impedance state prior to impressing data on the I/O lines.

data out (DQ0 – DQ7)

Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{OE}$ are brought low. In a read cycle, the output becomes valid after the access time interval t_{CAC} (which begins with the negative transition of $\overline{CAS}$) as long as t_{RAC} and t_{AA} are satisfied.

$\overline{\text{RAS}}$-only refresh

TMS416800

A refresh operation must be performed at least once every 64 ms to retain data. The refresh operation can be achieved by strobing each of the 4096 rows (A0–A11). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

TMS417800

A refresh operation must be performed at least once every 32 ms to retain data. The refresh operation can be achieved by strobing each of the 2048 rows (A0–A10). A normal read or write cycle refreshes all bits in each row that is selected. A $\overline{\text{RAS}}$-only operation can be used by holding $\overline{\text{CAS}}$ at the high (inactive) level, conserving power as the output buffers remain in the high-impedance state. Externally generated addresses must be used for a $\overline{\text{RAS}}$-only refresh.

hidden refresh

A hidden refresh can be performed while maintaining valid data at the output pin. The hidden refresh operation is accomplished by holding $\overline{\text{CAS}}$ at V_{IL} after a read or write operation and cycling $\overline{\text{RAS}}$ after a specified precharge period, similar to a $\overline{\text{RAS}}$-only refresh cycle. The external address is ignored, and the refresh address is generated internally.

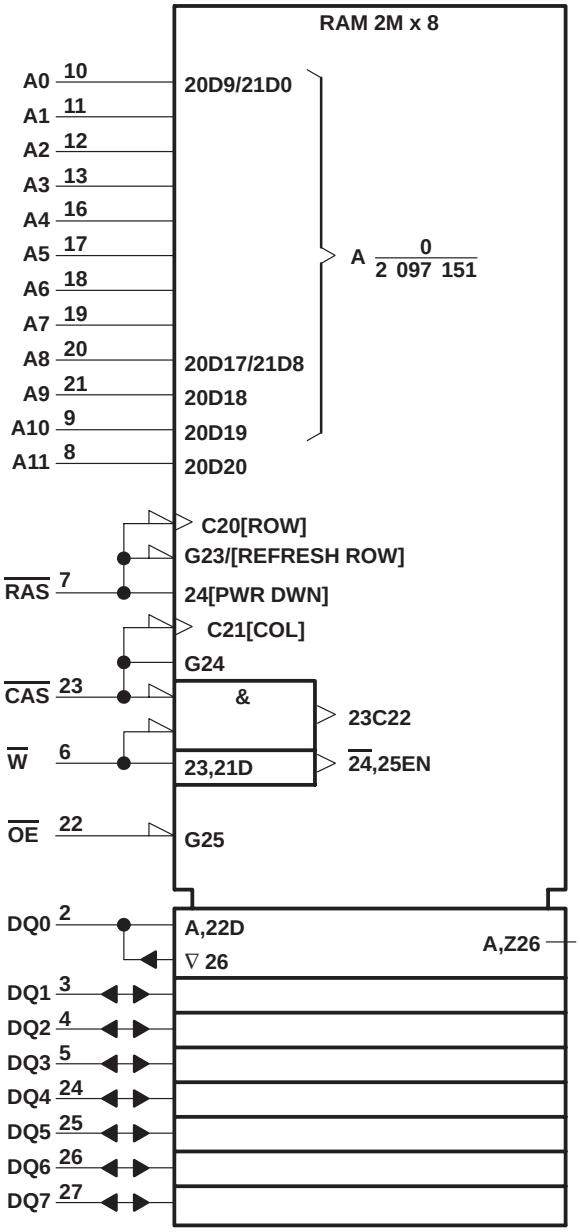
$\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ (CBR) refresh

CBR refresh is performed by bringing $\overline{\text{CAS}}$ low earlier than $\overline{\text{RAS}}$ (see parameter t_{CSR}) and then holding it low after $\overline{\text{RAS}}$ falls (see parameter t_{CHR}). For successive CBR refresh cycles, $\overline{\text{CAS}}$ can remain low while cycling $\overline{\text{RAS}}$. The external address is ignored, and the refresh address is generated internally.

power up

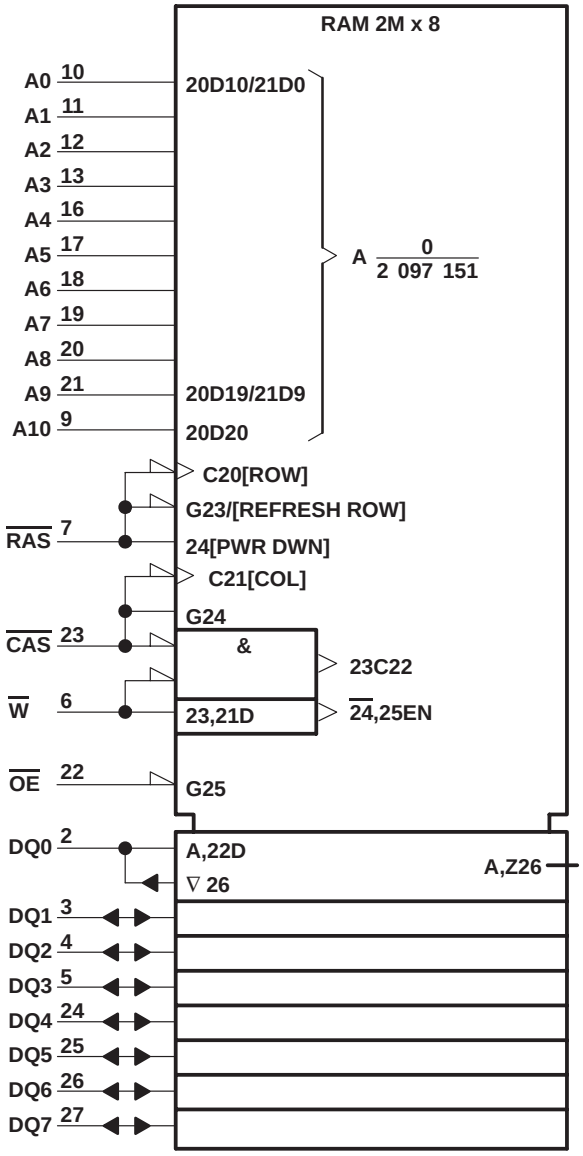
To achieve proper device operation, an initial pause of 200 µs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level. The eight initialization cycles must include at least one refresh ($\overline{\text{RAS}}$-only or CBR) cycle.

logic symbol for TMS416800†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

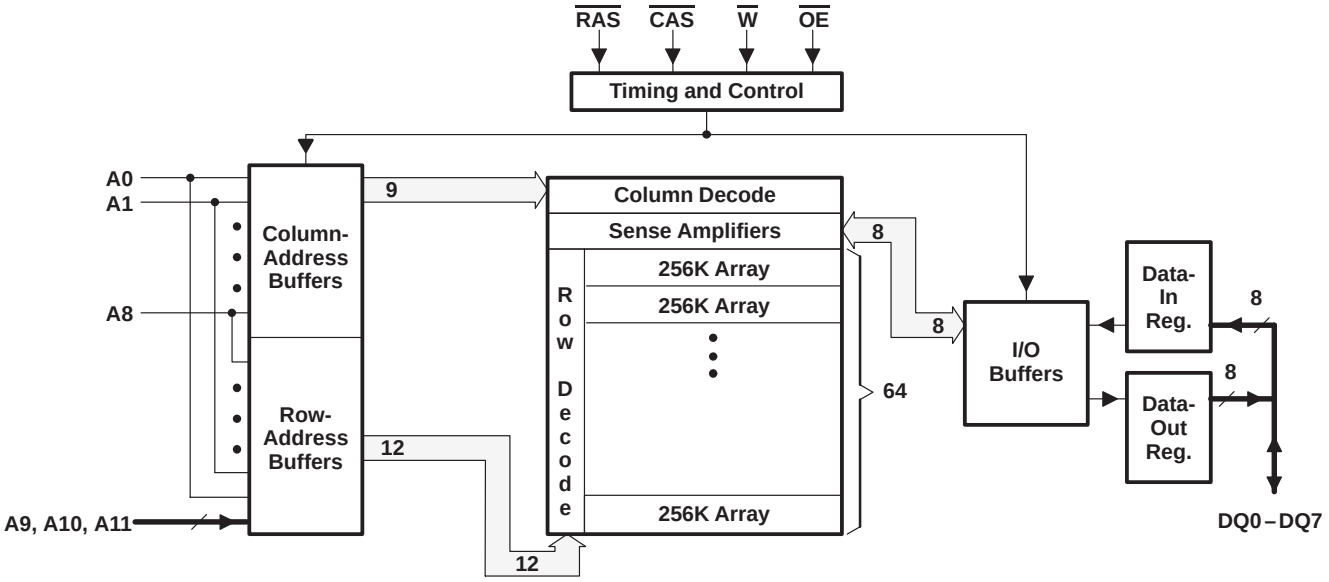
logic symbol for TMS417800†



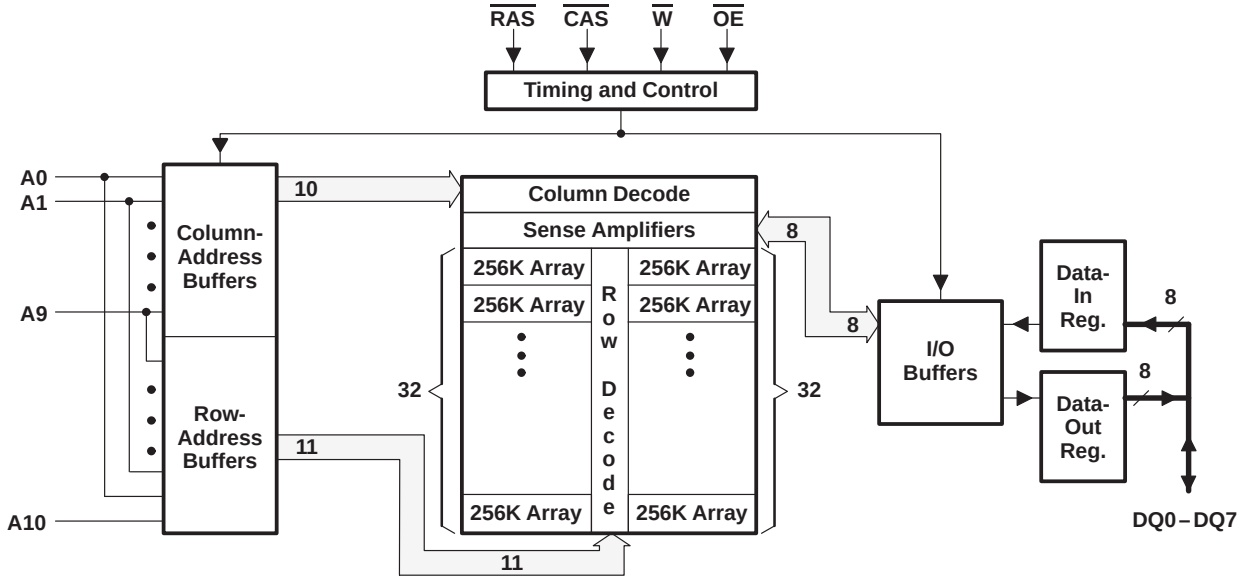
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 647-12.

functional block diagram

TMS416800



TMS417800



TEXAS INSTRUMENTS
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} . . . . . – 1 V to 7 V
Voltage range on any pin (see Note 1) . . . . . – 1 V to 7 V
Short-circuit output current . . . . . 50 mA
Power dissipation . . . . . 1 W
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range, T_{stg} . . . . . – 55°C to 125°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to V_{SS}.

recommended operating conditions

		TMS41x800			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	– 1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used for logic-voltage levels only.

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

TMS416800

PARAMETER		TEST CONDITIONS†	'416800-60		'416800-70		'416800-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		80		70		60	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, Minimum cycle, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		80		70		60	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $t_{\overline{PC}}$ = MIN, $\overline{RAS}$ low, $\overline{CAS}$ cycling		70		60		50	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

TMS417800

PARAMETER		TEST CONDITIONS†	'417800-60		'417800-70		'417800-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = – 5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_{CC} = 5.5 V, V_I = 0 V to 6.5 V, All others = 0 V to V_{CC}		± 10		± 10		± 10	µA
I_O	Output current (leakage)	$\overline{V_{CC}}$ = 5.5 V, V_O = 0 V to V_{CC}, $\overline{CAS}$ high		± 10		± 10		± 10	µA
I_{CC1}‡§	Read- or write-cycle current	V_{CC} = 5.5 V, Minimum cycle		110		100		90	mA
I_{CC2}	Standby current	V_{IH} = 2.4 V (TTL), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		2		2		2	mA
		V_{IH} = V_{CC} – 0.2 V (CMOS), After one memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high		1		1		1	mA
I_{CC3}‡§	Average refresh current ($\overline{RAS}$-only refresh or CBR)	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high ($\overline{RAS}$ only), Minimum cycle, $\overline{RAS}$ low after $\overline{CAS}$ low (CBR)		110		100		90	mA
I_{CC4}‡¶	Average page current	$\overline{V_{CC}}$ = 5.5 V, $\overline{RAS}$ low, $\overline{t_{PC}}$ = MIN, $\overline{CAS}$ cycling		70		60		50	mA

† For conditions shown as MIN/MAX, use the appropriate value specified in the timing requirements.
‡ Measured with outputs open
§ Measured with a maximum of one address change while $\overline{RAS}$ = V_{IL}
¶ Measured with a maximum of one address change while $\overline{CAS}$ = V_{IH}

capacitance over recommended ranges of supply voltage and operating free-air temperature, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, A0–A11†		5	pF
$C_{i(OE)}$	Input capacitance, $\overline{OE}$		7	pF
$C_{i(RC)}$	Input capacitance, $\overline{CAS}$ and $\overline{RAS}$		7	pF
$C_{i(W)}$	Input capacitance, $\overline{W}$		7	pF
C_o	Output capacitance		7	pF

† A11 is NC (no internal connection) for TMS417800.

NOTE 3: V_{CC} = NOM supply voltage ±10%, and the bias on pins under test is 0 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

PARAMETER		’41x800-60		’41x800-70		’41x800-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access time from column address		30		35		40	ns
t_{CAC}	Access time from $\overline{CAS}$		15		18		20	ns
t_{CPA}	Access time from $\overline{CAS}$ precharge		35		40		45	ns
t_{RAC}	Access time from $\overline{RAS}$		60		70		80	ns
t_{OEA}	Access time from $\overline{OE}$		15		18		20	ns
t_{CLZ}	Delay time, $\overline{CAS}$ to output in the low-impedance state	0		0		0		ns
t_{OH}	Output data hold time from $\overline{CAS}$	3		3		3		ns
t_{OHO}	Output data hold time from $\overline{OE}$	3		3		3		ns
t_{OFF}	Output buffer turn-off delay from $\overline{CAS}$ (see Note 5)	0	15	0	18	0	20	ns
t_{OEZ}	Output buffer turn-off delay from $\overline{OE}$ (see Note 5)	0	15	0	18	0	20	ns

NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.

5. t_{OFF} and t_{OEZ} are specified when the output is no longer driven.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (see Note 4)

		’41x800-60		’41x800-70		’41x800-80		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Cycle time, read	110		130		150		ns
t_{WC}	Cycle time, write	110		130		150		ns
t_{RWC}	Cycle time, read-write	155		181		205		ns
t_{PC}	Cycle time, page-mode read or write (see Note 6)	40		45		50		ns
t_{PRWC}	Cycle time, page-mode read-write	85		96		105		ns
t_{RASP}	Pulse duration, $\overline{RAS}$ active, page mode (see Note 7)	60	100 000	70	100 000	80	100 000	ns
t_{RAS}	Pulse duration, $\overline{RAS}$ active, nonpage mode (see Note 7)	60	10 000	70	10 000	80	10 000	ns
t_{CAS}	Pulse duration, $\overline{CAS}$ active (see Note 8)	15	10 000	18	10 000	20	10 000	ns
t_{CP}	Pulse duration, $\overline{CAS}$ precharge	10		10		10		ns
t_{RP}	Pulse duration, $\overline{RAS}$ precharge	40		50		60		ns
t_{WP}	Pulse duration, write command	10		10		10		ns
t_{ASC}	Setup time, column address	0		0		0		ns
t_{ASR}	Setup time, row address	0		0		0		ns
t_{DS}	Setup time, data-in (see Note 9)	0		0		0		ns
t_{RCS}	Setup time, read command	0		0		0		ns
t_{CWL}	Setup time, write command before $\overline{CAS}$ precharge	15		18		20		ns
t_{RWL}	Setup time, write command before $\overline{RAS}$ precharge	15		18		20		ns
t_{WCS}	Setup time, write command before $\overline{CAS}$ active (early-write only)	0		0		0		ns
t_{CSR}	Setup time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)	5		5		5		ns
t_{CAH}	Hold time, column address	10		15		15		ns
t_{DH}	Hold time, data-in (see Note 9)	10		15		15		ns
t_{RAH}	Hold time, row address	10		10		10		ns
t_{RCH}	Hold time, read command referenced to $\overline{CAS}$ (see Note 10)	0		0		0		ns
t_{RRH}	Hold time, read command referenced to $\overline{RAS}$ (see Note 10)	0		0		0		ns
t_{WCH}	Hold time, write command during $\overline{CAS}$ active (early-write only)	10		15		15		ns
t_{RHCP}	Hold time, $\overline{RAS}$ active from $\overline{CAS}$ precharge	35		40		45		ns
t_{OEH}	Hold time, $\overline{OE}$ command	15		18		20		ns
t_{ROH}	Hold time, $\overline{RAS}$ referenced to $\overline{OE}$	10		10		10		ns

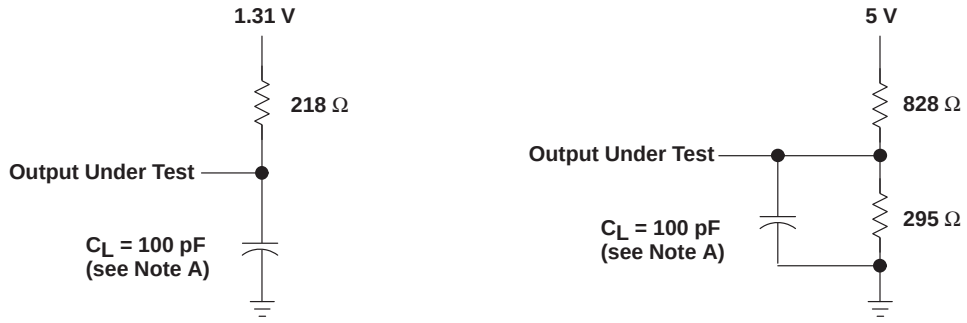
NOTES: 4. With ac parameters, it is assumed that t_T = 5 ns.
6. To ensure t_{PC} min, t_{ASC} should be ≥ to t_{CP}.
7. In a read-write cycle, t_{RWD} and t_{RWL} must be observed.
8. In a read-write cycle, t_{CWD} and t_{CWL} must be observed.
9. Referenced to the later of $\overline{CAS}$ or $\overline{W}$ in write operations
10. Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (continued)

			'41x800-60		'41x800-70		'41x800-80		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{AWD}	Delay time, column address to write command (read-write operation only)		55		63		70		ns
t_{CHR}	Delay time, $\overline{CAS}$ referenced to $\overline{RAS}$ (CBR refresh only)		10		10		10		ns
t_{CRP}	Delay time, $\overline{CAS}$ precharge to $\overline{RAS}$		5		5		5		ns
t_{CSH}	Delay time, $\overline{RAS}$ active to $\overline{CAS}$ precharge		60		70		80		ns
t_{CWD}	Delay time, $\overline{CAS}$ to write command (read-write operation only)		40		46		50		ns
t_{OED}	Delay time, $\overline{OE}$ to data in		15		18		20		ns
t_{RAD}	Delay time, $\overline{RAS}$ to column address (see Note 11)		15	30	15	35	15	40	ns
t_{RAL}	Delay time, column address to $\overline{RAS}$ precharge		30		35		40		ns
t_{CAL}	Delay time, column address to $\overline{CAS}$ precharge		30		35		40		ns
t_{RCD}	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (see Note 11)		20	45	20	52	20	60	ns
t_{RPC}	Delay time, $\overline{RAS}$ precharge to $\overline{CAS}$		0		0		0		ns
t_{RSH}	Delay time, $\overline{CAS}$ active to $\overline{RAS}$ precharge		15		18		20		ns
t_{RWD}	Delay time, $\overline{RAS}$ to write command (read-write operation only)		85		98		110		ns
t_{CPW}	Delay time, $\overline{CAS}$ precharge to write command (read-write only)		60		68		75		ns
t_{REF}	Refresh time interval	'416800		64		64		64	ms
		'417800		32		32		32	
t_T	Transition time		3	30	3	30	3	30	ns

NOTE 11: The maximum value is specified only to ensure access time.

PARAMETER MEASUREMENT INFORMATION



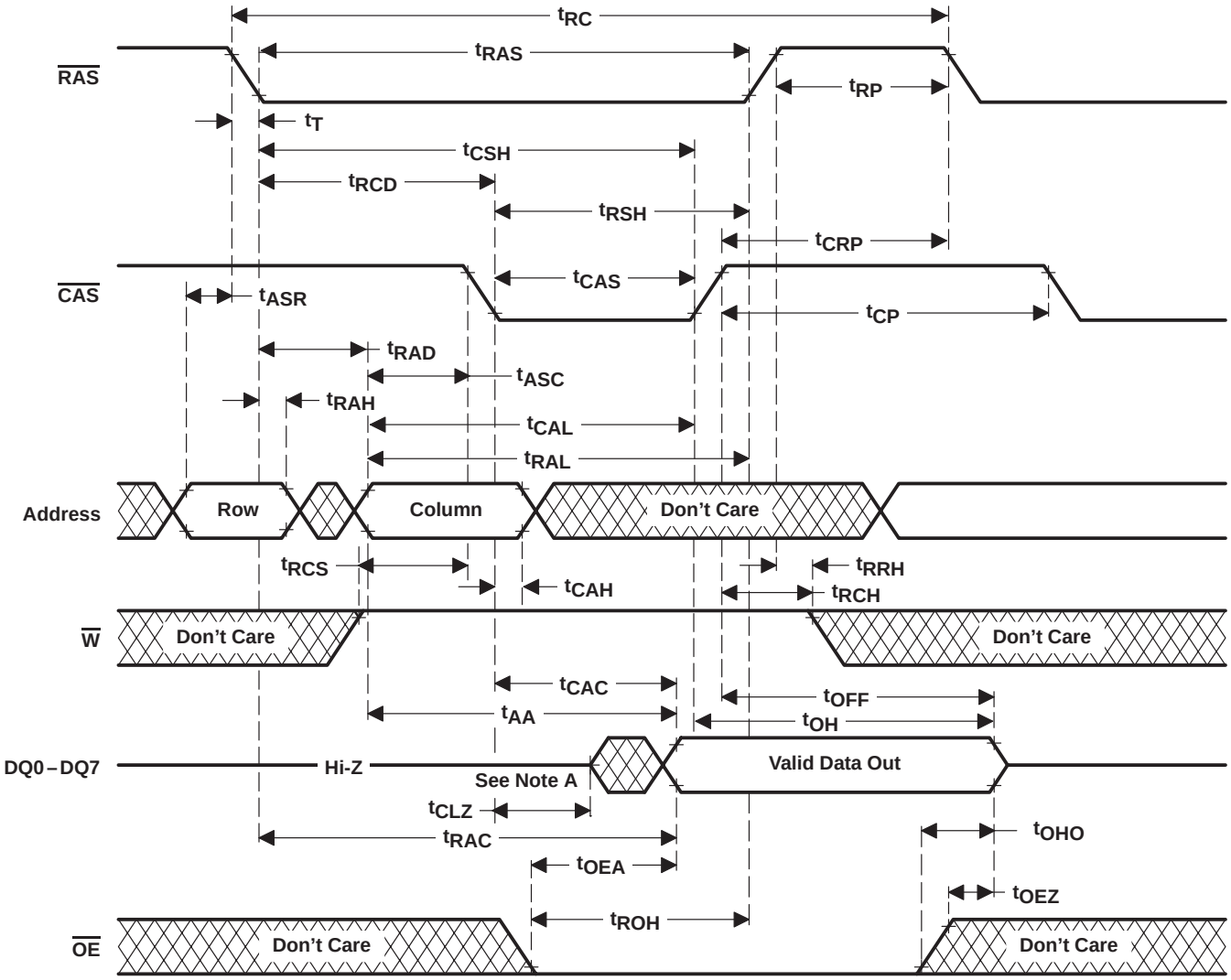
(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

NOTE A: C_L includes probe and fixture capacitance.

Figure 1. Load Circuits for Timing Parameters

PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 2. Read-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

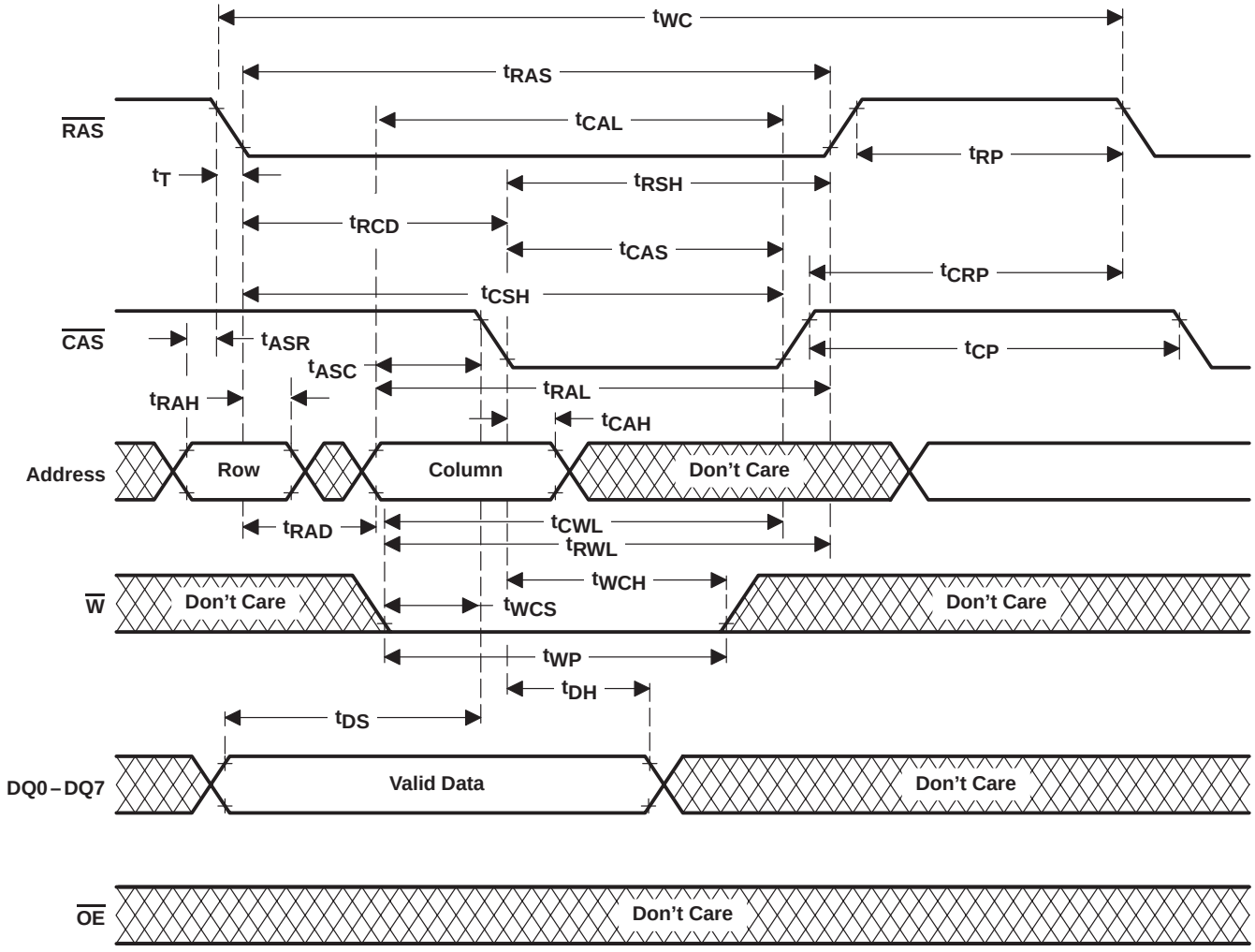


Figure 3. Early-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

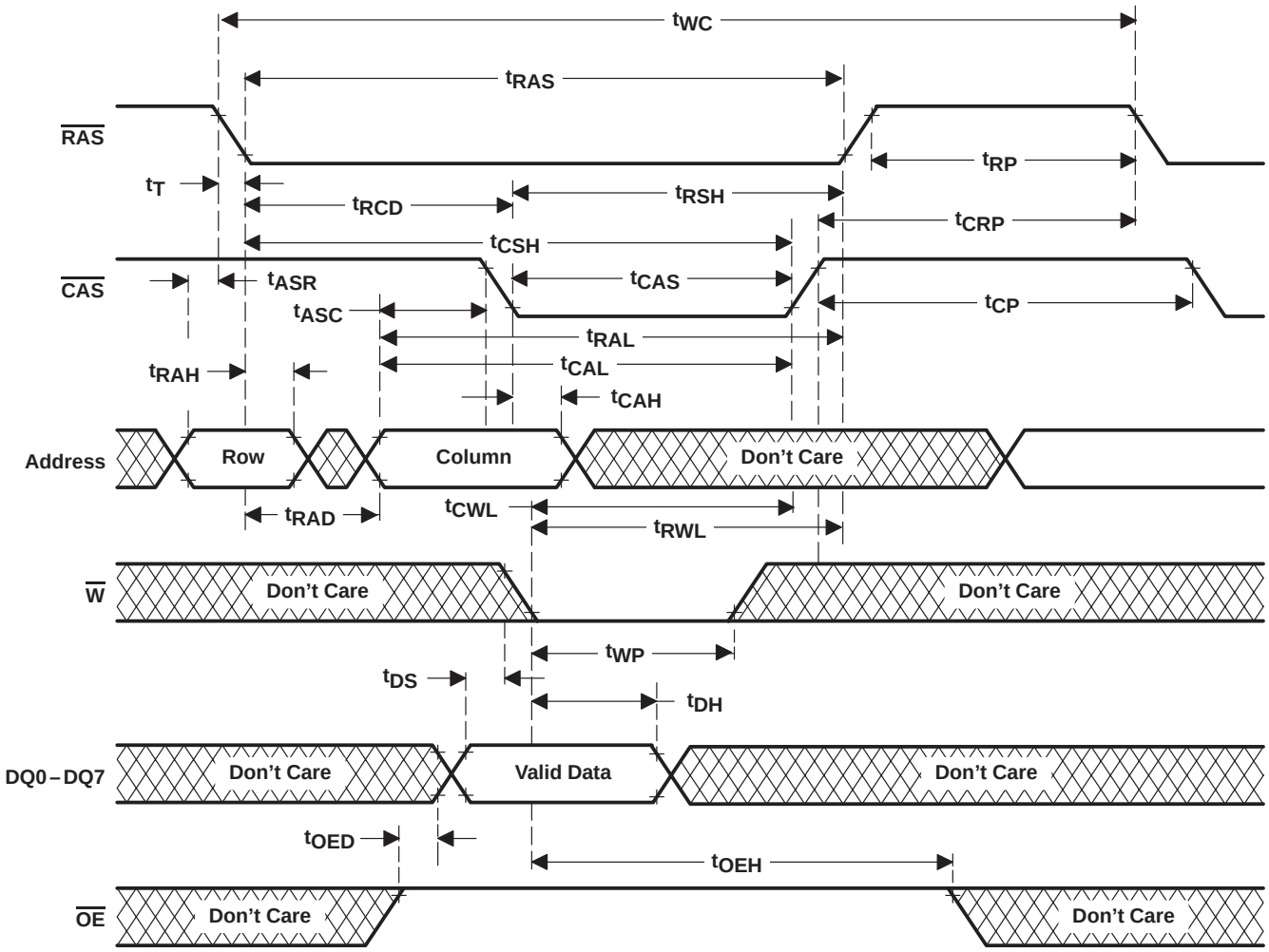
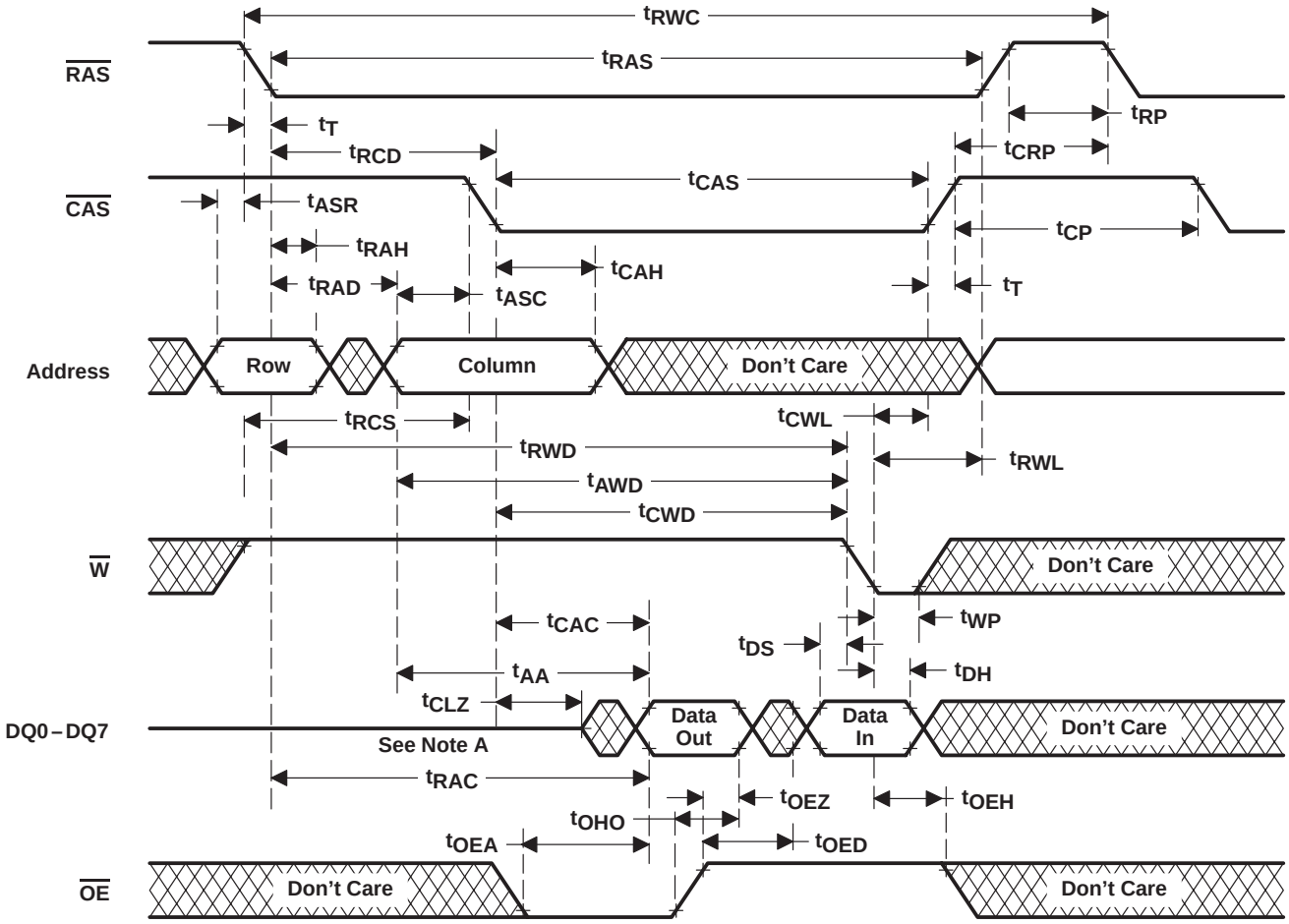


Figure 4. Write-Cycle Timing

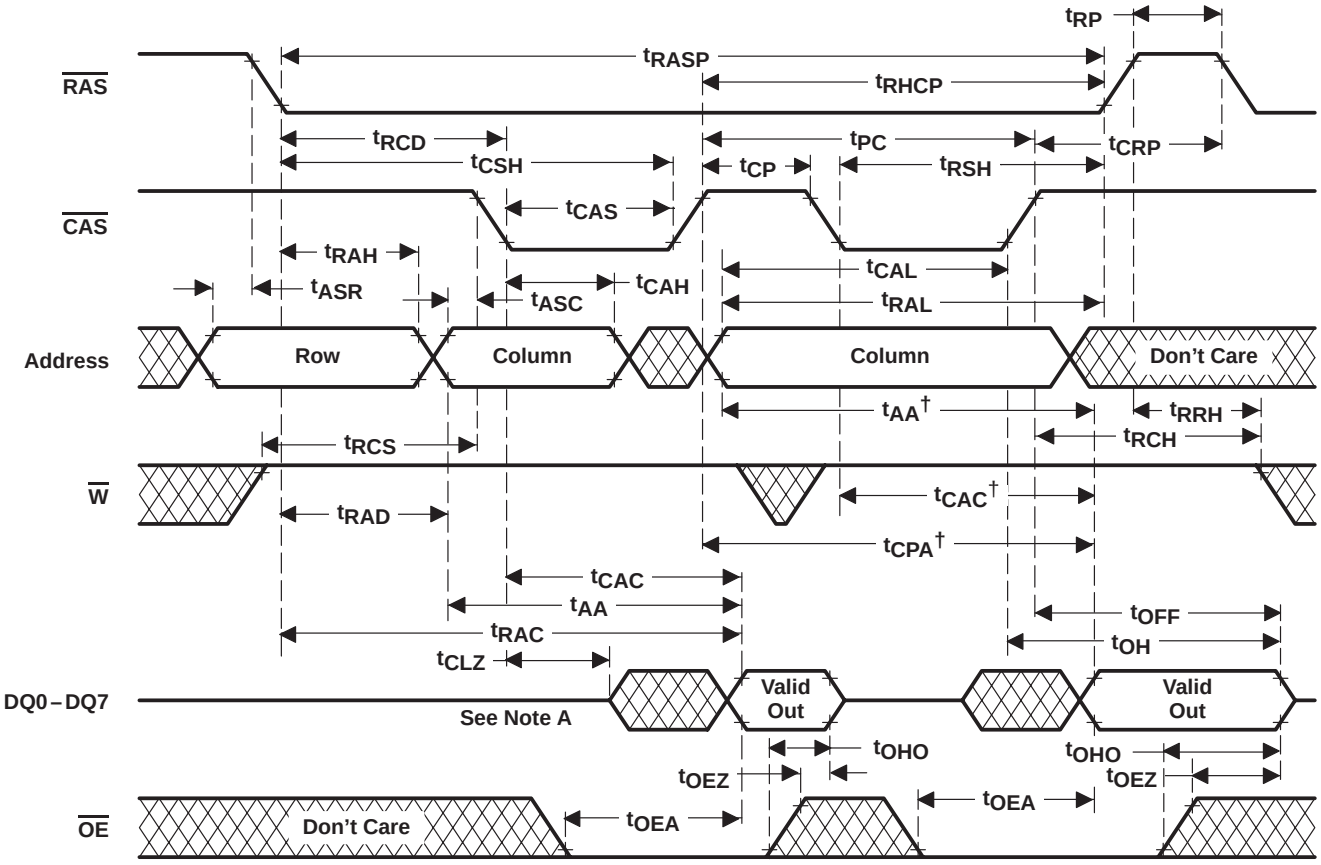
PARAMETER MEASUREMENT INFORMATION



NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 5. Read-Write-Cycle Timing

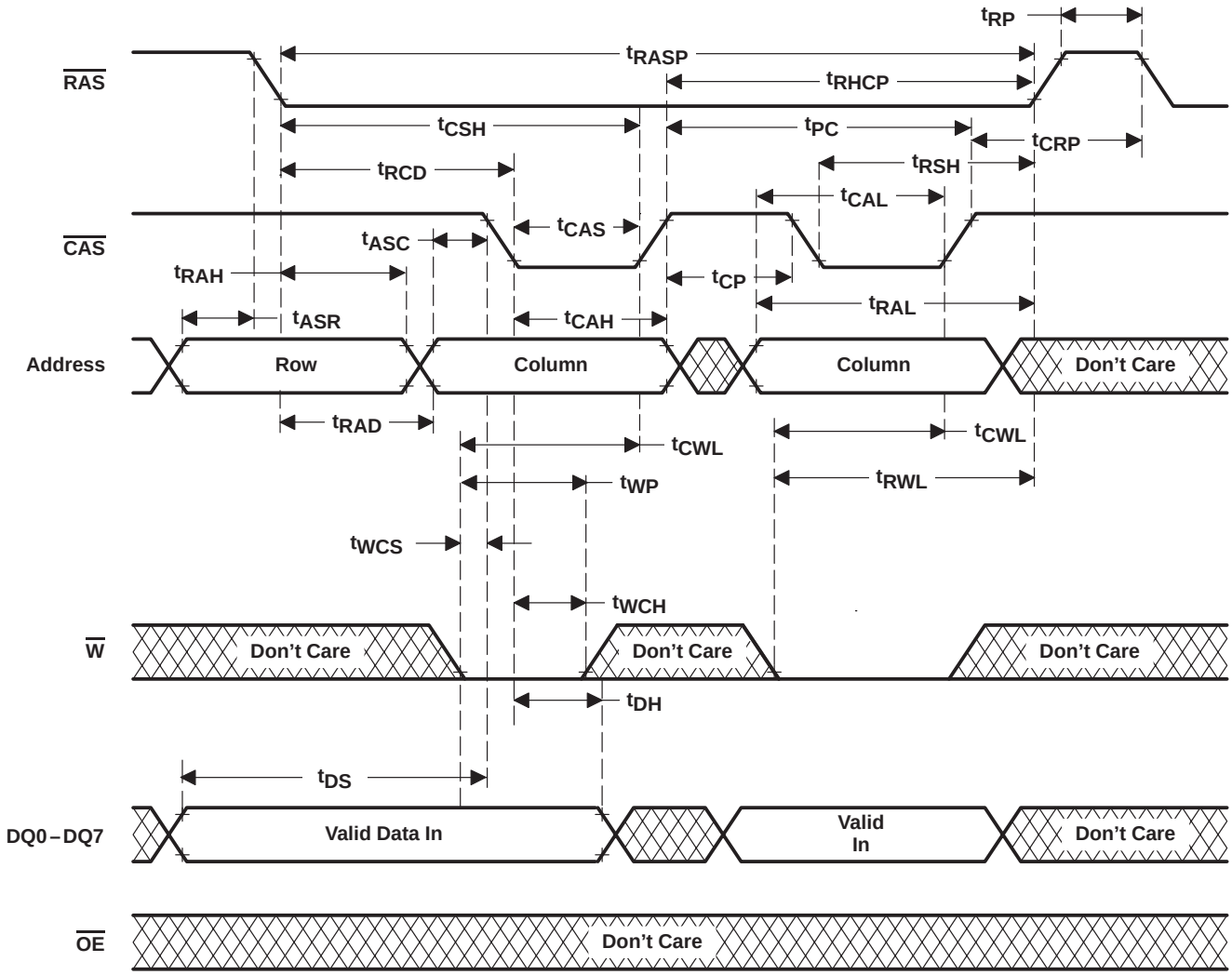
PARAMETER MEASUREMENT INFORMATION



† Access time is t_{CPA}-, t_{CAC}-, or t_{AA}-dependent.
NOTE A: Output can go from the high-impedance state to an invalid-data state prior to the specified access time.

Figure 6. Enhanced-Page-Mode Read-Cycle Timing

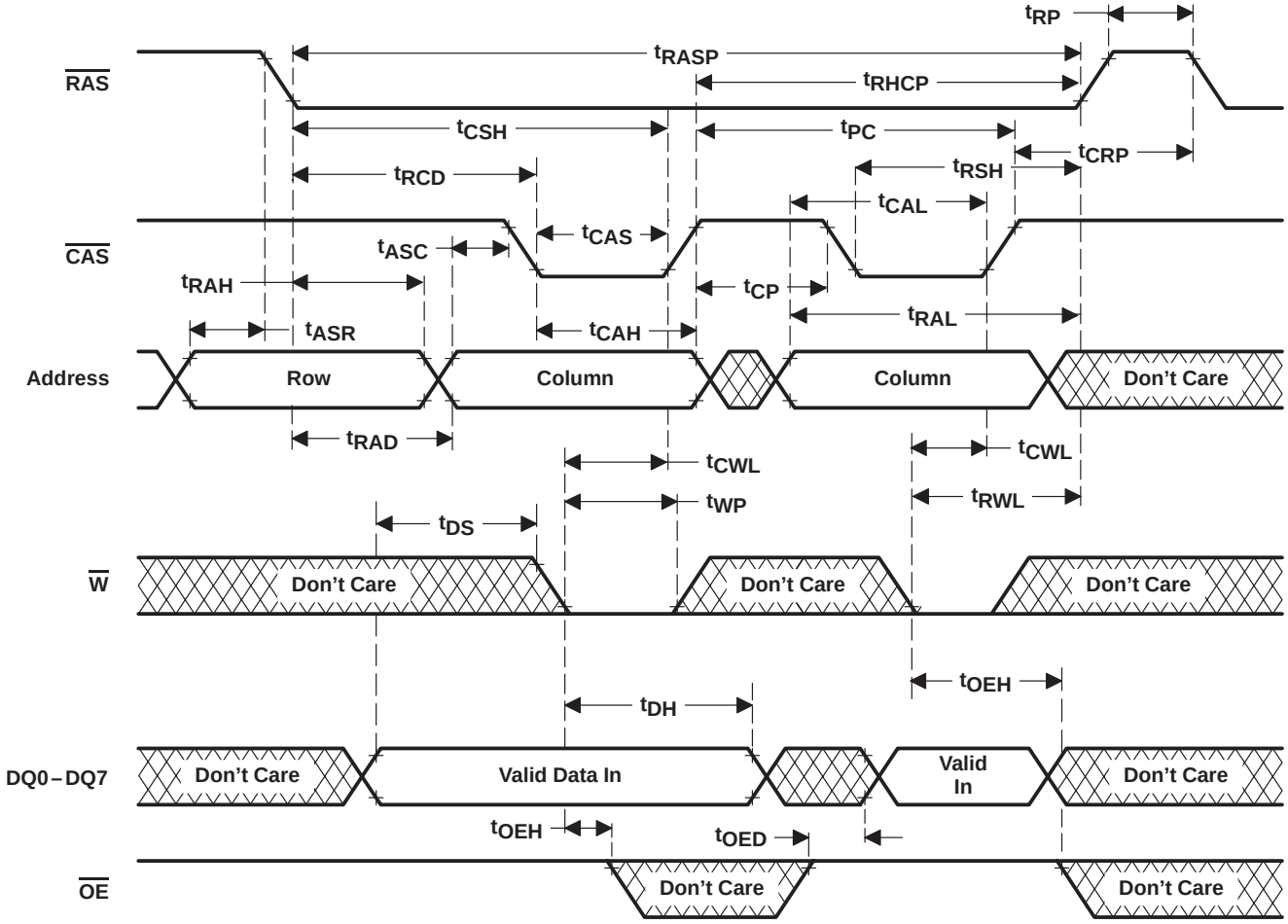
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 7. Enhanced-Page-Mode Early-Write-Cycle Timing

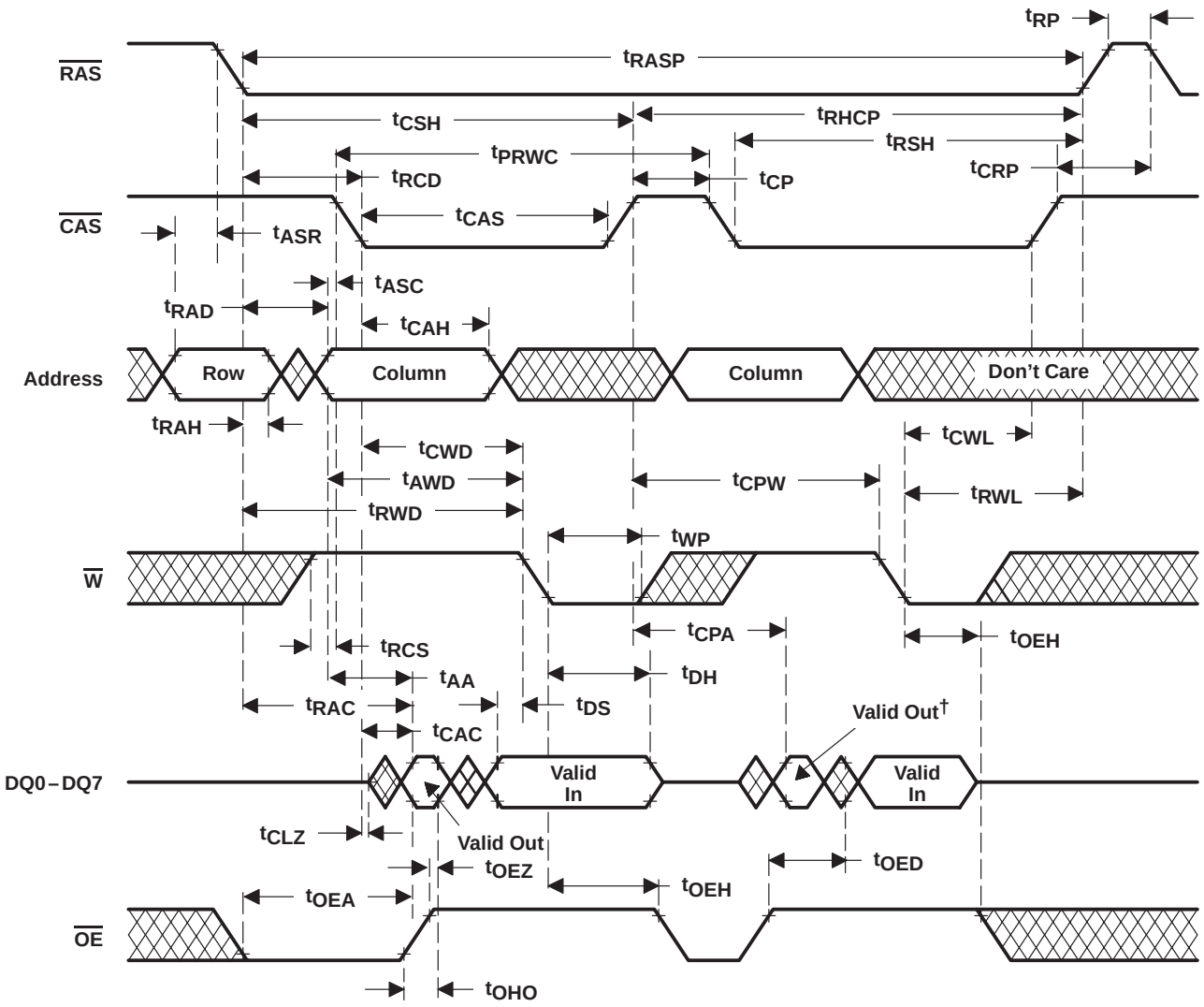
PARAMETER MEASUREMENT INFORMATION



NOTE A: A read cycle or a read-write cycle can be intermixed with write cycles as long as read and read-write timing specifications are not violated.

Figure 8. Enhanced-Page-Mode Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION



† Output can go from the high-impedance state to an invalid-data state prior to the specified access time.
NOTE A: A read or write cycle can be intermixed with read-write cycles as long as the read and write timing specifications are not violated.

Figure 9. Enhanced-Page-Mode Read-Write-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

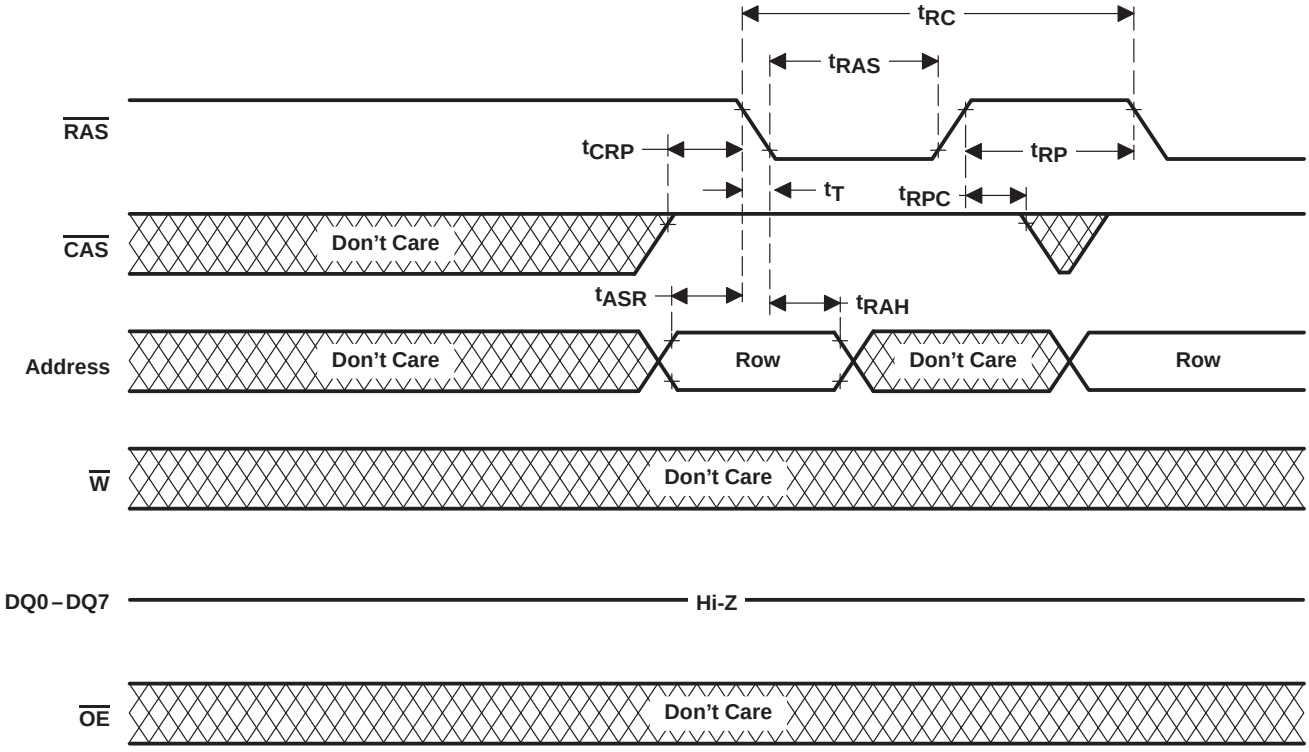


Figure 10. $\overline{\text{RAS}}$-Only Refresh-Cycle Timing

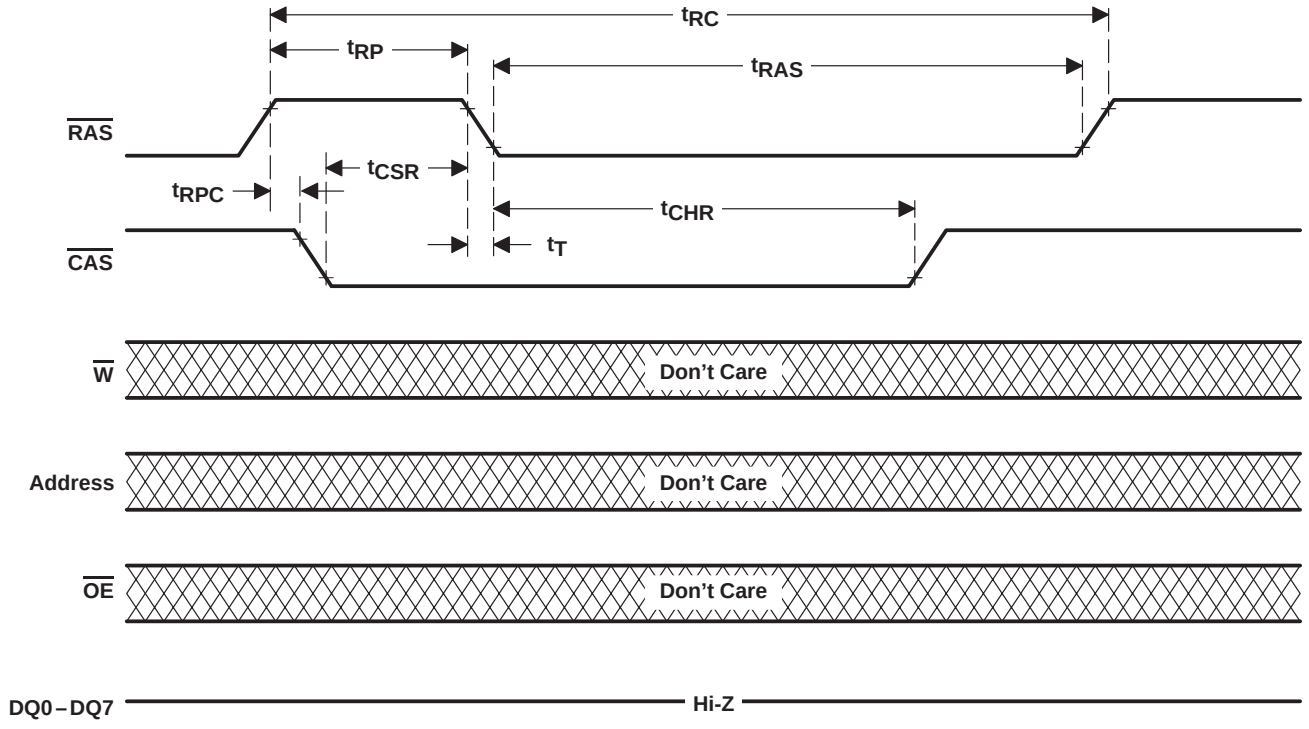


Figure 11. Automatic-CBR-Refresh-Cycle Timing

PARAMETER MEASUREMENT INFORMATION

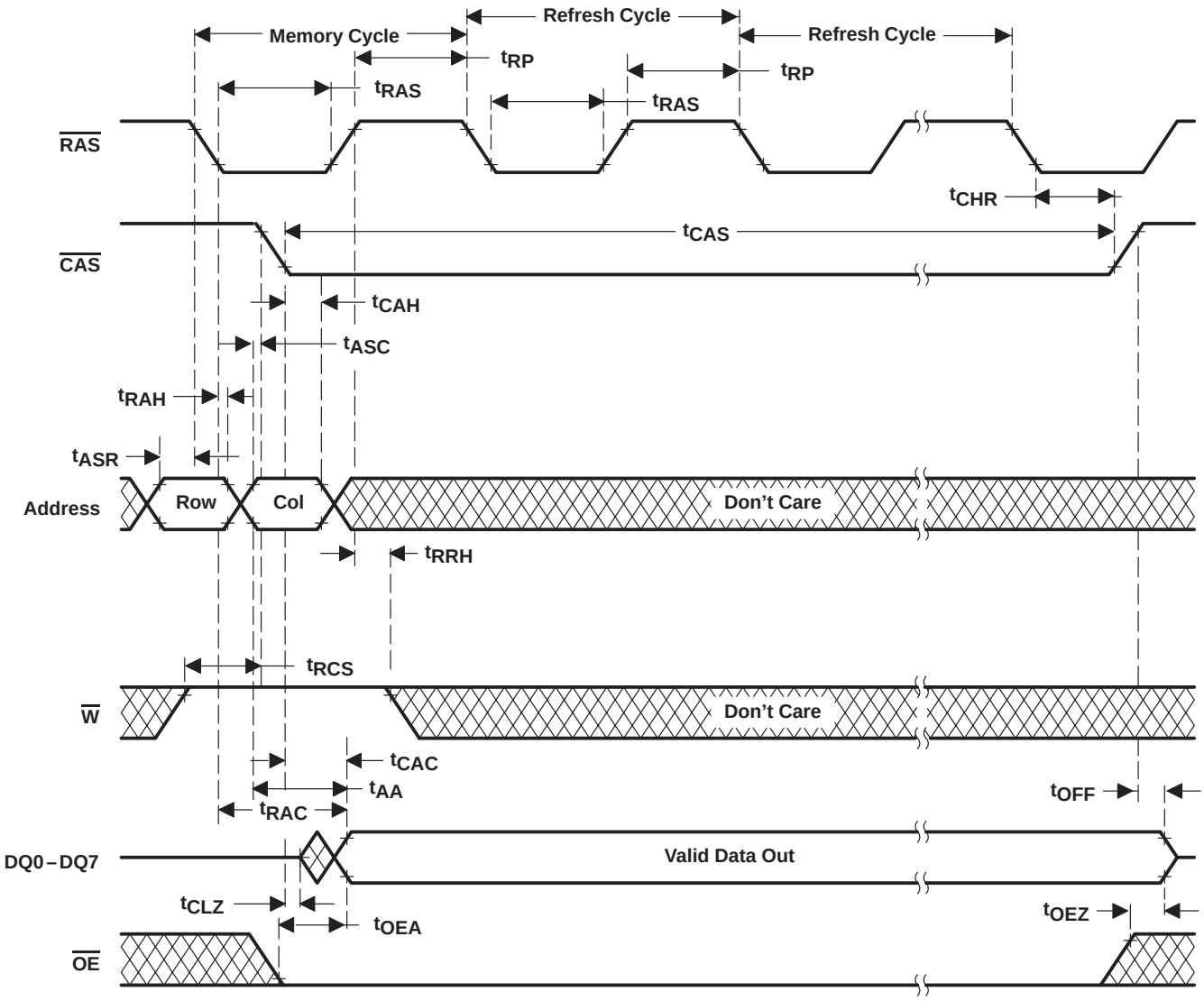


Figure 12. Hidden-Refresh-Cycle (Read) Timing

PARAMETER MEASUREMENT INFORMATION

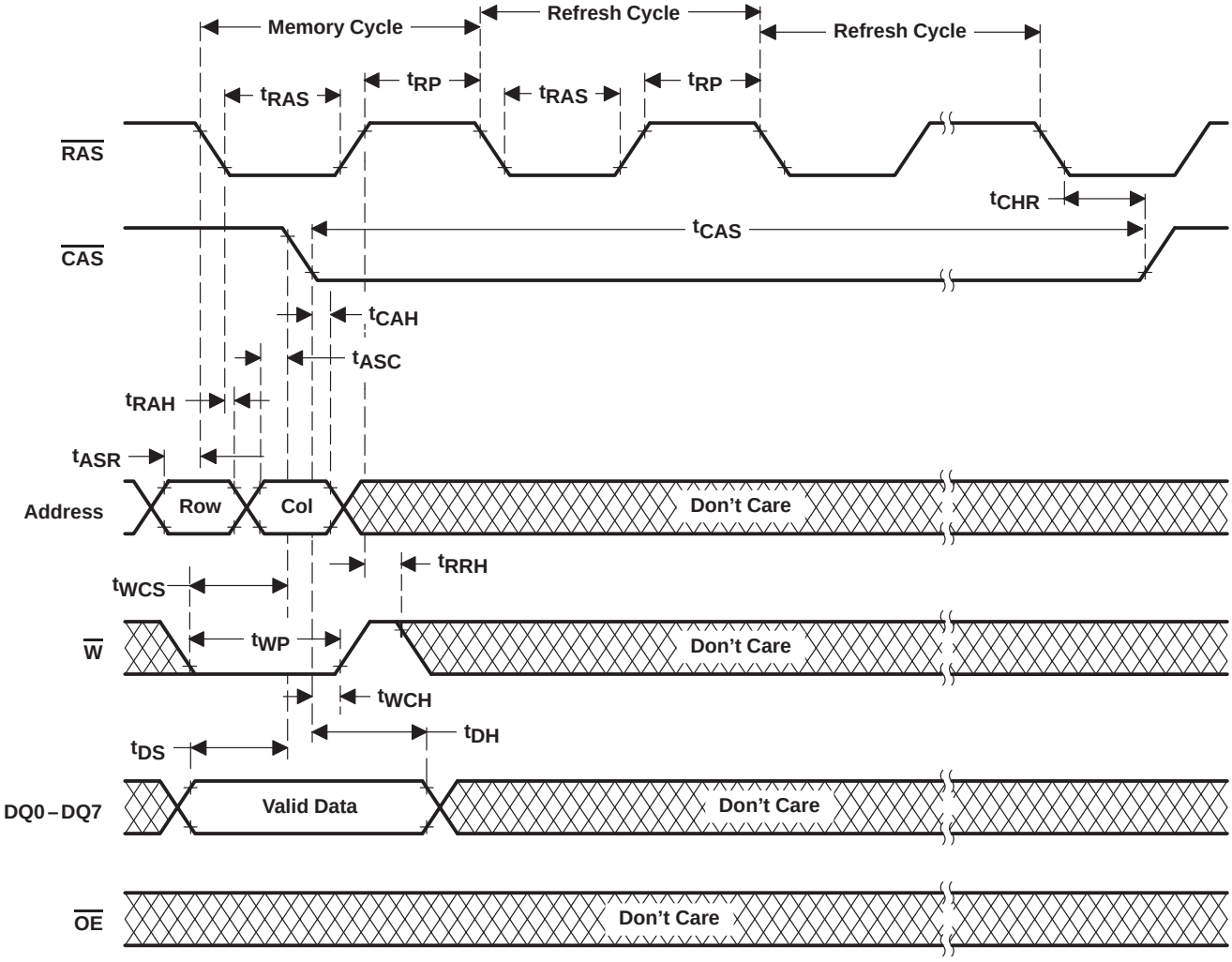
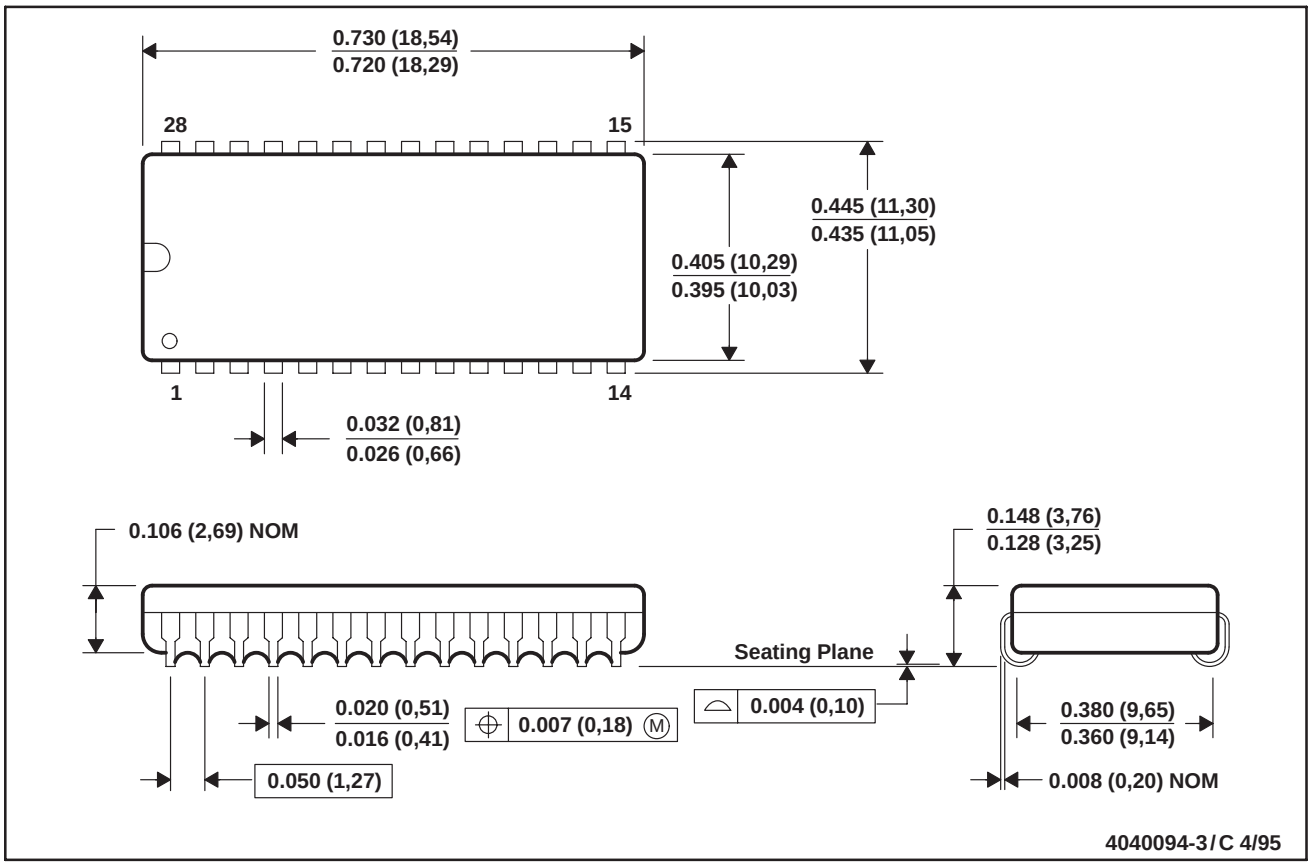


Figure 13. Hidden-Refresh-Cycle (Write) Timing

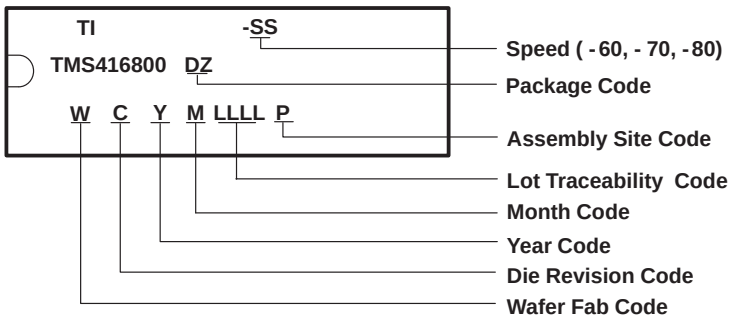
MECHANICAL DATA

DZ (R-PDSO-J28) **PLASTIC SMALL-OUTLINE J-LEAD PACKAGE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Plastic body dimensions do not include mold protrusion. Maximum mold protrusion is 0.005 (0,125).

device symbolization (TMS416800 illustrated)



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