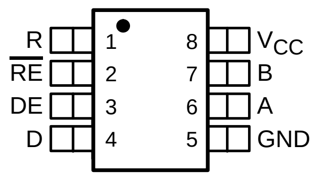
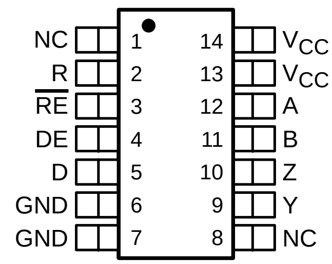
- **Low-Voltage Differential 30-Ω Line Drivers and Receivers for Signaling Rates† up to 100 Mbps**
- **Power Dissipation at 100 Mbps**
  - **Driver: 50 mW Typical**
  - **Receiver: 30 mW Typical**
- **Meets or Exceeds Current Revision of M-LVDS Standard TIA/EIA–899 for Multipoint Data Interchange**
- **Controlled Driver Output Voltage Transition Times for Improved Signal Quality**
- **–1-V to 3.4-V Common-Mode Voltage Range Allows Data Transfer With up to 2 V of Ground Noise**
- **Type-1 Receivers Incorporate 25 mV of Hysteresis**
- **Type-2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions**
- **Operates From a Single 3.3-V Supply**
- **Propagation Delay Times Typically 2.3 ns for Drivers and 5 ns for Receivers**
- **Power-Up/Down Glitch-Free Driver**
- **Driver Handles Operation Into a Continuous Short Circuit Without Damage**
- **Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V**
- **200-Mbps Devices Available (SN65MLVD201, 203, 206, and 207)**

SN65MLVD200D (Marked as MF200)
SN65MLVD204D (Marked as MF204)
(TOP VIEW)



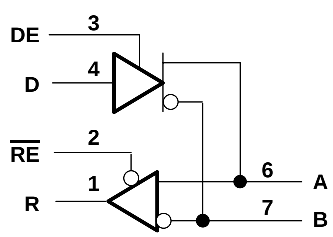
SN65MLVD202D (Marked as MLVD202)
SN65MLVD205D (Marked as MLVD205)
(TOP VIEW)



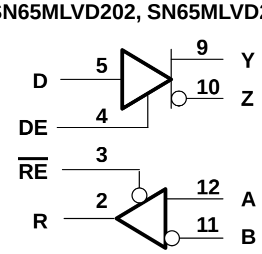
NC – No internal connection

logic diagram (positive logic)

SN65MLVD200, SN65MLVD204



SN65MLVD202, SN65MLVD205



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

†The signaling rate of a line is the number of voltage transitions that are made per second expressed in bps (bits per second) units.

description

This series of SN65MLVD20x devices are low-voltage differential line drivers and receivers complying with the proposed multipoint low-voltage differential signaling (M-LVDS) standard (TIA/EIA–899). These circuits are similar to their TIA/EIA-644 standard compliant LVDS counterparts, with added features to address multipoint applications. Driver output current has been increased to support doubly-terminated, 50-Ω load multipoint applications. Driver output slew rates are optimized for signaling rates up to 100 Mbps.

Types 1 and 2 receivers are available. Both types of receivers operate over a common-mode voltage range of –1 V to 3.4 V to provide increased noise immunity in harsh electrical environments. Type-1 receivers have their differential input voltage thresholds near zero volts (±50 mV), and include 25 mV of hysteresis to prevent output oscillations in the presence of noise. Type-2 receivers include an offset threshold to detect open-circuit, idle-bus, and other fault conditions, and provide a known output state under these conditions.

The intended application of these devices is in half-duplex or multipoint baseband data transmission over controlled impedance media of approximately 100-Ω characteristic impedance. The transmission media may be printed circuit board traces, backplanes, or cables. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other application-specific characteristics).

These devices are characterized for operation from –40°C to 85°C.

AVAILABLE OPTIONS

NOMINAL SIGNALING RATE, Mbps	FOOTPRINT	RECEIVER TYPE	PART NUMBER†
100	SN75176	Type 1	SN65MLVD200D
100	SN75ALS180	Type 1	SN65MLVD202D
100	SN75176	Type 2	SN65MLVD204D
100	SN75ALS180	Type 2	SN65MLVD205D

† The D package is available taped and reeled. Add the R suffix to the device type (e.g., SN65MLVD200DR)

Function Tables

TYPE-1 RECEIVER (200, 202)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 50$ mV	L	H
-50 mV $< V_{ID} < 50$ mV	L	?
$V_{ID} \leq -50$ mV	L	L
X	H	Z
X	Open	Z
Open Circuit	L	?

TYPE-2 RECEIVER (204, 205)

INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
$V_{ID} \geq 150$ mV	L	H
50 mV $< V_{ID} < 150$ mV	L	?
$V_{ID} \leq 50$ mV	L	L
X	H	Z
X	Open	Z
Open Circuit	L	L

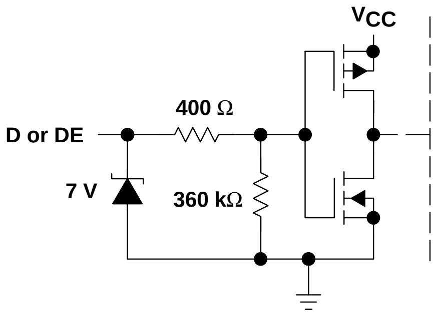
DRIVER

INPUT	ENABLE	OUTPUTS	
D	DE	A OR Y	B OR Z
L	H	L	H
H	H	H	L
OPEN	H	L	H
X	OPEN	Z	Z
X	L	Z	Z

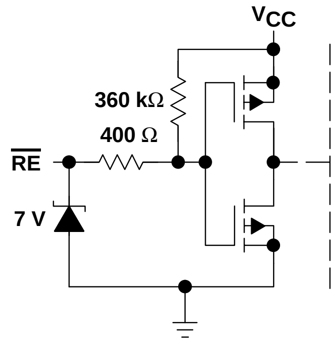
H = high level, L = low level, Z = high impedance, X = Don’t care, ? = indeterminate

equivalent input and output schematic diagrams

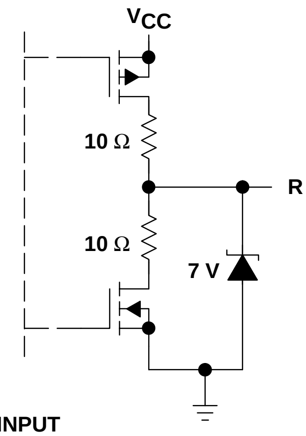
DRIVER INPUT AND DRIVER ENABLE



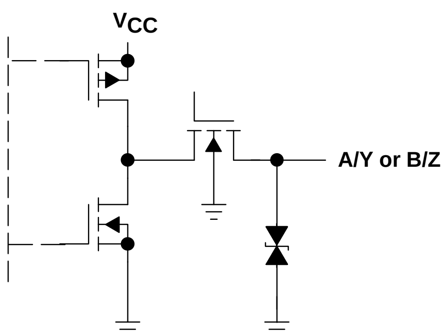
RECEIVER ENABLE



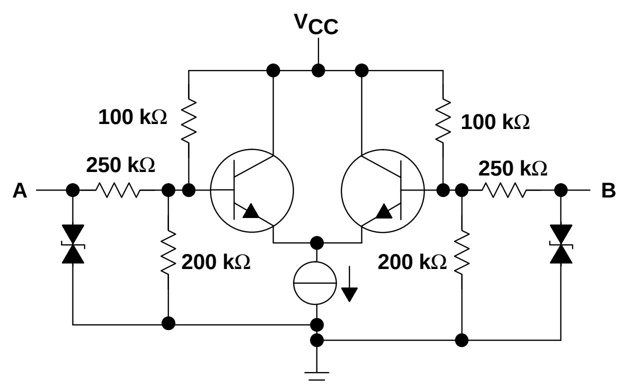
RECEIVER OUTPUT



DRIVER OUTPUT



RECEIVER INPUT



absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1) . . . . –0.5 V to 4 V
Input voltage range: D, DE, $\overline{RE}$ . . . . –0.5 V to 4 V
A, B (200, 204) . . . . –1.8 V to 4 V
A, B (202, 205) . . . . –4 V to 6 V
Output voltage range: R . . . . –0.3 V to 4 V
Y, Z, A, or B . . . . –1.8 V to 4 V
Electrostatic discharge: Human body model (see Note 2) A, B, Y, or Z . . . . ±3 kV
All pins . . . . ±2 kV
Charged-device model (see Note 3) All pins . . . . ±500 V
Continuous power dissipation . . . . (see Dissipation Rating table)
Storage temperature range . . . . –65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds . . . . 260°C

† Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
2. Tested in accordance with JEDEC Standard 22, Test Method A114-A.
3. Tested in accordance with JEDEC Standard 22, Test Method C101.

DISSIPATION RATING

PACKAGE	$T_A \le 25°C$ POWER RATING	OPERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
D(8)	725 mW	5.8 mW/°C	377 mW
D(14)	950 mW	7.6 mW/°C	494 mW

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	3	3.3	3.6	V
High-level input voltage, V_{IH}	2		V_{CC}	V
Low-level input voltage, V_{IL}	0		0.8	V
Magnitude of differential input voltage, $\lvert V_{ID} \rvert$	0.05		V_{CC}	V
Voltage at any bus terminal, V_A, V_Y, V_Z, or V_B	–1.4		3.8	V
Common-mode input voltage V_{CM}, $(V_A + V_B)/2$	–1		3.4	V
Receiver load capacitance, C_L	5		15	pF
Operating free-air temperature, T_A	–40		85	°C

device electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN†	TYP‡	MAX	UNIT
I_{CC}	Supply current	Receiver disabled and driver enabled	$\overline{RE}$ and DE at V_{CC}, R_L = 50 Ω, All others open		13	22	mA
		Driver and receiver disabled	$\overline{RE}$ at V_{CC}, DE at 0 V, R_L = No load, All others open		1	7	
		Receiver enabled and driver enabled	$\overline{RE}$ at 0 V, DE at V_{CC}, R_L = 50 Ω, All others open, No receiver load		16	26	
		Receiver enabled and driver disabled	$\overline{RE}$ at 0 V, DE at 0 V, All others open, No receiver load		4	11	

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
‡ All typical values are at 25°C and with a 3.3-V supply voltage.

driver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN†	TYP‡	MAX	UNIT
$\lvert V_{AB}\rvert$ or $\lvert V_{YZ}\rvert$	Differential output voltage magnitude	See Figure 2	480		650	mV
$\Delta\lvert V_{AB}\rvert$ or $\Delta\lvert V_{YZ}\rvert$	Change in differential output voltage magnitude between logic states	See Figure 2	–50		50	mV
$V_{OS(SS)}$	Steady-state common-mode output voltage	See Figure 3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in steady-state common-mode output voltage between logic states		–50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage				150	mV
$V_{A(OC)}$ or $V_{Y(OC)}$	Maximum steady-state open-circuit output voltage	See Figure 7	0		2.4	V
$V_{B(OC)}$ or $V_{Z(OC)}$	Maximum steady-state open-circuit output voltage		0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	See Figure 5			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output		$-0.2V_{SS}$			V
I_{IH}	High-level input current	V_{IH} = 2 V	0		10	µA
I_{IL}	Low-level input current	V_{IL} = 0.8 V	0		10	µA
I_{OS}	Differential short-circuit output current	See Figure 4			24	mA
I_{OZ}	High-impedance state output current (driver only)	$-1.4 V \le (V_Y \text{ or } V_Z) \le 3.8 V$, Other output at 1.2 V	–15		10	µA
$I_{O(OFF)}$	Power-off output current (driver only)	$-1.4 V \le (V_Y \text{ or } V_Z) \le 3.8 V$, $V_{CC} \le 1.5 V$, Other output at 1.2 V	–10		10	µA

† The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
‡ All typical values are at 25°C and with a 3.3-V supply voltage.

receiver electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold	Type 1	See Figure 8, Table 1 and Table 2			50	mV
		Type 2				150	
V_{IT-}	Negative-going differential input voltage threshold	Type 1		–50			mV
		Type 2		50			
$V_{ID(HYS)}$	Differential input voltage hysteresis, $V_{IT+} - V_{IT-}$	Type 1			25		mV
		Type 2			0		
V_{OH}	High-level output voltage		I_{OH} = –8 mA	2.4			V
V_{OL}	Low-level output voltage		I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current		V_{IH} = 2 V	–10		0	μA
I_{IL}	Low-level input current		V_{IL} = 0.8 V	–10		0	μA
I_{OZ}	High-impedance output current		V_O = 0 V or 3.6 V	–10		15	μA

† All typical values are at 25°C and with a 3.3-V supply voltage.

bus input and output electrical characteritics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_A	Receiver input or transceiver input/output current	V_A = 3.8 V, V_B = 1.2 V	0		32	μA
		V_A = 0 V or 2.4 V, V_B = 1.2 V	–20		20	
		V_A = –1.4 V, V_B = 1.2 V	–32		0	
I_B	Receiver input or transceiver input/output current	V_B = 3.8 V, V_A = 1.2 V	0		32	μA
		V_B = 0 V or 2.4 V, V_A = 1.2 V	–20		20	
		V_B = –1.4 V, V_A = 1.2 V	–32		0	
I_{AB}	Receiver input or transceiver input/output differential current ($I_A - I_B$)	$V_A = V_B$, $-1.4 \le V_A \le 3.8$ V	–4		4	μA
$I_{A(OFF)}$	Receiver input or transceiver input/output power-off current	V_A = 3.8 V, V_B = 1.2 V, $V_{CC} \le 1.5$ V	0		32	μA
		V_A = 0 V or 2.4 V, V_B = 1.2 V, $V_{CC} \le 1.5$ V	–20		20	
		V_A = –1.4 V, V_B = 1.2 V, $V_{CC} \le 1.5$ V	–32		0	
$I_{B(OFF)}$	Receiver input or transceiver input/output power-off current	V_B = 3.8 V, V_A = 1.2 V, $V_{CC} \le 1.5$ V	0		32	μA
		V_B = 0 V or 2.4 V, V_A = 1.2 V, $V_{CC} \le 1.5$ V	–20		20	
		V_B = –1.4 V, V_A = 1.2 V, $V_{CC} \le 1.5$ V	–32		0	
$I_{AB(OFF)}$	Receiver input or transceiver input/output power-off differential current ($I_A - I_B$)	$V_A = V_B$, $-1.4 \le V_A \le 3.8$ V, $V_{CC} \le 1.5$ V	–4		4	μA
C_A	Receiver input, driver high-impedance output, or transceiver input/output capacitance	V_A = 0.4 sin(2E8πt) +0.5, V_B = 1.2 V		3		pF
C_B		V_B = 0.4 sin(2E8πt) +0.5, V_A = 1.2 V		3		pF

† All typical values are at 25°C and with a 3.3-V supply voltage.

driver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 5	1.6	2.3	4.1	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1.6	2.3	4.1	ns
t_r	Differential output signal rise time		1.5	2	3	ns
t_f	Differential output signal fall time		1.5	2	3	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)			30		ps
$t_{sk(pp)}$	Part-to-part skew (see Note 4)				900	ps
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	See Figure 6	1.5	3.7	6.5	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output		1.5	3.7	6.5	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output		1.3	3.5	6.8	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output		1.8	3.5	6.1	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) (see Notes 5 and 6)	50-MHz clock input (see Figure 8)		23		ps
$t_{jit(cc)}$	Cycle-to-cycle jitter, peak (see Notes 5 and 6)	50-MHz clock input (see Figure 8)		180		ps
$t_{jit(pp)}$	Peak-to-peak jitter, (see Notes 5, 7, and 8)	100 Mbps 2^{15}–1 PRBS input (see Figure 8)		210		ps

† All typical values are at 25°C and with a 3.3-V supply voltage.

NOTES:
4. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
5. Jitter parameters are based on design and characterization. Stimulus system jitter of 11 ps $t_{jit(per)}$, 43 ps $t_{jit(cc)}$, or 54 ps $t_{jit(pp)}$ have been subtracted from the values.
6. Input voltage = 0 V to V_{CC}, $t_r = t_f \leq 1$ ns (20% to 80%), measured over 30k samples.
7. Input voltage = 0 V to V_{CC}, $t_r = t_f \leq 1$ ns (20% to 80%), measured over 100k samples.
8. Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

receiver switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 5 pF, See Figure 10		3	5	6.7	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3	4.6	6.7	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				400		ps
$t_{sk(pp)}$	Part-to-part skew (see Note 9)					1.5	ns
t_r	Output signal rise time			0.8	1.4	2	ns
t_f	Output signal fall time			0.8	1.5	2	ns
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, See Figure 10		3.4	5.8	9	ns
t_{PHL}	Propagation delay time, high-to-low-level output			3.4	5.4	9	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)				400		ps
$t_{sk(pp)}$	Part-to-part skew (see Note 9)					2.5	ns
t_r	Output signal rise time			1	2	2.6	ns
t_f	Output signal fall time			1	1.4	2.6	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 11		4.5	6	15	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output			2	3.4	5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output			3.5	9.8	15	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output			4	8.7	15	ns
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) (see Notes 10 and 11)	50-MHz clock input (see Figure 12)	Type 1		10		ps
			Type 2		10		
$t_{jit(cc)}$	Cycle-to-cycle jitter, peak (see Notes 10 and 11)	50-MHz clock input (see Figure 12)	Type 1		93		ps
			Type 2		86		
$t_{jit(pp)}$	Peak-to-peak jitter, (see Notes 10, 12, and 13)	100 Mbps 2^{15}–1 PRBS input (see Figure 12)	Type 1		850		ps
			Type 2		790		

† All typical values are at 25°C and with a 3.3-V supply voltage.

NOTES: 9. $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

10. Jitter parameters are based on design and characterization. Stimulus system jitter of 11 ps $t_{jit(per)}$, 43 ps $t_{jit(cc)}$, or 54 ps $t_{jit(pp)}$ have been subtracted from the values.

11. Differential input voltage = 250 $mV_{p–p}$ (Type 1) or 500 $mV_{p–p}$ (Type 2), V_{CM} = 1 V, $t_r = t_f \le 1$ ns (20% to 80%), measured over 30k samples.

12. Differential input voltage = 250 $mV_{p–p}$ (Type 1) or 500 $mV_{p–p}$ (Type 2), V_{CM} = 1 V, $t_r = t_f \le 1$ ns (20% to 80%), measured over 100k samples.

13. Peak-to-peak jitter includes jitter due to pulse skew ($t_{sk(p)}$).

PARAMETER MEASUREMENT INFORMATION

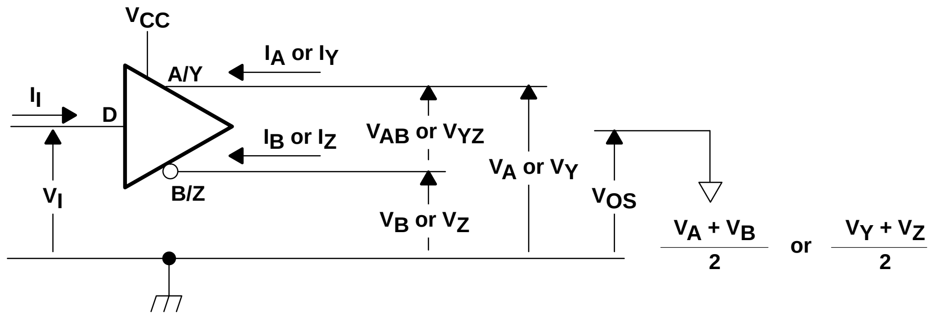
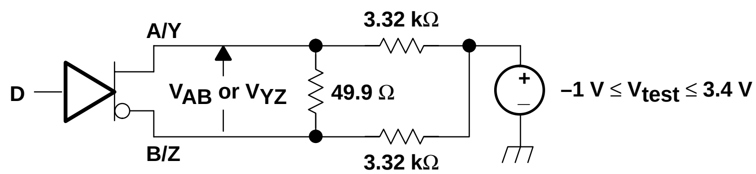
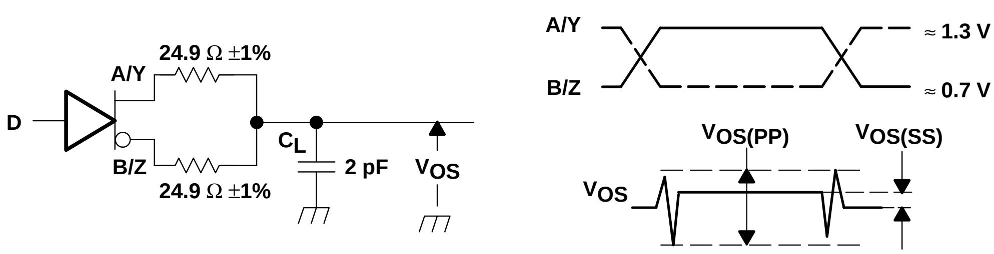


Figure 1. Driver Voltage and Current Definitions



NOTE: All resistors are 1% tolerance.

Figure 2. Differential Output Voltage Test Circuit



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤1 ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OS(PP)}$ is made on test equipment with a –3-dB bandwidth of at least 1 GHz.

Figure 3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

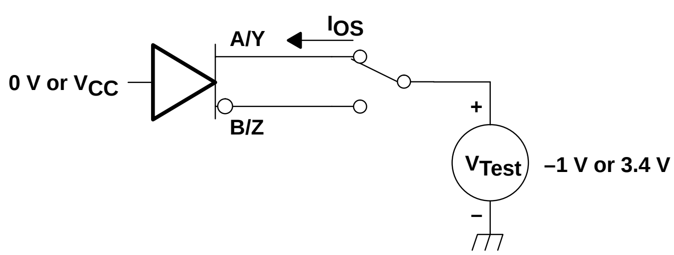
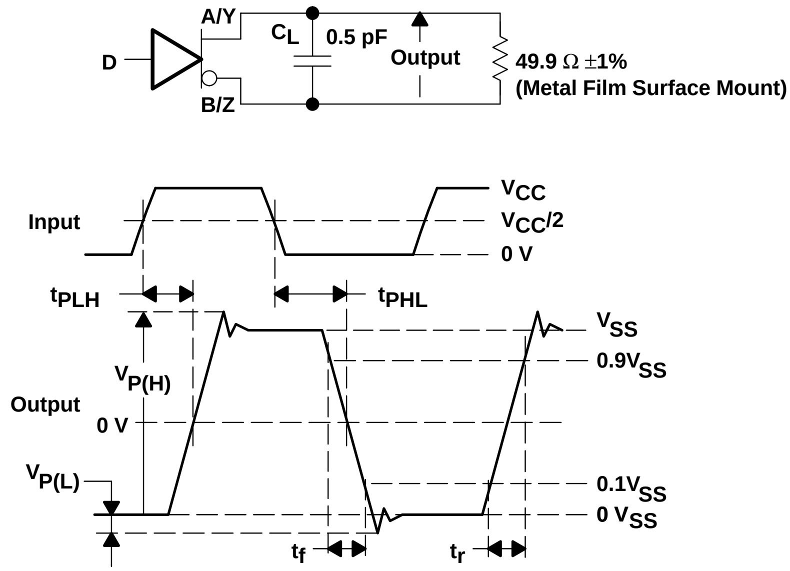


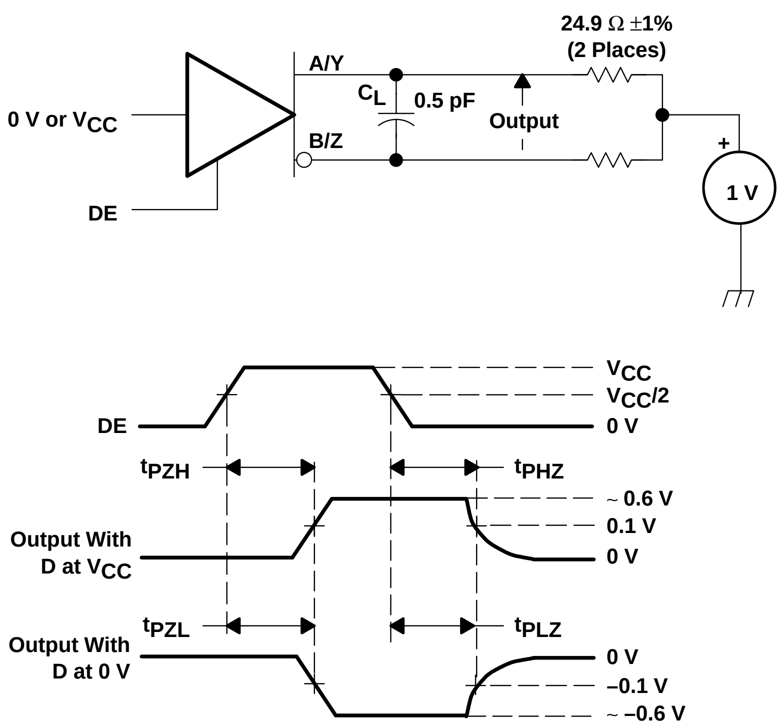
Figure 4. Driver Short-Circuit Test Circuit

PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ±0.05 µs. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤1 ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 6. Driver Enable and DIsable Time Circuit and Definitions

PARAMETER MEASUREMENT INFORMATION

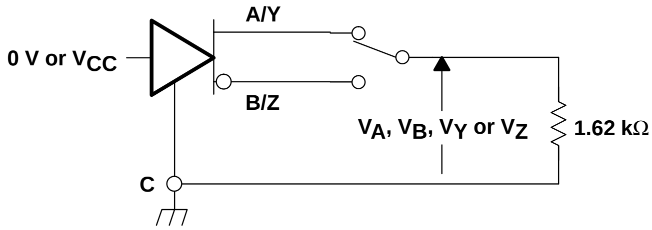
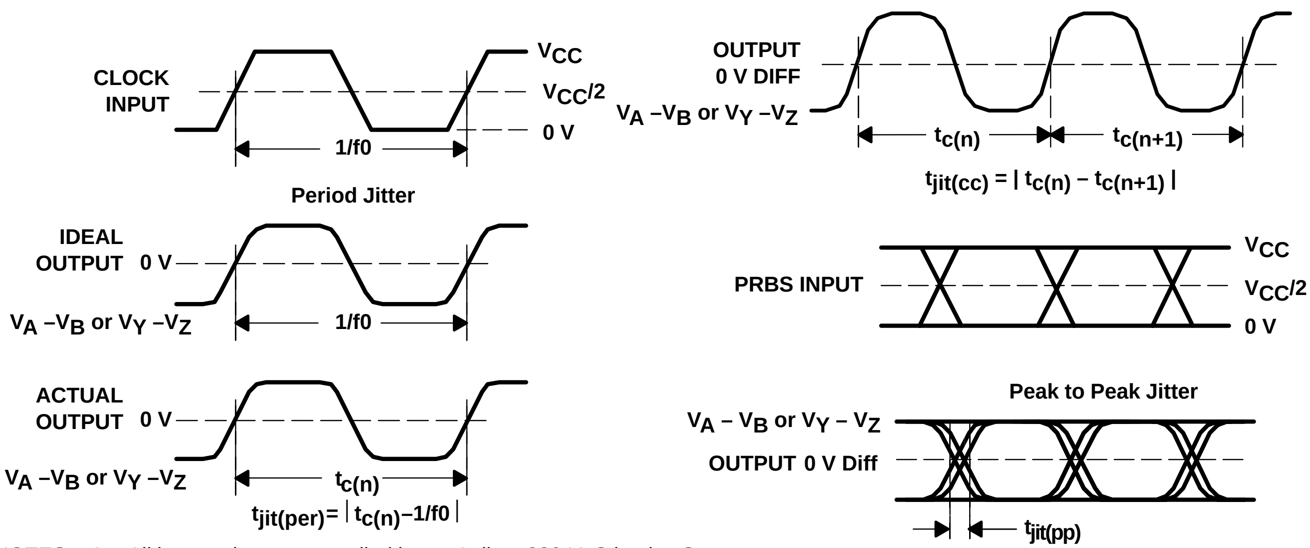


Figure 7. Maximum Steady-State Output Voltage Test Circuit



NOTES: A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200Mbps 2^{15}–1 PRBS input.

Figure 8. Driver Jitter Measurement Waveforms

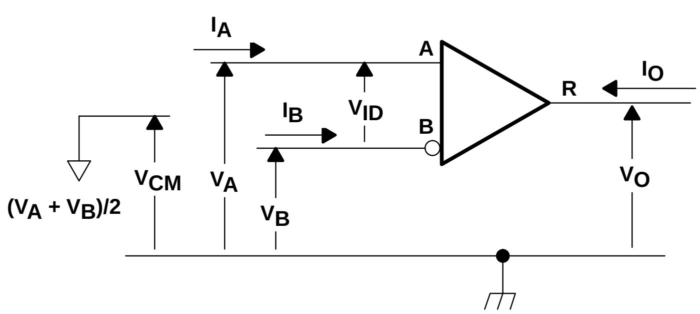


Figure 9. Receiver Voltage and Current Definitions

PARAMETER MEASUREMENT INFORMATION

Table 1. Type-1 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT
V_A	V_B	V_{ID}	V_{CM}	V_O
3.425 V	3.375 V	50 mV	3.4 V	H
3.375 V	3.425 V	–50 mV	3.4 V	L
–0.975 V	–1.025 V	50 mV	–1.0 V	H
–1.025 V	–0.975 V	–50 mV	–1.0 V	L
3.800 V	3.000 V	800 mV	3.4 V	H
3.000 V	3.800 V	–800 mV	3.4 V	L
–0.600 V	–1.400 V	800 mV	–1.0 V	H
–1.400 V	–0.600 V	–800 mV	–1.0 V	L

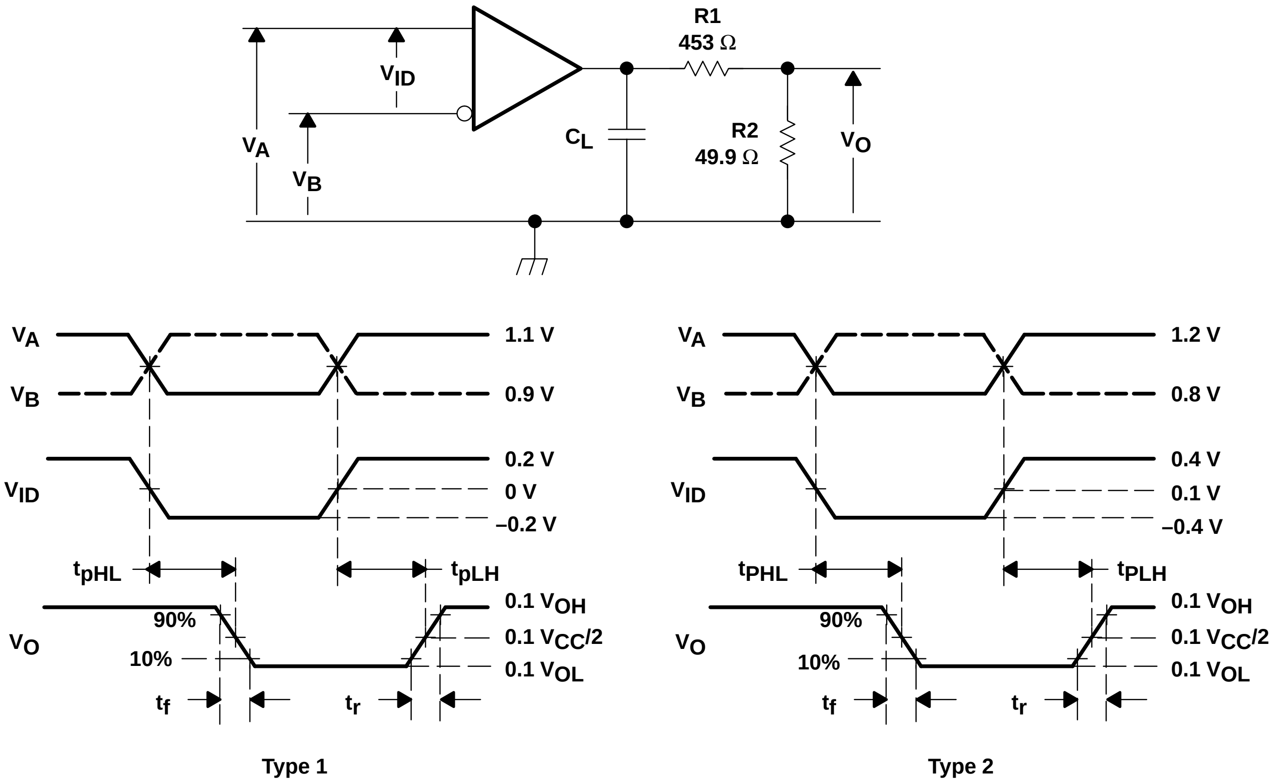
NOTE: H= high level, L = low level. Output state assumes receiver is enabled ($\overline{RE}$ is Low).

Table 2. Type-2 Receiver Input Threshold Test Voltages

APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON–MODE INPUT VOLTAGE	RECEIVER OUTPUT
V_A	V_B	V_{ID}	V_{CM}	V_O
3.475 V	3.325 V	150 mV	3.4 V	H
3.425 V	3.375 V	50 mV	3.4 V	L
–0.925 V	–1.075 V	150 mV	–1.0 V	H
–0.975 V	–1.025 V	50 mV	–1.0 V	L
3.800 V	3.000 V	800 mV	3.4 V	H
3.000 V	3.800 V	–800 mV	3.4 V	L
–0.600 V	–1.400 V	800 mV	–1.0 V	H
–1.400 V	–0.600 V	–800 mV	–1.0 V	L

NOTE: H= high level, L = low level. Output state assumes receiver is enabled ($\overline{RE}$ is Low).

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤1 ns, pulse repetition rate (PRR) = 1 Mpps, pulse width = 0.5 ±0.05 µs.

B. Resistors are 1% tolerance, metal film, and surface mount.

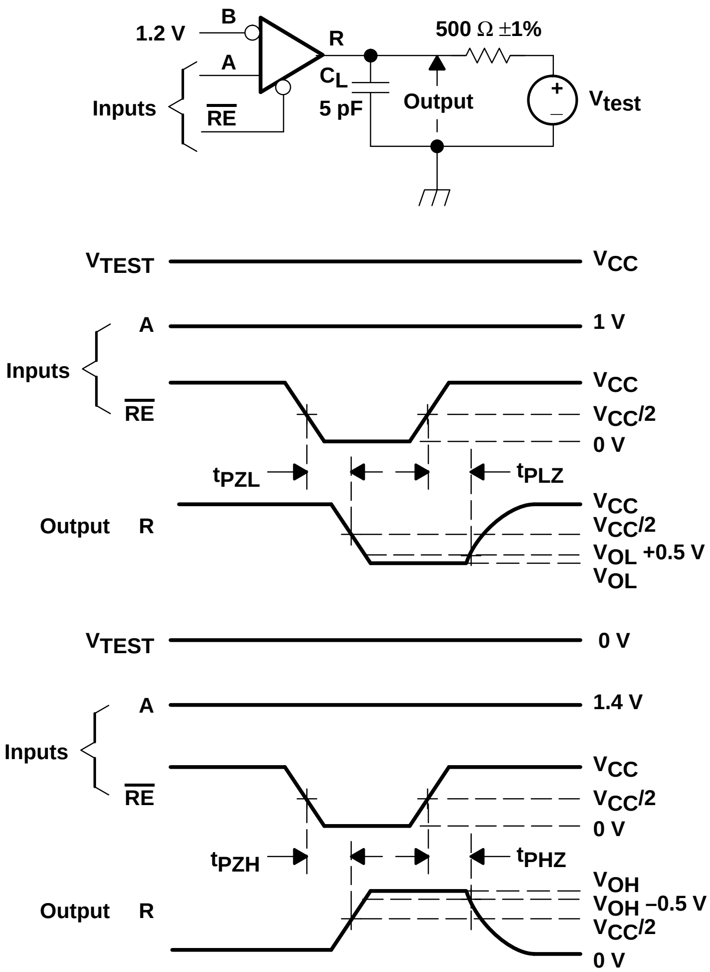
C. C_L is 20% tolerance, low-loss ceramic, and surface mount.

D. R1 and C_L are located within 2 cm of the D.U.T.

E. R2 is located within 15 cm of the D.U.T.

Figure 10. Receiver Timing Test Circuit and Waveforms

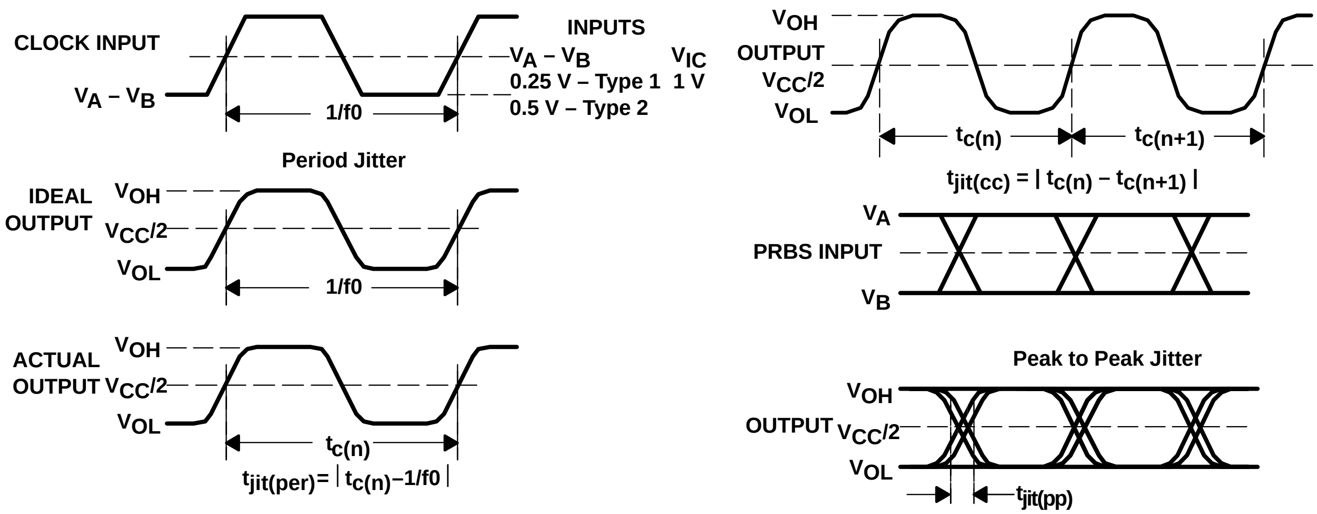
PARAMETER MEASUREMENT INFORMATION



NOTE: All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤1 ns, pulse repetition rate (PRR) = 0.25 Mpps, pulse width = 500 ±10 ns. C_L includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

Figure 11. Receiver Enable/Disable Time Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200Mbps 2^{15}–1 PRBS input.

Figure 12. Receiver Jitter Measurement Waveforms

TYPICAL CHARACTERISTICS

DRIVER LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE

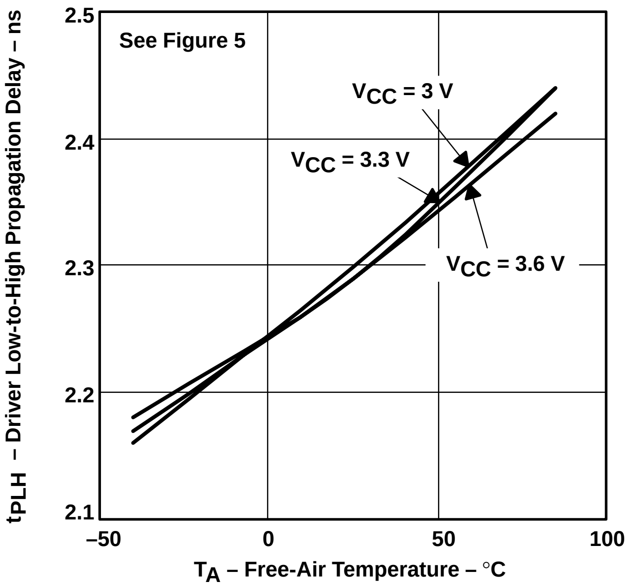


Figure 13

DRIVER HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE

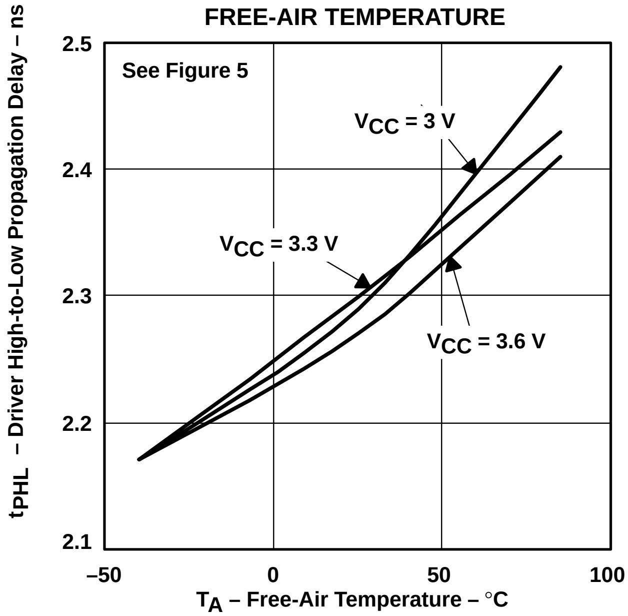


Figure 14

RECEIVER LOW-TO-HIGH PROPAGATION DELAY vs FREE-AIR TEMPERATURE

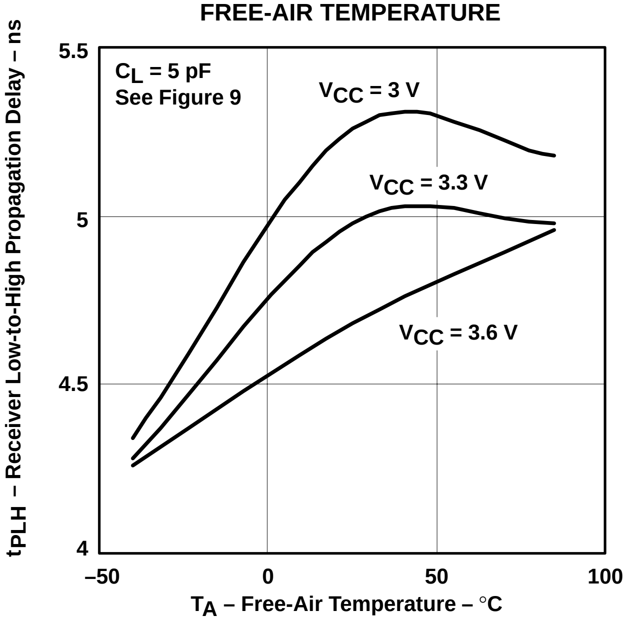


Figure 15

RECEIVER HIGH-TO-LOW PROPAGATION DELAY vs FREE-AIR TEMPERATURE

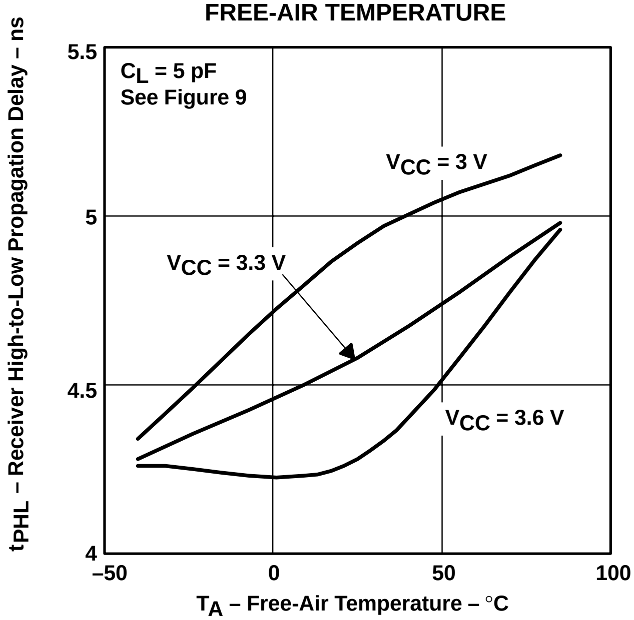


Figure 16

TYPICAL CHARACTERISTICS

DRIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

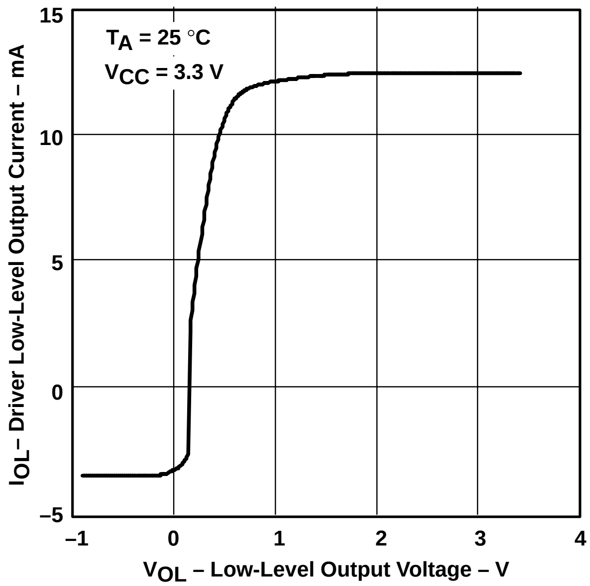


Figure 17

DRIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

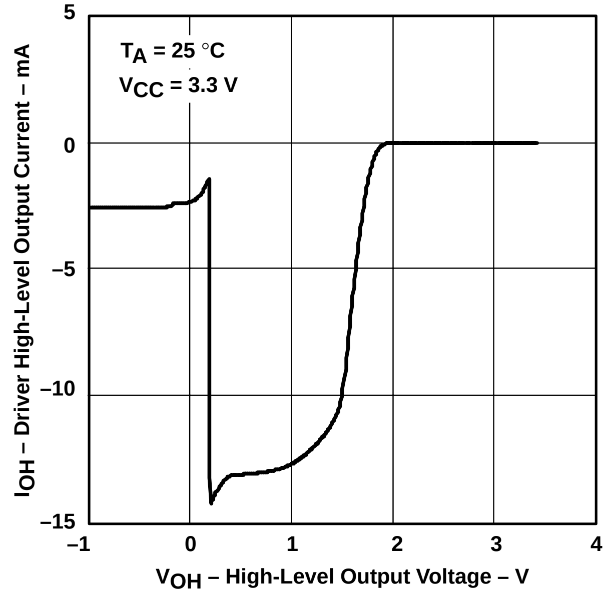


Figure 18

RECEIVER LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

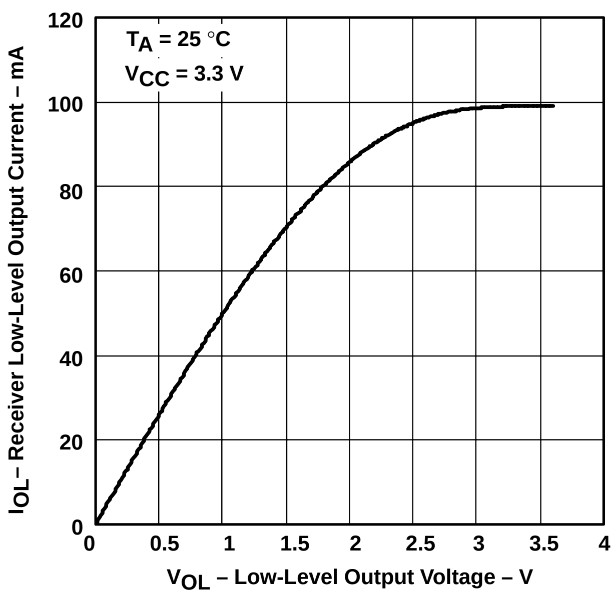


Figure 19

RECEIVER HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

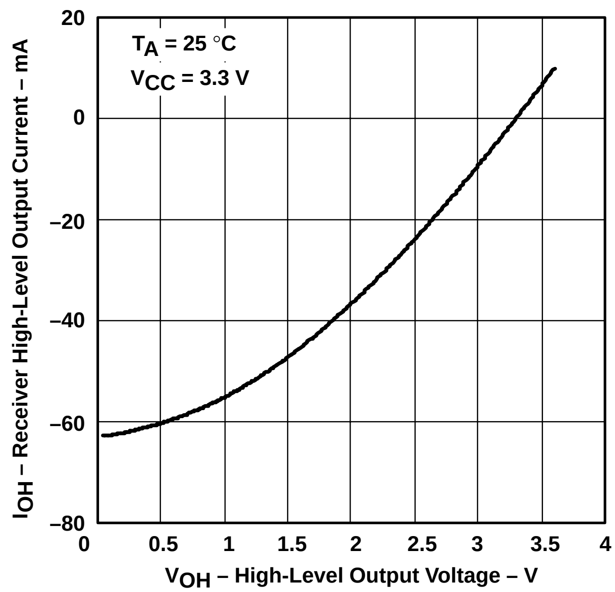


Figure 20

TYPICAL CHARACTERISTICS

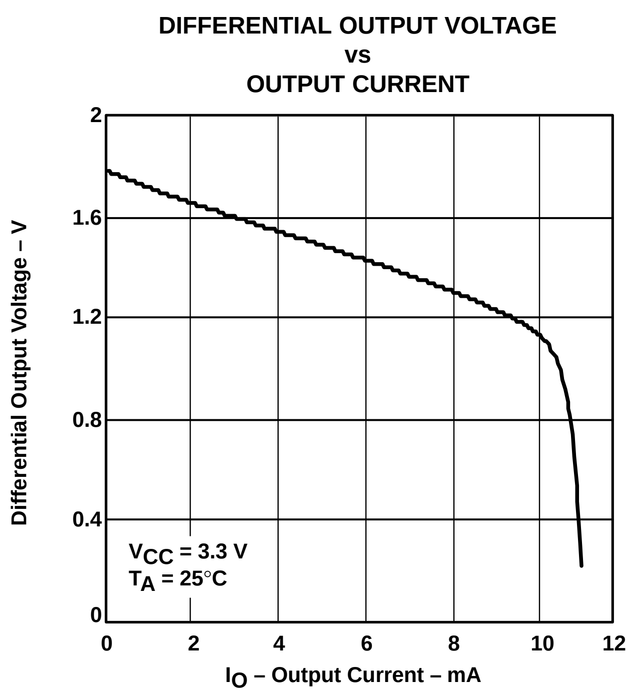


Figure 21

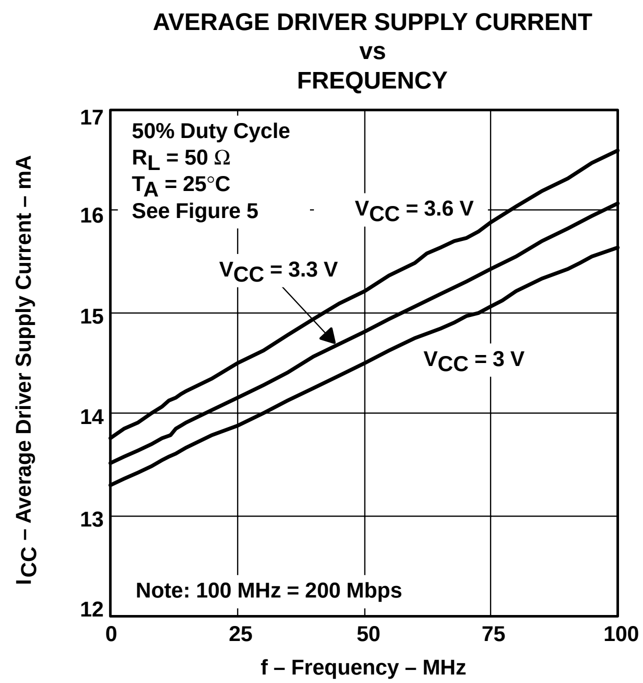


Figure 22

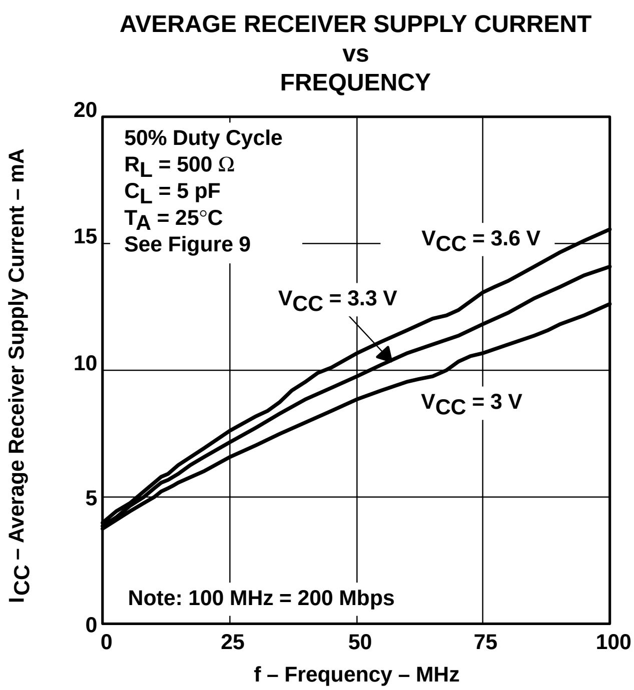


Figure 23

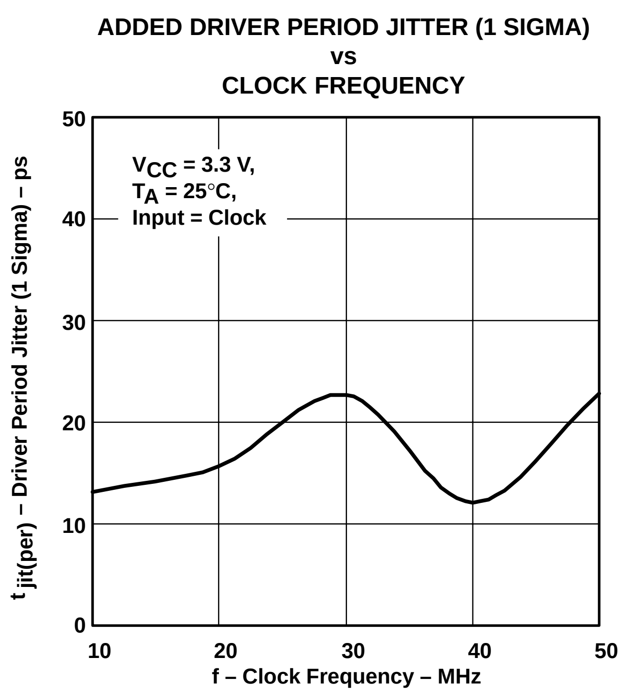


Figure 24

TYPICAL CHARACTERISTICS

ADDED TYPE 1 RECEIVER PERIOD JITTER (1 SIGMA) vs CLOCK FREQUENCY

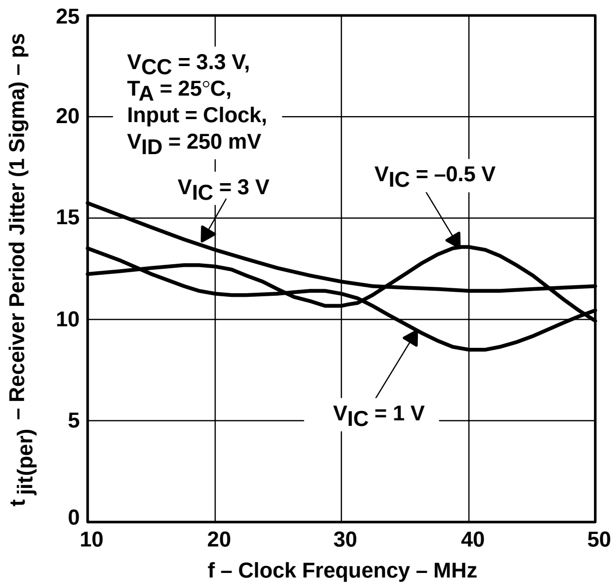


Figure 25

ADDED TYPE 2 RECEIVER PERIOD JITTER (1 SIGMA) vs CLOCK FREQUENCY

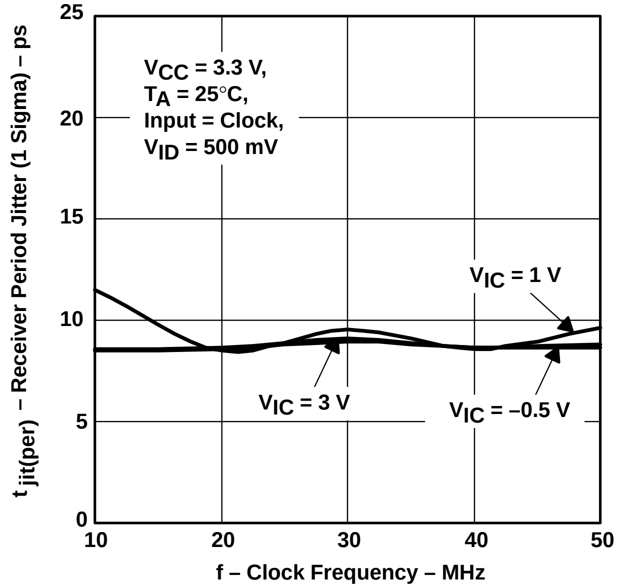


Figure 26

ADDED DRIVER CYCLE-TO-CYCLE JITTER (PEAK) vs CLOCK FREQUENCY

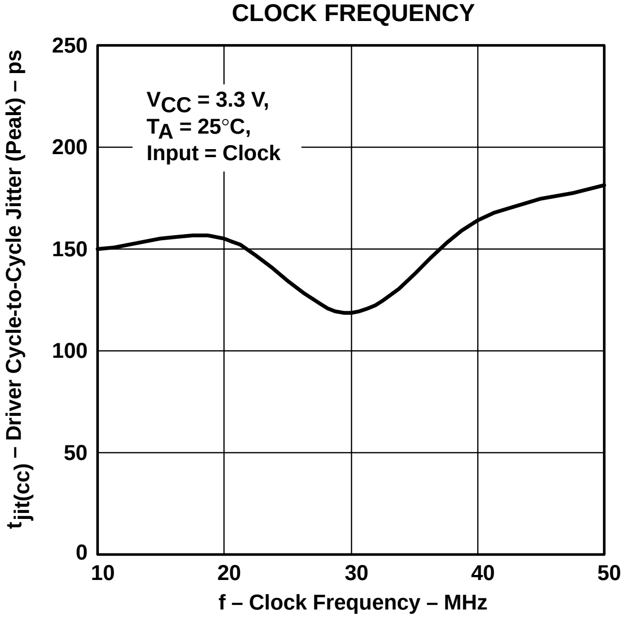


Figure 27

ADDED TYPE 1 RECEIVER CYCLE-TO-CYCLE JITTER (PEAK) vs CLOCK FREQUENCY

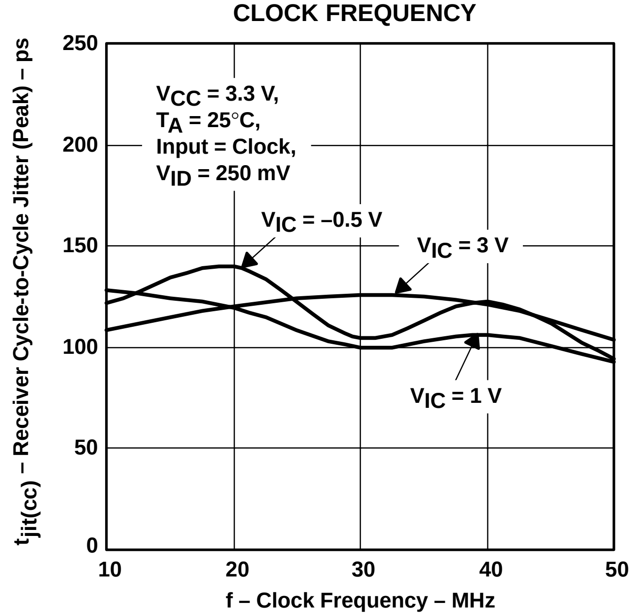


Figure 28

TYPICAL CHARACTERISTICS

ADDED TYPE 2 RECEIVER CYCLE-TO-CYCLE JITTER (PEAK)
vs
CLOCK FREQUENCY

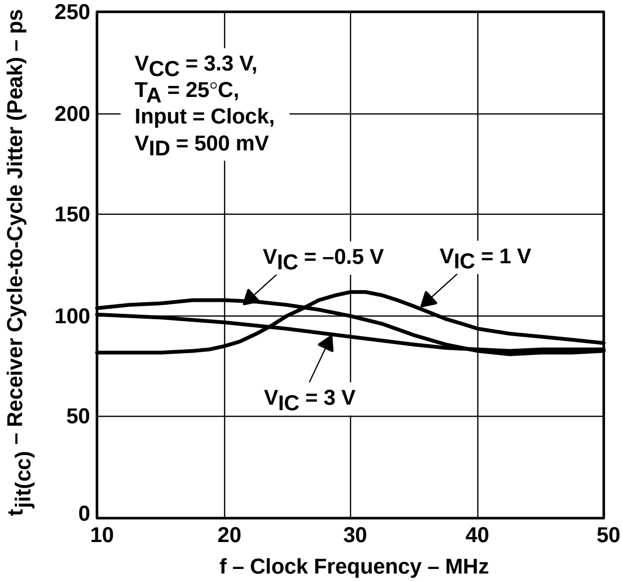


Figure 29

ADDED DRIVER PEAK-TO-PEAK JITTER
vs
DATA RATE

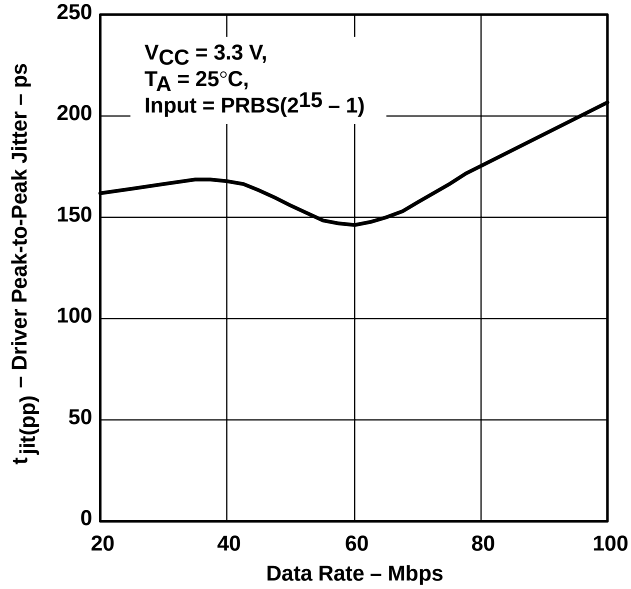


Figure 30

ADDED TYPE 1 RECEIVER PEAK-TO-PEAK JITTER
vs
DATA RATE

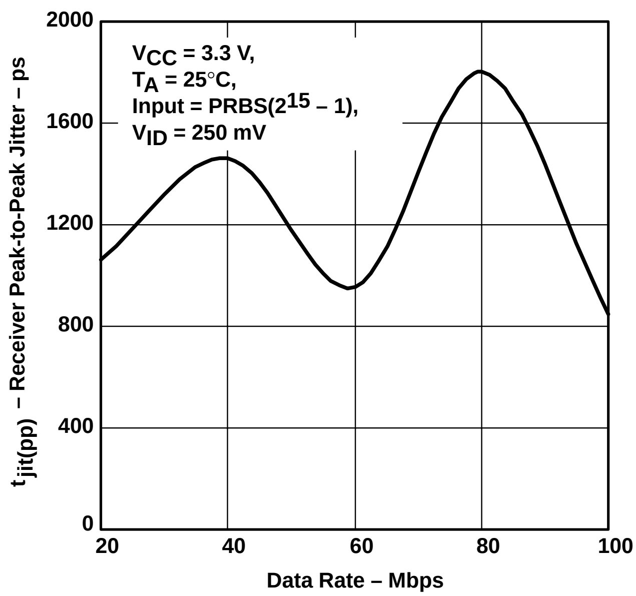


Figure 31

ADDED TYPE 2 RECEIVER PEAK-TO-PEAK JITTER
vs
DATA RATE

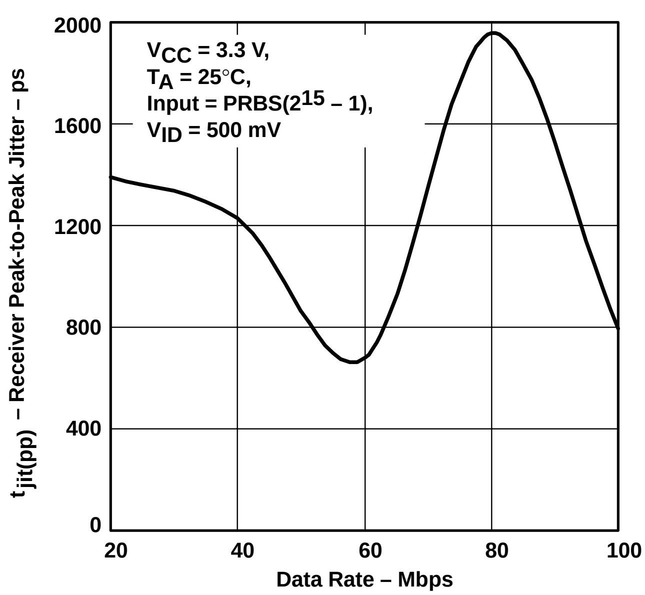


Figure 32

APPLICATION INFORMATION

Type-1 and Type-2 receivers

The M-LVDS standard defines Type-1 and Type-2 receivers. Type-1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. Type-1 receivers maximize the differential noise margin and are intended for maximum signaling rates. Type-2 receivers are intended for control signals and slower signaling rates. The impact on receiver output by the offset input can be seen in Table 3 and Figure 33.

Table 3. M-LVDS Receiver Input Voltage Threshold Requirements

Receiver Type	Output Low	Output High
1	–2.4 V ≤ V_{ID} ≤ –0.05 V	0.05 V ≤ V_{ID} ≤ 2.4 V
2	–2.4 V ≤ V_{ID} ≤ 0.05 V	0.15 V ≤ V_{ID} ≤ 2.4 V

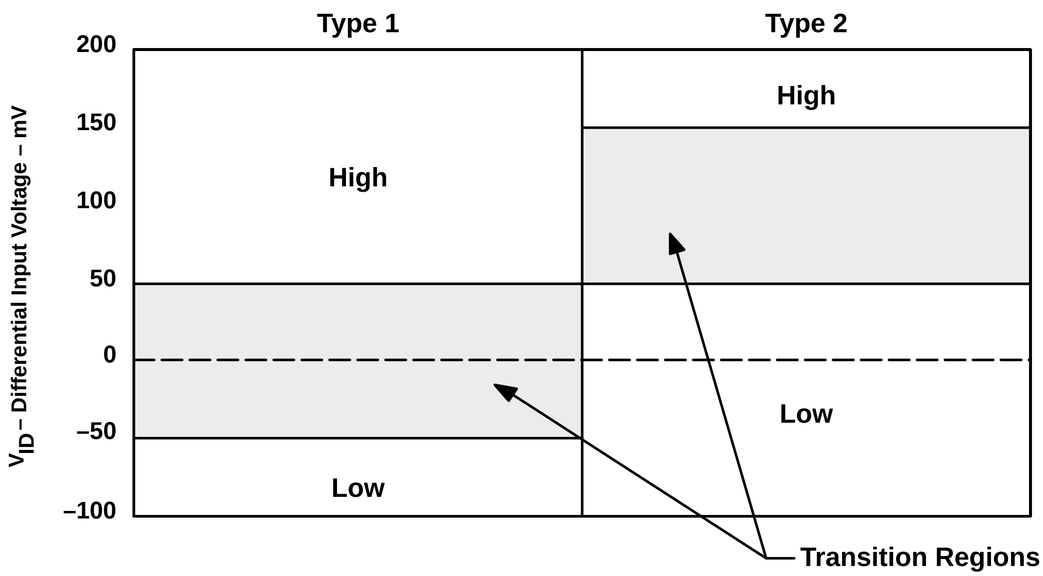


Figure 33. Receiver Differential Input Voltage Showing Transition Region

APPLICATION INFORMATION

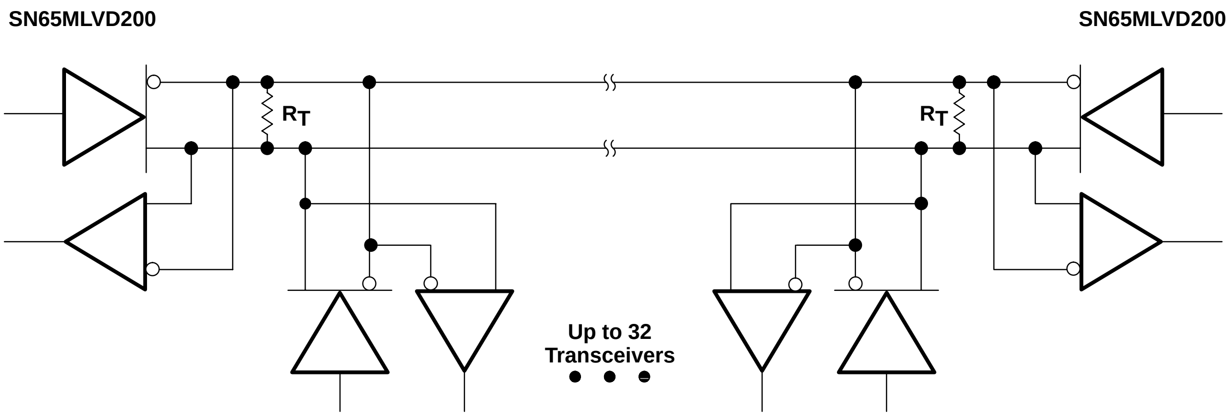
comparison of M-LVDS with RS-485

RS-485 applications are similar to M-LVDS. The two standards define balanced multipoint systems with some basic architecture changes due to the different applications. Table 4 gives a high-level comparison of the two different technologies.

Table 4. Comparison Between M-LVDS and RS-485 Standards

	Number of Loads	Differential Voltage Range	Common-Mode Voltage Range	Maximum Signaling Rate (Mbps)	Receiver Minimum Threshold
RS-485	32	1.5 V to 5 V	–7 V to 12 V	50 Mbps	±200 mV
M-LVDS	32	480 mV to 650 mV	–1 V to 3.4 V	500 Mbps	±50 mV

It can be seen that with the greater differential output voltage and common-mode voltage range of the RS-485-type device, it can handle longer signaling distances where M-LVDS offers ten times the signaling rate of RS-485.



NOTE A: The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 34. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65MLVD200D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DG4	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD200DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD202D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN65MLVD202DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN65MLVD202DRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN65MLVD204D	NRND	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204DR	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD204DRG4	NRND	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65MLVD205D	NRND	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN65MLVD205DR	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM
SN65MLVD205DRG4	NRND	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPD	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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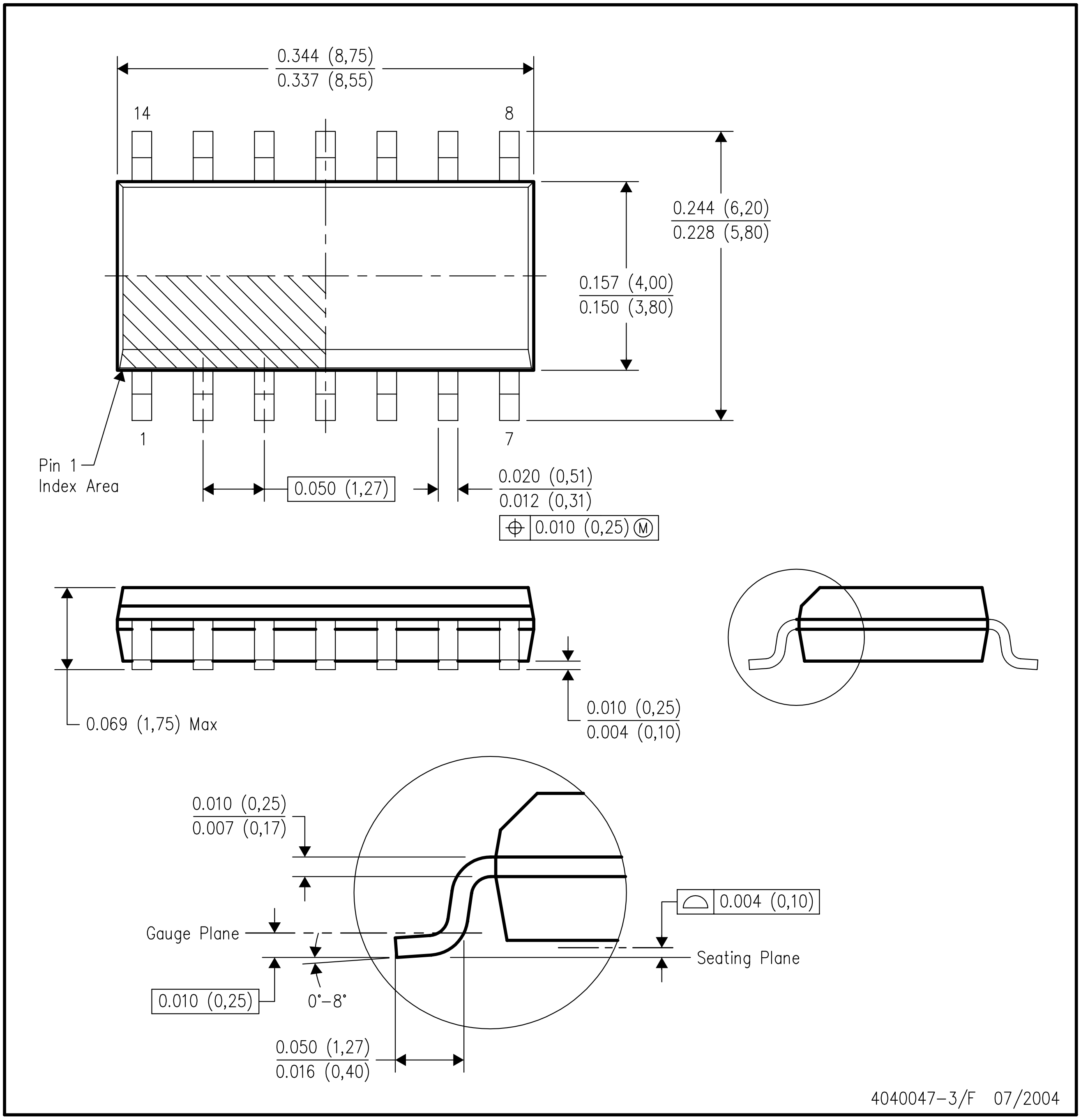
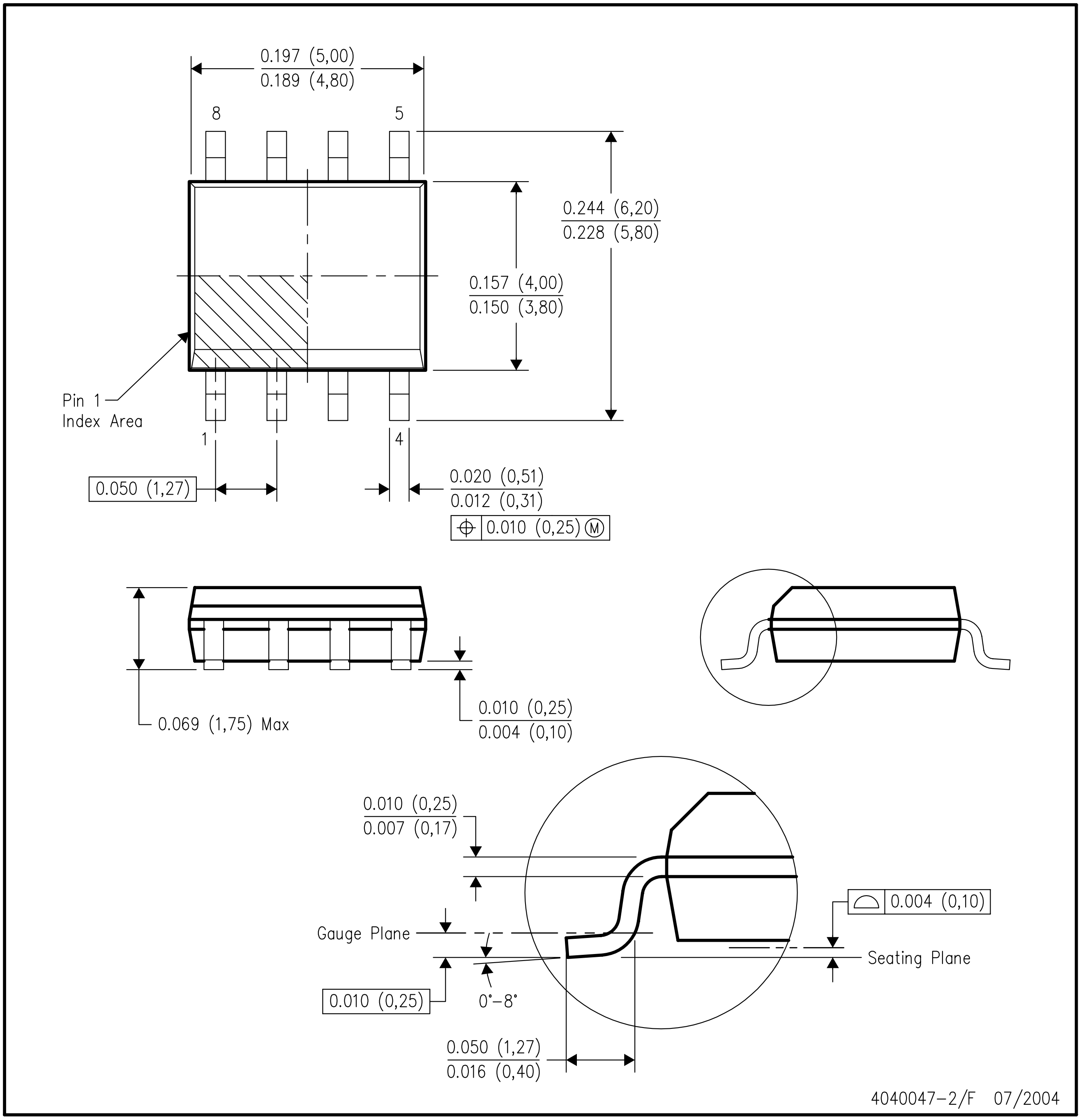
D (R–PDSO–G14) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS–012 variation AB.

D (R-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
- D. Falls within JEDEC MS-012 variation AA.

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