

# 54ABT/74ABT240

## Octal Buffer/Line Driver with TRI-STATE® Outputs

### General Description

The 'ABT240 is an inverting octal buffer and line driver designed to be employed as a memory address driver, clock driver and bus oriented transmitter or receiver which provides improved PC board density.

### Features

- Output sink capability of 64 mA, source capability of 32 mA
- Guaranteed latchup protection
- High impedance glitch free bus loading during entire power up and power down cycle
- Nondestructive hot insertion capability
- Standard Military Drawing (SMD)—5962-9318801

**Ordering Code:** See Section 10

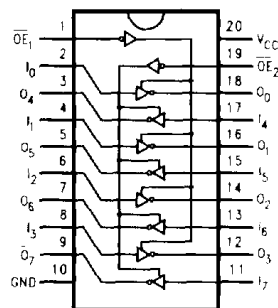
Commercial	Military	Package Number	Package Description
74ABT240CSC (Note 1)		M20B	20-Lead (0.300" Wide) Molded Small Outline, JEDEC
74ABT240CSJ (Note 1)		M20D	20-Lead (0.300" Wide) Molded Small Outline, EIAJ
	54ABT240J/883	J20A	20-Lead Ceramic Dual-In-Line
74ABT240CMSA (Note 1)		MSA20	20-Lead Molded Shrink Small Outline, EIAJ Type II
	54ABT240W/883	W20A	20-Lead Cerpak
	54ABT240E/883	E20A	20-Lead Ceramic Leadless Chip Carrier, Type C
74ABT240CMTC (Notes 1, 2)		MTC20	20-Lead Molded Thin Shrink Small Outline, JEDEC

**Note 1:** Devices also available in 13" reel. Use suffix SCX, SJX, MSAX, and MTCX.

**Note 2:** Contact factory for package availability.

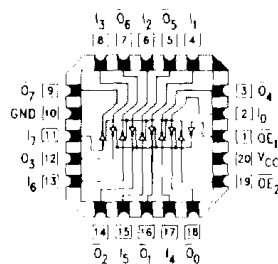
### Connection Diagrams

**Pin Assignment for Flatpak, SSOP and SOIC**



TL/F/11664-1

**Pin Assignment for LCC**



TL/F/11664-2

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	TRI-STATE Output Enable Inputs
$I_0 - I_7$	Inputs
$\overline{O}_0 - \overline{O}_7$	Outputs

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_2$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level    L = LOW Voltage Level    X = Immaterial    Z = High Impedance

## Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	
Ceramic	-55°C to +175°C
Plastic	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State in the HIGH State	-0.5V to 5.5V -0.5V to V <sub>CC</sub>
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)

DC Latchup Source Current (Across Comm Operating Range) -150 mA

Over Voltage Latchup (I/O) 10V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

## Recommended Operating Conditions

Free Air Ambient Temperature	
Military	-55°C to +125°C
Commercial	-40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	( $\Delta V/\Delta t$ )
Data Input	50 mV/ns
Enable Input	20 mV/ns

## DC Electrical Characteristics

Symbol	Parameter	ABT240			Units	V <sub>CC</sub>	Conditions
		Min	Typ	Max			
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA
V <sub>OH</sub>	Output HIGH Voltage	54ABT/74ABT	2.5		V	Min	I <sub>OH</sub> = -3 mA
		54ABT	2.0		V	Min	I <sub>OH</sub> = -24 mA
		74ABT	2.0		V	Min	I <sub>OH</sub> = -32 mA
V <sub>OL</sub>	Output LOW Voltage	54ABT		0.55	V	Min	I <sub>OL</sub> = 48 mA
		74ABT		0.55	V	Min	I <sub>OL</sub> = 64 mA
I <sub>IH</sub>	Input HIGH Current			5 5	μA	Max	V <sub>IN</sub> = 2.7V (Note 2) V <sub>IN</sub> = V <sub>CC</sub>
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7	μA	Max	V <sub>IN</sub> = 7.0V
I <sub>IL</sub>	Input LOW Current			-5 -5	μA	Max	V <sub>IN</sub> = 0.5V (Note 2) V <sub>IN</sub> = 0.0V
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OZH</sub>	Output Leakage Current			50	μA	0 - 5.5V	V <sub>OUT</sub> = 2.7V; $\overline{OE}_n = 2.0V$
I <sub>OZL</sub>	Output Leakage Current			-50	μA	0 - 5.5V	V <sub>OUT</sub> = 0.5V; $\overline{OE}_n = 2.0V$
I <sub>OS</sub>	Output Short-Circuit Current	-100		-275	mA	Max	V <sub>OUT</sub> = 0.0V
I <sub>CEX</sub>	Output High Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
I <sub>ZZ</sub>	Bus Drainage Test			100	μA	0.0	V <sub>OUT</sub> = 5.5V; All Others GND
I <sub>CCH</sub>	Power Supply Current			50	μA	Max	All Outputs HIGH
I <sub>CCL</sub>	Power Supply Current			30	mA	Max	All Outputs LOW
I <sub>CCZ</sub>	Power Supply Current			50	μA	Max	$\overline{OE}_n = V_{CC}$ ; All Others at V <sub>CC</sub> or Ground
I <sub>CC1</sub>	Additional I <sub>CC</sub> /Input	Outputs Enabled		1.5	mA	Max	V <sub>I</sub> = V <sub>CC</sub> - 2.1V Enable Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V Data Input V <sub>I</sub> = V <sub>CC</sub> - 2.1V All Others at V <sub>CC</sub> or Ground
		Outputs TRI-STATE		1.5	mA		
		Outputs TRI-STATE		50	μA		
I <sub>CCD</sub>	Dynamic I <sub>CC</sub> (Note 2)	No Load		0.1	mA/ MHz	Max	Outputs Open $\overline{OE}_n = GND$ , (Note 1) One Bit Toggling, 50% Duty Cycle

**Note 1:** For 8 bits toggling, I<sub>CCD</sub> < 0.8 mA/MHz.

**Note 2:** Guaranteed, but not tested.

## AC Electrical Characteristics (SOIC and SSOP package): See Section 2 for Waveforms

Symbol	Parameter	74ABT			54ABT		74ABT		Units	Fig. No.
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5\text{V}$ $C_L = 50\text{ pF}$			$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$		$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 4.5\text{V}-5.5\text{V}$ $C_L = 50\text{ pF}$			
		Min	Typ	Max	Min	Max	Min	Max		
$t_{PLH}$	Propagation Delay	1.0		4.8	0.8	5.5	1.0	4.8	ns	2-3, 5
$t_{PHL}$	Data to Outputs	1.6		4.8	1.0	5.5	1.6	4.8		
$t_{pZH}$	Output Enable	1.1		6.2	0.8	7.5	1.1	6.2	ns	2-4
$t_{pZL}$	Time	1.1		6.2	0.8	7.7	1.1	6.2		
$t_{pHZ}$	Output Disable	1.8		6.4	1.0	7.5	1.8	6.4	ns	2-4
$t_{pLZ}$	Time	1.6		5.8	1.0	7.2	1.6	5.8		

### Capacitance

Symbol	Parameter	Typ	Units	Conditions $T_A = 25^\circ\text{C}$
$C_{IN}$	Input Capacitance	5.0	pF	$V_{CC} = 0\text{V}$
$C_{OUT}$ (Note 1)	Output Capacitance	9.0	pF	$V_{CC} = 5.0\text{V}$

Note 1:  $C_{OUT}$  is measured at frequency  $f = 1\text{ MHz}$ , per MIL-STD-883B, Method 3012.