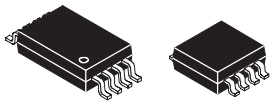


VOLTAGE PROTECTION FOR 2-, 3-, OR 4-CELL Lion BATTERIES (2ND PROTECTION)

FEATURES

- 2- ,3- , or 4-Cell Secondary Protection
- Low Power Consumption $I_{CC} < 2\ \mu A$ $(VCELL_{(ALL)} < V_{(PROTECT)})$
- High Accuracy Over Sense Voltage:
  - bq29400: 4.35 V ±25 mV
  - bq29401: 4.45 V ±25 mV
- Prefixed Protection Threshold Voltage
- Programmable Delay Time
- High Power Supply Ripple Rejection
- Stable During Pulse Charge Operation

APPLICATIONS

- 2nd Level Protection in Lion Battery Packs in
  - Notebook PCs
  - Portable Instrumentation
  - Medical and Test Equipment

DESCRIPTION

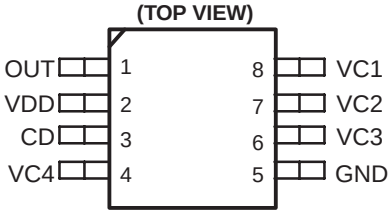
The bq29400 and bq29401 are BiCMOS secondary protection ICs for 2-, 3-, or 4-cell Lithium-Ion battery packs that incorporate a high-accuracy precision over voltage detection circuit. They include a programmable delay circuit for over voltage detection time.

FUNCTION

Each cell in a multiple cell pack is compared to an internal reference voltage. If one cell reaches an overvoltage condition, the protection sequence begins. The bq29400 and bq29401 start charging an external capacitor through the CD pin. When the CD pin voltage reaches 1.2 V, the OUT pin changes from a low level to a high level.

PW PACKAGE
(TOP VIEW)

DCT PACKAGE
(TOP VIEW)



ORDERING INFORMATION

T_A	$V_{(PROTECT)}$	PACKAGE			
		MSOP (DTC)	SYMBOL	TSSOP (PW)(1)	SYMBOL
−25°C to 85°C	4.35 V	bq29400DCT3	CIQ	bq29400PW	2400
	4.45 V	bq29401DCT3	CIR	bq29401PW	2401

(1) The bq29400 and bq29401 are available taped and reeled. Add an R suffix to the device type (e.g., bq29400PWR) to order tape and reel version.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1) (2)

		UNIT
Supply voltage range	(VDD)	−0.3 V to 28 V
Input voltage range	(VC1, VC2, VC3, VC4)	−0.3 V to 28 V
	(VC1 to VC2, VC2 to VC3, VC3 to VC4, VC4 to GND)	−0.3 V to 8 V
Output voltage range	(OUT)	−0.3 V to 28 V
	(CD)	−0.3 V to 28 V
Continuous total power dissipation		See Dissipation Rating Table
Storage temperature range, T_{stg}		−65°C to 150°C
Lead temperature (soldering, 10 sec)		300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground of this device except the differential voltage of VC1−VC2, VC2−VC3, VC3−VC4 and VC4−GND.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DCT	412 mW	3.3 mW/°C	264 mW	214 mW
PW	525 mW	4.2 mW/°C	336 mW	273 mW

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
Supply Voltage, V_{DD}		4.0		25	V
Input voltage range, V_I	VC1, VC2, VC3, VC4	0		V_{DD}	V
	VCn – VC(n+1), (n=1, 2, 3), VC4−GND	0		5.0	
Delay time capacitance, $t_{d(CD)}$	CD		0.22		µF
Voltage-monitor filter resistance	R_{IN}	100	1k		Ω
Voltage-monitor filter capacitance	C_{IN}	0.01	0.1		µF
Supply-voltage filter resistance	R_{VD}	0		100	Ω
Supply-voltage filter capacitance	C_{VD}		0.1		µF
Operating ambient temperature range, T_A		−25		85	°C

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITION	MIN	NOM	MAX	UNIT
$V_{(OA)}$	Over voltage detection accuracy			25	35	mV
		T_A = −20°C to 85°C		25	50	
$V_{(PROTECT)}$	Over voltage detection voltage(1)	bq29400		4.35		V
		bq29401		4.45		
V_{hys}	Over voltage detection hysteresis(1)			300		mV
I_I	Input current	V2, V3 , VC4 input VC1 = VC2 = VC3 = VC4 = 3.5 V (see Figure 1)			±0.3	µA
t_{D1}	Over voltage detection delay time	CD = 0.22 µF	1.0	1.5	2.0	S
$I_{(CD\_dis)}$	CD GND clamp current	CD = 1 V	5	12		µA
I_{CC}	Supply current	VC1 = VC2 = VC3 = VC4 = 3.5 V (see Figure 1)		2.0	3.0	µA
		VC1 = VC2 = VC3 = VC4 = 2.3 V (see Figure 1)		1.5	2.5	
I_{OH}	High-level output current	OUT = 3V, VC1 = VC2 = VC3 = VC4 = 4.5 V	−1			mA
I_{OL}	Low-level output current	OUT = 0.1 V VC1 = VC3 = VC4 = 3.5 V	5			µA

(1) Levels of the over-voltage detection and the hysteresis can be adjusted. For assistance contact Texas Instruments sales representative.

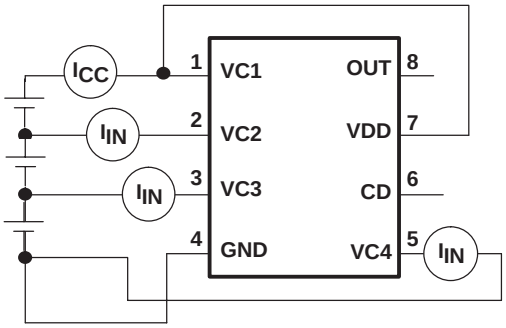
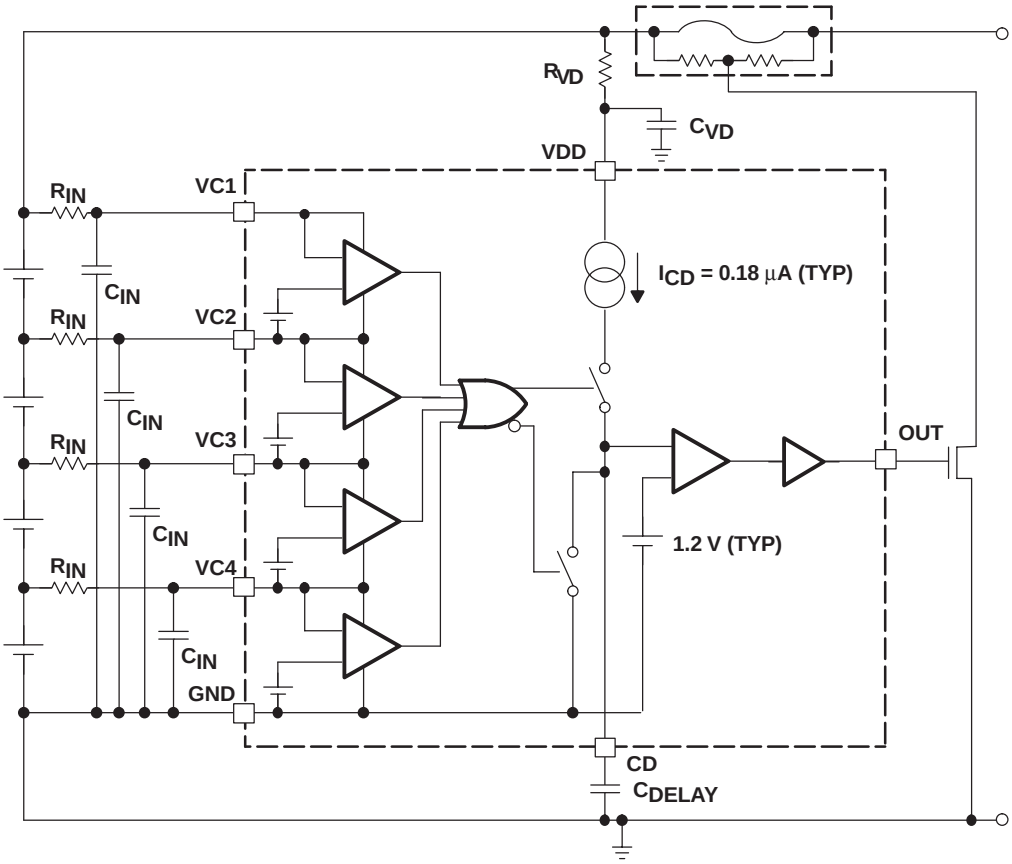


Figure 1. I_{CC}, I_{IN} Measurement (TSSOP Package)

Terminal Functions

TERMINAL NO.			DESCRIPTION
MSOP (DTC)	TSSOP (PW)	NAME	
8	1	VC1	Sense voltage input for most positive cell
7	2	VC2	Sense voltage input for second most positive cell
6	3	VC3	Sense voltage input for third most positive cell
5	4	GND	Ground pin
4	5	VC4	Sense voltage input for least positive cell
3	6	CD	An external capacitor is connected to determine the programmable delay time
2	7	VDD	Power supply
1	8	OUT	Output

FUNCTIONAL BLOCK DIAGRAM



OVERVOLTAGE PROTECTION

When one of the cell voltages exceeds $V_{(PROTECT)}$, an internal current source begins to charge the capacitor, $C_{(DELAY)}$, connected to the CD pin. If the voltage at the CD pin, $V_{CD,}$ reaches 1.2 V, the OUT pin is activated and transitions high. An externally connected NCH FET is activiated and blows the external fuse in the positive battery rail, see Figure 1, .

If all cell voltages fall below $V_{(PROTECT)}$ before the voltage at pin CD reaches 1.2 V, the delay time does not run out. An internal switch clamps the CD pin to GND and discharges the capacitor, $C_{(DELAY)}$, and secures the full delay time for the next occurring overvoltage event.

Once the pin OUT is activated, it transitions back from high to low after all battery cells reach $V_{(PROTECT)} - V_{hys}$.

DELAY TIME CALCULATION

The delay time is calculated as follows:

$$t_d = \frac{\left[1.2\ V \times C_{(DELAY)}\right]}{I_{CD}}$$

$$C_{(DELAY)} = \frac{\left[t_d \times I_{CD}\right]}{1.2\ V}$$

Where $I_{(CD)}$ = CD current source = 0.18 µA

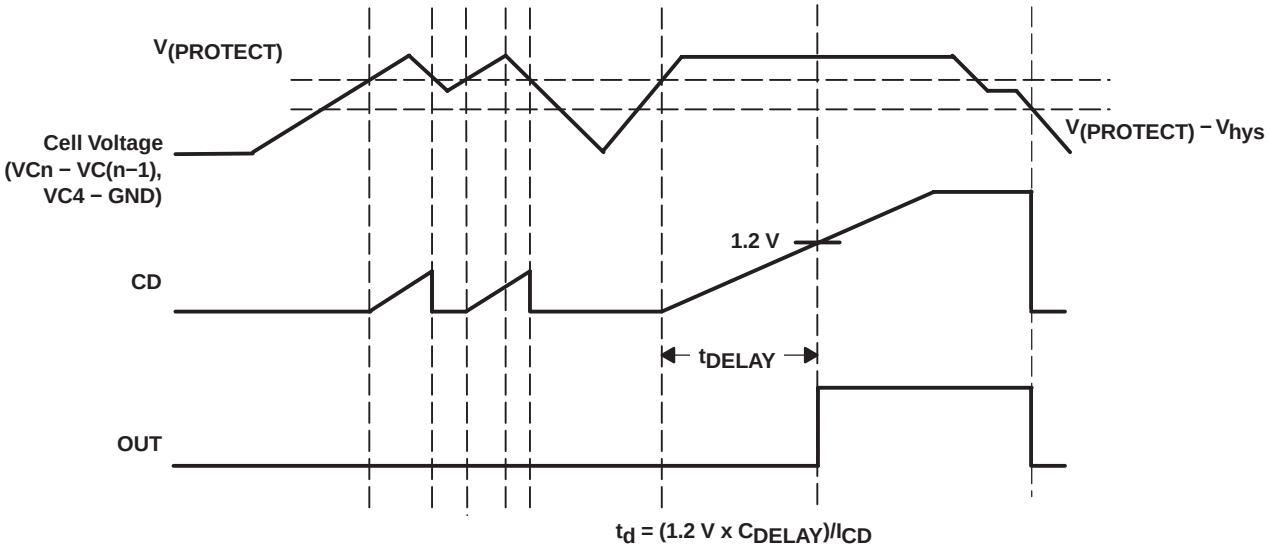


Figure 2. Timing for Overvoltage Sensing

APPLICATION INFORMATION

BATTERY CONNECTIONS

The following diagrams show the TSSOP package device in different cell configurations.

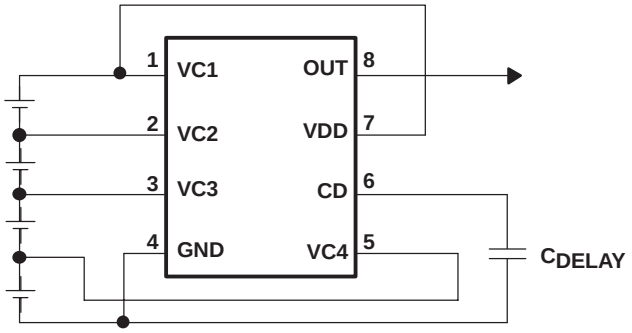


Figure 3. 4-Series Cell Configuration

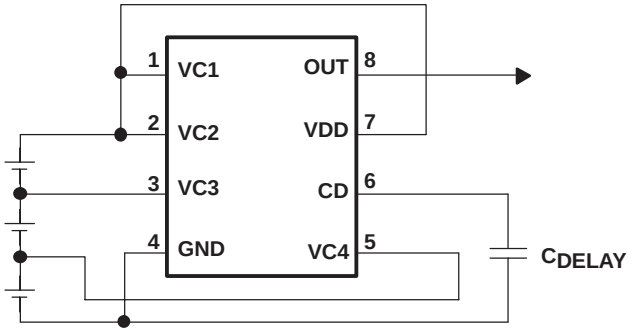


Figure 4. 3-Series Cell Configuration (Connect together VC1 and VC2)

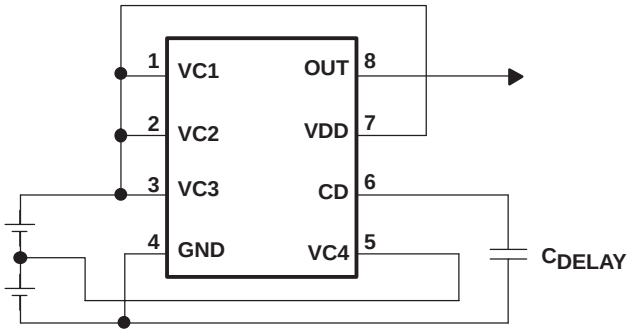


Figure 5. 2-Series Cell Configuration (Connect together VC1, VC2, and VC3)

CELL CONNECTIONS

To prevent incorrect output activation the following connection sequences must be used.

4−Series Cell Configuration

VC1(=VDD) → VC2 → VC3 → VC4 → GND or

GND → VC4 → VC3 → VC2 → VC1(=VDD)

3−Series Cell Configuration

VC1(=VC2=VDD) → VC3 → VC4 → GND or

GND → VC4 → VC3 → VC1(=VC2=VDD)

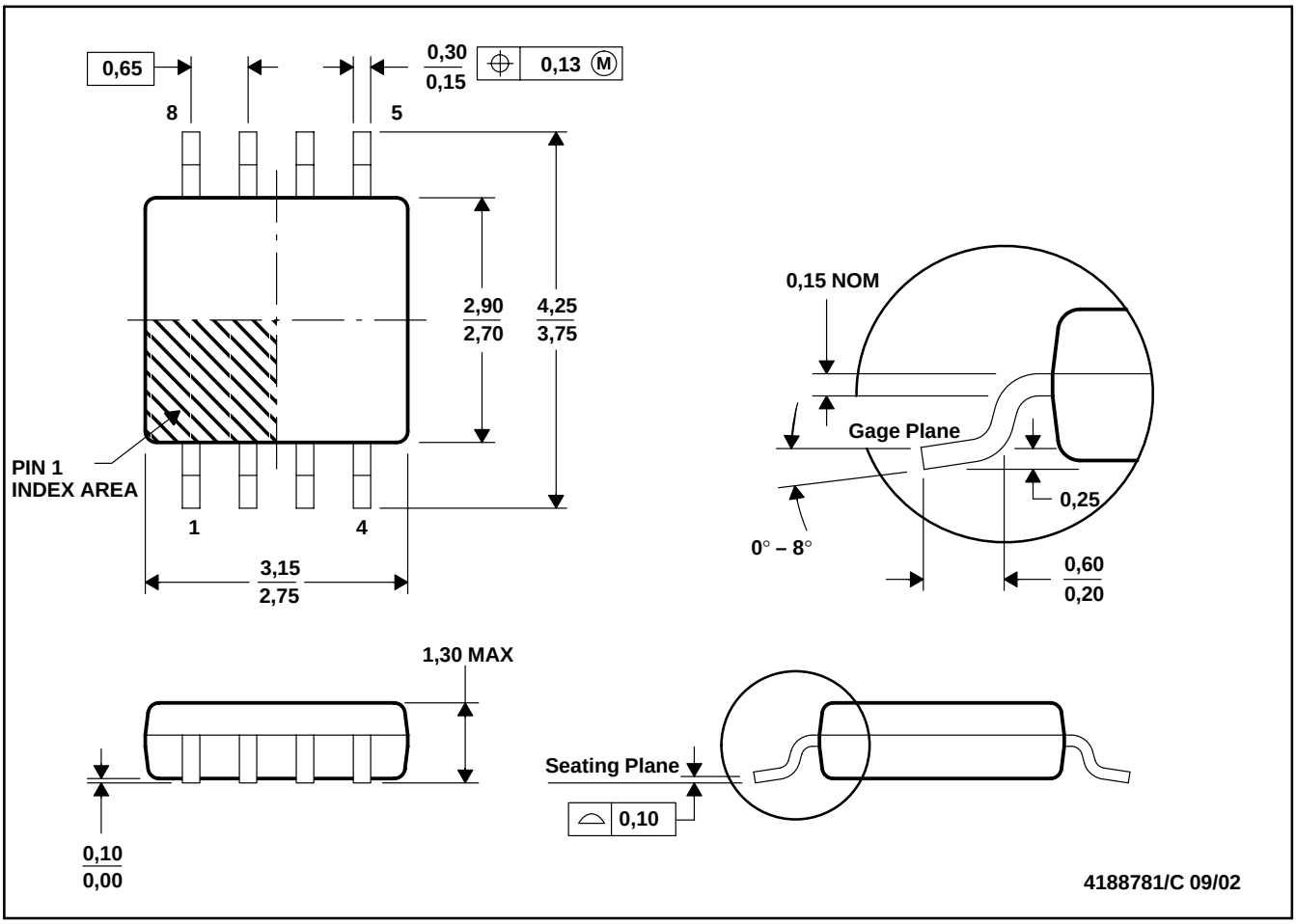
2−Series Cell Configuration

VC1(=VC2=VC3=VDD) → VC4 → GND or

GND → VC4 → VC1(=VC2=VC3=VDD)

MPDS049B – MAY 1999 – REVISED OCTOBER 2002

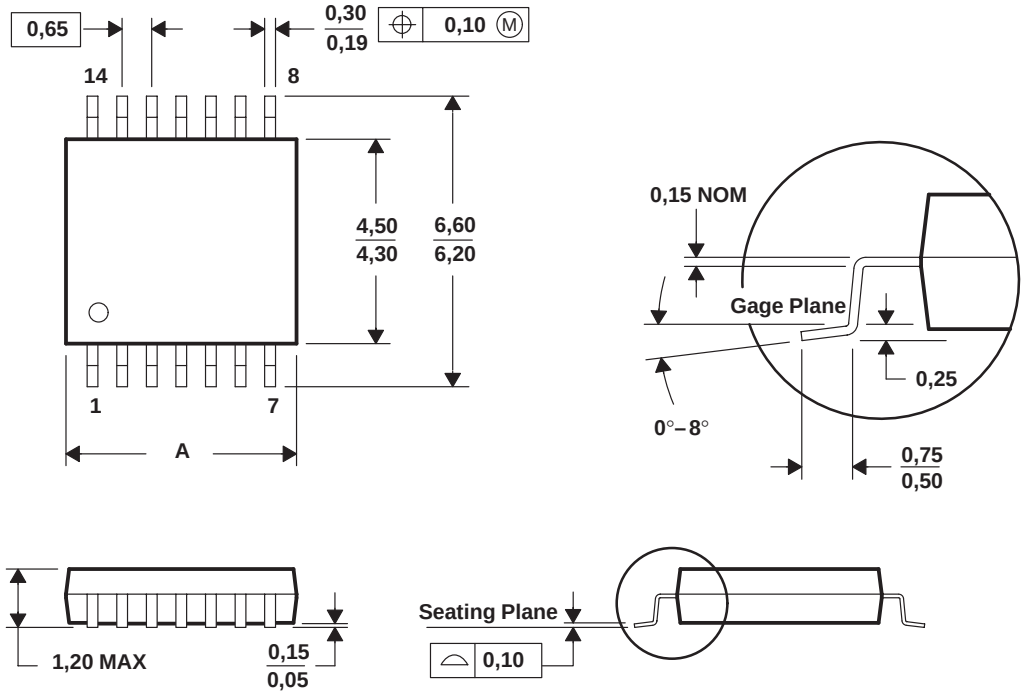
DCT (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion
D. Falls within JEDEC MO-187 variation DA.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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