SMBus Thermal Sensor with External Diode Input

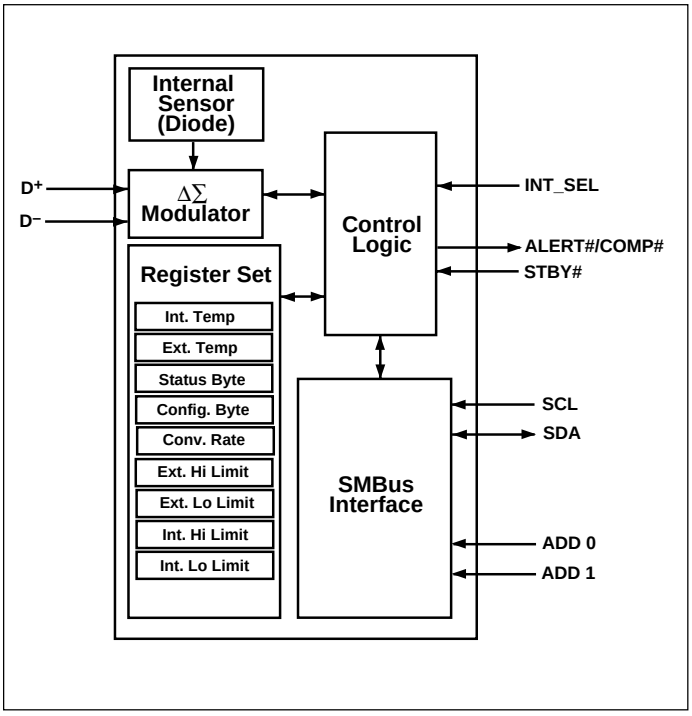
FEATURES

- **Backward Compliant to Older APM Systems**
- **Includes Internal** and **External Sensing Capability**
- **Outputs Temperature As 8-Bit Digital Word**
- **Solid State Temperature Sensing; 1°C Resolution**
- **3.0 – 5.5V Operating Range**
- **Independent Internal and External Threshold Set-Points With ALERT#/COMP# Interrupt Output**
- **SMBus 2-Wire Serial Interface**
- **Up To Nine TC1068s May Share the Same Bus**
- **Standby Mode for Low Standby Power**
- **Low Power ..... 70 μA (max) Operating ..... 10 μA (max) Standby Mode**
- **16-Pin Plastic QSOP Package**

TYPICAL APPLICATIONS

- **Thermal Protection For Intel "Deschutes" Pentium™II and Other High Performance CPUs with Integrated On-Board Diode — No Sensor Mounting Problems!**
- **Accurate Thermal Sensing From Any Si Junction Diode**
- **Thermal Management in Electronic Systems: Computers, Network Equipment, Power Supplies**

BLOCK DIAGRAM



GENERAL DESCRIPTION

The TC1068 is a serially programmable temperature sensor optimized for monitoring modern high performance CPUs with on-board integrated thermal diodes. Temperature data is converted from the CPU's thermal diode outputs and made available as an 8-bit digital word.

Communication with the TC1068 is accomplished via the standard System Management Bus (SMBus) commonly used in modern computer systems. This permits reading the current internal/external temperature, programming the threshold setpoints, and configuring the device. Additionally, an interrupt is generated on the ALERT#/COMP# pin when temperature moves outside the preset threshold windows in either direction.

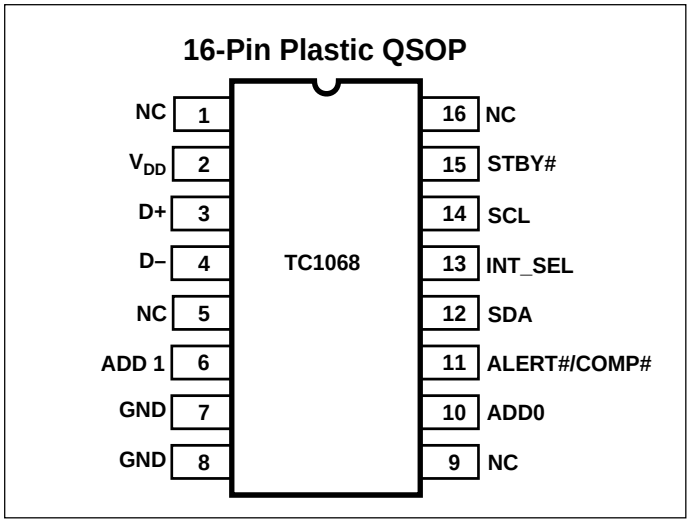
A Standby command may be sent via the SMBus or by signaling the STBY# input pin to activate the low-power Standby mode. Registers can be accessed while in Standby mode. Address selection inputs allow up to nine TC1068s to share the same 2-wire SMBus for multi-zone monitoring.

All registers can be read by the host, and both polled and interrupt driven systems are easily accommodated. Small size, low installed cost, and ease of use make the TC1068 an ideal choice for implementing sophisticated system management schemes, such as ACPI.

ORDERING INFORMATION

Part No.	Package	Temp. Range
TC1068MQR	QSOP-16	–55°C to +125°C
TCM1617EV	**Evaluation Kit Available**	

PIN CONFIGURATION



TC1068

ABSOLUTE MAXIMUM RATINGS*

Power Supply Voltage (V_{DD}) 6V
Voltage On Any Pin ..... (GND – 0.3V) to (V_{DD} + 0.3V)
Operating Temperature (T_A) ..... –55°C to +125°C
Storage Temperature (T_{STG}) ..... –65°C to +150°C
SMBus Input/Output Current ..... –1 mA to +50 mA
D– Input Current ..... ±1 mA

*Static-sensitive device. Unused devices must be stored in conductive material. Protect devices from static discharge and static fields. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS: V_{DD} = 3.3V, –55°C ≤ T_A ≤ 125°C, unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply						
V_{DD}	Power Supply Voltage	–55 ≤ T_A ≤ +125°C	3.0	—	5.5	V
$V_{UV-LOCK}$	V_{DD} Undervoltage Lockout Threshold		2.4	2.80	2.95	V
V_{POR}	Power-On Reset Threshold	V_{DD} Falling Edge	1.0	1.7	2.3	V
I_{DD}	Operating Current	0.25 Conv./Sec Rate SMBus Inactive (Note 1)	—	—	70	µA
I_{DD}	Operating Current	2 Conv./Sec Rate SMBus Inactive (Note 1)	—	—	180	µA
$I_{DD-STANDBY}$	Standby Supply Current	V_{DD} = 3.3V SMBus Active	—	—	100	µA
$I_{DD-STANDBY}$	Standby Supply Current	V_{DD} = 3.3V, SMBus Inactive	—	—	10	µA
$I_{ADD-BIAS}$	ADD[1:0] Bias Current	Power-Up Only	—	160	—	µA
ALERT#/COMP# Output						
V_{OL}	Output Low Voltage	I_{OL} = 1.0 mA (Note 3)	—	—	0.4	V
ADD[1:0]						
V_{IL}	Logic Input Low		—	—	V_{DD} x 0.3	V
V_{IH}	Logic Input High		V_{DD} x 0.7	—	—	V
STBY# Input						
V_{IL}	Logic Input Low		—	—	V_{DD} x .3	V
V_{IH}	Logic Input High		V_{DD} x .7	—	—	V
INT_SEL						
V_{IL}	Logic Input Low		—	—	V_{DD} x .3	V
V_{IH}	Logic Input High		V_{DD} x .7	—	—	V
R_P	Internal Pull-up Resistance		—	500	—	KΩ
Temp-to-Bits Converter						
T_{RES}	Basic Temperature Resolution		—	1	—	°C
T_{IERR1}	Internal Diode Temperature	+60°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ +125°C –55°C ≤ T_A < 0°C	–2 –3 —	— — ±3	+2 +3 —	°C °C °C
T_{EERR}	External Diode Temperature (Note 4)	+60°C ≤ T_A ≤ +100°C 0°C ≤ T_A ≤ +125°C –55°C ≤ T_A < 0°C	–3 –5 —	— — ±5	+3 +5 —	°C °C °C

ELECTRICAL CHARACTERISTICS (CONT): V_{DD} = 3.3V, –55°C ≤ T_A ≤ 125°C,unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DIODE-HIGH}$	External Diode High Source Current	(D+) – (D–) ~ 0.65V	—	100	—	µA
$I_{DIODE-LOW}$	External Diode Low Source Current	(D+) – (D–) ~ 0.65V	—	10	—	µA
$V_{D-SOURCE}$	D– Source Voltage		—	0.7	—	V
t_{CONV}	Conversion Time	From CHIP STOP to Conv. Complete (Note 2)	54	83	112	msec
ΔCR	Conversion Rate Accuracy	See Conversion Rate Register Desc.	–35	—	+35	%
2-Wire SMBus Interface						
V_{IH}	Logic Input High		2.2	—	—	V
V_{IL}	Logic Input Low		—	—	0.8	V
V_{OL}	SDA Output Low	I_{OL} = 2 mA (Note 3) I_{OL} = 4 mA (Note 3)	— —	— —	0.4 0.6	V V
C_{IN}	Input Capacitance SDA, SCL		—	5	—	pF
I_{LEAK}	I/O Leakage		–1	0.1	1	µA

SMBus PORT AC TIMING: V_{DD} = 3.3V, –55 ≤ (T_A = T_J) ≤ 125°C; C_L = 80 pF, unless otherwise noted.

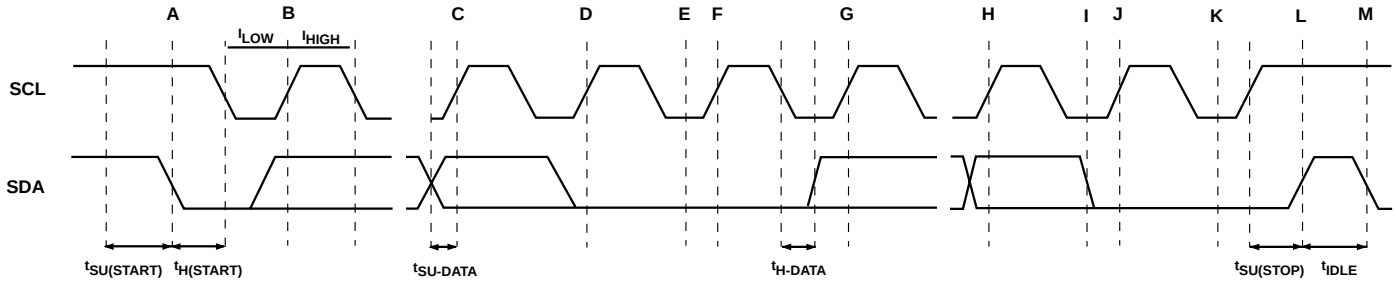
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
f_{SMB}	SMBus Clock Frequency		10	—	100	KHz
t_{LOW}	Low Clock Period	10% to 10%	4.7	—	—	µsec
t_{HIGH}	High Clock Period	90% to 90%	4	—	—	µsec
t_R	SMBus Rise Time	10% to 90%	—	—	1,000	nsec
t_F	SMBus Fall Time	90% to 10%	—	—	300	nsec
$t_{SU(START)}$	Start Condition Setup Time (for Repeated Start Condition)	90% SCL to 10% SDA	4	—	—	µsec
$t_{H(START)}$	Start Condition Hold Time		4	—	—	µsec
$t_{SU-DATA}$	Data in Setup Time		1000	—	—	nsec
t_{H-DATA}	Data in Hold Time		1250	—	—	nsec
$t_{SU(STOP)}$	Stop Condition Setup Time		4	—	—	µsec
t_{IDLE}	Bus Free Time Prior to New Transition		4.7	—	—	µsec

NOTES:
1. Operating current is an average value (including external diode injection pulse current) integrated over multiple conversion cycles. Transient current may exceed this specification.
2. For true reccurring conversion time see Conversion Rate register description.
3. Output current should be minimized for best temperature accuracy. Power dissipation within the TC1068 will cause self-heating and temperature drift error.
4. Refer to Application Note 64.

TC1068

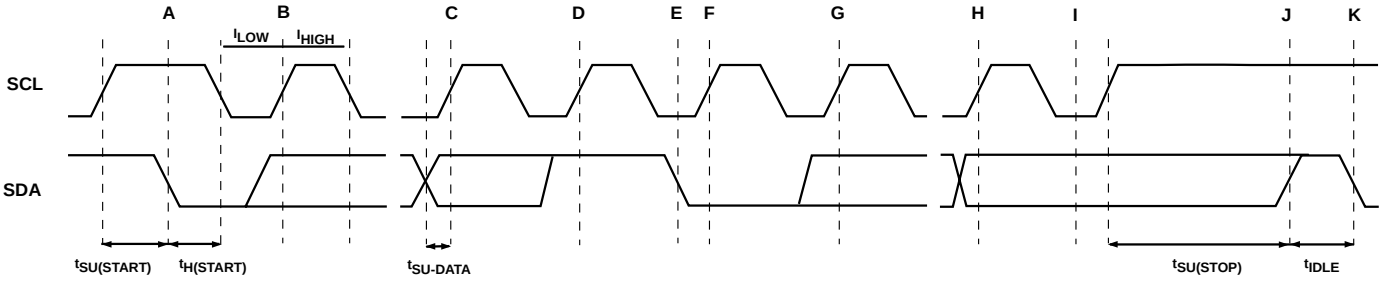
TIMING DIAGRAMS

SMBUS Writing Timing Diagram



A = Start Condition
B = MSB of Address Clocked into Slave
C = LSB of Address Clocked into Slave
D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Slave
H = LSB of Data Clocked into Slave
I = Slave Pulls SDA Line Low
J = Acknowledge Clocked into Master
K = Acknowledge Clock Pulse
L = Stop Condition, Data Executed by Slave
M = New Start Condition

SMBUS Read Timing Diagram



A = Start Condition
B = MSB of Address Clocked into Slave
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D = R/$\overline{W}$ Bit Clocked into Slave
E = Slave Pulls SDA Line Low
F = Acknowledge Bit Clocked into Master
G = MSB of Data Clocked into Master
H = LSB of Data Clocked into Master
I = Acknowledge Clock Pulse
J = Stop Condition
K = New Start Condition

PIN DESCRIPTION

Pin Number	Symbol	Type	Description
2	V_{DD}	Power	Power Supply Input
3	D+	Bi-Directional	Current Source and A/D Positive Input
4	D–	Bi-Directional	Current Sink and A/D Negative Input
6,10	ADD[1:0]	Input	Address Select Pins (See Address Decode Table)
7,8	GND	Power	System Ground
11	ALERT#/COMP#	Output	SMBus Interrupt (SMBALERT#) or Comparator Output
12	SDA	Bi-Directional	SMBus Serial Data
14	SCL	Input	SMBus Serial Clock
15	STBY#	Input	Standby Enable
13	INT_SEL	Input	Selects ALERT# or COMP# Output on Pin 11
1, 5, 9, 16	NC	—	Not Connected

PIN DESCRIPTION

SCL

Input. SMBus serial clock. Clocks data into and out of the TC1068. See System Management Bus Specification, rev. 1.0, for timing diagrams.

SDA

Bidirectional. Serial data is transferred on the SMBus in both directions using this pin. See System Management Bus Specification, rev. 1.0, for timing diagrams.

ADD1, ADD0

Inputs. Sets the 7-bit SMBus address. These pins are “tri-state,” and the SMBus addresses are specified in the Address Decode Table.

(**NOTE:** The tri-state scheme allows up to nine TC1068s on a single bus. A match between the TC1068’s address and the address specified in the serial bit stream must be made to initiate communication. Many SMBus-compatible devices with other addresses may share the same 2-wire bus (see System Management Bus Specification, rev. 1.0, for address allocations). These pins are only active at power-on reset, and will latch into the appropriate states.

ALERT#/COMP#*

Output, Open Collector, Active Low. The ALERT# output corresponds to the general SMBALERT# signal and indicates an interrupt event. The TC1068 will respond to the standard SMBus Alert Response Address (see SMBus Specification 1.0) and associated protocol when ALERT# is asserted. Normally, the ALERT# output will be asserted and latched when any of the following occurs:

1. INT_TEMP equal to or exceeds INT_HLIM
2. INT_TEMP below INT_LLIM
3. EXT_TEMP equal to or exceeds EXT_HLIM
4. EXT_TEMP below EXT_LLIM
5. External Diode “Open”

The operation of the ALERT# output is controlled by the MASK1 bit in the CONFIG register. If the MASK1 bit is set to “1,” no interrupts will be generated on ALERT#. The ALERT# output is cleared and rearmed by the Alert Response Address (ARA). This output may be WIRE-ORed with similar outputs from other SMBus devices. If the alarm condition persists after the ARA, the ALERT# output will be immediately re-asserted.

(**NOTE:** A pull-up resistor is necessary on ALERT# since it is an open-drain output. Current sourced from the pull-up resistor causes power dissipation and may cause internal heating of the TC1068. To avoid affecting the accuracy of internal temperature readings, the pull-up resistors should be made as large as possible.)

Normally the COMP# output will be asserted upon the following events:

1. EXT_TEMP equal to or exceeds EXT_HLIM
2. External Diode “Open”

COMP# will be de-asserted upon the following event: EXT_TEMP below EXT_HLIM.

The operation of the COMP# output is controlled by the MASK1 bit in the CONFIG register. If the MASK1 bit is set to “1,” no interrupts will be generated on COMP#. This output may be WIRE-ORed with similar outputs from other SMBus devices. Note: A pull-up resistor is necessary on COMP# since it is an open-drain output. Current sourced from the

pull-up resistor causes power dissipation and may cause internal heating of the TC1068. To avoid affecting the accuracy of internal temperature readings, the pull-up resistors should be made as large as possible. *Pin 11's function is selected with pin 13 (INT_SEL) — see INT_SEL.

INT_SEL

Input. The operation of Pin 11 is defined by the state of this pin. There is an internal pull-up to V_{DD}. If INT_SEL is high, Pin 11 will function as ALERT#. If INT_SEL is grounded, Pin 11 will function as COMP#.

STBY#

Input. The activation of Standby mode may be achieved using either the STBY# pin or the CHIP STOP bit (CONFIG register). If STBY# is pulled low, the TC1068 unconditionally enters its low-power Standby mode (I_{DD} = 10 µA, max). The temperature-to-digital conversion process is halted, but ALERT# and OS# remain functional. The TC1068's bus interface remains active, and all registers may be read from and written to normally. The INT_TEMP and EXT_TEMP registers will contain whatever data was valid at the time of Standby. (Transitions on SDA or SCL due to external bus activity may increase the Standby power consumption.)

D+

Bi-directional. This pin connects to the anode of the external diode and is the positive A/D input. Current is injected into the external diode from the TC1068, and the temperature proportional V_{BE} is measured and converted to digital temperature data.

D–

Bi-directional. This pin connects to the cathode of the external diode. Current is sunk from the external diode into the TC1068 through this pin. It also is the negative input terminal to the TC1068's A/D converter. This node is kept at approximately 0.7V above GROUND.

V_{DD}

Input. Power supply input. See electrical specifications.

GND

Input. Ground return for all TC1068 functions.

FUNCTIONAL DESCRIPTION

The TC1068 acquires and converts temperature information from two separate sources, both silicon junction diodes, with a basic accuracy of ±1°C. One is located on the TC1068 die; the other is connected externally. This external diode may be located on another IC die. The analog-to-digital converter on the TC1068 alternately converts temperature data from the two sensors and stores them separately in internal registers.

The system interface is a slave SMBus port with an ALERT# (SMBALERT#) and COMP# interrupt outputs. The ALERT# interrupt is triggered when one or more of four preset temperature thresholds are tripped (see Figure 1). These four thresholds are user-programmable via the SMBus port. The COMP# interrupt is triggered when EXT_TEMP equals or exceeds EXT_HLIM. Additionally, the temperature data can be read at any time through the SMBus port. Nine SMBus addresses are programmable for the TC1068, which allows for a multi-sensor configuration. Also, there is low-power Standby mode where temperature acquisition is suspended.

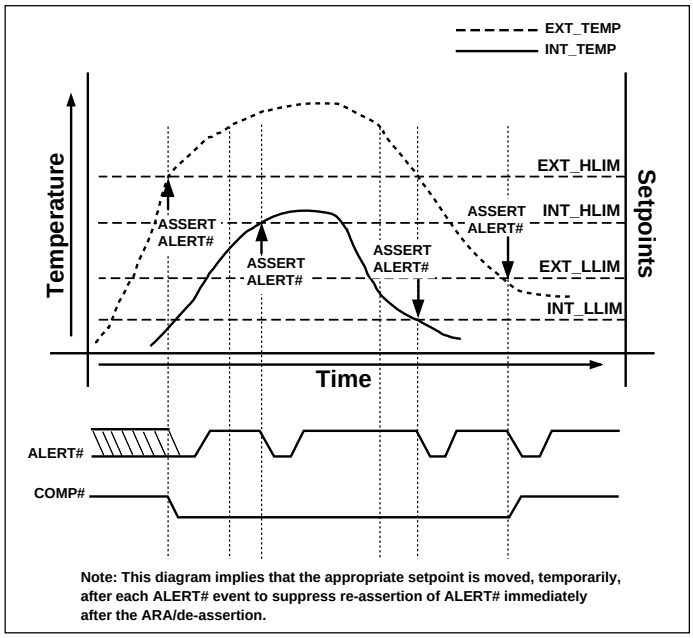


Figure 1. Temperature-vs-Setpoint Event Generation

STANDBY MODE

The TC1068 allows the host to put it into a low power mode (I_{DD} = 10 µA, max) Standby mode. In this mode, the A/D converter is halted, and the temperature data registers are frozen. The SMBus port operates normally. Standby mode can be enabled with either the STBY# input pin or the CHIP STOP bit in the CONFIG register. The following table summarizes this operation.

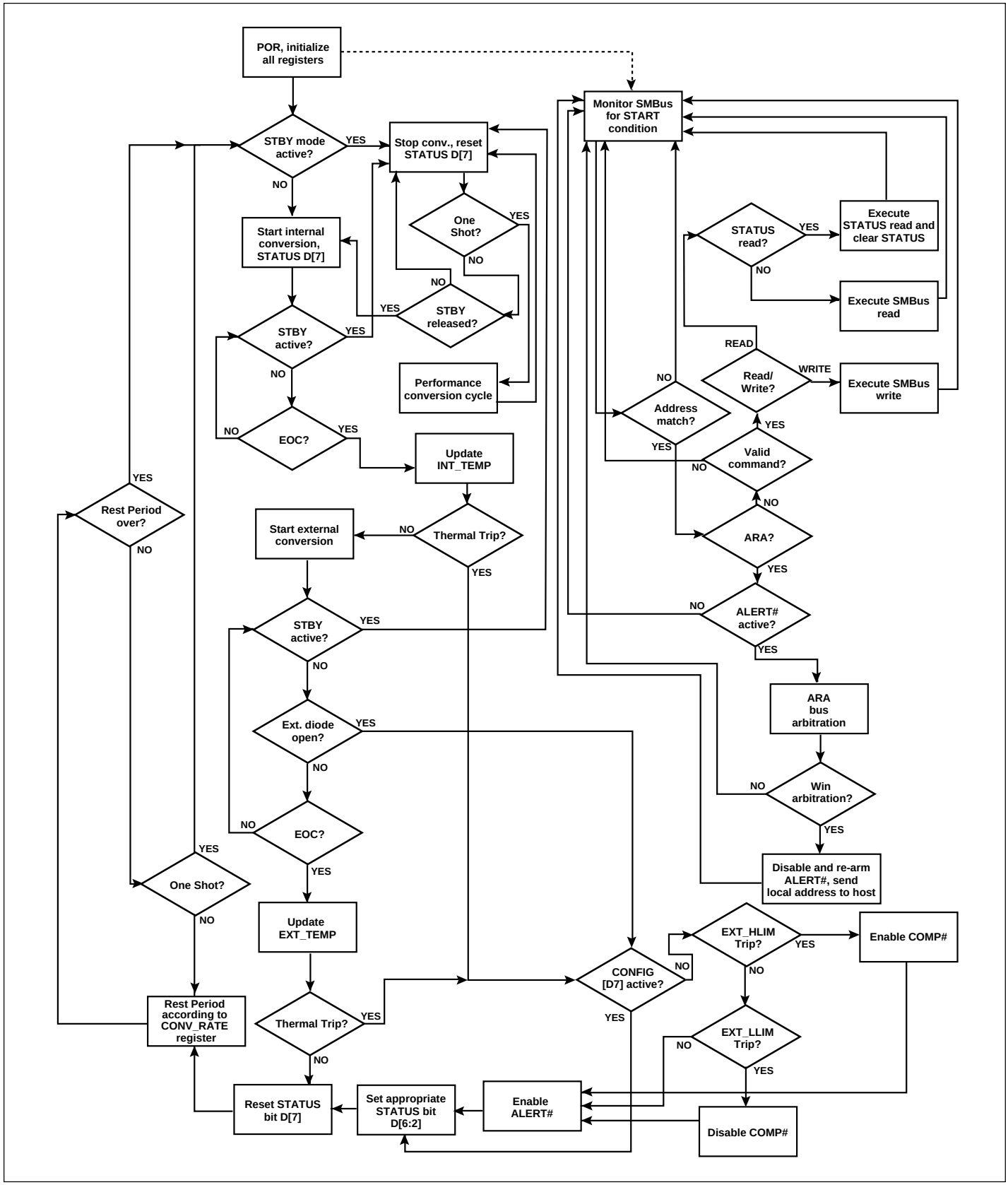


Figure 2. TC1068 Functional Description Flowchart

Standby Mode Operation			
STBY#	**Chip Stop Bit**	**One Shot?**	**Operating Mode**
0	Don't Care	Don't Care	Standby
1	0	Don't Care	Normal
1	1	No	Standby
1	1	Yes	Normal (1 Conversion Only, then Standby)

SMBus SLAVE ADDRESS

The two pins ADD1 and ADD0 are tri-state input pins which determine the 7-bit SMBus slave address of the TC1068. The address is latched during POR. The allowable addresses are summarized in the following table.

Address Decode Table		
ADD0	**ADD1**	**SMBus Address**
0	0	0011 000
0	open (3-state)	0011 001
0	1	0011 010
open (3-state)	0	0101 001
open (3-state)	open (3-state)	0101 010
open (3-state)	1	0101 011
1	0	1001 100
1	open (3-state)	1001 101
1	1	1001 110

SERIAL PORT OPERATION

The Serial Clock input (SCL) and bi-directional data port (SDAT) form a 2-wire bi-directional serial port for programming and interrogating the TC1068. The following conventions are used in the bus architecture in the followingtable.

All transfers take place under control of a host, usually a CPU or microcontroller, acting as the Master, which provides the clock signal for all transfers. The TC1068 *always* operates as a slave. The serial protocol is illustrated in Figure 3. All data transfers have two phases; all bytes are transferred MSB first. Accesses are initiated by a start condition (START), followed by a device address byte and one or more data bytes. The device address byte includes a Read/Write selection bit. Each access must be terminated by a Stop Condition (STOP). A convention called *Acknowledge* (ACK) confirms receipt of each byte. Note that SDA can change only during periods when SCL is LOW (SDA changes while SCL is High are reserved for Start and Stop conditions.)

TC1068 Serial Bus Conventions	
Term	**Explanation**
Transmitter	The device sending data to the bus.
Receiver	The device receiving data from the bus.
Master	The device which controls the bus: initiating transfers (START), generating the clock, and terminating transfers (STOP).
Slave	The device addressed by the master.
Start	A unique condition signaling the beginning of a transfer indicated by SDA falling (High – Low) while SCL is high.
Stop	A unique condition signaling the end of a transfer indicated by SDA rising (Low – High) while SCL is high.
ACK	A receiver acknowledges the receipt of each byte with this unique condition. The receiver drives SDA low during SCL high of the ACK clock-pulse. The Master provides the clock pulse for the ACK cycle.
Busy	Communication is not possible because the bus is in use.
NOT Busy	When the bus is idle, both SDA and SCL will remain high.
Data Valid	The state of SDA must remain stable during the High period of SCL in order for a data bit to be considered valid. SDA only changes state while SCL is low during normal data transfers (see Start and Stop conditions).

Start Condition (START)

The TC1068 continuously monitors the SDA and SCL lines for a start condition (a High to Low transition of SDA while SCL is High), and will not respond until this condition is met.

Address Byte

Immediately following the Start Condition, the host must transmit the address byte to the TC1068. The states of ADD1 and ADD0 during power-up determine the 7-bit SMBus address for the TC1068. The 7-bit address transmitted in the serial bit stream must match for the TC1068 to respond with an Acknowledge (indicating the TC1068 is on the bus and ready to accept data). The eighth bit in the Address Byte is a Read-Write Bit. This bit is 1 for a read operation or 0 for a write operation.

Acknowledge (ACK)

Acknowledge (ACK) provides a positive handshake between the host and the TC1068. The host releases SDA after transmitting eight bits, then generates a ninth clock cycle to allow the TC1068 to pull the SDA line Low to

Write Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	DATA	ACK	P
	7 Bits			8 Bits		8 Bits		

Slave Address

Command Byte: selects which register you are writing to.

Data Byte: data goes into the register set by the command byte.

Read Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits			7 Bits			8 Bits		

Slave Address

Command Byte: selects which register you are reading from.

Slave Address: repeated due to change in data-flow direction.

Data Byte: reads from the register set by the command byte.

Send Byte Format

S	ADDRESS	WR	ACK	COMMAND	ACK	P
	7 Bits			8 Bits		

Command Byte: sends command with no data, usually used for one-shot command.

Receive Byte Format

S	ADDRESS	RD	ACK	DATA	NACK	P
	7 Bits			8 Bits		

Data Byte: reads data from the register commanded by the last Read Byte.

S = Start Condition
P = Stop Condition
Shaded = Slave Transmission

Figure 3. SMBus Protocols

acknowledge that it successfully received the previous eight bit of data or address.

Data Byte

After a successful ACK of the address byte, the host must transmit the data byte to be written or clock out the data to be read. (See the appropriate timing diagrams.) ACK will be generated after a successful write of a data byte into the TC1068.

Stop Condition (STOP)

Communications must be terminated by a stop condition (a Low to High transition of SDA while SCL is High). The Stop Condition must be communicated by the transmitter to the TC1068. (See TCN75 data sheet for serial bus timing diagrams.)

Command Byte Description

Command	Code	Function
RIT	00h	Read Internal Temp (INT_TEMP)
RET	01h	Read External Temp (EXT_TEMP)
RS	02h	Read Status Byte (STATUS)
RC	03h	Read Configuration Byte (CONFIG)
RCR	04h	Read Conversion Rate Byte (CONV_RATE)
RIHL	05h	Read Internal High Limit (INT_HLIM)
RILL	06h	Read Internal Low Limit (INT_LLIM)
REHL	07h	Read External High Limit (EXT_HLIM)
RELL	08h	Read External Low Limit (EXT_LLIM)
WC	09h	Write Configuration Byte (CONFIG)
WCR	0Ah	Write Conversion Rate Byte (CONV_RATE)
WIHL	0Bh	Write Internal High Limit (INT_HLIM)
WILL	0Ch	Write Internal Low Limit (INT_LLIM)
WEHL	0Dh	Write External High Limit (EXT_HLIM)
WELL	0Eh	Write External Low Limit (EXT_LLIM)
OSHT	0Fh	One Shot Temp Measurement
RMID	FEh	Read Manufacturer ID (MFR_ID)
RMREV	FFh	Read Manufacturer Revision Number (MFR_REV)

NOTE: Proper device operation is NOT guaranteed if undefined locations (10h to FDh) are addressed. In case of erroneous SMBus operation (RECEIVE_BYTE command issued immediately after WRITE_BYTE command) the TC1068 will ACKnowledge the address and return 1111 1111b to signify an error. Under no condition will it implement an SMBus "timeout."

REGISTER SET AND PROGRAMMER'S MODEL

TC1068 Command Set

The TC1068 supports four SMBus command protocols. These are READ_BYTE, WRITE_BYTE, SEND_BYTE, and RECEIVE_BYTE. See System Management Bus Specification Rev. 1.0 for details.

Configuration Register (Config), 8-Bits, Read/Write

Configuration Register (Config)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Mask1	Chip Stop	Reserved					

Bit	POR State	Function	Operation
D[7]	1	Interrupt Mask (see text)	1 = mask ALERT#/ COMP# 0 = don't mask ALERT #/COMP#
D[6]	0	Standby switch	1 = standby, 0 = normal
D[5] – D[0]	0	Reserved – Always returns zero when read.	N/A

A/D Conversion Rate Register (CONV_RATE), 8-Bits, Read/Write

A/D Conversion Rate Register (CONV_RATE)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Reserved					MSB	X	LSB

Bit	POR State	Function	Operation
D[7:3]	0	Reserved – Always returns zero when read.	N/A
D[2:0]	010b	Conversion rate bits.	See below.

A/D Conversion Rate Selection

D2	D1	D0	Conversion Rate Sa/sec
0	0	0	0.0625
0	0	1	0.125
0	1	0	0.25
0	1	1	0.5
1	0	0	1.0
1	0	1	2.0
1	1	0	4.0
1	1	1	8.0

NOTE: Conversion rate denotes actual sampling of both internal *and* external sensors.

Temperature Registers, 8-Bits, Read-Only (INT_TEMP, EXT_TEMP)

The binary value (2's complement format) in these two registers represents temperature of the internal and external sensors following a conversion cycle. The registers are automatically updated in an alternating manner.

Internal Temperature Register (INT_TEMP)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

External Temperature Register (EXT_TEMP)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

Temperature Threshold Setpoint Registers, 8-Bits, Read-Write (INT_HLIM, INT_LLIM, EXT_HLIM, EXT_LLIM)

These registers store the values of the upper and lower temperature setpoints for event detection. The value is in 2's-complement binary. INT_HLIM and INT_LLIM are compared with the INT_TEMP value, and EXT_HLIM and EXT_LLIM are compared with EXT_TEMP. These registers may be written at any time.

Internal High Limit Setpoint Register (INT_HLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

Internal Low Limit Setpoint Register (INT_LLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

External High Limit Setpoint Register (EXT_HLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

External Low Limit Setpoint Register (EXT_LLIM)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	x	x	x	x	x	x	LSB

NOTE: POR states:

INT_HLIM	01111111b	+127°C
INT_LLIM	11001001b	–55°C
EXT_HLIM	01111111b	+127°C
EXT_LLIM	11001001b	–55°C

In the two temperature data and four threshold setpoint registers, each unit value represents one degree (Celsius). The value is in 2's-complement binary format such that a reading of 00000000b corresponds to 0°C. Examples of this temperature-to-binary value relationship are shown in the following table.

Temperature-to-Digital Value Conversion (INT_TEMP, EXT_TEMP, INT_HLIM, INT_LLIM, EXT_HLIM, EXT_LLIM)

Actual Temperature	Rounded Temperature	Binary Value	Hex Value
+130.00°C	+127°C	01111111	7F
+127.00°C	+127°C	01111111	7F
+126.50°C	+127°C	01111111	7F
+25.25°C	+25°C	00011001	19
+0.50°C	+1°C	00000001	01
+0.25°C	0°C	00000000	00
0.00°C	0°C	00000000	00
–0.25°C	0°C	00000000	00
–0.50°C	0°C	00000000	00
–0.75°C	–1°C	11111111	FF
–1.00°C	–1°C	11111111	FF
–25.00°C	–25°C	11100111	E7
–25.25°C	–25°C	11100110	E7
–54.75°C	–55°C	11001001	C9
–55.00°C	–55°C	11001001	C9
–65.00°C	–65°C	10111111	BF

TC1068

Status Register (Status), 8-Bits, Read Only:

Status Register (Status)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
Busy	Flag1	Flag2	Flag3	Flag4	Flag5	Flag6	Reserved

Bit(s)	POR State	Function	Operation*
D[7]	0	Signal A/D converter is busy.	1 = A/D busy, 0 = A/D idle
D[6]	0	Interrupt flag for INT_HLIM event	1 = interrupt occurred, 0 = none
D[5]	0	Interrupt flag for INT_LLIM event	1 = interrupt occurred, 0 = none
D[4]	0	Interrupt flag for EXT_HLIM event	1 = interrupt occurred, 0 = none
D[3]	0	Interrupt flag for EXT_LLIM event	1 = interrupt occurred, 0 = none
D[2]	0	External diode “fault” flag	1 = external diode fault 0 = external diode OK
D[1:0]	0	Reserved – Always returns zero.	N/A

NOTE: All status bits are cleared after a read operation is performed on STATUS. The EXT_TEMP register will read +127°C if an external diode “open”.

Manufacturer’s Identification Register (MFR_ID), 8-Bits, Read Only:

Manufacturer’s Identification Register (MFR_ID)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	X	X	X	X	X	X	LSB

Manufacturer’s Revision Register (MFR_REV), 8-Bits, Read Only:

Manufacturer’s Revision Register (MFR_REV)

D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
MSB	X	X	X	X	X	X	LSB

Register Set Summary:

The TC1068’s register set is summarized in the following table. All registers are 8-bits wide.

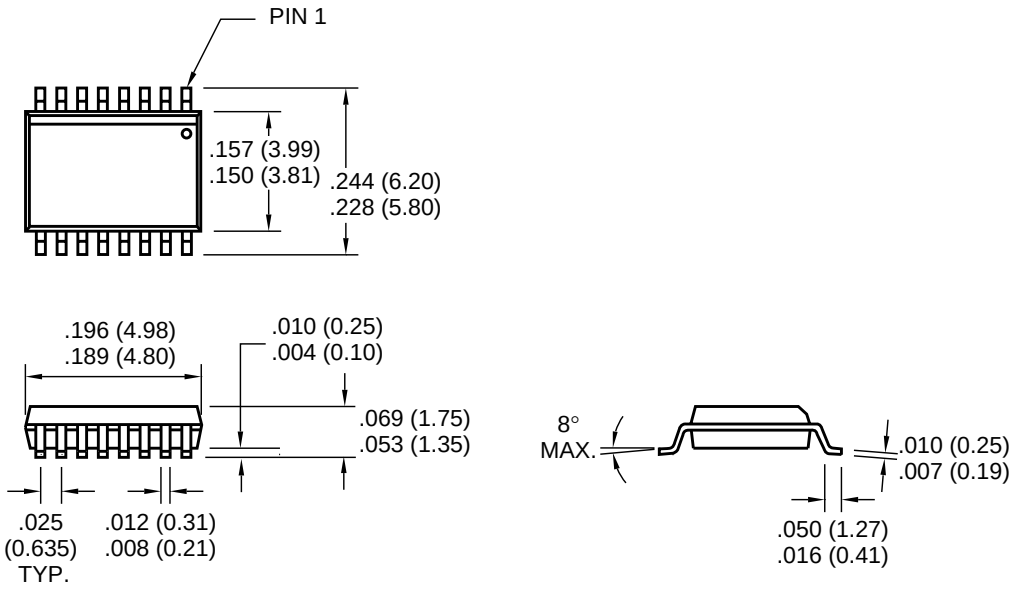
Name	Description	POR State	Read	Write
INT_TEMP	Internal sensor temperature (2’s complement)	0000 0000b*	✓	
EXT_TEMP	External sensor temperature (2’s complement)	0000 0000b*	✓	
STATUS	STATUS register	0000 0000b	✓	
CONFIG	CONFIG register	1000 0000b	✓	✓
CONV_RATE	A/D conversion rate register	0000 0010b	✓	✓
INT_HLIM	Internal high limit (2’s complement)	0111 1111b	✓	✓
INT_LLIM	Internal low limit (2’s complement)	1100 1001b	✓	✓
EXT_HLIM	External high limit (2’s complement)	0111 1111b	✓	✓
EXT_LLIM	External low limit (2’s complement)	1100 1001b	✓	✓
MFR_ID	ASCII for letter “T” (Microchip)	0101 0100b	✓	
MFR_REV	Serial device revision #	**	✓	

***NOTE:** The INT_TEMP and EXT_TEMP register immediately will be updated by the A/D converter after POR. If STBY# is low at power-up, INT_TEMP and EXT_TEMP will remain in POR state (0000 0000b).

**MFR_REV will sequence 01h, 02h, 03h, etc. by mask changes.

PACKAGE DIMENSIONS

16-Pin QSOP (Narrow)



Dimensions: inches (mm)

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