

FEATURES

- 3.3V and 5V power supply options
- 50ps output-to-output skew
- Synchronous enable/disable
- Master Reset for synchronization
- Internal 75KΩ input pull-down resistors
- Available in 20-pin SOIC package

**Precision Edge®****DESCRIPTION**

The SY10/100EL38/L are low skew ÷2, ÷4/6 clock generation chips designed explicitly for low skew clock generation applications. The internal dividers are synchronous to each other, therefore, the common output edges are all precisely aligned. The devices can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. In addition, by using the VBB output, a sinusoidal source can be AC-coupled into the device. If a single-ended input is to be used, the VBB output should be connected to the CLK input and bypassed to ground via a 0.01μF capacitor. The VBB output is designed to act as the switching reference for the input of the EL38/L under single-ended input conditions. As a result, this pin can only source/sink up to 0.5mA of current.

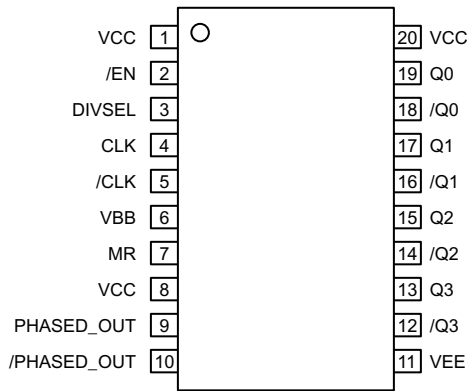
The common enable (\overline{EN}) is synchronous so that the internal dividers will only be enabled/disabled when the internal clock is already in the LOW state. This avoids any chance of generating a runt clock pulse on the internal clock when the device is enabled/disabled as can happen with an asynchronous control. An internal runt pulse could lead to losing synchronization between the internal divider stages. The internal enable flip-flop is clocked on the falling edge of the input clock, therefore, all associated specification limits are referenced to the negative edge of the clock input.

The Phase_Out output will go HIGH for one clock cycle whenever the ÷2 and the ÷4/6 outputs are both transitioning from a LOW to a HIGH. This output allows for clock synchronization within the system.

Upon start-up, the internal flip-flops will attain a random state; the master reset (MR) input allows for the synchronization of the internal dividers, as well as for multiple EL38/Ls in a system.

PACKAGE/ORDERING INFORMATION

Ordering Information⁽¹⁾



20-Pin SOIC (Z20-1)

| Part Number | Package Type | Operating Range | Package Marking | Lead Finish |
|----------------------------------|--------------|-----------------|--|----------------|
| SY10EL38LZC | Z20-1 | Commercial | SY10EL38LZC | Sn-Pb |
| SY10EL38LZCTR ⁽²⁾ | Z20-1 | Commercial | SY10EL38LZC | Sn-Pb |
| SY100EL38LZC | Z20-1 | Commercial | SY100EL38LZC | Sn-Pb |
| SY100EL38LZCTR ⁽²⁾ | Z20-1 | Commercial | SY100EL38LZC | Sn-Pb |
| SY10EL38LZI | Z20-1 | Industrial | SY10EL38LZI | Sn-Pb |
| SY10EL38LZITR ⁽²⁾ | Z20-1 | Industrial | SY10EL38LZI | Sn-Pb |
| SY100EL38LZI | Z20-1 | Industrial | SY100EL38LZI | Sn-Pb |
| SY100EL38LZITR ⁽²⁾ | Z20-1 | Industrial | SY100EL38LZI | Sn-Pb |
| SY10EL38LZG ⁽³⁾ | Z20-1 | Industrial | SY10EL38LZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY10EL38LZGTR ^(2, 3) | Z20-1 | Industrial | SY10EL38LZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EL38LZG ⁽³⁾ | Z20-1 | Industrial | SY100EL38LZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |
| SY100EL38LZGTR ^(2, 3) | Z20-1 | Industrial | SY100EL38LZG with Pb-Free bar-line indicator | Pb-Free NiPdAu |

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC Electricals only.
2. Tape and Reel.
3. Pb-Free package is recommended for new designs.

PIN NAMES

| Pin | Function |
|---------------------------------|---------------------------------|
| CLK | Differential Clock Inputs |
| $\overline{\text{EN}}$ | Synchronous Enable |
| MR | Master Reset |
| V _{BB} | Reference Output |
| Q ₀ , Q ₁ | Differential $\div 2$ Outputs |
| Q ₂ , Q ₃ | Differential $\div 4/6$ Outputs |
| DIVSEL | Frequency Select Input |

TRUTH TABLE

| CLK | $\overline{\text{EN}}$ | MR | Function |
|-----|------------------------|----|------------------------|
| Z | L | L | Divide |
| ZZ | H | L | Hold Q ₀₋₃ |
| X | X | H | Reset Q ₀₋₃ |

NOTE:

Z = LOW-to-HIGH transition

ZZ = HIGH-to-LOW transition

| DIVSEL | Q ₂ , Q ₃ OUTPUTS |
|--------|---|
| 0 | Divide by 4 |
| 1 | Divide by 6 |

DC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

| Symbol | Parameter | T _A = -40°C | | | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit |
|-----------------|--------------------------|------------------------|------|-------|----------------------|------|-------|------------------------|------|-------|------------------------|------|-------|------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | |
| I _{EE} | Power Supply Current | | | | | | | | | | | | | mA |
| | 10EL | 35 | 50 | 65 | 35 | — | 65 | 35 | — | 65 | 35 | — | 65 | |
| | 100EL | 35 | 50 | 65 | 35 | — | 65 | 35 | — | 65 | 35 | — | 75 | |
| V _{BB} | Output Reference Voltage | | | | | | | | | | | | | V |
| | 10EL | -1.43 | — | -1.30 | -1.38 | — | -1.27 | -1.35 | — | -1.25 | -1.31 | — | -1.19 | |
| | 100EL | -1.38 | — | -1.26 | -1.38 | — | -1.26 | -1.38 | — | -1.26 | -1.38 | — | -1.26 | |
| I _{IH} | Input High Current | — | — | 150 | — | — | 150 | — | — | 150 | — | — | 150 | μA |

NOTE:

1. Parametric values specified at:
- | | | |
|---------------------------|---------------------|------------------|
| 5 volt Power Supply Range | 100EL38 Series: | -4.2V to -5.5V. |
| | 10EL38 Series | -4.75V to -5.5V. |
| 3 volt Power Supply Range | 10/100EL38L Series: | -3.0V to -3.8V. |

AC ELECTRICAL CHARACTERISTICS⁽¹⁾V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND

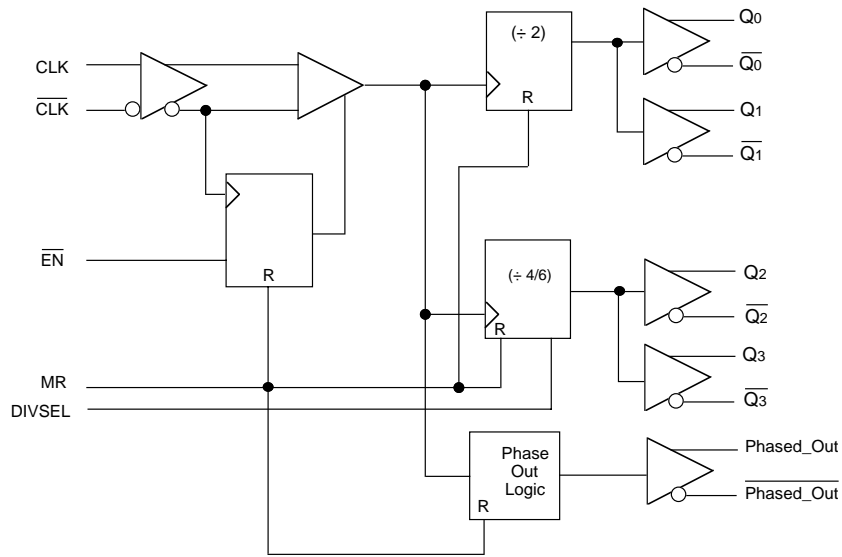
| Symbol | Parameter | T _A = -40°C | | | T _A = 0°C | | | T _A = +25°C | | | T _A = +85°C | | | Unit | |
|----------------------------------|---|------------------------|------|------|----------------------|------|------|------------------------|------|------|------------------------|------|------|------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| f _{MAX} | Maximum Toggle Frequency | 1000 | — | — | 1000 | — | — | 1000 | — | — | 1000 | — | — | MHz | |
| t _{PD} | Propagation Delay to Output | | | | | | | | | | | | | ps | |
| | CLK → Output (Diff.) | 950 | — | 1150 | 950 | — | 1150 | 970 | — | 1170 | 1050 | — | 1250 | | |
| | CLK → Output (S.E.) | 900 | — | 1200 | 900 | — | 1200 | 920 | — | 1220 | 1000 | — | 1300 | | |
| | MR → Output | 600 | — | 900 | 600 | — | 900 | 600 | — | 900 | 600 | — | 900 | | |
| t _{skew} | Within-Device Skew ⁽²⁾ Q ₀ — Q ₃ | — | — | 50 | — | — | 50 | — | — | 50 | — | — | 50 | ps | |
| | All | — | — | 75 | — | — | 75 | — | — | 75 | — | — | 75 | | |
| | Part-to-Part Q ₀ — Q ₃ (Diff.) | — | — | 200 | — | — | 200 | — | — | 200 | — | — | 200 | | |
| | All | — | — | 240 | — | — | 240 | — | — | 240 | — | — | 240 | | |
| t _s | Set-up Time $\overline{EN} \rightarrow \overline{CLK}$ | 300 | 150 | — | — | 150 | — | — | 150 | — | — | 150 | — | ps | |
| | DIVSEL → CLK | 300 | — | — | — | — | — | — | — | — | — | — | — | | |
| t _H | Hold Time $\overline{CLK} \rightarrow \overline{EN}$ | 400 | 150 | — | 400 | 150 | — | 400 | 150 | — | 400 | 150 | — | ps | |
| | CLK → DIVSEL | 400 | 200 | — | 400 | 200 | — | 400 | 200 | — | 400 | 200 | — | | |
| V _{PP} | Minimum Input Swing ⁽³⁾ CLK | 250 | — | — | 250 | — | — | 250 | — | — | 250 | — | — | mV | |
| V _{CMR} | Common Mode Range ⁽⁴⁾ CLK | -1.3 | — | -0.4 | -1.4 | — | -0.4 | -1.4 | — | -0.4 | -1.4 | — | -0.4 | V | |
| t _{RR} | Reset Recovery Time | — | — | 100 | — | — | 100 | — | — | 100 | — | — | 100 | ps | |
| t _{PW} | Minimum Pulse Width CLK | 800 | — | — | 800 | — | — | 800 | — | — | 800 | — | — | ps | |
| | MR | 700 | — | — | 700 | — | — | 700 | — | — | 700 | — | — | | |
| t _r t _f | Output Rise/Fall Times (20% — 80%) | Q | 280 | — | 550 | 280 | — | 550 | 280 | — | 550 | 280 | — | 550 | ps |

NOTES:

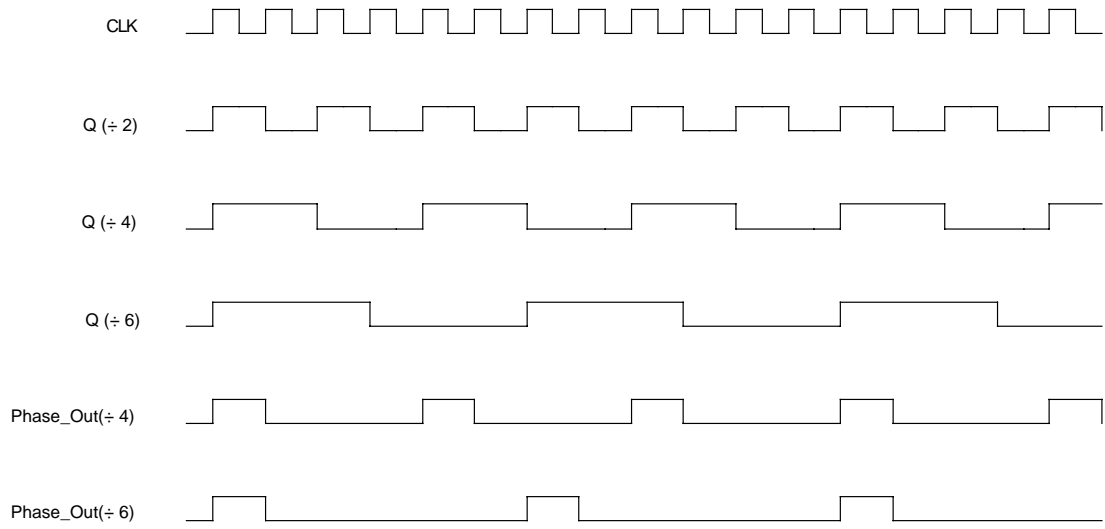
- Parametric values specified at:

| | | |
|---------------------------|---------------------|------------------|
| 5 volt Power Supply Range | 100EL38 Series: | -4.2V to -5.5V. |
| | 10EL38 Series | -4.75V to -5.5V. |
| 3 volt Power Supply Range | 10/100EL38L Series: | -3.0V to -3.8V. |
- Skew is measured between outputs under identical transitions.
- Minimum input swing for which AC parameters are guaranteed. The device will function reliably with differential inputs down to 100mV.
- The CMR range is referenced to the most positive side of the differential input signal. Normal operation is obtained if the HIGH level falls within the specified range and the peak-to-peak voltage lies between V_{PP} min. and 1V. The lower end of the CMR range varies 1:1 with V_{EE}. The numbers in the spec table assume a nominal V_{EE} = -3.3V. Note for PECL operation, the V_{CMR} (min) will be fixed at 3.3V - I_{VCMR} (min)I.

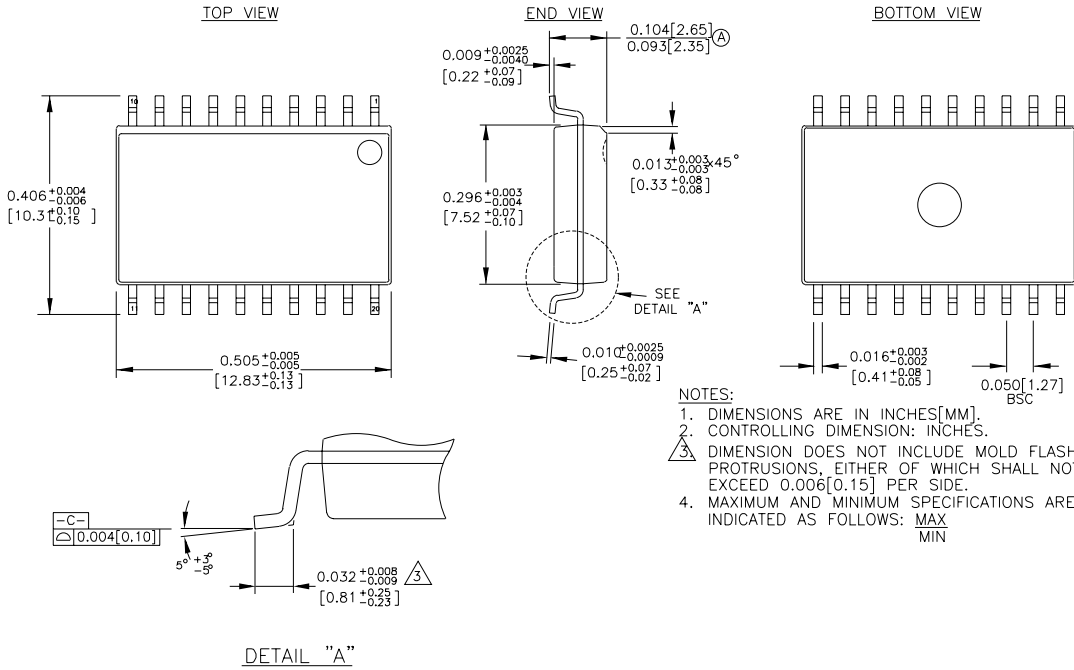
LOGIC DIAGRAM



TIMING DIAGRAMS



20-PIN SOIC .300" WIDE (Z20-1)



Rev. 03

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