# STGIPS10K60T

SLLIMM™
small low-loss intelligent molded module

Preliminary data

Features

- IPM 10 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- Short-circuit rugged IGBTs
- $V_{CE(sat)}$ negative temperature coefficient
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Undervoltage lockout
- Internal bootstrap diode
- Interlocking function
- Shut down function
- DBC substrate leading to low thermal resistance
- Isolation rating of 2500 Vrms/min
- 5 kΩ NTC for temperature control

SDIP-25L
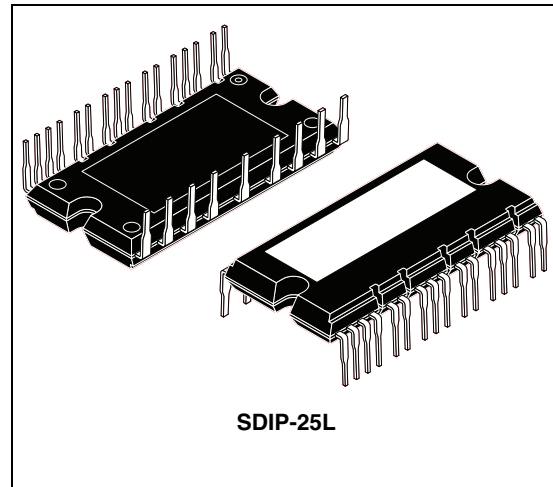
Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners and sewing machines

Description

This intelligent power module provides a compact, high performance AC motor drive in a simple, rugged design. Combining ST proprietary control ICs with the most advanced short-circuit-rugged IGBT system technology, this device is ideal for 3-phase inverters in applications such as home appliances and air conditioners. SLLIMM™ is a trademark of STMicroelectronics.

Table 1.   Device summary

Order code	Marking	Package	Packaging
STGIPS10K60T	GIPS10K60T	SDIP-25L	Tube

www.st.com

Contents

1 Internal block diagram and pin configuration

Figure 1. Internal block diagram
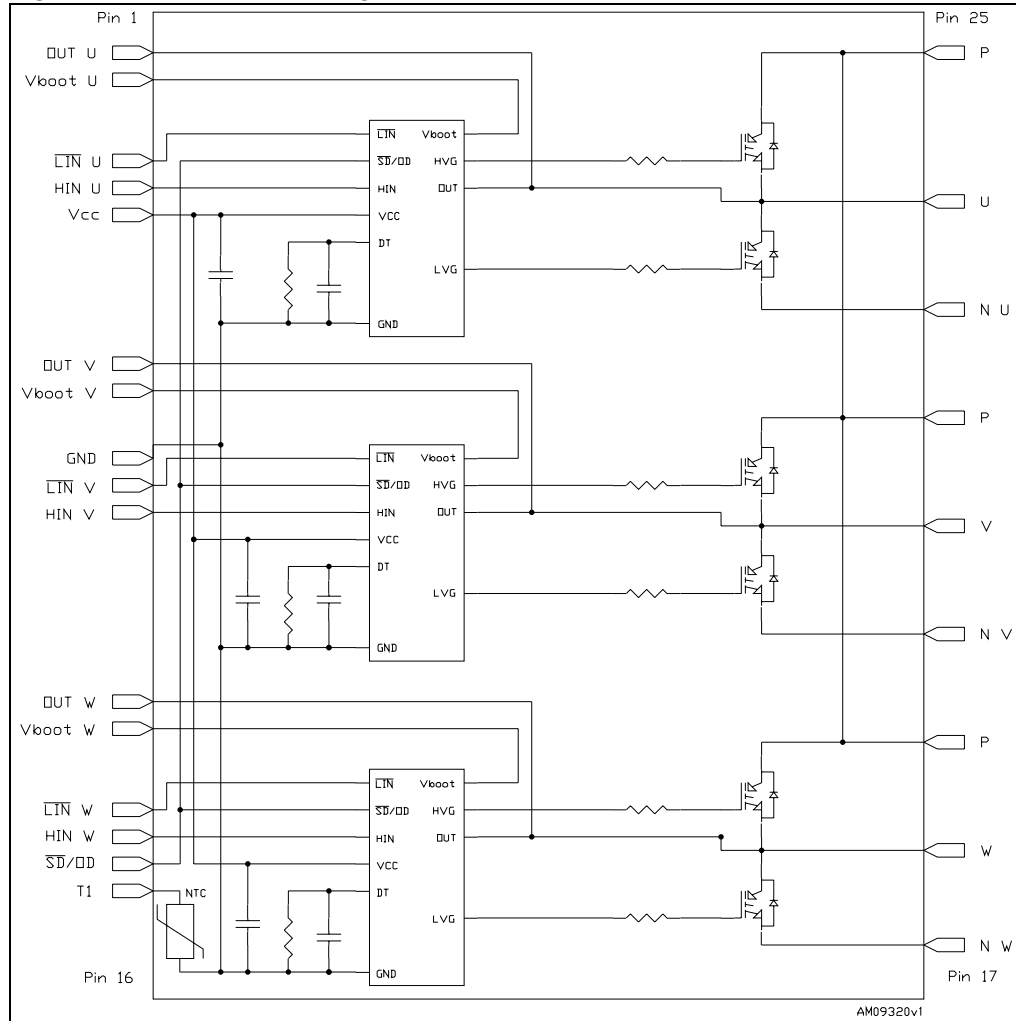
Table 2. Pin description

Pin n°	Symbol	Description
1	OUT_U	High side reference output for U phase
2	$V_{boot\ U}$	Bootstrap voltage for U phase
3	$\overline{LIN}_U$	Low side logic input for U phase
4	HIN_U	High side logic input for U phase
5	V_{CC}	Low voltage power supply
6	OUT_V	High side reference output for V phase
7	$V_{boot\ V}$	Bootstrap voltage for V phase
8	GND	Ground
9	$\overline{LIN}_V$	Low side logic input for V phase
10	HIN_V	High side logic input for V phase
11	OUT_W	High side reference output for W phase
12	$V_{boot\ W}$	Bootstrap voltage for W phase
13	$\overline{LIN}_W$	Low side logic input for W phase
14	HIN_W	High side logic input for W phase
15	$\overline{SD}$ / OD	Shut down logic input (active low) / open drain (comparator output)
16	T1	NTC thermistor terminal
17	N_W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N_V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N_U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)
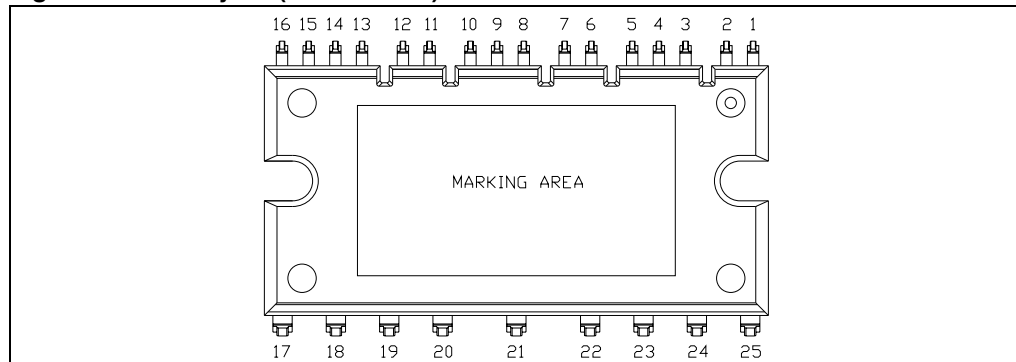
2   Electrical ratings

2.1   Absolute maximum ratings

Table 3.   Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U, N_V, N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U, N_V, N_W	500	V
V_{CES}	Each IGBT collector emitter voltage (V_{IN}[1] = 0)	600	V
$\pm\ I_C$ [2]	Each IGBT continuous collector current at $T_C = 25°C$	10	A
$\pm\ I_{CP}$ [3]	Each IGBT pulsed collector current	20	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25°C$	33	W
t_{scw}	Short-circuit withstand time, $V_{CE} = 0.5\ V_{(BR)CES}$ $T_j = 125\ °C$, $V_{CC} = V_{boot} = 15\ V$, V_{IN} [1] = 5 V	5	µs

1.   Applied between HIN_i, LIN_i and GND for i = U, V, W.

2.   Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3.   Pulse width limited by max junction temperature.

Table 4.   Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U, OUT_V, OUT_W - GND	V_{boot} - 21 to V_{boot} + 0.3	V
V_{CC}	Low voltage power supply	-0.3 to +21	V
V_{boot}	Bootstrap voltage applied between $V_{boot\ i}$ - OUT_i for i = U, V, W	-0.3 to 620	V
V_{IN}	Logic input voltage applied between HIN, $\overline{LIN}$ and GND	-0.3 to 15	V
$V_{\overline{SD}/OD}$	Open drain voltage	-0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

Table 5.   Total system

Symbol	Parameter	Value	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, t = 60 sec.)	2500	V
T_C	Module case operation temperature	-40 to 125	°C
T_J [1]	Operating junction temperature	-40 to 150	°C

1. The maximum junction temperature rating of the power chips integrated within the SDIP module is 150°C ($@T_C \leq 100°C$). To ensure safe operation of the SDIP module, the average junction temperature should be limited to $T_J(avg) \leq 125°C$ ($@T_C \leq 100°C$)

2.2   Thermal data

Table 6.   Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT max.	3.8	°C/W
	Thermal resistance junction-case single diode max.	5.5	°C/W

3   Electrical characteristics

T_J = 25 °C unless otherwise specified.

Table 7.   Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot}$ = 15 V, $V_{IN}^{(1)}$= 5 V, I_C = 5 A	-	2.1	2.5	V
		$V_{CC} = V_{boot}$ = 15 V, $V_{IN}^{(1)}$= 5 V, I_C = 5 A, T_j = 125 °C	-	1.8		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)}$ = 0 "logic state")	V_{CE} = 600 V $V_{CC} = V_{boot}$ = 15 V	-		150	µA
V_F	Diode forward voltage	($V_{IN}^{(1)}$ = 0 "logic state"), I_C = 5 A	-		1.9	V
Inductive load switching time and energy						
t_{on}	Turn-on time	V_{DD} = 300 V, $V_{CC} = V_{boot}$ = 15 V, $V_{IN}^{(1)}$= 0 ÷ 5 V, I_C = 5 A (see *Figure 4*)	-	320	-	ns
$t_{c(on)}$	Crossover time (on)		-	70	-	
t_{off}	Turn-off time		-	430	-	
$t_{c(off)}$	Crossover time (off)		-	135	-	
t_{rr}	Reverse recovery time		-	130	-	
E_{on}	Turn-on switching losses		-	65	-	µJ
E_{off}	Turn-off switching losses		-	75	-	

1.   Applied between HIN_i, LIN_i and GND for i = U, V, W.

Note: *t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.*
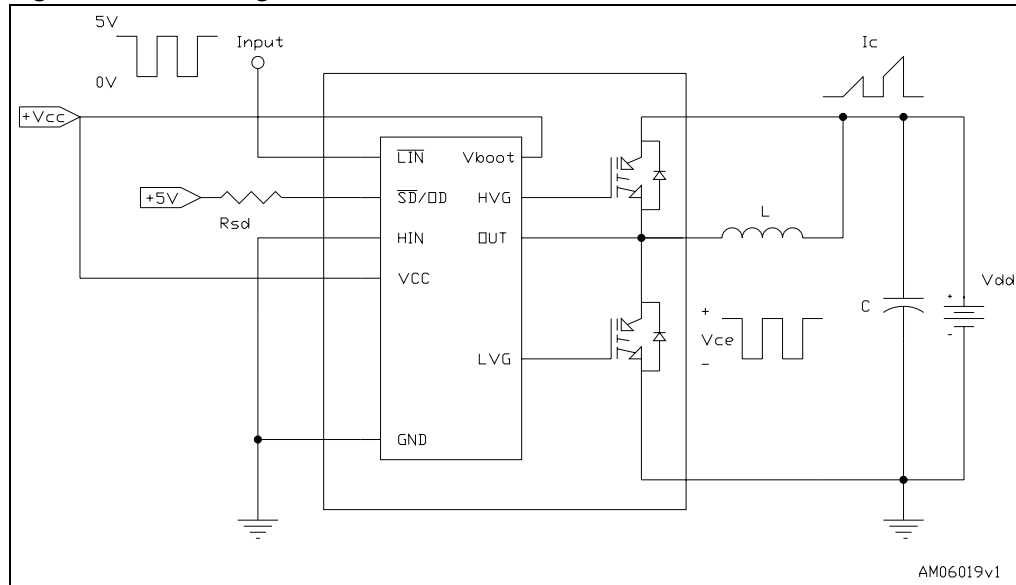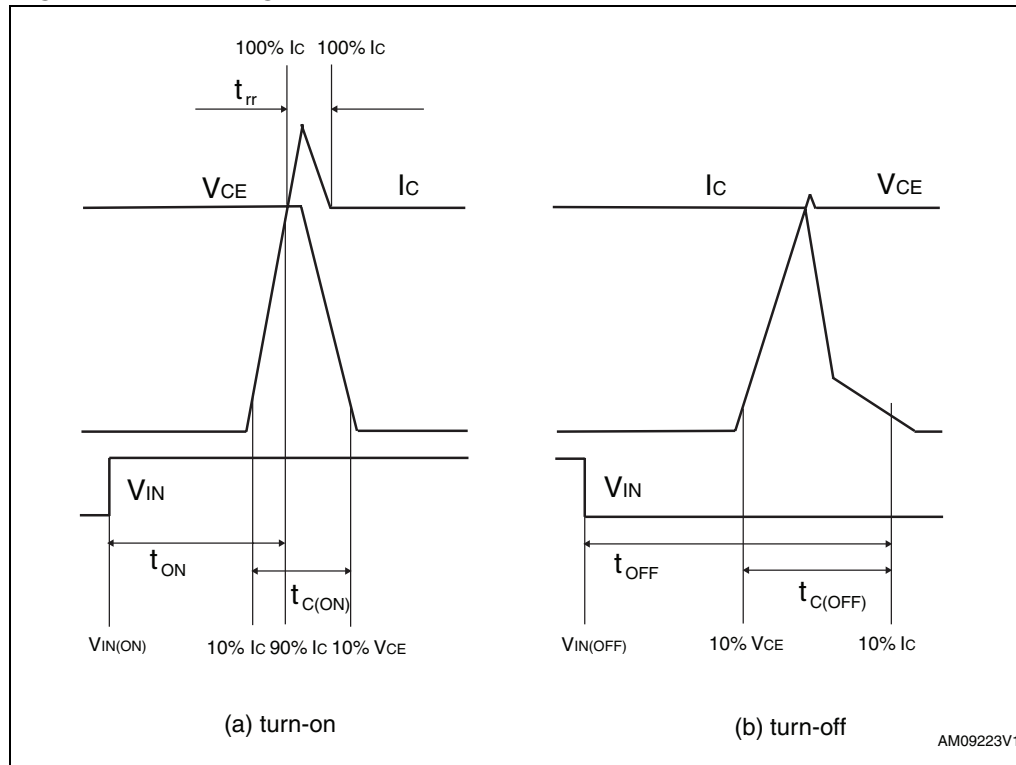
Figure 3.   Switching time test circuit

Figure 4.   Switching time definition

Note: *Figure 4 "Switching time definition" refers to HIN inputs (active high). For $\overline{LIN}$ inputs (active low), V_{IN} polarity must be inverted for turn-on and turn-off.*

3.1 Control part

Table 8.   Low voltage power supply (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{cc_hys}	V_{cc} UV hysteresis		1.2	1.5	1.8	V
V_{cc_thON}	V_{cc} UV turn ON threshold		11.5	12	12.5	V
V_{cc_thOFF}	V_{cc} UV turn OFF threshold		10	10.5	11	V
I_{qccu}	Undervoltage quiescent supply current	V_{CC} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V; HIN = 0			450	µA
I_{qcc}	Quiescent current	V_{cc} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ = 5 V HIN = 0			3.5	mA

Table 9.   Bootstrapped voltage (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{BS_hys}	V_{BS} UV hysteresis		1.2	1.5	1.8	V
V_{BS_thON}	V_{BS} UV turn ON threshold		10.6	11.5	12.4	V
V_{BS_thOFF}	V_{BS} UV turn OFF threshold		9.1	10	10.9	V
I_{QBSU}	Undervoltage V_{BS} quiescent current	V_{BS} = 10 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V		70	110	µA
I_{QBS}	V_{BS} quiescent current	V_{BS} = 15 V $\overline{SD}$/OD = 5 V; $\overline{LIN}$ and HIN = 5 V		150	210	µA
$R_{DS(on)}$	Bootstrap driver on resistance	LVG ON		120		Ω

Table 10.   Logic inputs (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic "1" input bias current	HIN = 15 V	110	175	260	µA
I_{HINl}	HIN logic "0" input bias current	HIN = 0 V			1	µA
I_{LINl}	$\overline{LIN}$ logic "1" input bias current	$\overline{LIN}$ = 0 V	3	6	20	µA
I_{LINh}	$\overline{LIN}$ logic "0" input bias current	$\overline{LIN}$ = 15 V			1	µA
I_{SDh}	$\overline{SD}$ logic "0" input bias current	$\overline{SD}$ = 15 V	30	120	300	µA
I_{SDl}	$\overline{SD}$ logic "1" input bias current	$\overline{SD}$ = 0 V			3	µA
Dt	Dead time	see *Figure 8*		600		ns

Table 11. Shut down characteristics (V_{CC} = 15 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{ol}	Open drain low level output voltage	I_{od} = - 3 mA	-		0.5	V
t_{sd}	Shut down to high / low side driver propagation delay	V_{OUT} = 0, V_{boot} = V_{CC}, V_{IN} = 0 to 3.3 V	50	125	200	ns

Table 12. Truth table

Condition	Logic input (V_I)			Output	
	$\overline{SD}$/OD	$\overline{LIN}$	HIN	LVG	HVG
Shutdown enable half-bridge tri-state	L	X	X	L	L
Interlocking half-bridge tri-state	H	L	H	L	L
0 ''logic state" half-bridge tri-state	H	H	L	L	L
1 "logic state" low side direct driving	H	L	L	H	L
1 "logic state" high side direct driving	H	H	H	L	H

Note: *X: don't care*

Figure 5. Maximum $I_{C(RMS)}$ current vs. switching frequency [1]
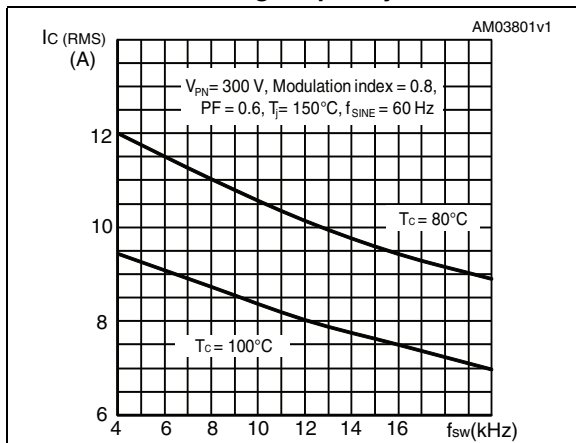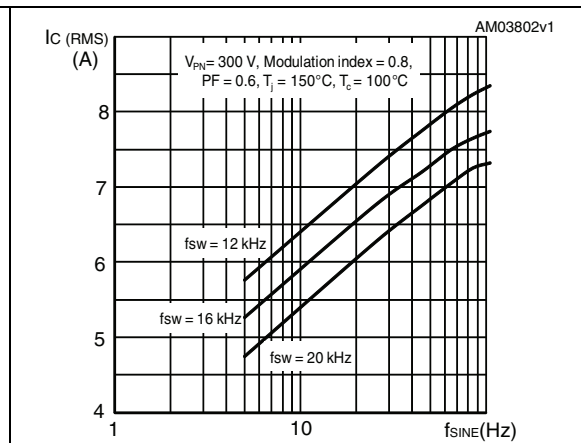

Figure 6. Maximum $I_{C(RMS)}$ current vs. f_{SINE} [1]

1. Simulated curves refer to typical IGBT parameters and maximum R_{thJC}.
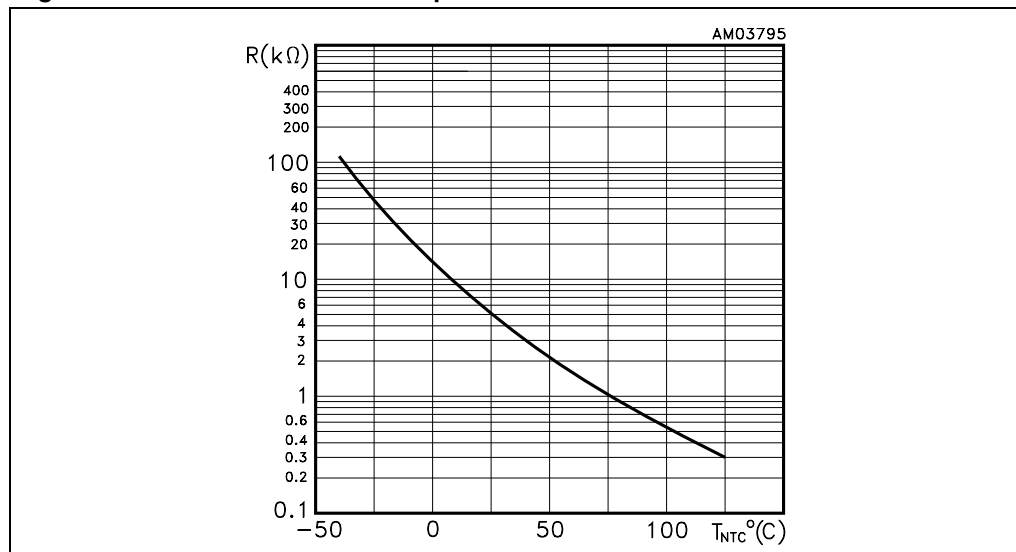
3.1.1 NTC thermistor

Table 13. NTC thermistor

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit.
R_{25}	Resistance	$T_C = 25°C$		5		$k\Omega$
R_{125}	Resistance	$T_C = 125°C$		300		Ω
B	B-constant	$T_C = 25°C$		3435		K
T	Operating temperature		-40		125	°C

Equation 1: resistance variation vs. temperature

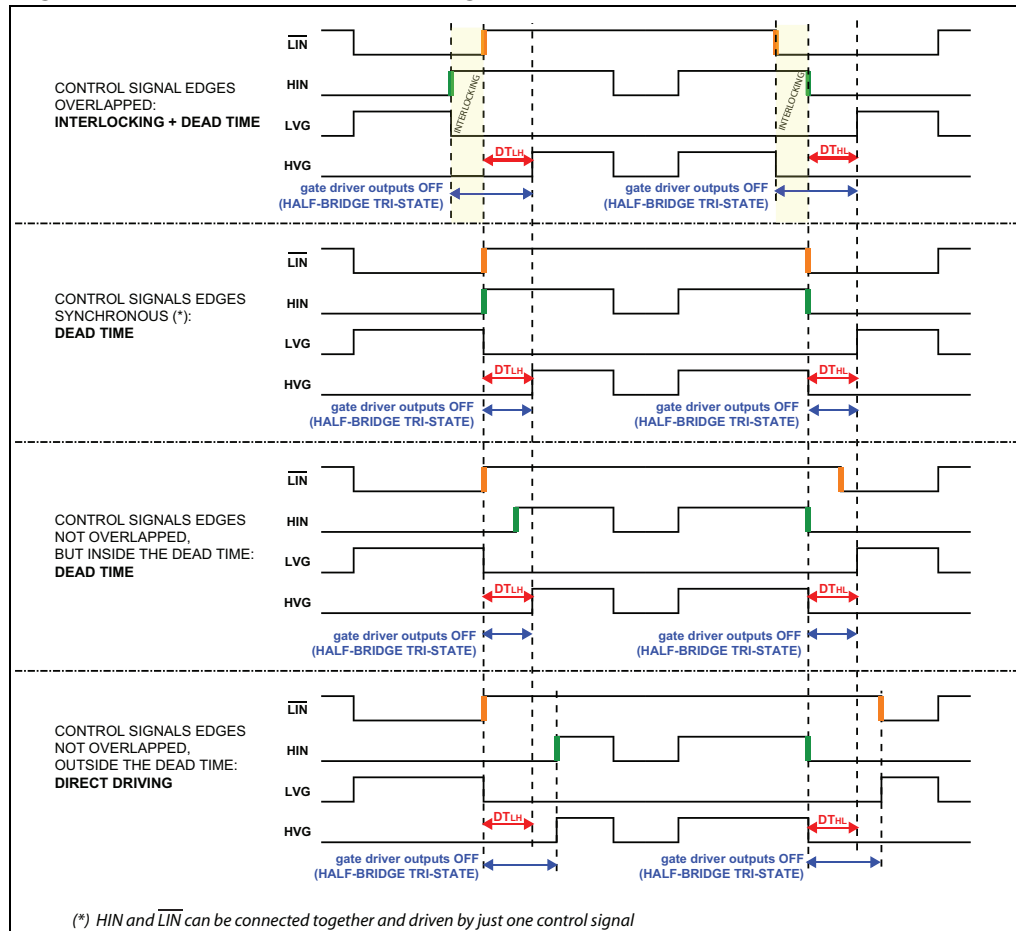$$R(T) = R_{25} \cdot e^{B\left(\frac{1}{T} - \frac{1}{298}\right)}$$

Where T are temperatures in Kelvins.

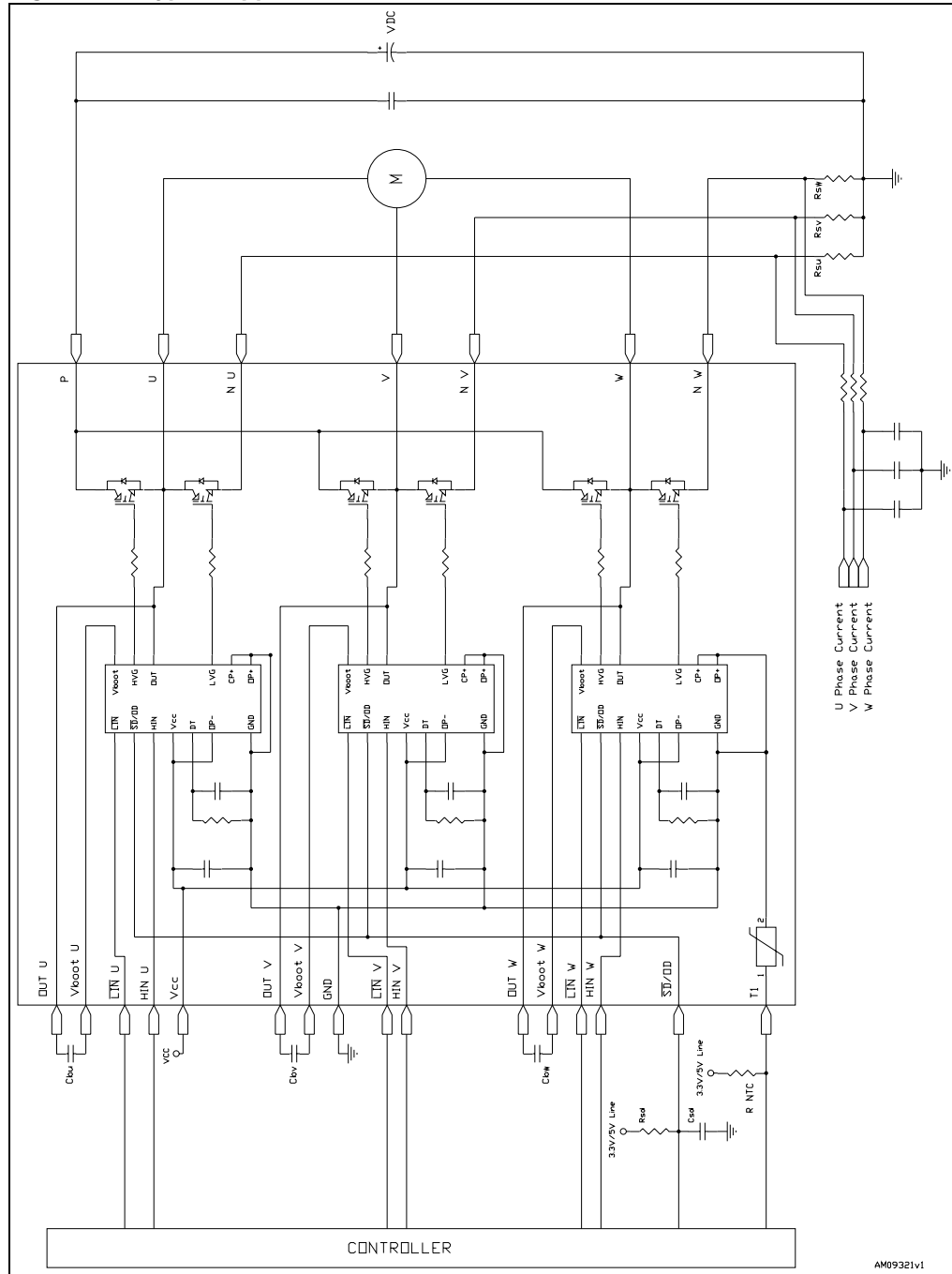**Figure 7. NTC resistance vs. temperature**

3.2 Waveforms definitions

Figure 8. Dead time and interlocking waveforms definitions

(*) HIN and $\overline{LIN}$ can be connected together and driven by just one control signal

4   Applications information

Figure 9.   Typical application circuit

4.1   Recommendations

- Input signal HIN is active high logic. A 85 kΩ (typ.) pull down resistor is built-in for each high side input. If an external RC filter is used, for noise immunity, pay attention to the variation of the input signal level.

- Input signal /LIN is active low logic. A 720 kΩ (typ.) pull-up resistor, connected to an internal 5V regulator through a diode, is built-in for each low side input.

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.

- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.

- Each capacitor should be located as nearby the pins of IPM as possible.

- Low inductance shunt resistors should be used for phase leg current sensing.

- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.

- The $\overline{\text{SD}}$/OD signal should be pulled up to 5 V / 3.3 V with an external resistor.

Table 14.   Recommended operating conditions

Symbol	Parameter	Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P-Nu, Nv, Nw		300	400	V
V_{CC}	Control supply voltage	Applied between V_{CC}-GND	13.5	15	18	V
V_{BS}	High side bias voltage	Applied between V_{BOOTi}-OUT_i for i = U, V, W	13		18	V
t_{dead}	Blanking time to prevent Arm-short	For each input signal	1			μs
f_{PWM}	PWM input signal	-40°C < T_c < 100°C -40°C < T_j < 125°C			20	kHz

# 5   Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Please refer to dedicated technical note TN0107 for mounting instructions.
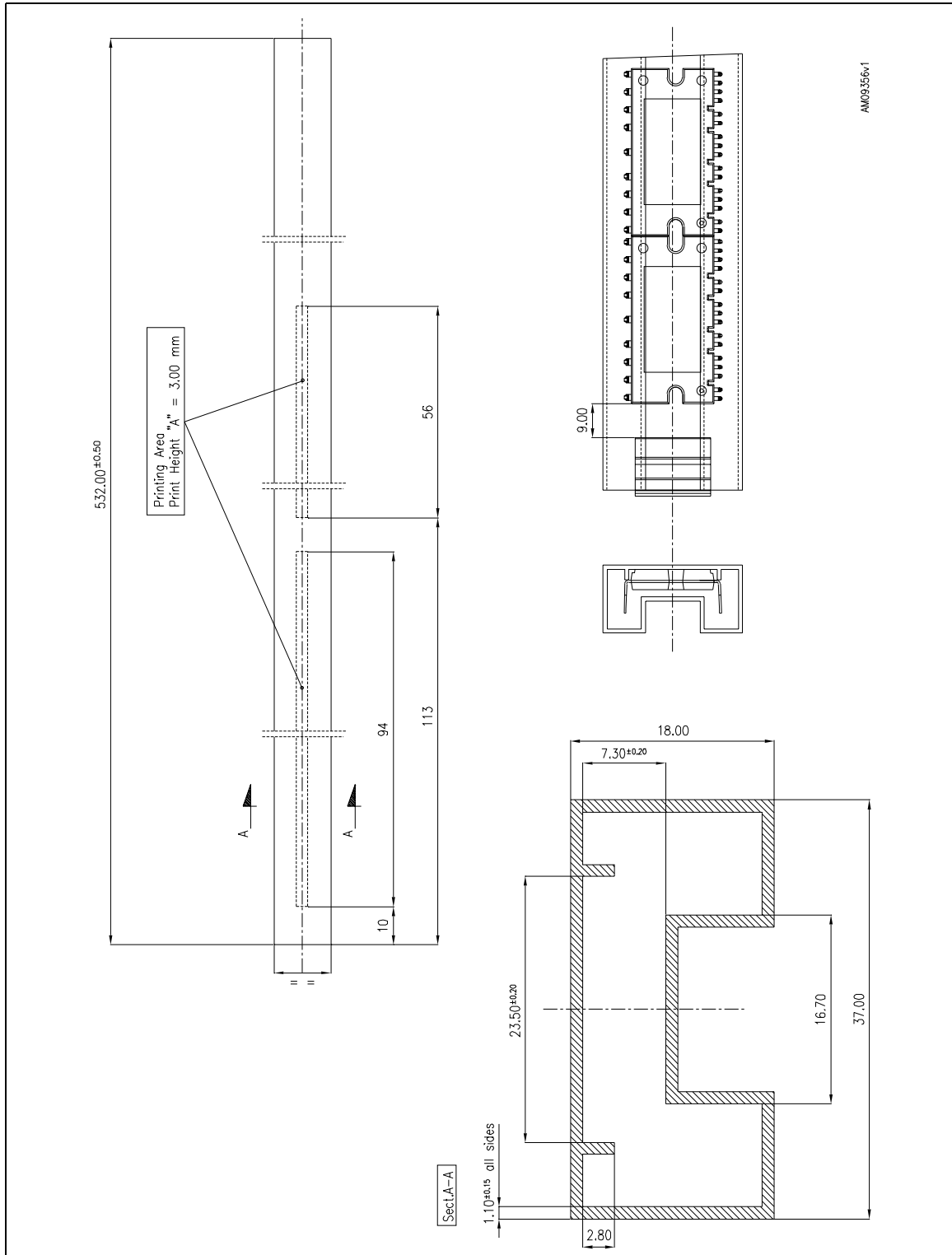
Table 15.   SDIP-25L mechanical data

Dim.	(mm.)		
	Min.	Typ.	Max.
A	44		44.8
A1	0.95		1.75
A2	1.2		2
A3	39		39.8
B	21.6		22.4
B1	11.45		12.25
B2	24.83	25.22	25.63
C	5		5.8
C1	6.4		7.4
C2	11.1		12.1
e	1.95	2.35	2.75
e1	3.2	3.6	4
e2	4.3	4.7	5.1
e3	6.1	6.5	6.9
F	0.8	1.0	1.2
F1	0.3	0.5	0.7
R	1.35		2.15
T	0.4	0.55	0.7

Figure 10. SDIP-25L drawing dimensions
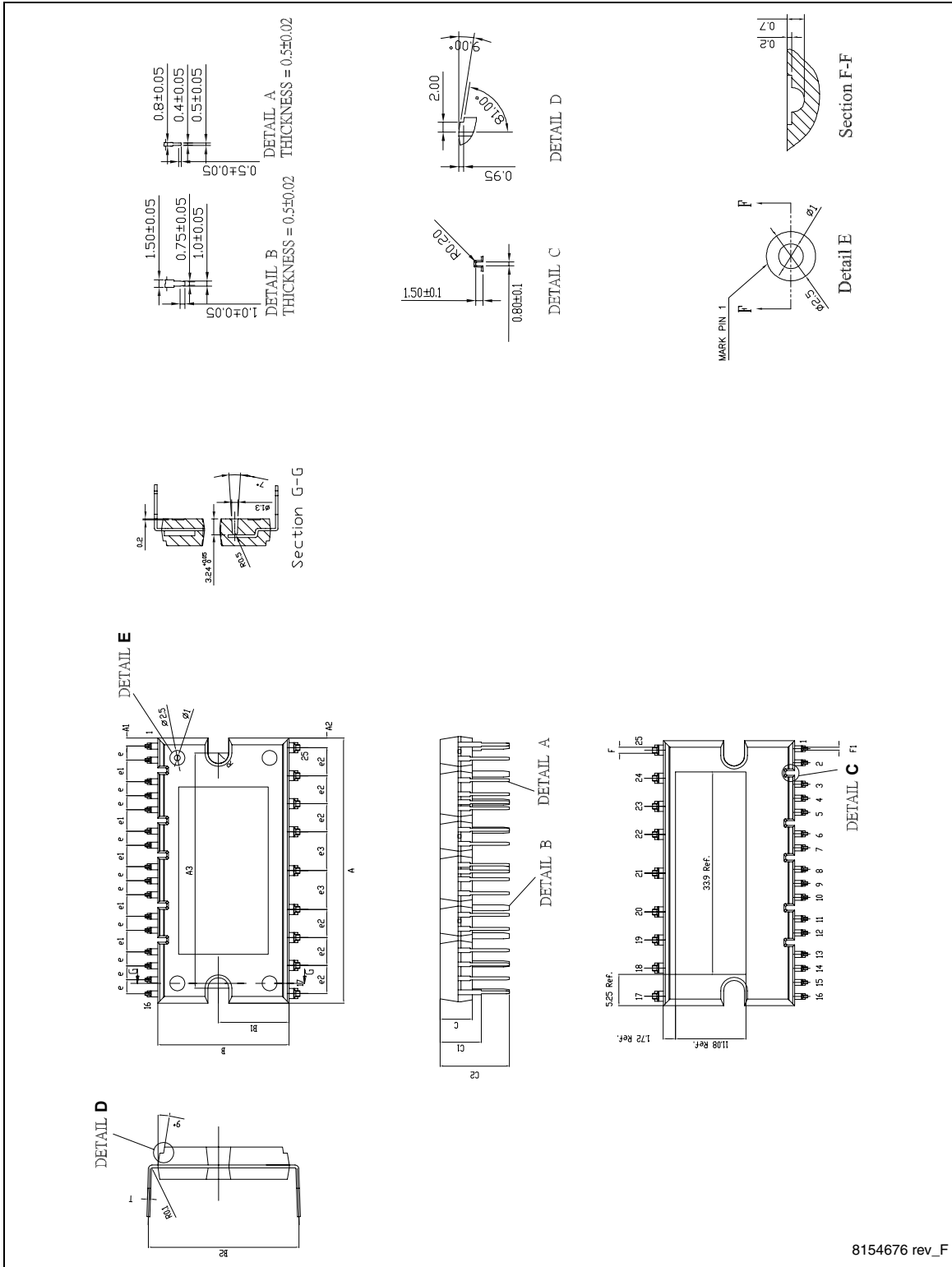
8154676 rev_F

Figure 11.   Packaging specifications of SDIP-25L package

6 Revision history

Table 16.   Document revision history

Date	Revision	Changes
07-Mar-2011	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com