EMIF01-TV01F3

IPAD™

EMI filter and ESD protection

Main application

- TV analog signal in TV_OUT interface

Description

The EMIF01-TV01F3 is a highly integrated array designed to suppress EMI/RFI noise and provide impedance matching for mobile phone and portable applications. The EMIF01-TV01F3 is in a flip-chip package to offer space saving and high RF performance.

This low pass filter includes ESD protection circuitry which prevents damage to the application when subjected to ESD surges up to 15 kV.

Benefits

- EMI symmetrical (I/O) low-pass filter
- High efficiency EMI filtering
- Lead-free package
- 400 µm pitch
- Very low PCB space consumption: 0.6 mm^2
- Very thin package: 0.6 mm
- High reliability offered by monolithic integration
- Reduction of parasitic elements through CSP integration

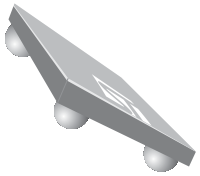
Complies with the following standards:

IEC 61000-4-2:

Level 4 on internal and external pins	15 kV (air discharge)
	8 kV (contact discharge)

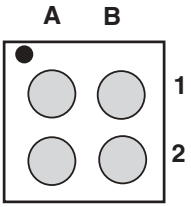
MIL STD 883F - Method 3015.7 Class 3

TM: IPAD id a trademark of STMicroelectronics



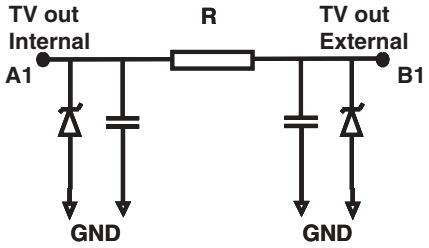
Flip-Chip (4 Bumps)

Pin configuration (bump side)



Pin	Description	Pin	Description
A1	TV OUT internal	B1	TV OUT external
A2	GND	B2	GND

Configuration



Order code

Part Number	Marking
EMIF01-TV01F3	HC

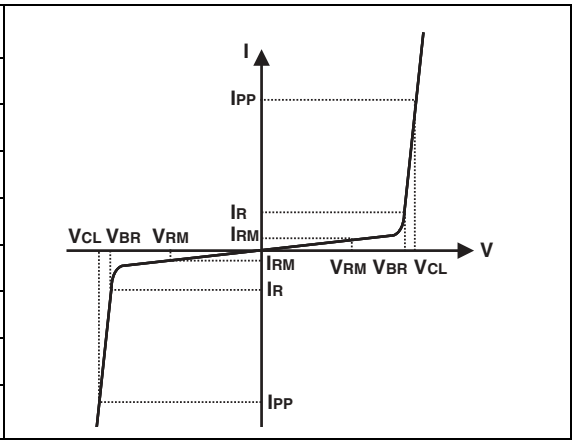
1 Characteristics

1.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{PP}	**Internal pin (A1) and External pin (B1):** ESD discharge IEC 61000-4-2, air discharge ESD discharge IEC 61000-4-2, contact discharge	 15 8	kV
T_j	Maximum junction temperature	125	° C
T_{op}	Operating temperature range	-30 to + 85	° C
P	Maximum power dissipation:	80	mW
T_{stg}	Storage temperature range	-55 to +150	° C

1.2 Electrical characteristics (T_{amb} = 25° C)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current @ V_{RM}
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic impedance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input & Output
C_{line}	Input capacitance per line



Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6		8	V
I_{RM}	V_{RM} = 3 V			0.2	µA
R	Tolerance ± 5%		75		Ω
C_{line}	V_R = 0 V		30	35	pF

Figure 1. S21 (db) attenuation measurement

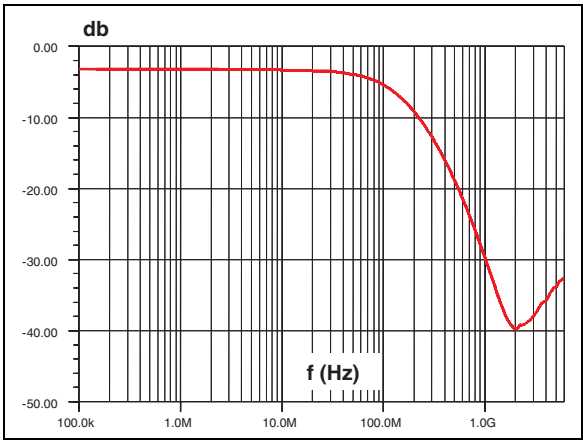


Figure 2. ESD response to IEC 61000-4-2 (+15 kV air discharge)

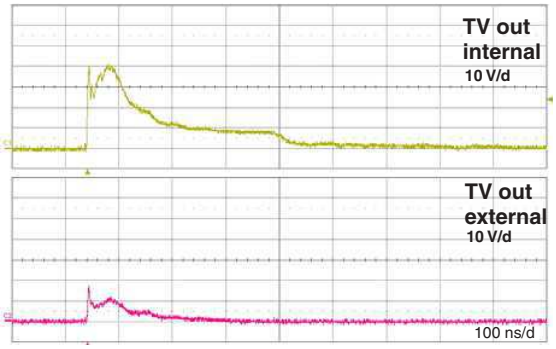


Figure 3. ESD response to IEC 61000-4-2 (-15 kV air discharge)

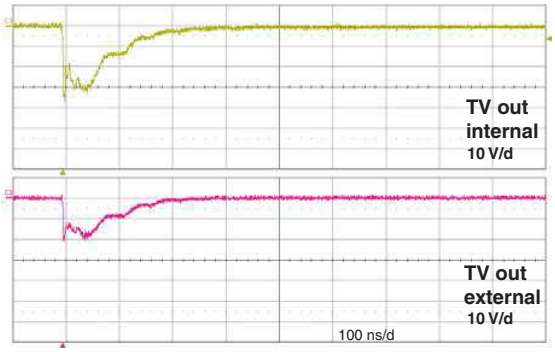


Figure 4. Line capacitance versus applied voltage

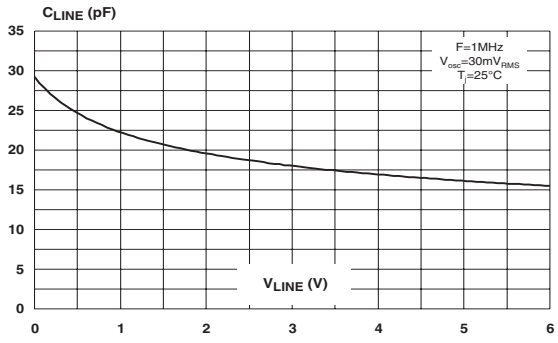


Figure 5. Aplac model

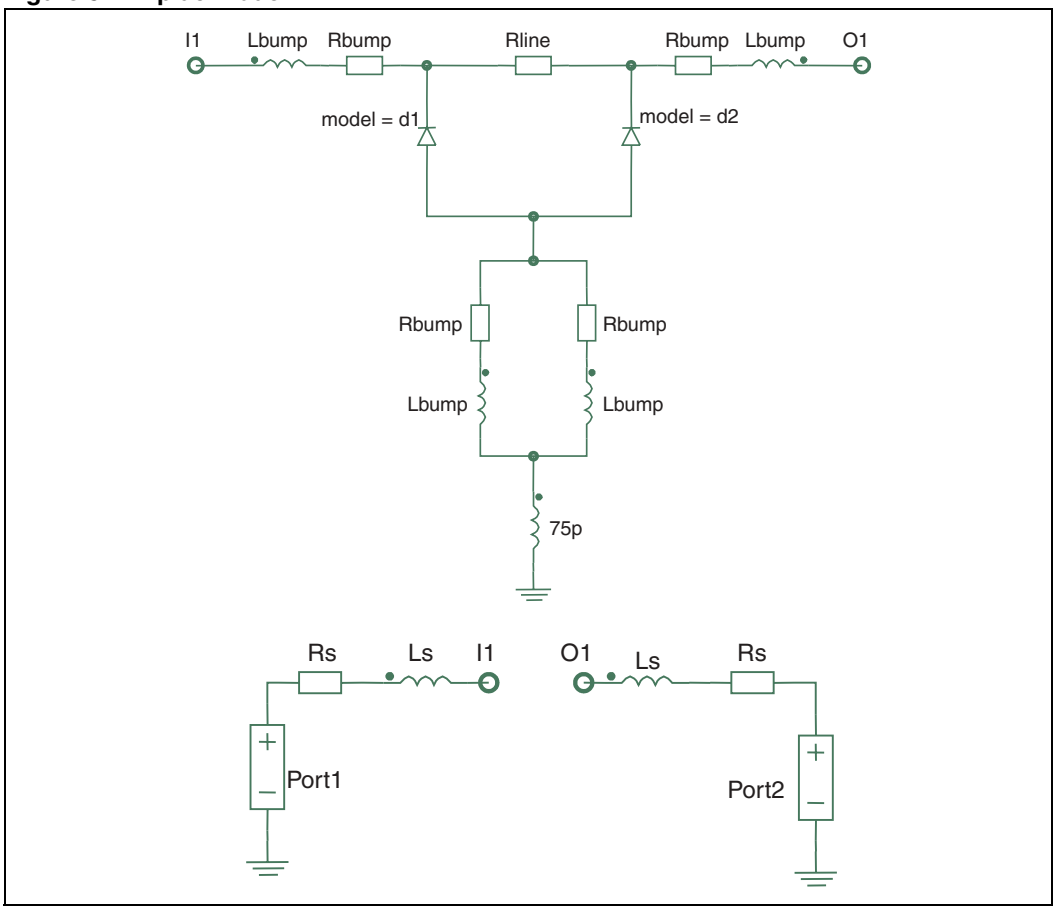


Figure 6. Aplac parameters

Variables	Diode D1	Diode D2
aplacvar Rline 75	BV=7	BV=7
aplacvar C_d1 17.5p	IBV=1m	IBV=1m
aplacvar C_d2 17.5p	CJO=C_d1	CJO=C_d2
aplacvar Ls 950pH	M=0.28	M=0.28
aplacvar Rs 150m	RS=0.48	RS=0.7
aplacvar Lbump96pH	VJ=0.6	VJ=0.6
aplacvar Rbump 20m	TT=100n	TT=100n
aplacvar Lgnd 75pH		

2 Ordering information scheme

EMIF yy - xx zz Fx

EMI Filter

Number of lines

Information
x = resistance value (Ohms)
z = capacitance value / 10 (pF)
or
2 letters = application
2 digits = version

Package
F = Flip-Chip
x = 3: Lead free, Pitch = 400 µm, Bump = 255 µm

3 Package information

Figure 7. Mechanical data

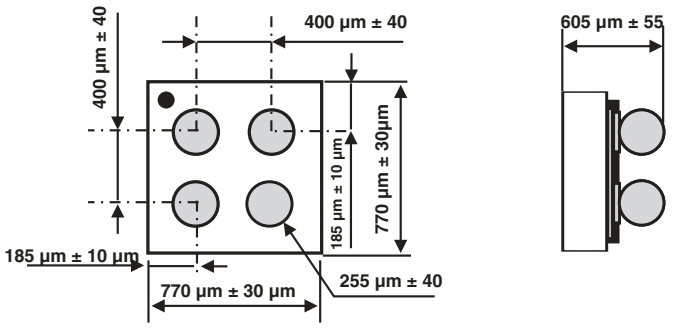


Figure 8. Foot print recommendations

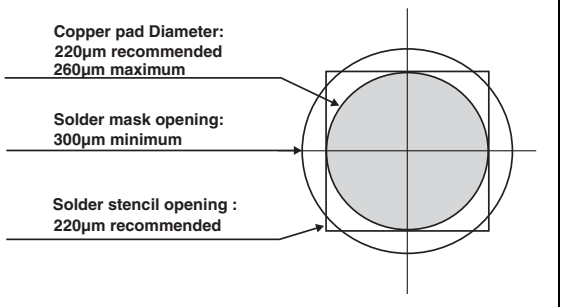


Figure 9. Marking

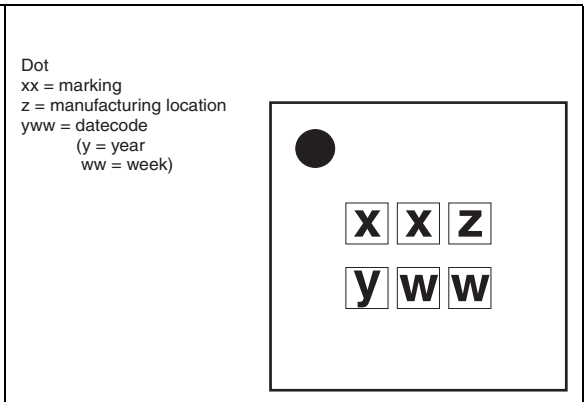
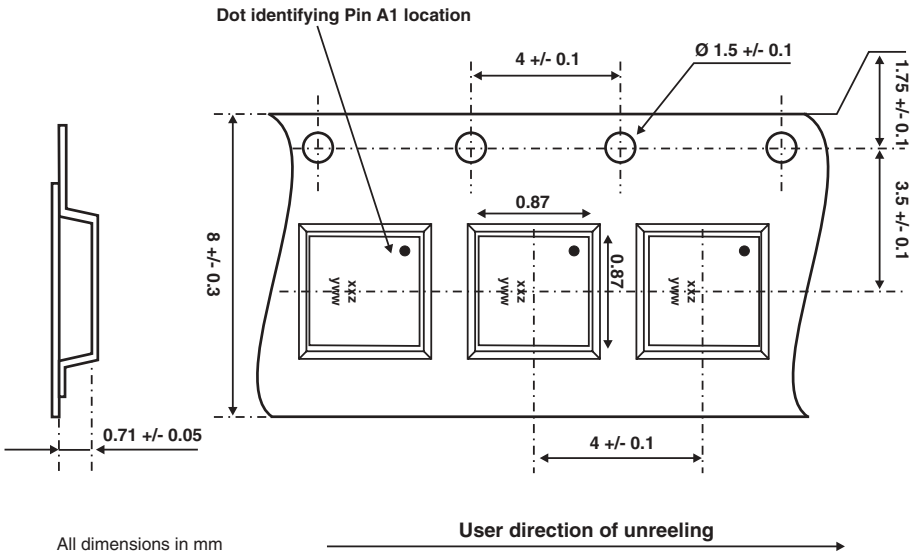


Figure 10. Flip-chip tape and reel specifications



In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

4 Ordering information

Part Number	Marking	Package	Weight	Base qty	Delivery mode
EMIF01-TV01F3	HC	Flip-Chip	0.79 mg	5000	Tape and reel (7”)

Note: More information is available in the application notes:
AN1235: “Flip-Chip: Package description and recommendations for use”
AN1751: "EMI Filters: Recommendations and measurements"

5 Revision history

Date	Revision	Changes
09-Feb-2006	1	Initial release.