Abridged Version

# SR1760ACA4
## +5/-5V 4-CHANNEL MR READ/WRITE DEVICE

**Prototype**

April, 2000

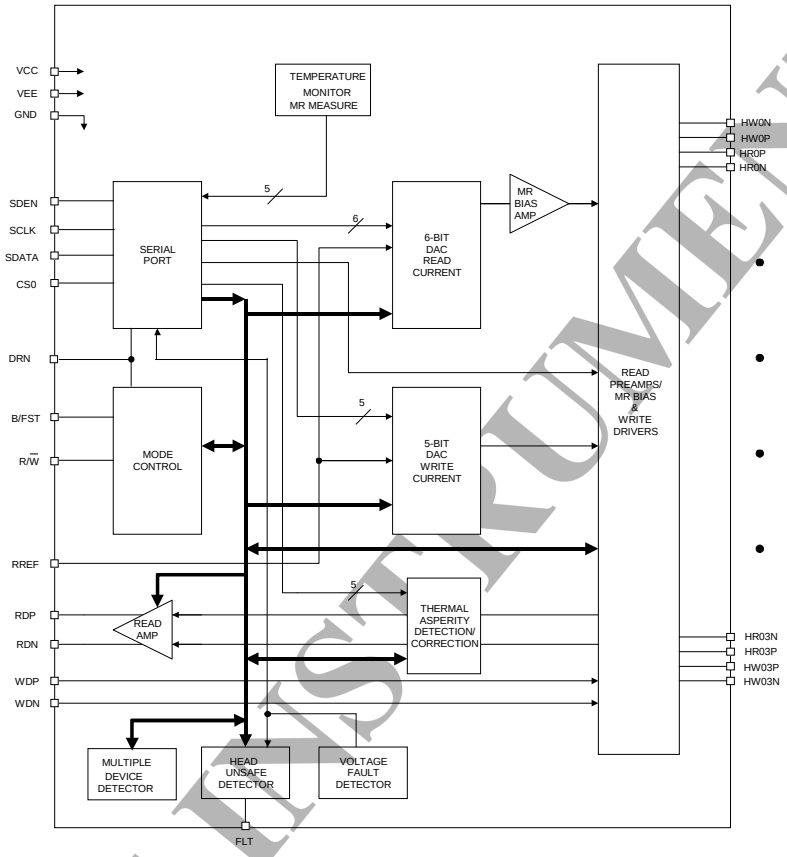
## DESCRIPTION

The TI SR1760ACA4 is a BiCMOS monolithic integrated circuit designed for use with four-terminal Magneto-Resistive recording heads. The reader architecture is MR voltage bias/voltage sense, current bias/voltage sense and will support a user data rate of up to 700 Mbits/sec. A read/write capable serial port is provided to enable the implementation of on-chip MR bias and Write current DACs. The device provides a write driver, low-noise read amplifier, serial port controlled head selection, write current, MR read bias current and read and write fault detection circuitry for up to four channels. The device requires +5V and -5V and comes in die form or 48-pin TQFP package.

## FEATURES

- **+5V ±10%, -5V ±10% supplies**
- **Supply voltage fault monitor**
- **MR head resistance range = 25 – 80Ω**
- **MR bias current range =2.5 – 10mA (6-bit)**
- **Programmable read gain = 41, 44 and 47 dB @ RMR=45Ω**
- **Programmable read bandwidth, 400MHz min (lower –3dB, higher –3dB and high frequency boost)**
- **Read input voltage noise = 0.55 nV/√Hz @RMR=0**
- **Read input current noise = 10 pA/√Hz @RMR=45 IMR=5mA**
- **MR measurement mode**
- **Write to read recovery = TBD ns (to 10mV of baseline)**
- **Write current rise/fall time = 550ps (nominal, 10-90%,Iw=50mA,Lh=45nH, Rh=16Ω, C=1pf)**
- **Programmable write current range = 10 – 50mA 0-pk (5-bit)**
- **3V compatible analog and digital interface**
- **Voltage or current mode PECL write data input**
- **Thermal asperity detection and correction**
- **Temperature monitor**

## BLOCK DIAGRAM




## FUNCTIONAL DESCRIPTION

The TI SR1760ACA4 addresses up to 4 four-terminal MR heads providing write drive or read bias and amplification. The selection of the chip is done via controls CS0, CS1 and STWN in conjunction with the serial interface address bits A1 and A2. CS0 is a device pin and has an internal pull up resistor. CS1 is internally tied to a low level for the SR1760ACA4. Serial port bit STWN activates servo track writing and is located in Register 0. CS0 and CS1 must be matched by two address bits A1 and A2 respectively for a preamp to be selected. The three-line serial data interface, with both read/write capabilities, is used to control head selection, write current, MR bias current, and mode control. The serial data port includes 10 read/write capable data registers and 1 read-only ID register. The three serial interface pins, SDEN, SDATA and SCLK, have internal pull-down resistors.