Si8460/61/62/63

Ultra Low Power Six-Channel Digital Isolator

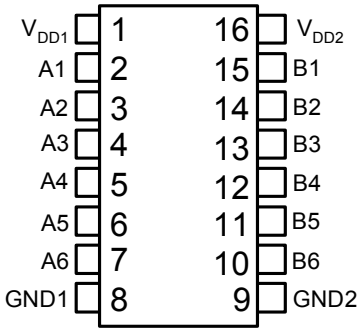
Features

- High-speed operation:
  DC – 150 Mbps
- Low propagation delay:
  <10 ns typical
- Wide Operating Supply Voltage:
  2.75–5.5 V
- Ultra low power
  5 V Operation:
  - <1.25 mA per channel at 1 Mbps
  - <2 mA per channel at 10 Mbps
  - <6 mA per channel at 100 Mbps

  2.75 V Operation:
  - <1.25 mA per channel at 1 Mbps
  - <2 mA per channel at 10 Mbps
  - <4 mA per channel at 100 Mbps
- Precise timing:
  2 ns pulse width distortion
  1 ns channel-channel matching
  2 ns pulse width skew
- Up to 2500 V_{RMS} isolation
- Transient Immunity: 25 kV/µs
- DC correct
- No start-up initialization required
- <30 µs startup time
- High temperature operation:
  125 °C at 150 Mbps
- Narrow body SOIC-16 package
- RoHS-compliant

Pin Assignments

Narrow Body SOIC



Top View

Applications

- Isolated switch mode supplies
- Isolated ADC, DAC
- Motor control
- Power factor correction systems

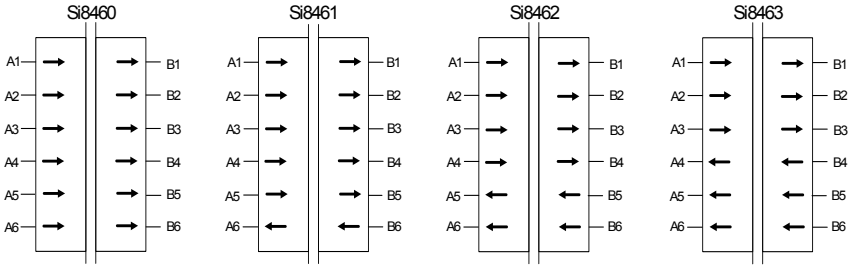
Safety Regulatory Approvals*

- UL recognition: 2500 V_{RMS} for 1 Minute per UL1577
- CSA component acceptance notice
- VDE certification conformity
  - IEC 60747-5-2 (VDE0884 Part 2)

Description

Silicon Lab's family of ultra low power digital isolators are CMOS devices that employ an RF coupler to transmit digital information across an isolation barrier. Very high speed operation at low power levels is achieved. These devices are available in a 16-pin narrow body SOIC package. Two speed grade options (1 and 150 Mbps) are available and achieve typical propagation delays of less than 10 ns.

Block Diagram



***Note:** Pending.

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1. Electrical Specifications

Table 1. Electrical Characteristics[1]

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	4.8	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
Output Impedance	Z_O	VDD = 5 V, 25 °C	—	50[2]	—	Ω
DC Supply Current (All inputs 0 V or at Supply)						
Si8460Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	3	TBD	
Si8461Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	4	TBD	
Si8462Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
Si8463Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8461Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 1. Electrical Characteristics[1] (Continued)

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8462Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8463Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx						
V_{DD1}			—	7	TBD	mA
V_{DD2}			—	28	TBD	
Si8461Bx						
V_{DD1}			—	14	TBD	mA
V_{DD2}			—	33	TBD	
Si8462Bx						
V_{DD1}			—	20	TBD	mA
V_{DD2}			—	27	TBD	
Si8463Bx						
V_{DD1}			—	18	TBD	mA
V_{DD2}			—	18	TBD	
Timing Characteristics						
Si846xA						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xB						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5	8	15	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	3	ns
Propagation Delay Skew[3]	$t_{PSK(P-P)}$		—	—	10	ns

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

Table 1. Electrical Characteristics[1] (Continued)

(V_{DD1} = 5 V±10%, V_{DD2} = 5 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Channel-Channel Skew	t_{PSK}		—	—	3	ns
For All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2	—	ns
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2	—	ns
Common Mode Transient Immunity	CMTI	V_I = V_{DD} or 0 V	20	25	—	kV/µs
Start-up Time[4]	t_{SU}		—	30	—	µs

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. The nominal output impedance of an isolator driver channel is approximately 50 Ω, ±40%, which is a combination of the value of the on-chip series termination resistor and channel resistance of the output driver FET. When driving loads where transmission line effects will be a factor, output pins should be terminated with 50 Ω controlled impedance PCB traces.
3. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
4. Start-up time is the time period from the application of power to valid data at the output.

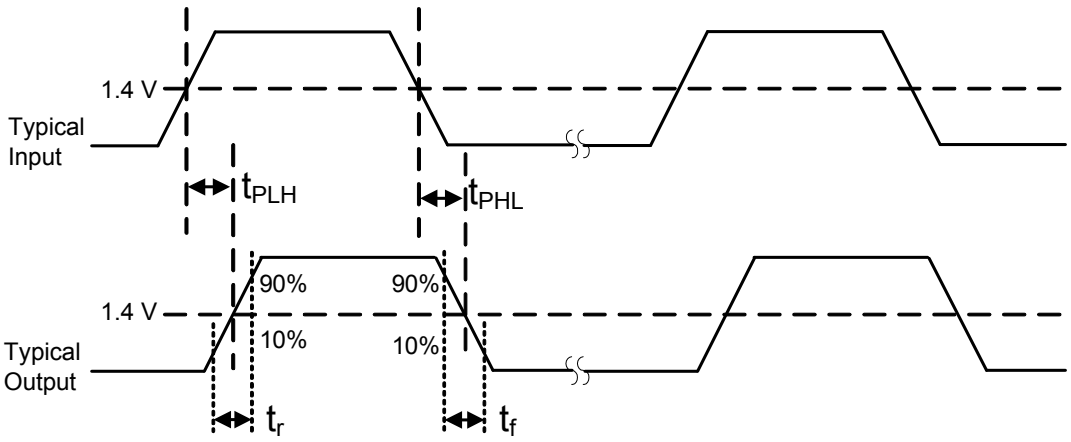


Figure 1. Propagation Delay Timing

Table 2. Electrical Characteristics[1]

(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	3.1	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8460Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	3	TBD	
Si8461Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	4	TBD	
Si8462Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
Si8463Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	mA
V_{DD2}		All inputs 0 DC	—	3	TBD	
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8461Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8462Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8463Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx						
V_{DD1}			—	6	TBD	mA
V_{DD2}			—	21	TBD	
Si8461Bx						
V_{DD1}			—	10	TBD	mA
V_{DD2}			—	19	TBD	
Si8462Bx						
V_{DD1}			—	12	TBD	mA
V_{DD2}			—	16	TBD	
Si8463Bx						
V_{DD1}			—	13	TBD	mA
V_{DD2}			—	13	TBD	
Timing Characteristics						
Si846xA						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xB						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5	8	15	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	3	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	10	ns
Channel-Channel Skew	t_{PSK}		—	—	3	ns
For All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2	—	ns

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 2. Electrical Characteristics[1] (Continued)

(V_{DD1} = 3.3 V±10%, V_{DD2} = 3.3 V±10%, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	V_I = V_{DD} or 0 V	20	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	30	—	µs

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1]

(V_{DD1} = 2.75 V, V_{DD2} = 2.75 V, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
High Level Input Voltage	V_{IH}		2.0	—	—	V
Low Level Input Voltage	V_{IL}		—	—	0.8	V
High Level Output Voltage	V_{OH}	Ioh = –4 mA	V_{DD1},V_{DD2} – 0.4	2.3	—	V
Low Level Output Voltage	V_{OL}	Iol = 4 mA	—	0.2	0.4	V
Input Leakage Current	I_L		—	—	±10	µA
DC Supply Current (All inputs 0 V or at supply)						
Si8460Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	
V_{DD2}		All inputs 0 DC	—	3	TBD	mA
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	3	TBD	
Si8461Ax, Bx						
V_{DD1}		All inputs 0 DC	—	2	TBD	
V_{DD2}		All inputs 0 DC	—	3	TBD	mA
V_{DD1}		All inputs 1 DC	—	7	TBD	
V_{DD2}		All inputs 1 DC	—	4	TBD	
Si8462Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	
V_{DD2}		All inputs 0 DC	—	3	TBD	mA
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
Si8463Ax, Bx						
V_{DD1}		All inputs 0 DC	—	3	TBD	
V_{DD2}		All inputs 0 DC	—	3	TBD	mA
V_{DD1}		All inputs 1 DC	—	6	TBD	
V_{DD2}		All inputs 1 DC	—	6	TBD	
1 Mbps Supply Current (All inputs = 500 kHz square wave, Cl = 15 pF on all outputs)						
Si8460Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8461Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
Si8462Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.75 V, V_{DD2} = 2.75 V, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Si8463Ax, Bx						
V_{DD1}			—	5	TBD	mA
V_{DD2}			—	4	TBD	
100 Mbps Supply Current (All inputs = 50 MHz square wave, Cl = 15 pF on all outputs)						
Si8460Bx						
V_{DD1}			—	6	TBD	mA
V_{DD2}			—	18	TBD	
Si8461Bx						
V_{DD1}			—	9	TBD	mA
V_{DD2}			—	15	TBD	
Si8462Bx						
V_{DD1}			—	11	TBD	mA
V_{DD2}			—	13	TBD	
Si8463Bx						
V_{DD1}			—	12	TBD	mA
V_{DD2}			—	12	TBD	
Timing Characteristics						
Si846xA						
Maximum Data Rate			0	—	1	Mbps
Minimum Pulse Width			—	—	250	ns
Propagation Delay	t_{PHL},t_{PLH}	See Figure 1	—	—	35	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	25	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	40	ns
Channel-Channel Skew	t_{PSK}		—	—	35	ns
Si846xB						
Maximum Data Rate			0	—	150	Mbps
Minimum Pulse Width			—	—	6	ns
Propagation Delay	t_{PHL}, t_{PLH}	See Figure 1	5	8	15	ns
Pulse Width Distortion $\lvert t_{PLH} - t_{PHL} \rvert$	PWD	See Figure 1	—	—	3	ns
Propagation Delay Skew[2]	$t_{PSK(P-P)}$		—	—	10	ns
Channel-Channel Skew	t_{PSK}		—	—	3	ns
For All Models						
Output Rise Time	t_r	C_L = 15 pF See Figure 1	—	2	—	ns

Notes:

1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 3. Electrical Characteristics[1] (Continued)

(V_{DD1} = 2.75 V, V_{DD2} = 2.75 V, T_A = –40 to 125 ºC; applies to narrow-body SOIC package)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Output Fall Time	t_f	C_L = 15 pF See Figure 1	—	2	—	ns
Common Mode Transient Immunity at Logic Low Output	CMTI	V_I = V_{DD} or 0 V	20	25	—	kV/µs
Start-up Time[3]	t_{SU}		—	30	—	µs

Notes:
1. Electrical specification values are preliminary. Various specifications will be adjusted to reflect actual performance as final product characterization data becomes available.
2. $t_{PSK(P-P)}$ is the magnitude of the difference in propagation delay times measured between different units operating at the same supply voltages, load, and ambient temperature.
3. Start-up time is the time period from the application of power to valid data at the output.

Table 4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit
Storage Temperature	T_{STG}	–65	—	150	ºC
Ambient Temperature Under Bias	T_A	–40	—	125	ºC
Supply Voltage	V_{DD1}, V_{DD2}	–0.5	—	6	V
Input Voltage	V_I	–0.5	—	V_{DD} + 0.5	V
Output Voltage	V_O	–0.5	—	V_{DD} + 0.5	V
Output Current Drive Channel	L_O	—	—	10	mA
Lead Solder Temperature (10 s)		—	—	260	ºC
Maximum Isolation Voltage (1 s)		—	—	3600	V_{RMS}

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to conditions as specified in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may degrade performance.

Table 5. Recommended Operating Conditions

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Ambient Operating Temperature*	T_A	150 Mbps, 15 pF, 5 V	–40	25	125	ºC
Supply Voltage	V_{DD1}		2.75	—	5.5	V
	V_{DD2}		2.75	—	5.5	V

***Note:** The maximum ambient temperature is dependent on data frequency, output loading, number of operating channels, and supply voltage.

Table 6. Regulatory Information*

CSA
The Si846x is certified under CSA Component Acceptance Notice. For more details, see File 232873.
VDE
The Si846x is certified according to IEC 60747-5-2. For more details, see File 5006301-4880-0001.
UL
The Si846x is certified under UL1577 component recognition program. For more details, see File E257455.
***Note:** Pending. All 2.5 kV_{RMS} rated devices are production tested to 3.6 kV_{RMS} for 1 sec. For more information, see "6. Ordering Guide" on page 25.

Table 7. Insulation and Safety-Related Specifications

Parameter	Symbol	Test Condition	Value	Unit
			NB SOIC-16	
Minimum Air Gap (Clearance)	L(IO1)		5.0	mm
Minimum External Tracking (Creepage)	L(IO2)		4.6	mm
Minimum Internal Gap (Internal Clearance)			0.008	mm
Tracking Resistance (Comparative Tracking Index)	CTI	DIN IEC 60112/VDE 0303 Part 1	>175	V
Resistance (Input-Output)[1]	R_{IO}		10^{12}	Ω
Capacitance (Input-Output)[1]	C_{IO}	f = 1 MHz	2	pF
Input Capacitance[2]	C_I		4.0	pF

Notes:
1. To determine resistance and capacitance, the Si846x is converted into a 2-terminal device. Pins 1–8 are shorted together to form the first terminal and pins 9–16 are shorted together to form the second terminal. The parameters are then measured between these two terminals.
2. Measured from input pin to ground.

Table 8. IEC 60664-1 (VDE 0884 Part 2) Ratings

Parameter	Test Conditions	Specification
Basic isolation group	Material Group	IIIa
Installation Classification	Rated Mains Voltages ≤ 150 V_{RMS}	I-IV
	Rated Mains Voltages ≤ 300 V_{RMS}	I-III
	Rated Mains Voltages ≤ 400 V_{RMS}	I-II

Table 9. IEC 60747-5-2 Insulation Characteristics for Si846xxB*

Parameter	Symbol	Test Condition	Characteristic	Unit
Maximum Working Insulation Voltage	V_{IORM}		560	V peak
Input to Output Test Voltage	V_{PR}	Method a After Environmental Tests Subgroup 1 (V_{IORM} x 1.6 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	896	V peak
		Method b1 (V_{IORM} x 1.875 = V_{PR}, 100% Production Test, t_m = 1 sec, Partial Discharge < 5 pC)	1050	
		After Input and/or Safety Test Subgroup 2/3 (V_{IORM} x 1.2 = V_{PR}, t_m = 60 sec, Partial Discharge < 5 pC)	672	
Highest Allowable Overvoltage (Transient Overvoltage, t_{TR} = 10 sec)	V_{TR}		4000	V peak
Pollution Degree (DIN VDE 0110, Table 1)			2	
Insulation Resistance at T_S, V_{IO} = 500 V	R_S		$>10^9$	Ω

***Note:** This isolator is suitable for basic electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The Si84xx provides a climate classification of 40/125/21.

Table 10. IEC Safety Limiting Values[1]

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
					NB SOIC-16	
Case Temperature	T_S		—	—	150	°C
Safety input, output, or supply current	I_S	θ_{JA} = 105 °C/W (NB SOIC-16), V_I = 5.5 V, T_J = 150 °C, T_A = 25 °C	—	—	215	mA
Device Power Dissipation[2]	P_D		—	—	415	mW

Notes:
1. Maximum value allowed in the event of a failure; also see the thermal derating curve in Figure 2.
2. The Si8460 is tested with V_{DD1} = V_{DD2} = 5.5 V, T_J = 150 ºC, C_L = 15 pF, input a 150 Mbps 50% duty cycle square wave.

Table 11. Thermal Characteristics

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
				NB SOIC-16		
IC Junction-to-Case Thermal Resistance	θ_{JC}	Thermocouple located at center of package	—	45	—	ºC/W
IC Junction-to-Air Thermal Resistance	θ_{JA}		—	105	—	ºC/W

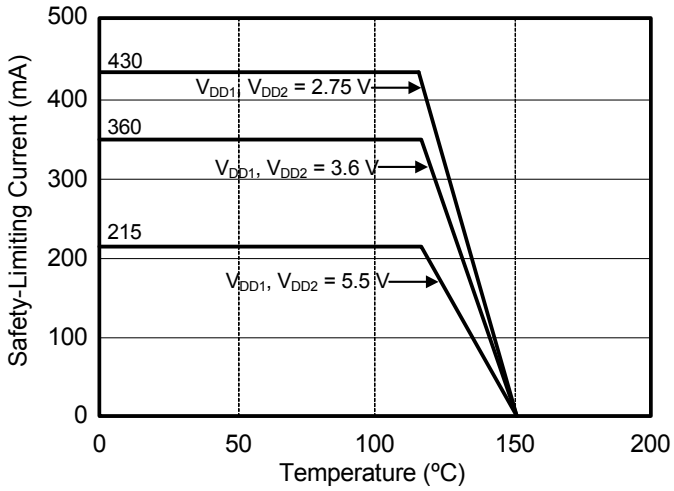


Figure 2. (NB SOIC-16) Thermal Derating Curve, Dependence of Safety Limiting Values with Case Temperature per DIN EN 60747-5-2

2. Typical Performance Characteristics

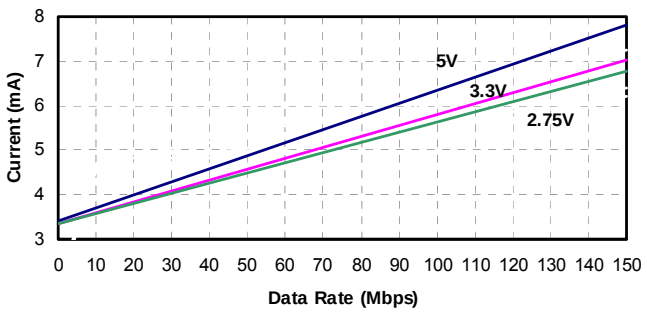


Figure 3. Si8460 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation

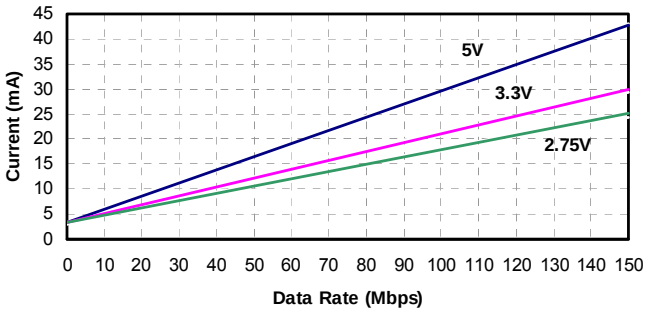


Figure 4. Si8460 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

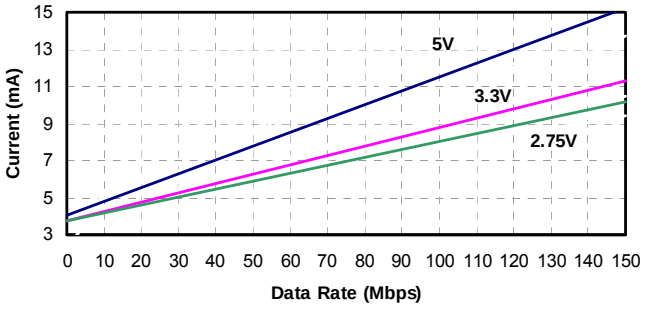


Figure 5. Si8461 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

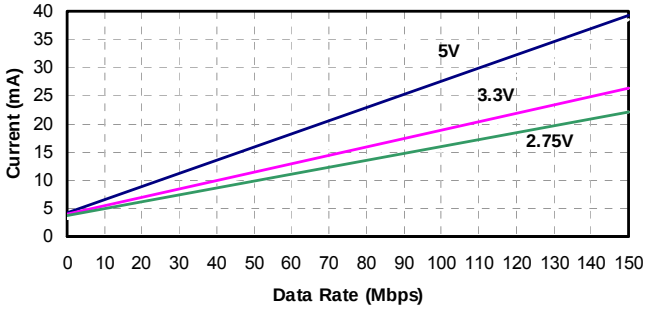


Figure 6. Si8461 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

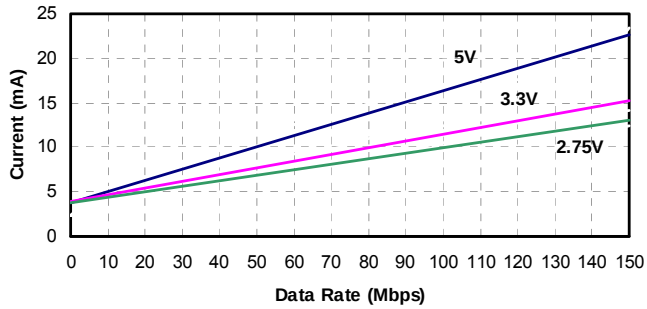


Figure 7. Si8462 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

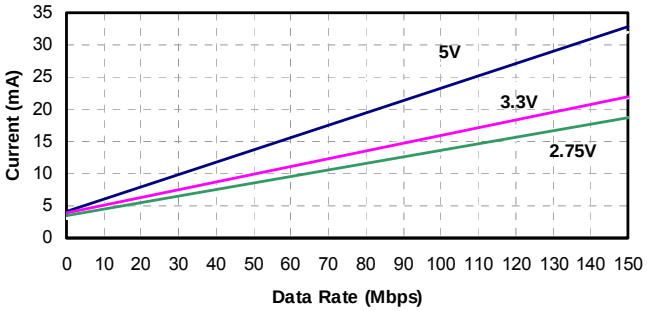


Figure 8. Si8462 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

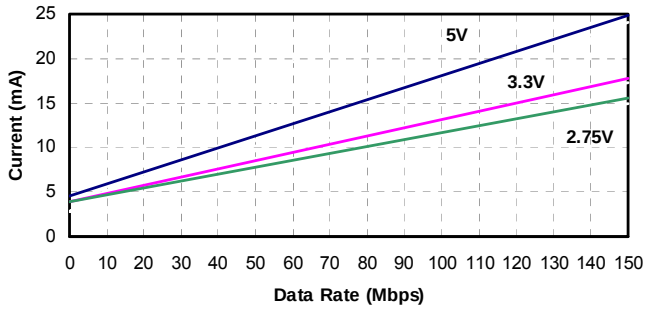


Figure 9. Si8463 Typical V_{DD1} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

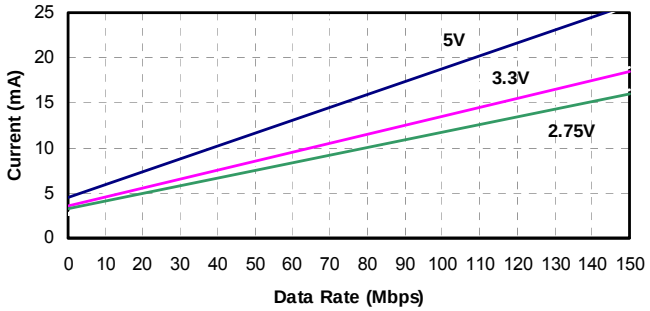


Figure 10. Si8463 Typical V_{DD2} Supply Current vs. Data Rate 5, 3.3, and 2.75 V Operation (15 pF Load)

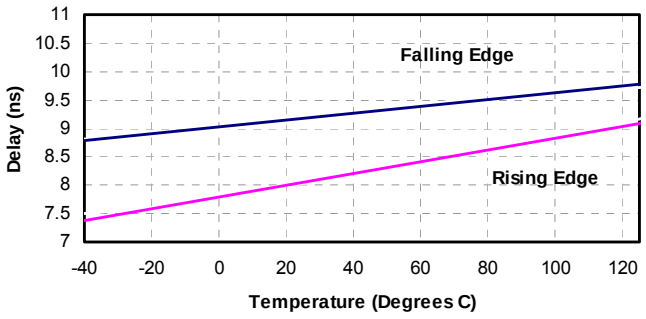


Figure 11. Propagation Delay vs. Temperature 5 V Operation

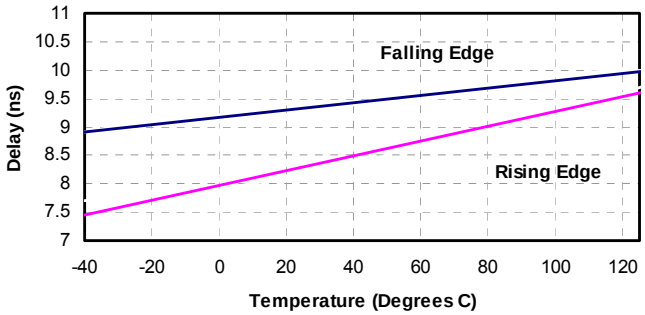


Figure 12. Propagation Delay vs. Temperature 3.3 V Operation

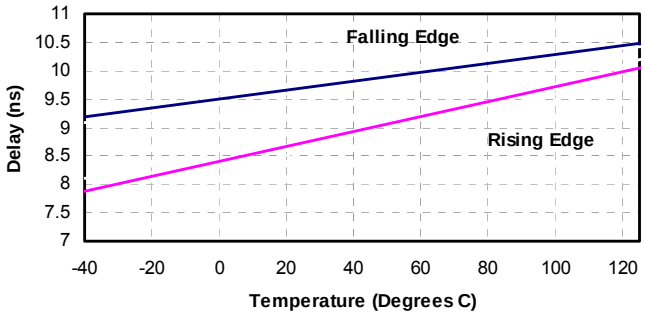


Figure 13. Propagation Delay vs. Temperature 2.75 V Operation

3. Application Information

3.1. Theory of Operation

The operation of an Si846x channel is analogous to that of an opto coupler, except an RF carrier is modulated instead of light. This simple architecture provides a robust isolated data path and requires no special considerations or initialization at start-up. A simplified block diagram for a single Si846x channel is shown in Figure 14.

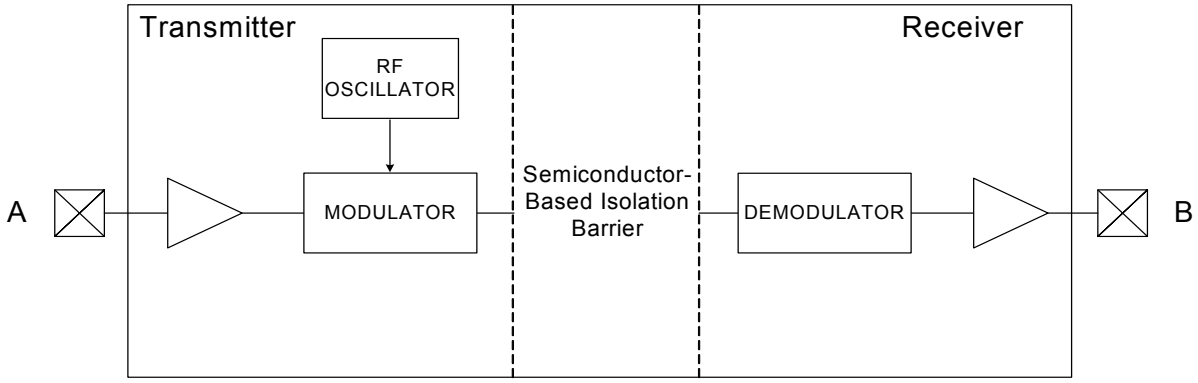


Figure 14. Simplified Channel Diagram

A channel consists of an RF Transmitter and RF Receiver separated by a semiconductor-based isolation barrier. Referring to the Transmitter, input A modulates the carrier provided by an RF oscillator using on/off keying. The Receiver contains a demodulator that decodes the input state according to its RF energy content and applies the result to output B via the output driver. This RF on/off keying scheme is superior to pulse code schemes as it provides best-in-class noise immunity, low power consumption, and better immunity to magnetic fields. See Figure 15 for more details.

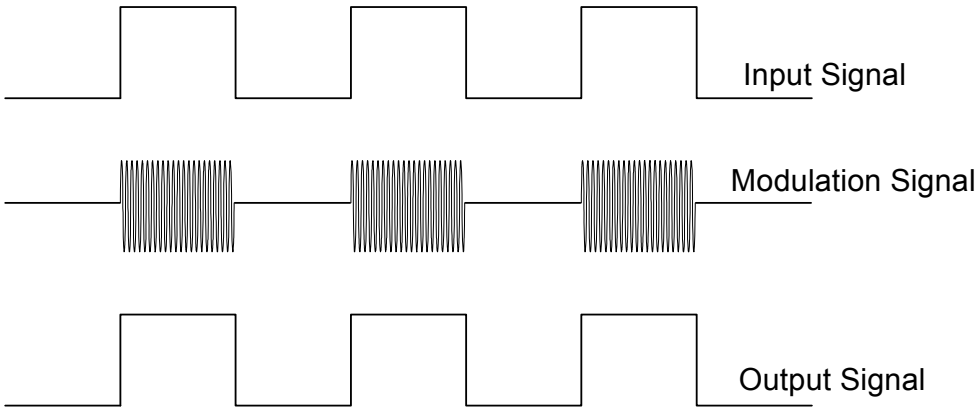


Figure 15. Modulation Scheme

3.2. Eye Diagram

Figure 16 illustrates an eye-diagram taken on an Si8460. For the data source, the test used an Anritsu (MP1763C) Pulse Pattern Generator set to 1000 ns/div. The output of the generator's clock and data from an Si8460 were captured on an oscilloscope. The results illustrate that data integrity was maintained even at the high data rate of 150 Mbps. The results also show that 2 ns pulse width distortion and 250 ps peak jitter were exhibited.

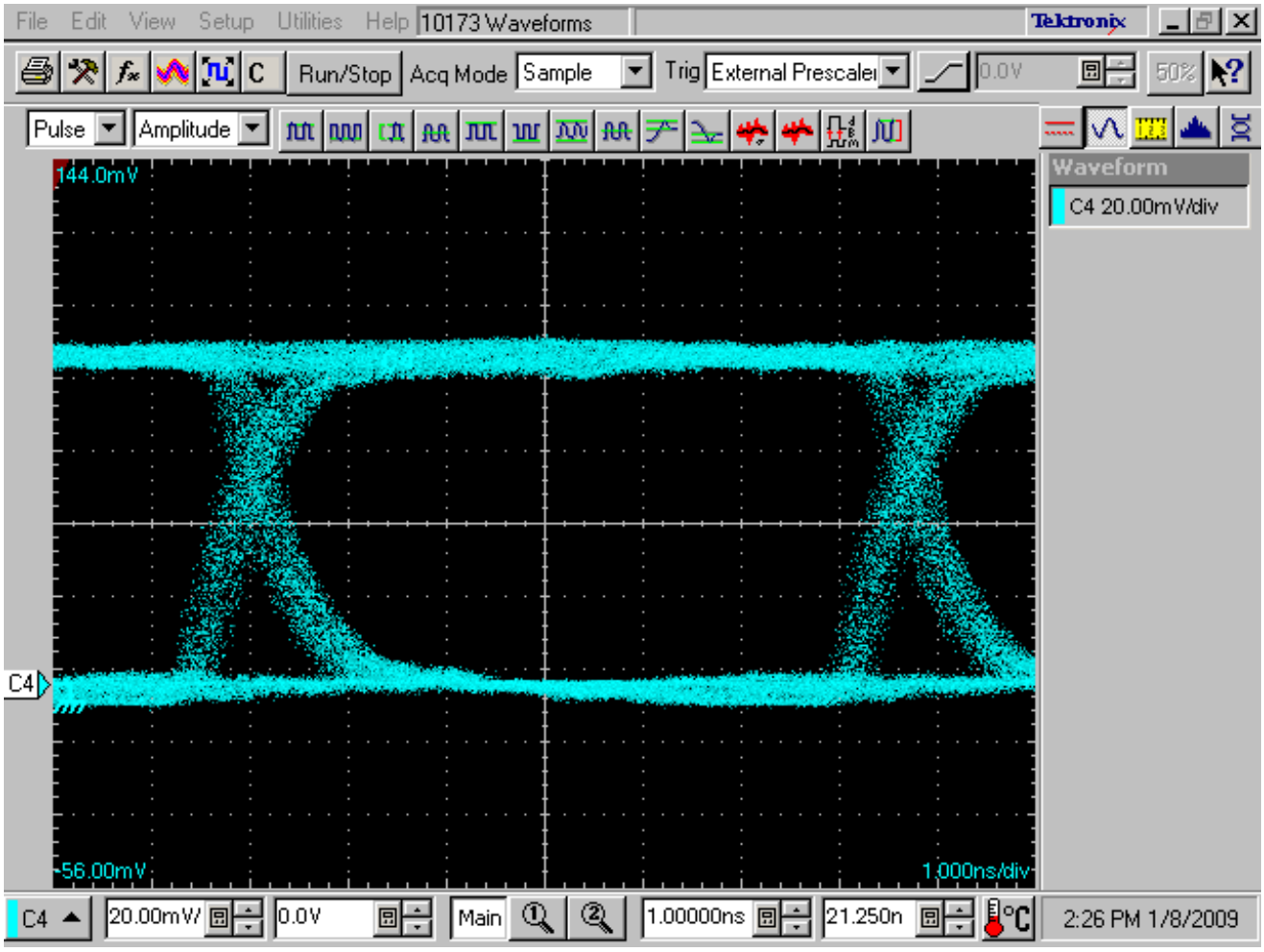


Figure 16. Eye Diagram

4. Layout Recommendations

Dielectric isolation is a set of specifications produced by the safety regulatory agencies from around the world that describes the physical construction of electrical equipment that derives power from a high-voltage power system such as 100–240 V_{AC} systems or industrial power systems. The dielectric test (or HIPOT test) given in the safety specifications places a very high voltage between the input power pins of a product and the user circuits and the user touchable surfaces of the product. For the IEC relating to products deriving their power from the 220–240 V power grids, the test voltage is 2500 V_{AC} (or 3750 V_{DC}—the peak equivalent voltage).

There are two terms described in the safety specifications:

- Creepage—the distance along the insulating surface an arc may travel.
- Clearance—the distance through the shortest path through air that an arc may travel.

Figure 17 illustrates the accepted method of providing the proper creepage distance along the surface. For a 220–240 V_{AC} application, this distance is 8 mm and the wide body SOIC package must be used. There must be no copper traces within this 8 mm exclusion area, and the surface should have a conformal coating such as solder resist. The digital isolator chip must straddle this exclusion area.

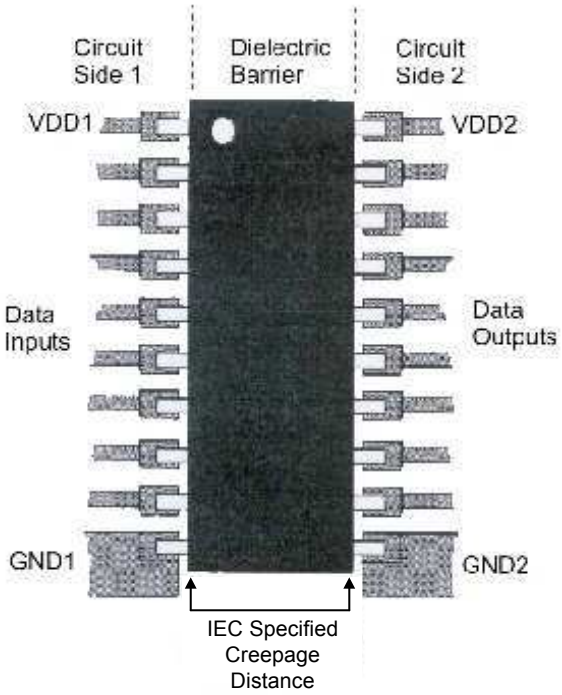


Figure 17. Creepage Distance

4.1. Supply Bypass

The Si846x requires a 1 µF bypass capacitor between V_{DD1} and GND1 and V_{DD2} and GND2. The capacitor should be placed as close as possible to the package.

4.2. Input and Output Characteristics

The Si846x inputs and outputs are standard CMOS drivers/receivers. Table 12 details powered and unpowered operation of the Si846x.

Table 12. Si846x Operation Table

V_I Input[1,2]	VDDI State[1,3,4]	VDDO State[1,3,4]	V_O Output[1,2]	Comments
H	P	P	H	Enabled, normal operation
L	P	P	L	
X	P	P	Hi-Z	Disabled
X	UP	P	L	Upon the transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs.
X	UP	P	Hi-Z	Disabled
X	P	UP	L	Upon the transition of VDDI from unpowered to powered, V_O returns to the same state as V_I in less than 1 µs, if EN is in either the H or NC state.

Notes:

1. VDDI and VDDO are the input and output power supplies. V_I and V_O are the respective input and output terminals.
2. X = not applicable; H = Logic High; L = Logic Low; Hi-Z = High Impedance.
3. "Powered" state (P) is defined as 2.75 V < VDD < 5.5 V.
4. "Unpowered" state (UP) is defined as VDD = 0 V.

4.3. RF Radiated Emissions

The Si846x family uses a RF carrier frequency of approximately 700 MHz. This results in a small amount of radiated emissions at this frequency and its harmonics. The radiation is not from the IC chip but due to a small amount of RF energy driving the isolated ground planes which can act as a dipole antenna.

The unshielded Si846x evaluation board passes FCC requirements. Table 13 shows measured emissions compared to FCC requirements.

Radiated emissions can be reduced if the circuit board is enclosed in a shielded enclosure or if the PCB is a less efficient antenna.

Table 13. Radiated Emissions*

Frequency (GHz)	Measured (dBµV/m)	FCC Spec (dBµV/m)	Compared to Spec (dB)
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
TBD	TBD	TBD	TBD
***Note:** Data table to be updated pending final characterization.			

4.4. RF Immunity and Common Mode Transient Immunity

The Si846x family has very high common mode transient immunity while transmitting data. This is typically measured by applying a square pulse with very fast rise/fall times between the isolated grounds. Measurements show no failures at 25 kV/µs. During a high surge event the output may glitch low for up to 20–30 ns, but the output corrects immediately after the surge event.

The Si846x family passes the industrial requirements of CISPR24 for RF immunity of 10 V/m using an unshielded evaluation board. As shown in Figure 18, the isolated ground planes form a parasitic dipole antenna, while Figure 19 shows the RMS common mode voltage versus frequency above which the Si846x becomes susceptible to data corruption. To avoid compromising data, care must be taken to keep RF common-mode voltage below the envelope specified in Figure 19. The PCB should be laid-out to not act as an efficient antenna for the RF frequency of interest. RF susceptibility is also significantly reduced when the end system is housed in a metal enclosure, or otherwise shielded.

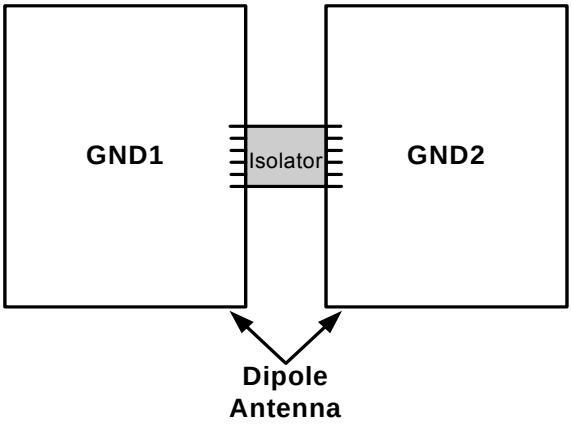


Figure 18. Dipole Antenna

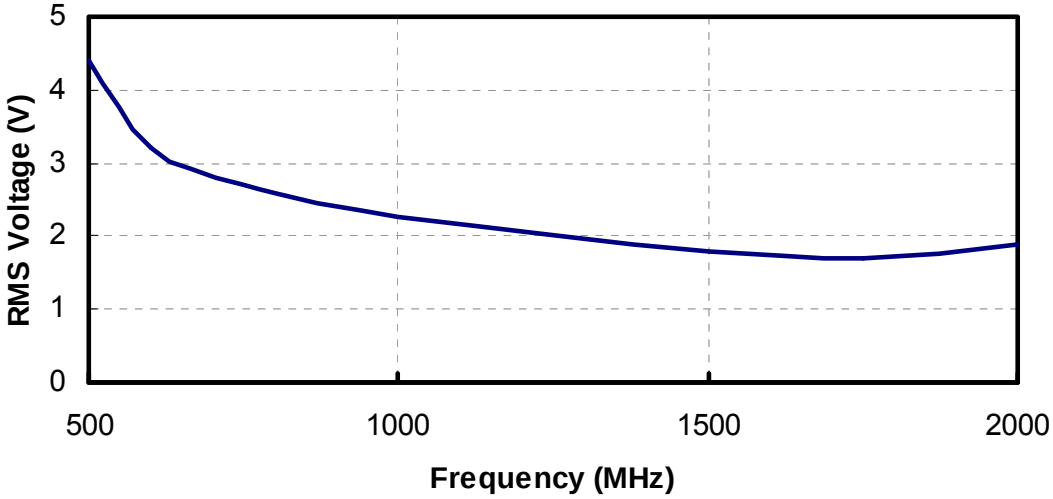
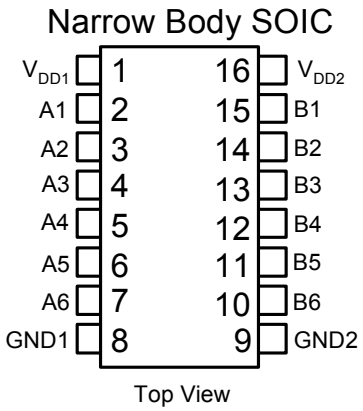


Figure 19. RMS Common Mode Voltage vs. Frequency (Data to be Updated Pending Final Characterization)

5. Pin Descriptions



Name	SOIC-16 Pin#	Type	Description
V_{DD1}	1	Supply	Side 1 power supply.
A1	2	Digital Input	Side 1 digital input.
A2	3	Digital Input	Side 1 digital input.
A3	4	Digital Input	Side 1 digital input.
A4	5	Digital I/O	Side 1 digital input or output.
A5	6	Digital I/O	Side 1 digital input or output.
A6	7	Digital I/O	Side 1 digital input or output.
GND1	8	Ground	Side 1 ground.
GND2	9	Ground	Side 2 ground.
B6	10	Digital I/O	Side 2 digital input or output.
B5	11	Digital I/O	Side 2 digital input or output.
B4	12	Digital I/O	Side 2 digital input or output.
B3	13	Digital Output	Side 2 digital output.
B2	14	Digital Output	Side 2 digital output.
B1	15	Digital Output	Side 2 digital output.
V_{DD2}	16	Supply	Side 2 power supply.

6. Ordering Guide

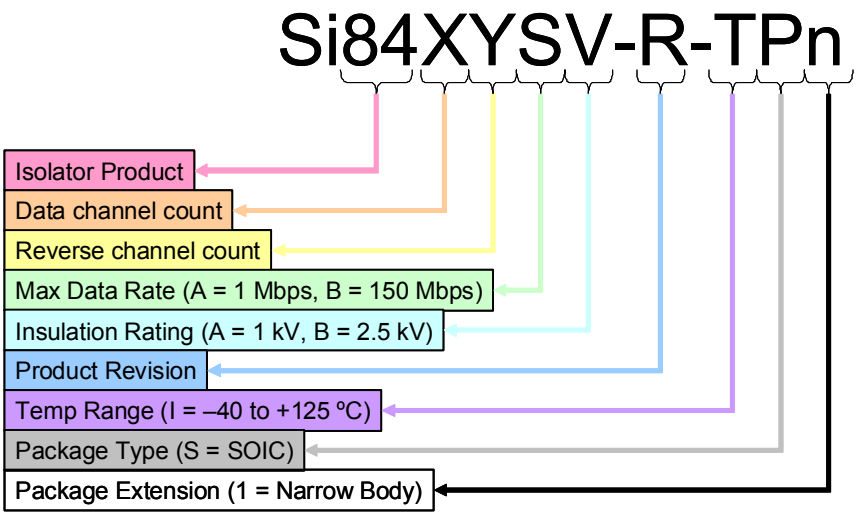


Figure 20. Ordering Part Number (OPN) Convention

Table 14. Ordering Guide for Valid OPNs

Ordering Part Number (OPN)	Number of Inputs VDD1 Side	Number of Inputs VDD2 Side	Maximum Data Rate (Mbps)	Isolation Rating	Temp Range	Package Type	Legacy Part Equivalent
Si8460AA-A-IS1	6	0	1	1 kVrms	–40 to 125 °C	NB SOIC-16	—
Si8460BA-A-IS1	6	0	150				—
Si8461AA-A-IS1	5	1	1				—
Si8461BA-A-IS1	5	1	150				—
Si8462AA-A-IS1	4	2	1				—
Si8462BA-A-IS1	4	2	150				—
Si8463AA-A-IS1	3	3	1				—
Si8463BA-A-IS1	3	3	150				—
Si8460AB-A-IS1	6	0	1	2.5 kVrms	–40 to 125 °C	NB SOIC-16	—
Si8460BB-A-IS1	6	0	150				—
Si8461AB-A-IS1	5	1	1				—
Si8461BB-A-IS1	5	1	150				—
Si8462AB-A-IS1	4	2	1				—
Si8462BB-A-IS1	4	2	150				—
Si8463AB-A-IS1	3	3	1				—
Si8463BB-A-IS1	3	3	150				—

Note: All packages are Pb-free and RoHS compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry standard classifications, and peak solder temperature.

7. Package Outline: 16-Pin Narrow Body SOIC

Figure 21 illustrates the package details for the Si846x in a 16-pin narrow-body SOIC (SO-16). Table 15 lists the values for the dimensions shown in the illustration. All packages are Pb-free and RoHS compliant. Moisture sensitivity level is MSL3 with peak reflow temperature of 260 °C according to the JEDEC industry classification and peak solder temperature.

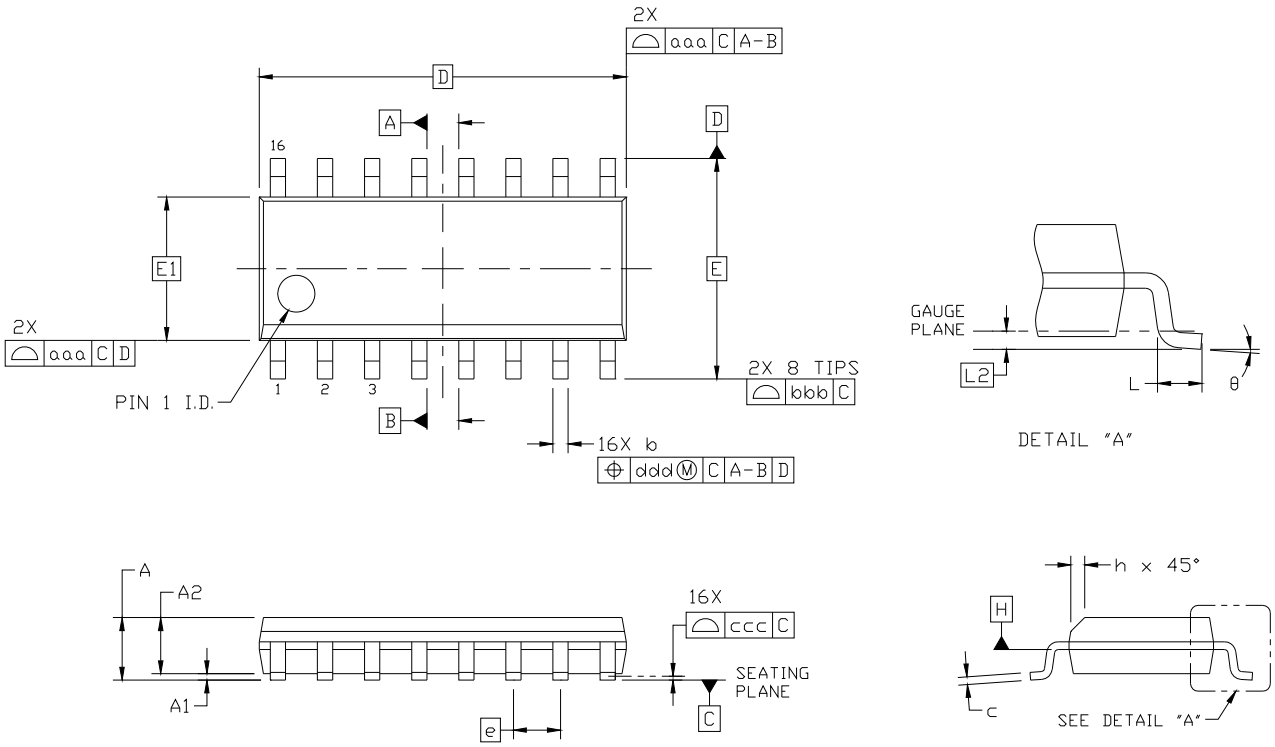


Figure 21. 16-pin Small Outline Integrated Circuit (SOIC) Package

Table 15. Package Diagram Dimensions

Dimension	Min	Max
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.17	0.25
D	9.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27

Table 15. Package Diagram Dimensions (Continued)

L2	0.25 BSC	
h	0.25	0.50
θ	0°	8°
aaa	0.10	
bbb	0.20	
ccc	0.10	
ddd	0.25	

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MS-012, Variation AC.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

8. Top Marking

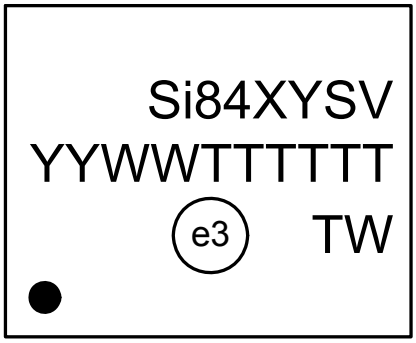


Figure 22. Si8460/61/62/63 Top Marking

Table 16. Top Marking Explanation

Line 1 Marking:	Base Part Number Ordering Options (See Ordering Guide for more information).	Si84 = Isolator product series XY = Channel Configuration X = # of data channels (6, 5, 4, 3, 2, 1) Y = # of reverse channels (3, 2, 1, 0) S = Speed Grade A = 1 Mbps; B = 150 Mbps V = Insulation rating A = 1 kV; B = 2.5 kV
Line 2 Marking:	YY = Year WW = Workweek	Assigned by Assembly House. Corresponds to the year and workweek of the mold date.
	TTTTTT = Mfg Code	Manufacturing Code from Assembly House
Line 3 Marking:	Circle = 1.5 mm Diameter (Center-Justified)	“e3” Pb-Free Symbol
	Country of Origin ISO Code Abbreviation	TW = Taiwan

NOTES:

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