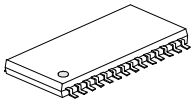
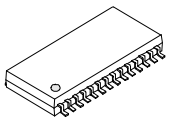
INTELLIGENT +3.0V TO +5.5V RS-232 THREE DRIVERS AND FIVE RECEIVERS WITH LOW POWER SHUTDOWN

DESCRIPTION

The SPB3243 products are 3 driver/5 receiver RS-232 transceiver solutions intended for portable or handheld applications such as notebook and palmtop computers. The SPB3243 includes one complementary receiver that remains alert to monitor an external device's Ring Indicate signal while the device is shutdown. The SPB3243E and EB devices feature slew-rate limited outputs for reduced crosstalk and EMI. The "U" and "H" series are optimized for high speed with data rates up to 1Mbps, easily meeting the demands of high speed RS-232 applications. The SPB3243 series uses an internal high-efficiency, charge-pump power supply that requires only 0.1μF capacitors in 3.3V operation. This charge pump and driver architecture allow the SPB3243 series to deliver compliant RS-232 performance from a single power supply ranging from +3.0V to +5.5V. The AUTO ON-LINE® feature allows the device to automatically "wake-up" during a shutdown state when an RS-232 cable is connected and a connected peripheral is turned on. Otherwise, the device automatically shuts itself down drawing less than 1μA.



SSOP-28-300-0.65



SOP-28-375-1.27

FEATURES

* Meets true EIA/TIA-232-F Standards from a +3.0V to +5.5V power supply
* Interoperable with EIA/TIA-232 and adheres to EIA/TIA-562 down to a +2.7V power source
* AUTO ON-LINE® circuitry automatically wakes up from a 1μA shutdown
* Regulated Charge Pump Yields Stable RS-232 Outputs Regardless of V_{CC} Variations
* Enhanced ESD Specifications:
  -- ±15kV Human Body Model
  -- ±15kV IEC1000-4-2 Air Discharge
  -- ±8kV IEC1000-4-2 Contact Discharge
* 250 kbps min. transmission rate (EB)
* 1000 kbps min. transmission rate (EU)
* Ideal for High Speed RS-232 Applications

APPLICATIONS

* Portable Applications
* Hand-held Applications
* Notebook Computers
* Palmtop Computers
* Mouse-Driving Applications
* High Speed RS-232

ORDERING INFORMATION

Device	Temperature Range	Package	Device	Temperature Range	Package
SPB3243EBCA	0℃~70℃	SSOP-28-300-0.65	SPB3243EUCA	0℃~70℃	SSOP-28-300-0.65
SPB3243EBCT	0℃~70℃	SOP-28-375-1.27	SPB3243EUCT	0℃~70℃	SOP-28-375-1.27
SPB3243EBEA	-40℃~85℃	SSOP-28-300-0.65	SPB3243EUEA	-40℃~85℃	SSOP-28-300-0.65
SPB3243EBET	-40℃~85℃	SOP-28-375-1.27	SPB3243EUET	-40℃~85℃	SOP-28-375-1.27
SPB3243ECA	0℃~70℃	SSOP-28-300-0.65	SPB3243EEA	-40℃~85℃	SSOP-28-300-0.65
SPB3243ECT	0℃~70℃	SOP-28-375-1.27	SPB3243EET	-40℃~85℃	SOP-28-375-1.27

SELECTION TABLE

Device	Power Supplies	RS-232 Drivers	RS-232 Receivers	External Components	AUTO ON-LINE® Circuitry	TTL3-State	NO.of pins	Gauranteed Data Rate	ESD Rating
SPB3243	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	120	2kV
SPB3243E	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	120	15kV
SPB3243B	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	250	2kV
SPB3243EB	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	250	15kV
SPB3243U	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	1000	2kV
SPB3243EU	+3.0V~+5.5V	3	5	4 capacitors	YES	YES	28	1000	15kV

ABSOLUTE MAXIMUM RATING

Parameter	Value	Unit
V_{CC}	-0.3 ~ +6.0	V
V+(Note1)	-0.3 ~ +7.0	V
V-(Note1)	+0.3 ~ -7.0	V
V++|V-|(Note1)	+13	V
I_{CC}(DC V_{CC} or GND Current)	±100	mA
Input Voltages		
TxIN, $\overline{SHDN}$, $\overline{ONLINE}$	-0.3 ~ (V_{CC}+6.0)	V
RxIN	±15	V
Output Voltages		
TxOUT	±13.2	V
RxOUT, $\overline{STATUS}$	-0.3 ~ (V_{CC}+0.3)	V
Short-Circuit Duration		
TxOUT	Continuous	
Storage Temperature	-65 ~ +150	℃
Power Dissipation Per Package		
SSOP-28-300-0.65	900 (derate11.2mW/℃ above +70℃)	mW
SOP-28-375-1.27	1000 (derate12.7mW/℃ above +70℃)	mW

Note 1: V+ and V- can have maximum magnitudes of 7V, but their absolute difference cannot exceed 13V.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, the following specifications apply for Vcc= +3.0V~+5.5V, $T_{amb}=T_{MIN}$~T_{MAX}, C1-C4=0.1μF, Typical Values are at V_{CC}=+3.3V or +5.0V and T_{amb}=25℃)

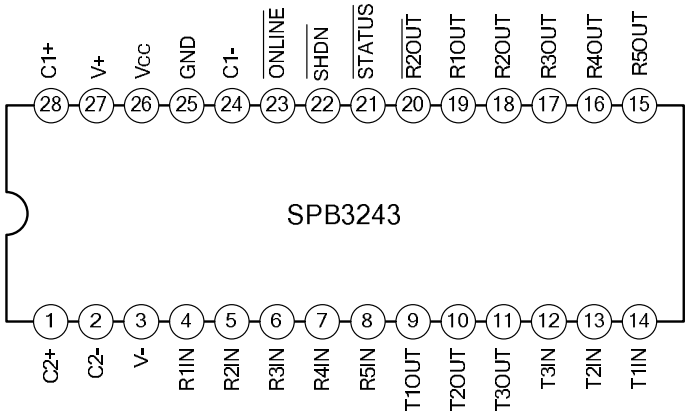
Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
DC CHARACTERISTICS						
Supply Current, AUTO ON-LINE®	I_{CC}	All R_XIN open, $\overline{ONLINE}$=GND, $\overline{SHDN}$= V_{CC} , V_{CC}=+3.3V, T_{amb}=25°C, T_XIN=GND or V_{CC}		1.0	10	μA
Supply Current, Shutdown	I_{OFF}	$\overline{SHDN}$ =GND, V_{CC}=+3.3V, T_{amb}=25°C, T_XIN=GND or V_{CC}		1.0	10	μA
Supply Current, AUTO ON-LINE® Disabled	I_{CCN}	$\overline{ONLINE}$= $\overline{SHDN}$ =V_{CC}, no load, V_{CC}=+3.3V, T_{amb}=25℃, T_XIN=GND or V_{CC}		0.3	1.0	mA
LOGIC INPUTS AND RECEIVER OUTPUTS						
Input Logic Threshold		V_{CC}=+3.3V or 5.0V, T_XIN, $\overline{SHDN}$, $\overline{ONLINE}$				
LOW	V_{RIL}				0.8	V
HIGH	V_{RIH}		2.4			V
Input Leakage Current	I_{RIN}	T_XIN, $\overline{SHDN}$, $\overline{ONLINE}$ T_{amb}=25° C, V_{IN}=0V to V_{CC}		±0.01	±1.0	μA
Output Leakage Current	I_{ROUT}	Receivers Disabled, V_{OUT}=0V to V_{CC}		±0.05	±10	μA
Output Voltage LOW	V_{ROL}	I_{OUT}=1.6mA			0.4	V
Output Voltage HIGH	V_{ROH}	I_{OUT}=-1.0mA	V_{CC}-0.6	V_{CC}-0.1		V
DRIVER OUTPUTS						
Output Voltage Swing	V_{DOUT}	All driver outputs loaded with 3kΩ to GND, T_{amb}=25 ℃	±5.0	±5.4		V
Output Resistance	R_{DOUT}	V_{CC} = V+ = V- = 0V, V_{OUT} = ±2V	300			Ω
Output Short-Circuit Current	I_{DOUTS}	V_{OUT} = 0V		±35	±60	mA
Output Leakage Current	I_{DOUTS}	V_{CC}=0V to3.0V to 5.5V, V_{OUT}= ±12V, Driver disabled			±25	μA
RECEIVER INPUTS						
Input Voltage Range	V_{RIN}		-15		15	V
Input Threshold LOW	V_{RIL}	V_{CC} = +3.3V	0.6	1.2		V
Input Threshold LOW	V_{RIL}	V_{CC} = +5.0V	0.8	1.5		V
Input Threshold HIGH	V_{RIH}	V_{CC} = +3.3V		1.5	2.4	V
Input Threshold HIGH	V_{RIH}	V_{CC} = +5.0V		1.8	2.4	V
Input Hysteresis	V_{RHIN}			0.3		V
Input Resistance	R_{RIN}		3	5	7	kΩ
ATUO ON-LINE® CIRCUITRY CHARACTERISTICS ($\overline{ONLINE}$ =GND, $\overline{SHDN}$ =V_{CC})25°C						
$\overline{STATUS}$ Output Voltage LOW	V_{SOL}	I_{OUT}=1.6mA			0.4	V
$\overline{STATUS}$ Output Voltage HIGH	V_{SOH}	I_{OUT}=-1.0mA	V_{CC}-0.6			V

(To be continued)

(Continued)

Characteristics	Symbol	Conditions	Min.	Typ.	Max.	Unit
Receiver Threshold to Drivers Enabled	t_{ONLINE}	*Figure 10*		350		µs
Receiver Positive or Negative Threshold to $\overline{STATUS}$ HIGH	t_{STSH}	*Figure 10*		0.2		µs
Receiver Positive or Negative Threshold to $\overline{STATUS}$ LOW	t_{STSL}	*Figure 10*		30		µs
TIMING CHARACTERISTICS						
Maximum Data Rate (U)		R_L=3kΩ, C_L=250pF, One driver active	1000			kbps
Maximum Data Rate (H)		R_L=3kΩ,C_L=1000pF,One driver active	460			kbps
Maximum Data Rate (B)			250			kbps
Maximum Data Rate (-)			120			kbps
Receiver Propagation Delay	t_{PHL}	Receiver Input to Receiver Output , C_L=150pF		0.15		µs
Receiver Propagation Delay	t_{PLH}			0.15		
Receiver Output Enable Time	t_{ROE}	Normal operation		200		ns
Receiver Output Disable Time	t_{RON}	Normal operation		200		ns
Driver Skew (E,EB)	t_{DS}	$\|t_{PHL} - t_{PLH}\|$		100	500	ns
Driver Skew (EU)	t_{DS}			50	100	
Receiver Skew	t_{RS}	$\|t_{PHL} - t_{PLH}\|$		50		ns
Transition-Region Slew Rate(U)	V_{TRS}	V_{CC}=3.3V, R_L=3KΩ, T_{amb} = 25°C , measurements taken from -3.0V to +3.0V or +3.0V to -3.0V		90		V/µs
Transition-Region Slew Rate (EB)	V_{TRS}		6		30	

PIN CONFIGURATION



PIN DESCRIPTION

Pin no.	Pin name	I/O	Functions
1	C2+	-	Positive terminal of the inverting charge-pump capacitor.
2	C2-	-	Negative terminal of the inverting charge-pump capacitor.
3	V-	-	Regulated -5.5V output generated by the charge pump.
4	R1IN	-I	RS-232 receiver input.
5	R2IN	-I	RS-232 receiver input.
6	R3IN	I	RS-232 receiver input.
7	R4IN	I	RS-232 receiver input.
8	R5IN	I	RS-232 receiver input.
9	T1OUT	O	RS-232 driver output.
10	T2OUT	O	RS-232 driver output.
11	T3OUT	O	RS-232 driver output.
12	T3IN	I	TTL/CMOS driver input.
13	T2IN	I	TTL/CMOS driver input.
14	T1IN	I	TTL/CMOS driver input.
15	R5OUT	O	TTL/CMOS receiver output.
16	R4OUT	O	TTL/CMOS receiver output.
17	R3OUT	O	TTL/CMOS receiver output.
18	R2OUT	O	TTL/CMOS receiver output.
19	R1OUT	O	TTL/CMOS receiver output.
20	$\overline{\text{R2OUT}}$	O	Non-inverting receiver-2 output, active in shutdown.
21	$\overline{\textbf{STATUS}}$	O	TTL/CMOS Output indicating online and shutdown status.
22	$\overline{\text{SHDN}}$	I	Apply logic LOW to shut down drivers and charge pump. This overrides all AUTO ON-LINE® circuitry and $\overline{\text{ONLINE}}$ (refer to *Table 2*).
23	$\overline{\text{ONLINE}}$	I	Apply logic HIGH to override Auto-Online circuitry keeping drivers active ($\overline{\text{SHDN}}$ must also be logic HIGH, refer to *Table 2*).
24	C1-	-	Negative terminal of the voltage doubler charge-pump capacitor.
25	GND	-	Ground.
26	V_{CC}	-	+3.0V to +5.5V supply voltage.
27	V+	-	Regulated +5.5V output generated by the charge pump.
28	C1+	-	Positive terminal of the voltage doubler charge-pump capacitor.

FUNCTION DESCRIPTION

The SPB3243 transceivers meet the EIA/TIA-232 and ITU-T V.28/V.24 communication protocols and can be implemented in battery-powered, portable, or hand-held applications such as notebook or palmtop computers. The SPB3243 devices feature on-board charge pump circuitry that generates ±5.5V RS-232 voltage levels from a single +3.0V to +5.5V power supply. The SPB3243EU devices can operate at a data rate of 1000kbps fully loaded.

The SPB3243 is a 3-driver/5-receiver device, ideal for portable or hand-held applications. The SPB3243 includes one complementary always-active receiver that can monitor an external device (such as a modem) in shutdown. This aids in protecting the UART or serial controller IC by preventing forward biasing of the protection diodes where VCC may be disconnected.

The SPB3243 series is an ideal choice for power sensitive designs. The SPB3243 devices feature AUTO ON-LINE® circuitry which reduces the power supply drain to a 1μA supply current. In many portable or hand-held applications, an RS-232 cable can be disconnected or a connected peripheral can be turned off. Under these conditions, the internal charge pump and the drivers will be shut down. Otherwise, the system automatically comes online. This feature allows design engineers to address power saving concerns without major design changes.

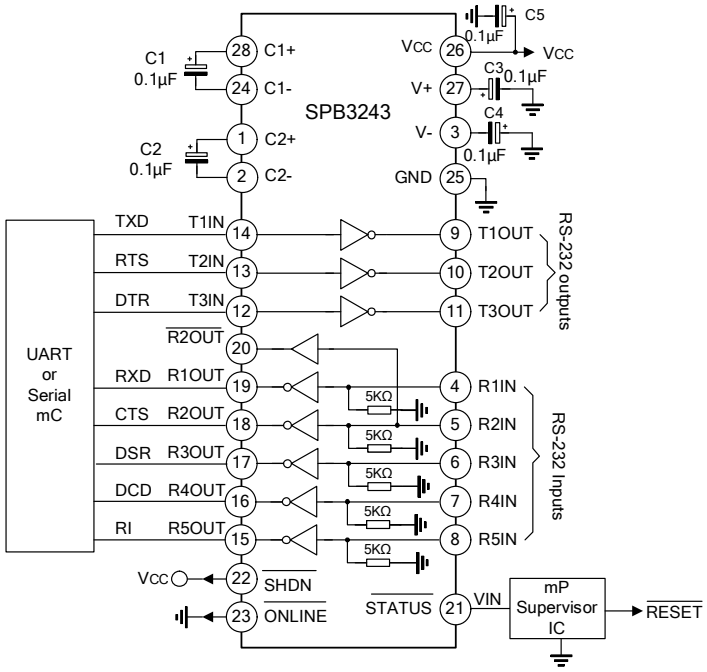


Figure 1. Interface Circuitry Controlled by Microprocessor Supervisory Circuit

THEROY OF OPERATION

The SPB3243 series is made up of four basic circuit blocks:

1. Drivers
2. Receivers
3. Charge Pump
4. AUTO ON-LINE® circuitry.

DRIVERS

The drivers are inverting level transmitters that convert TTL or CMOS logic levels to 5.0V EIA/ TIA-232 levels with an inverted sense relative to the input logic levels. Typically, the RS-232 output voltage swing is ±5.4V with no load and ±5V minimum fully loaded. The driver outputs are protected against infinite short-circuits to ground without degradation in reliability. These drivers comply with the EIA-TIA-232-F and all previous RS-232 versions. Unused drivers inputs should be connected to GND or Vcc.

The drivers have a minimum data rate of 250kbps (EB) or 1000kbps (EU) fully loaded.

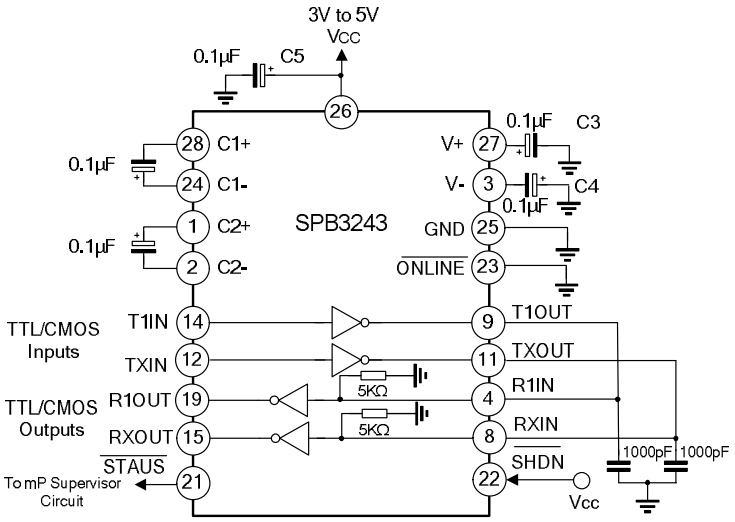


Figure 2. Loopback Test Circuit for RS-232 Driver Data Transmission Rates

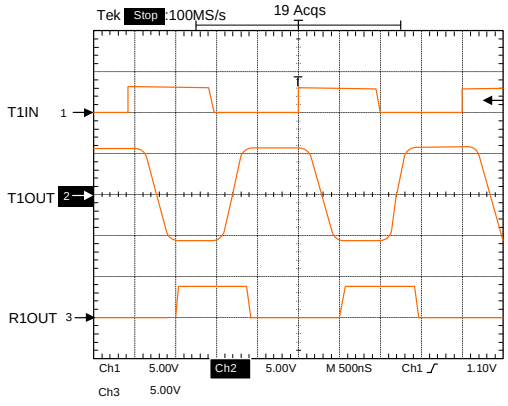


Figure 3. Loopback Test Circuit Result at 1Mbps

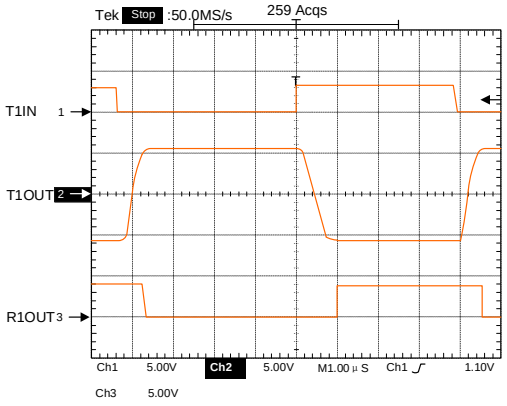


Figure 4. Loopback Test Circuit Result at 250kbps

Figure 2 shows a loopback test circuit used to test the RS-232 Drivers. *Figure 3* shows the test results where one driver was active at 1Mbps and all three drivers loaded with an RS-232 receiver in parallel with a 250pF capacitor. *Figure 4* shows the test results of the loopback circuit with all drivers active at 250kbps with typical RS-232 loads in parallel with 1000pF capacitors. A superior RS-232 data transmission rate of 1Mbps makes the SPB3243EU an ideal match for high speed LAN and personal computer peripheral applications.

RECEIVERS

The receivers convert ±5.0V EIA/TIA-232 levels to TTL or CMOS logic output levels. Receivers are active when the AUTO ON-LINE® circuitry is enabled or when in shutdown. During the shutdown, the receivers will continue to be active. If there is no activity present at the receivers for a period longer than 100μs or when SHUTDOWN is enabled, the device goes into a standby mode where the circuit draws 1μA. The truth table logic of the SPB3243 driver and receiver outputs can be found in *Table 1*.

Table 1. $\overline{SHDN}$ Truth Tables

DEVICE:SPB3243EU			
$\overline{SHDN}$	TxOUT	RxOUT	$\overline{R2OUT}$
0	High Z	High Z	Active
1	Active	Active	Active

Note: In AUTO ON-LINE® Mode where $\overline{ONLINE}$ =GND and $\overline{SHDN}$ = VCC, the device will shut down if there is no activity present at the Receiver inputs.

The SPB3243 includes an additional non-inverting receiver with an output R2OUT. R2OUT is an extra output that remains active and monitors activity while the other receiver outputs are forced into high impedance. This allows Ring Indicator (RI) from a peripheral to be monitored without forward biasing the TTL/CMOS inputs of the other devices connected to the receiver outputs.

Since receiver input is usually from a transmission line where long cable lengths and system interference can degrade the signal, the inputs have a typical hysteresis margin of 300mV. This ensures that the receiver is virtually immune to noisy transmission lines. Should an input be left unconnected, an internal 5kΩ pulldown resistor to ground will commit the output of the receiver to a HIGH state.

CHARGE PUMP

The charge pump uses a unique approach compared to older less–efficient designs. The charge pump still requires four external capacitors, but uses a four–phase voltage shifting technique to attain symmetrical 5.5V power supplies. The internal power supply consists of a regulated dual charge pump that provides output voltages 5.5V regardless of the input voltage (VCC) over the +3.0V to +5.5V range. This is important to maintain compliant RS-232 levels regardless of power supply fluctuations.

The charge pump operates in a discontinuous mode using an internal oscillator. If the output voltages are less than a magnitude of 5.5V, the charge pump is enabled. If the output voltages exceed a magnitude of 5.5V, the charge pump is disabled. This oscillator controls the four phases of the voltage shifting. A description of each phase follows.

Phase 1

VSS charge storage — During this phase of the clock cycle, the positive side of capacitors C1 and C2 are initially charged to VCC. C1+ is then switched to GND and the charge in C1 – is transferred to C2–. Since C2+ is connected to VCC, the voltage potential across capacitor C2 is now 2 times VCC.

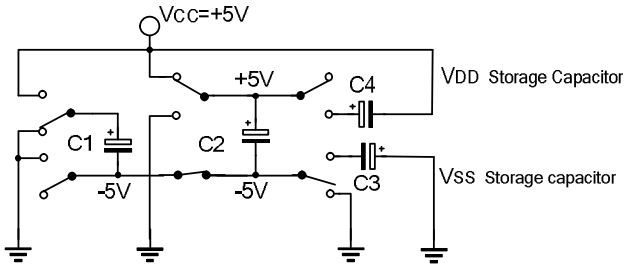


Figure 5. Charge Pump— Phase 1

Phase 2

VSS transfer — Phase two of the clock connects the negative terminal of C2 to the VSS storage capacitor and the positive terminal of C2 to GND. This transfers a negative generated voltage to C3. This generated voltage is regulated to a minimum voltage of -5.5V. Simultaneous with the transfer of the voltage to C3, the positive side of capacitor C1 is switched to VCC and the negative side is connected to GND.

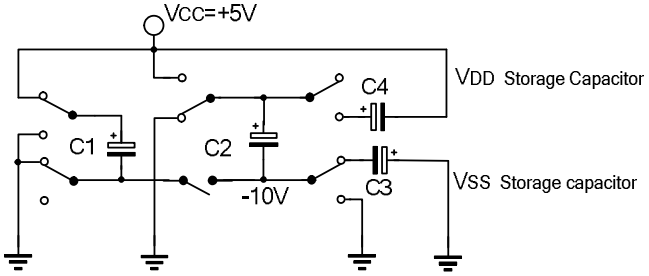


Figure6. Charge Pump— Phase 2

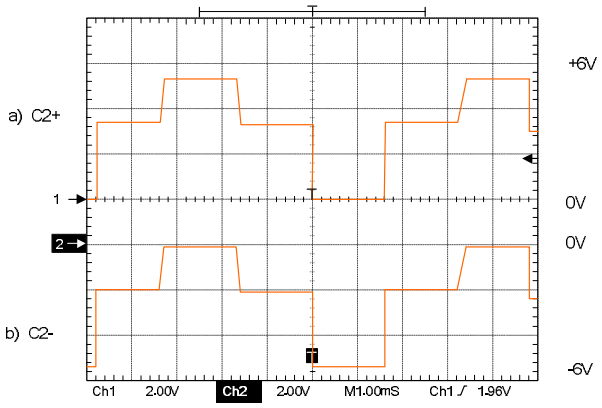


Figure 7. Charge Pump Waveforms

Phase 3

VDD charge storage — The third phase of the clock is identical to the first phase — the charge transferred in C1 produces –VCC in the negative terminal of C1, which is applied to the negative side of capacitor C2. Since C2 + is at VCC, the voltage potential across C2 is 2 times VCC.

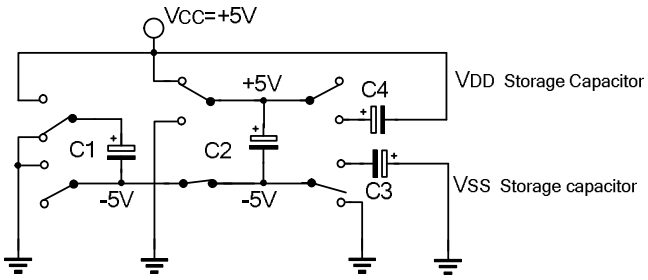


Figure 8. Charge Pump— Phase 3

Phase 4

VDD transfer — The fourth phase of the clock connects the negative terminal of C2 to GND, and transfers this positive generated voltage across C2 to C4, the VDD storage capacitor. This voltage is regulated to +5.5V. At this voltage, the internal oscillator is disabled. Simultaneous with the transfer of the voltage to C4, the positive side of capacitor C1 is switched to VCC and the negative side is connected to GND, allowing the charge pump cycle to begin again. The charge pump cycle will continue as long as the operational conditions for the internal oscillator are present.

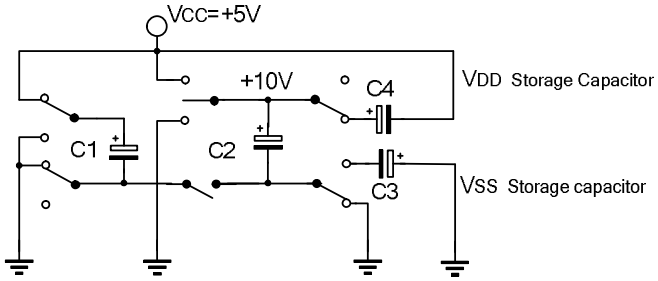


Figure 9. Charge Pump— Phase 4

Since both V+ and V– are separately generated from VCC, in a no-load condition V+ and V– will be symmetrical. Older charge pump approaches that generate V– from V+ will show a decrease in the magnitude of V– compared to V+ due to the inherent inefficiencies in the design. The clock rate for the charge pump typically operates at greater than 250kHz. The external capacitors can be as low as 0.1μF with a 16V breakdown voltage rating.

The charge pumps are designed to operate reliably with a range of low cost capacitors. Either polarized or non polarized capacitors may be used. If polarized capacitors are used they should be oriented as shown in the Typical Operating Circuit. The V+ capacitor may be connected to either ground or VCC (polarity reversed.)

The charge pump operates with 0.1μF capacitors for 3.3V operation. For other supply voltages, see the table for required capacitor values. Do not use values smaller than those listed. Increasing the capacitor values (e.g., by doubling in value) reduces ripple on the transmitter outputs and may slightly reduce power consumption. C2, C3, and C4 can be increased without changing C1's value.

For best charge pump efficiency locate the charge pump and bypass capacitors as close as possible to the IC. Surface mount capacitors are best for this purpose. Using capacitors with lower equivalent series resistance (ESR) and selfinductance, along with minimizing parasitic PCB trace inductance will optimize charge pump operation. Designers are also advised to consider that capacitor values may shift over time and operating temperature.

Minimum recommended charge pump capacitor value	
Input Voltage Vcc	Charge pump capacitor value for SPB32XX
3.0V to 3.6V	C1 –C4 = 0.1μF
4.5V to 5.5V	C1 = 0.047μF, C2-C4 = 0.33μF
3.0V to 5.5V	C1 –C4 = 0.22μF

AUTO ONLINE CIRCUITRY

The SPB3243 devices have a patent pending AUTO ON-LINE® circuitry on board that saves power in applications such as laptop computers, palmtop (PDA) computers and other portable systems.

The SPB3243 devices incorporate an AUTO ONLINE ® circuit that automatically enables itself when the external transmitters are enabled and the cable is connected. Conversely, the AUTO ON-LINE® circuit also disables most of the internal circuitry when the device is not being used and goes into a standby mode where the device typically draws 1mA. This function can also be externally controlled by the $\overline{\text{ONLINE}}$ pin. When this pin is tied to a logic LOW, the AUTO ON-LINE® function is active. Once active, the device is enabled until there is no activity on the receiver inputs. The receiver input typically sees at least ±3V, which are generated from the transmitters at the other end of the cable with a ±5V minimum. When the external transmitters are disabled or the cable is disconnected, the receiver inputs will be pulled down by their internal 5kΩ resistors to ground. When this occurs over a period of time, the internal transmitters will be disabled and the device goes into a shutdown or standby mode. When $\overline{\text{ONLINE}}$ is HIGH, the AUTO ON-LINE® mode is disabled.

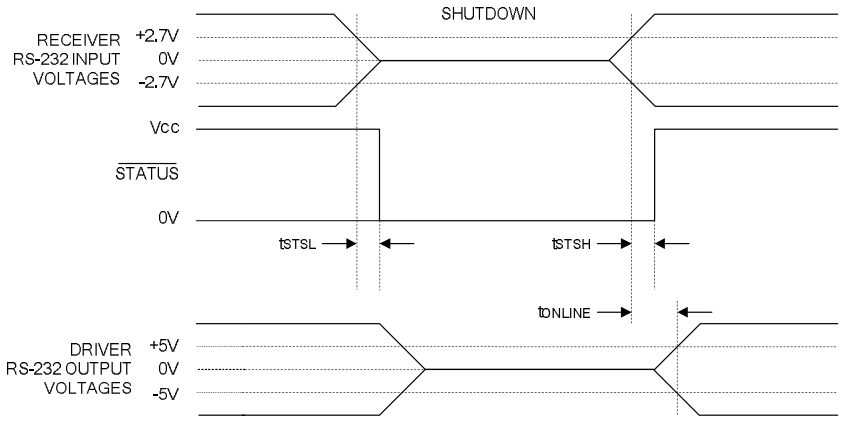


Figure 10. AUTO ON-LINE® Timing Waveforms

The AUTO ON-LINE® circuit has two stages:

1) Inactive Detection

2) Accumulated Delay

The first stage, shown in *Figure 11*, detects an inactive input. A logic HIGH is asserted on RxINACT if the cable is disconnected or the external transmitters are disabled. Otherwise, RxINACT will be at a logic LOW. This circuit is duplicated for each of the other receivers.

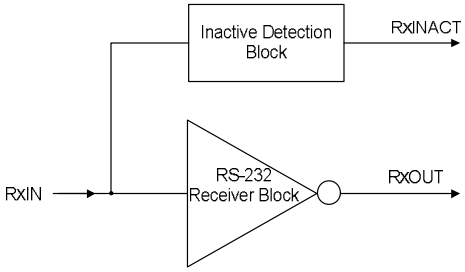


Figure 11. Stage I of AUTO ON-LINE® Circuitry

The second stage of the AUTO ON-LINE® circuitry, shown in *Figure 12*, processes all the receiver's RxINACT signals with an accumulated delay that disables the device to a 1µA supply current.

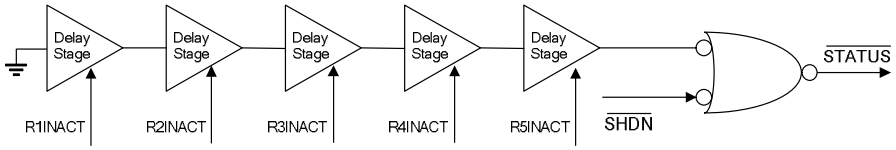


Figure 12. Stage II of AUTO ON-LINE® Circuitry

The $\overline{\text{STATUS}}$ pin goes to a logic LOW when the cable is disconnected, the external transmitters are disabled, or the $\overline{\text{SHDN}}$ pin is invoked. The typical accumulated delay is around 20µs.

When the SPB3243 drivers or internal charge pump are disabled, the supply current is reduced to 1µA. This can commonly occur in hand-held or portable applications where the RS-232 cable is disconnected or the RS-232 drivers of the connected peripheral are turned off.

The AUTO ON-LINE® mode can be disabled by the $\overline{\text{SHDN}}$ pin. If this pin is a logic LOW, the AUTO ON-LINE® function will not operate regardless of the logic state of the $\overline{\text{ONLINE}}$ pin. *Table 2* summarizes the logic of the AUTO ONLINE ® operating modes. The truth table logic of the SPB3243 driver and receiver outputs can be found in *Table 2*

Table 2. AUTO ON-LINE® Logic

RS-232 SIGNAL AT RECEIVER INPUT	$\overline{\text{SHDN}}$ INPUT	$\overline{\text{ONLINE}}$ INPUT	$\overline{\text{STATUS}}$ OUTPUT	TRANSCEIVER STATUS
YES	HIGH	LOW	HIGH	Normal Operation*(Auto-Online)*
NO	HIGH	HIGH	LOW	Normal Operation
NO	HIGH	LOW	LOW	Shutdown*(Auto-Online)*
YES	LOW	HIGH/LOW	HIGH	Shutdown
NO	LOW	HIGH/LOW	LOW	Shutdown

The $\overline{\text{STATUS}}$ pin outputs a logic LOW signal if the device is shut down. This pin goes to a logic HIGH when the external transmitters are enabled and the cable is connected.

When the SPB3243 devices are shut down, the charge pumps are turned off. V+ charge pump output decays to VCC, the V- output decays to GND. The decay time will depend on the size of capacitors used for the charge pump. Once in shutdown, the time required to exit the shut down state and have valid V+ and V- levels is typically 200µs.

For easy programming, the $\overline{\text{STATUS}}$ can be used to indicate DSR or a Ring Indicator signal. Tying $\overline{\text{ONLINE}}$ and $\overline{\text{SHDN}}$ together will bypass the AUTO ON-LINE® circuitry so this connection acts like a shutdown

input pin.

The SPB3243 driver outputs are able to maintain voltage under loading of up to 2.5mA per driver, ensuring sufficient output for mouse-driving applications.

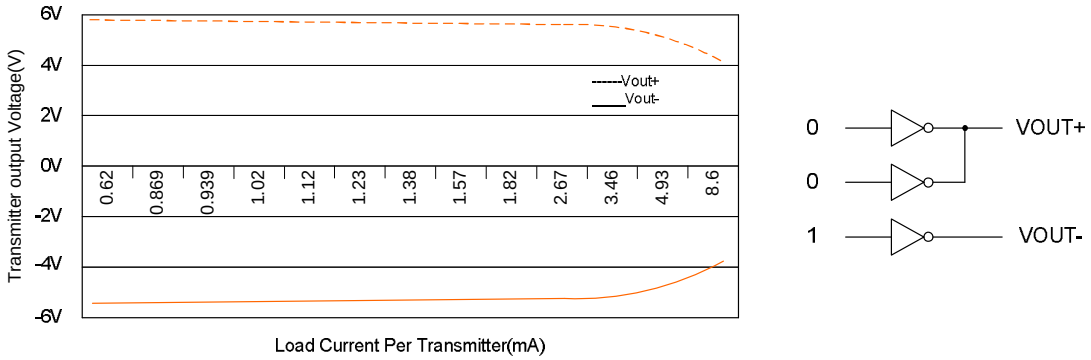


Figure 13. SPB3243 Driver Output Voltages vs.Load Current per Transmitter

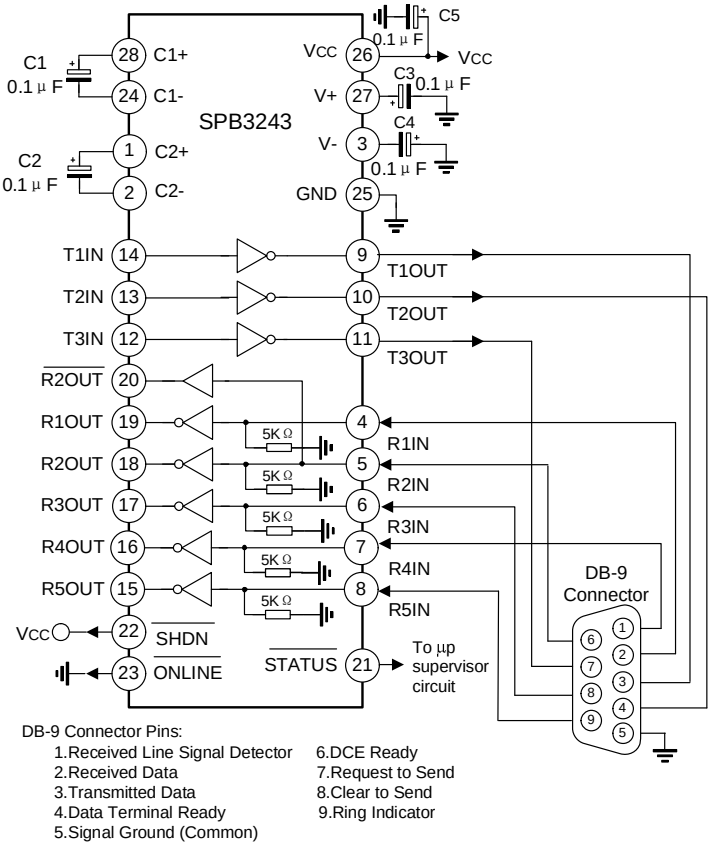


Figure 14. Circuit for the connectivity of the SPB3243 with a DB-9 connector

ESD TOLERANCE

The SPB3243 series incorporates ruggedized ESD cells on all driver output and receiver input pins. The ESD structure is improved over our previous family for more rugged applications and environments sensitive to electro-static discharges and associated transients. The improved ESD tolerance is at least ±15kV without

damage nor latch-up.

There are different methods of ESD testing applied:

a) MIL-STD-883, Method 3015.7

b) IEC1000-4-2 Air-Discharge

c) IEC1000-4-2 Direct Contact

The Human Body Model has been the generally accepted ESD testing method for semiconductors. This method is also specified in MIL-STD-883, Method 3015.7 for ESD testing. The premise of this ESD test is to simulate the human body's potential to store electro-static energy and discharge it to an integrated circuit. The simulation is performed by using a test model as shown in *Figure 15*. This method will test the IC's capability to withstand an ESD transient during normal handling such as in manufacturing areas where the ICs tend to be handled frequently.

The IEC-1000-4-2, formerly IEC801-2, is generally used for testing ESD on equipment and systems. For system manufacturers, they must guarantee a certain amount of ESD protection since the system itself is exposed to the outside environment and human presence. The premise with IEC1000-4-2 is that the system is required to withstand an amount of static electricity when ESD is applied to points and surfaces of the equipment that are accessible to personnel during normal usage. The transceiver IC receives most of the ESD current when the ESD source is applied to the connector pins. The test circuit for IEC1000-4-2 is shown on *Figure 16*. There are two methods within IEC1000-4-2, the Air Discharge method and the Contact Discharge method.

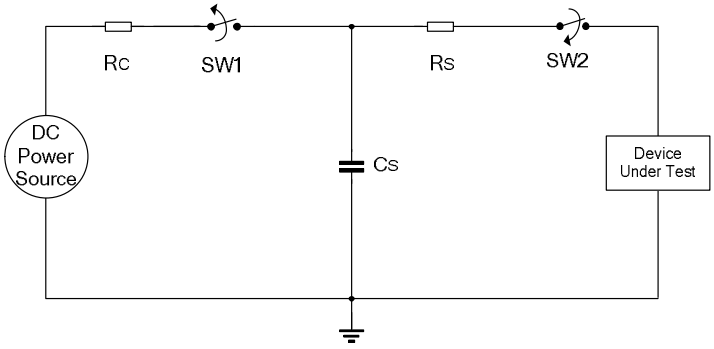


Figure 15 ESD Test Circuit for Human Body Model

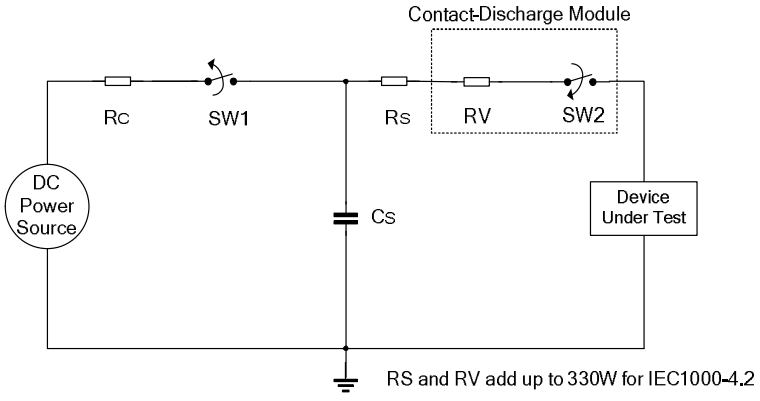


Figure 16. ESD Test Circuit for IEC1000-4-2

With the Air Discharge Method, an ESD voltage is applied to the equipment under test (EUT) through air. This simulates an electrically charged person ready to connect a cable onto the rear of the system only to find an

unpleasant zap just before the person touches the back panel. The high energy potential on the person discharges through an arcing path to the rear panel of the system before he or she even touches the system. This energy, whether discharged directly or through air, is predominantly a function of the discharge current rather than the discharge voltage. Variables with an air discharge such as approach speed of the object carrying the ESD potential to the system and humidity will tend to change the discharge current. For example, the rise time of the discharge current varies with the approach speed.

The Contact Discharge Method applies the ESD current directly to the EUT. This method was devised to reduce the unpredictability of the ESD arc. The discharge current rise time is constant since the energy is directly transferred without the air-gap arc. In situations such as hand held systems, the ESD charge can be directly discharged to the equipment from a person already holding the equipment. The current is transferred on to the keypad or the serial port of the equipment directly and then travels through the PCB and finally to the IC.

The circuit models in *Figures 15 and 16* represent the typical ESD testing circuit used for all three methods. The C_S is initially charged with the DC power supply when the first switch (SW1) is on. Now that the capacitor is charged, the second switch (SW2) is on while SW1 switches off. The voltage stored in the capacitor is then applied through R_S, the current limiting resistor, onto the device under test (DUT). In ESD tests, the SW2 switch is pulsed so that the device under test receives a duration of voltage.

For the Human Body Model, the current limiting resistor (R_S) and the source capacitor (C_S) are 1.5kΩ and 100pF, respectively. For IEC-1000-4-2, the current limiting resistor (R_S) and the source capacitor (C_S) are 330Ω and 150pF, respectively.

The higher C_S value and lower R_S value in the IEC1000-4-2 model are more stringent than the Human Body Model. The larger storage capacitor injects a higher voltage to the test point when SW2 is switched on. The lower current limiting resistor increases the current charge onto the test point.

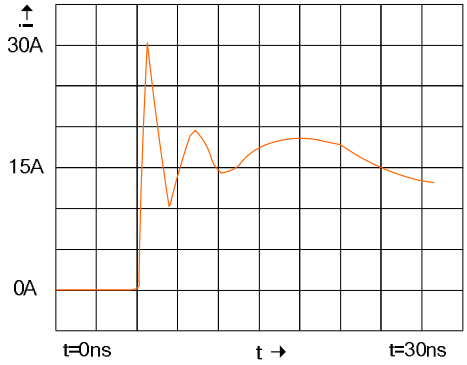
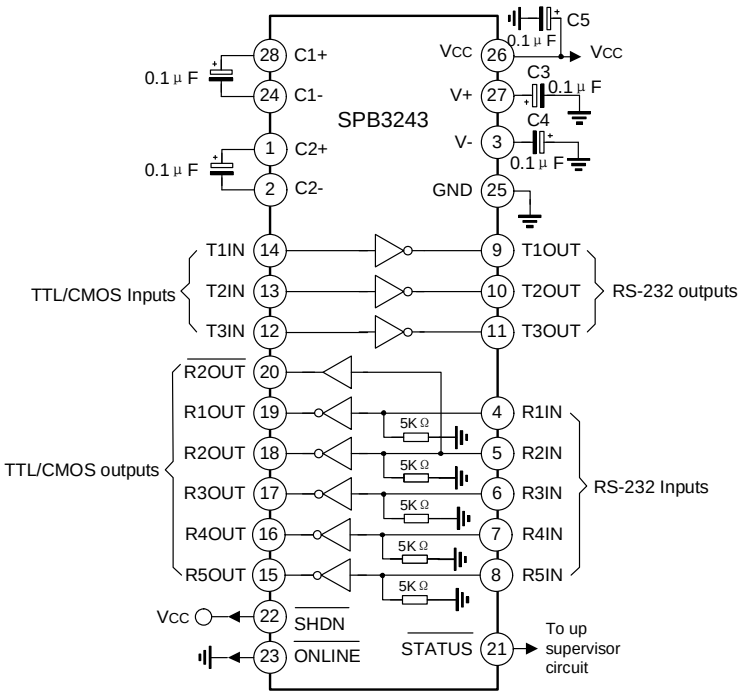


Figure 17. ESD Test Waveform for IEC1000-4-2

Table 3. Transceiver ESD Tolerance Levels

DEVICE PIN TESTED	HUMAN BODY MODEL	IEC1000-4-2		
		Air Discharge	Direct Contact	Level
Driver Outputs	±15kV	±15kV	±8kV	4
Receiver Inputs	±15kV	±15kV	±8kV	4

TYPICAL APPLICATION CIRCUIT



ELECTRICAL CHARACTERISTICS CURVES

(Unless otherwise noted, the following performance characteristics apply for Vcc = 3.3V, 1000kbps data rate, all drivers loaded with 3kΩ, 0.1μF charge pump capacitors, and Tamb= 25℃ .)

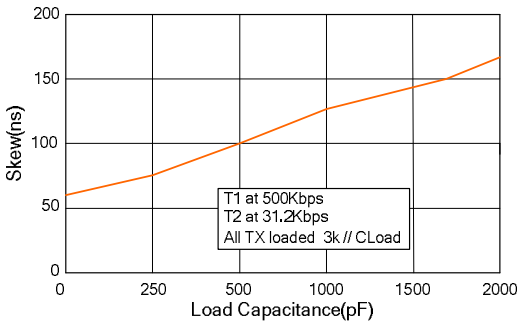


Figure 18. Transmitter Skew VS. Load Capacitance

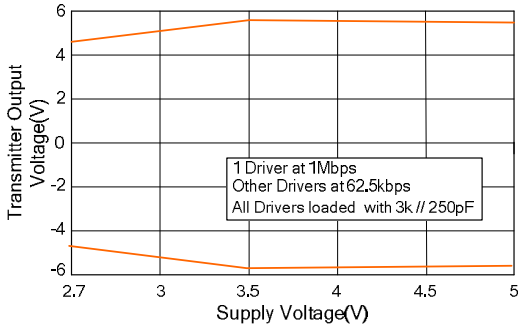


Figure 19.Transmitter Output Voltage VS. Supply Voltage for the SPB3243EU

ELECTRICAL CHARACTERISTICS CURVES(Continued)

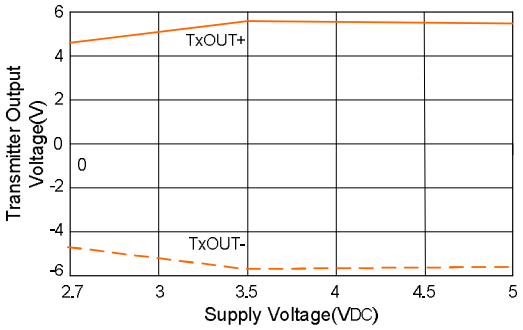


Figure 20. Transmitter Output Voltage VS. Supply Voltage for the SPB3243EU

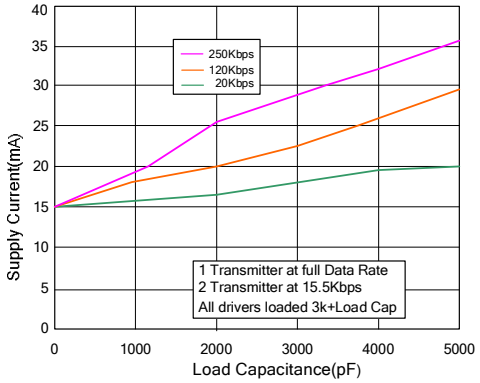


Figure 21. Supply Current VS. Load Capacitance for the SPB3243EU

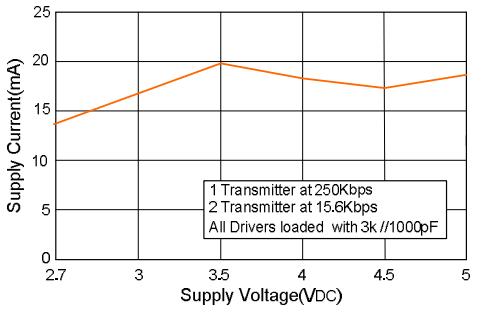


Figure 22. Supply Current VS. Supply Voltage for the SPB3243EU

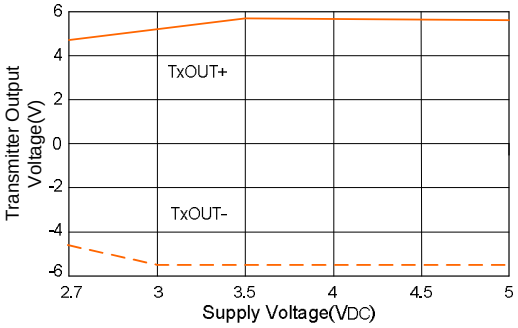


Figure 23. Transmitter Output Voltage VS. Supply Voltage for the SPB3243EU

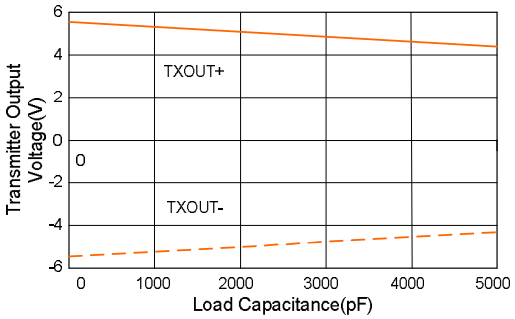


Figure 24. Transmitter Output Voltage VS. Load Capacitance

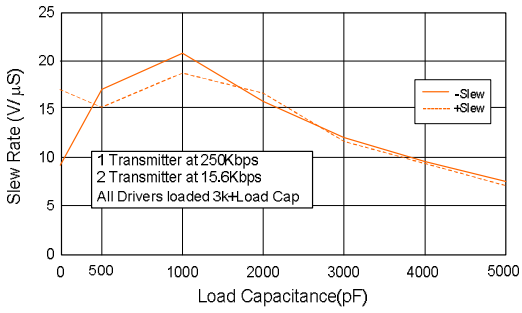


Figure 25. Slew Rate VS. Load Capacitance

ELECTRICAL CHARACTERISTICS CURVES(Continued)

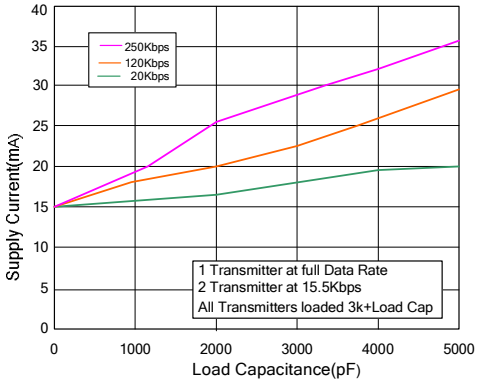


Figure 26. Supply Current VS. Load Capacitance

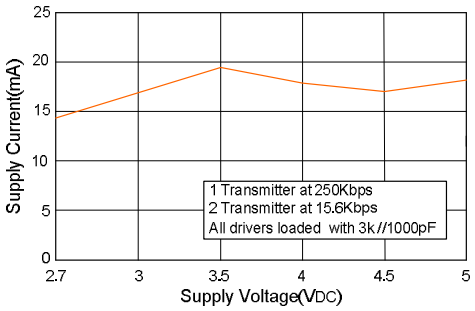
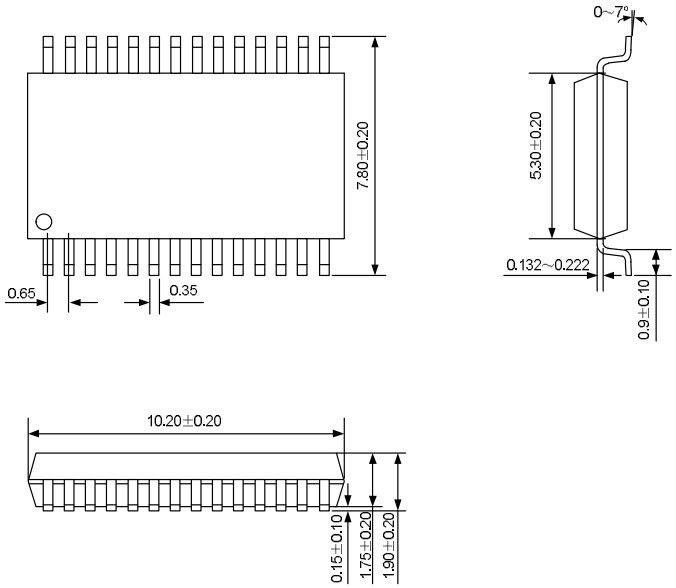


Figure 27. Supply Current VS. Supply Voltage

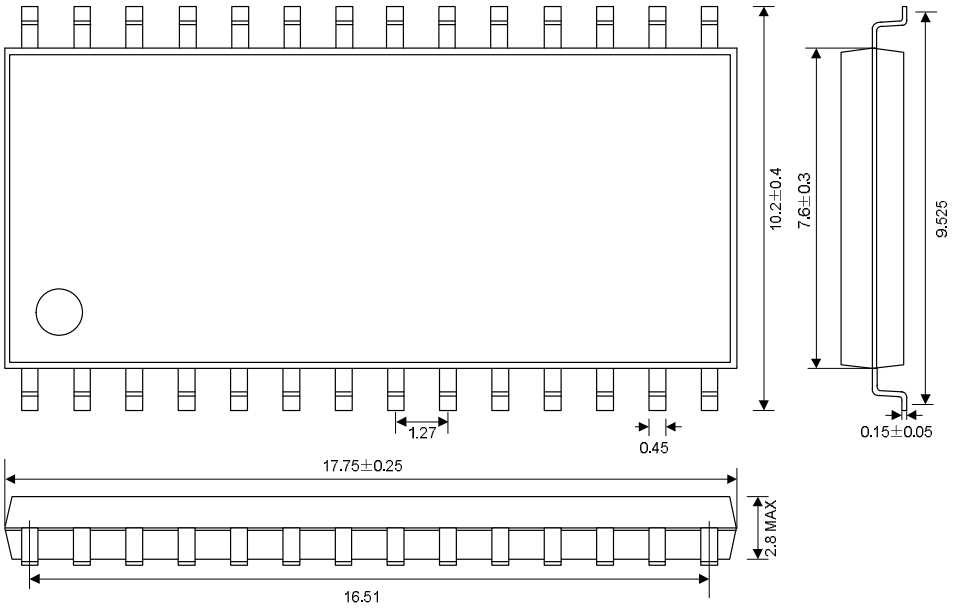
PACKAGE OUTLINE

SSOP-28-300-0.65 **Unit: mm**



PACKAGE OUTLINE(Continued)

SOP-28-375-1.27 Unit: mm



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