ENERGY METERING IC WITH PULSE OUTPUT

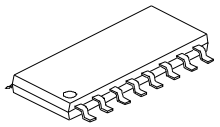
DESCRIPTION

The SC3333 is a high accuracy electrical energy measurement IC that can provides superior stability and accuracy over extremes in environmental conditions and over time. The SC3333 does not exhibit any creep when there is no load.

The SC3333 supplies average real power information on the low frequency outputs F1 and F2. This logic outputs may be used to directly drive an electromechanically counter or interface to an MCU. The CF logic output gives instantaneous real power information. This output is intended to be used for calibration purposes, or interfacing to an MCU.

The SC3333 includes a power supply monitoring circuit on the VDD supply pin. If the supply falls below 4V, the SC3333 will be reset and F1, F2 will be set to logic high, CF will be set to logic low at the same time.

The SC3333 provides synchronous frequency output for auto-reading meter system. The CF logic output is synchronous with the F1 and F2 logic output to ensure the show value of the meter is consonant with the real value.



SOP-16-225-1.27

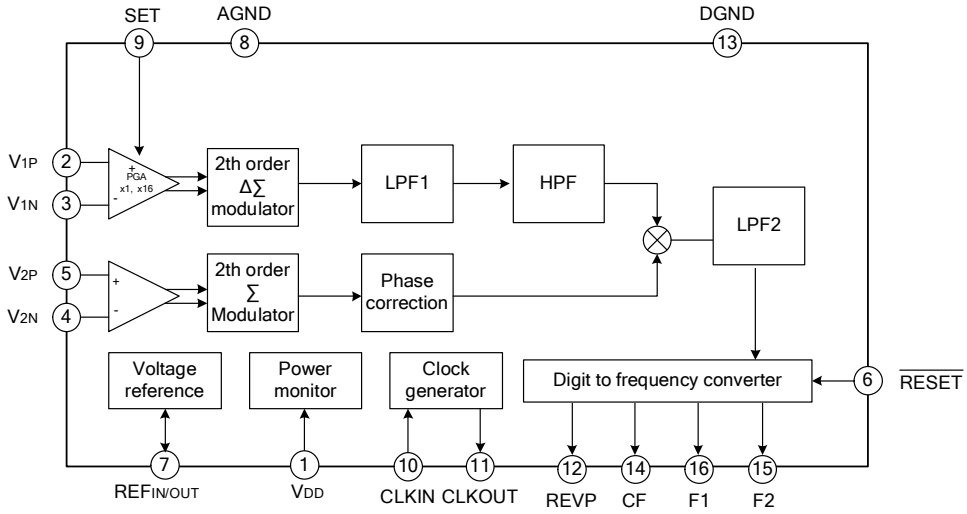
ORDERING INFORMATION

Device	Package
SC3333	SOP-16-225-1.27

FEATURES

* Single 5V supply, low power.
* On-chip power supply monitoring.
* On-chip reference with external overdrive capability.
* Supplies average real power on the frequency outputs F1 and F2, which can drive for electromechanical counters directly.
* The high frequency output CF is intended for calibration and supplies instantaneous real power.
* Less than 0.1% error over a dynamic range of 500 to 1.
* On-chip creep protection (No load threshold).
* The logic output REVP can be used to indicate a potential miswiring or negative power.
* A PGA in the current channel make flexible to select the shunt and burden resistance.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING (Tamb=25°C, unless otherwise specified)

Characteristics	Symbol	Ratings	Unit
V_{DD} to AGND/DGND	V_{DD}	-0.3 ~ +7	V
Analog Input Voltage to AGND V_{1P}, V_{1N}, V_{2P} and V_{2N}	AV_{IN}	-6 ~ +6	V
Reference Input voltage to AGND	V_{REF}	-0.3 ~ V_{DD}+0.3	V
Digital Input Voltage to DGND	DV_{IN}	-0.3 ~ V_{DD}+0.3	V
Digital Output Voltage to DGND	DV_{OUT}	-0.3 ~ V_{DD}+0.3	V
Power Dissipation	P_D	450	mW
Operating Temperature Range	T_{OPR}	-40~ +85	°C
Storage Temperature	T_{STG}	-65~ +150	°C
Junction Temperature	T_J	+150	°C

ELECTRICAL CHARACTERISTICS (Tamb=25°C, unless otherwise specified)

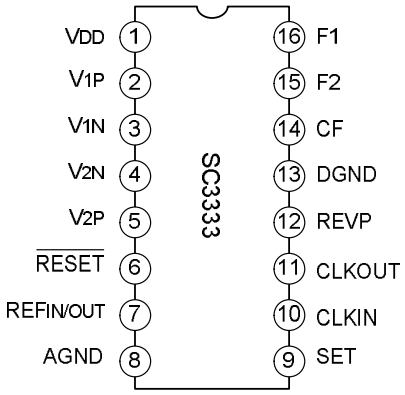
Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Power Supply							
Power Supply		V_{DD}	5V±5%	4.75	--	5.25	V
Analog Input Current		AI_{DD}	(2mA) TYP.	--	--	3	mA
Digital Input Current		DI_{DD}	(1.5mA) TYP.	--	--	2.5	
ACCURACY							
Measurement Error[1] on Channel 1	Gain=1	E_M	Over a dynamic range 500 to 1	--	0.1	--	%
	Gain=16		Over a dynamic range 500 to 1	--	0.1	--	%

(To be continued)

(Continued)

Characteristics		Symbol	Test conditions	Min.	Typ.	Max.	Unit
Phase Error[1] Between Channels	V1 Phase Lag 37°	E_P	--	--	--	±0.1	°
	V1 Phase Lag 60°			--	--	±0.1	°
Output Frequency Rejection (AC)		C_{FA}	V_1=100mV, V_2=100mV, SET=0	--	0.01	--	%
Output Frequency Rejection (DC)		C_{FD}	V_1=100mV, V_2=100mV, V_{DD}=5V±250mV	--	0.01	--	%
ANALOG INPUTS							
Maximum Signal Levels		LEVS	V_{1P}, V_{IN} V_{2N} and V_{2P} to AGND	--	--	±1	V
Input Impedance (DC)		I_{MIN}	C_{LKIN}=3.58MHz	400	--	--	kΩ
Bandwidth (-3dB)		BW	C_{LKIN}/256, C_{LKIN}=3.58MHz	--	14	--	kHz
ADC Offset Error[1,2]		EADC		--	--	15	mV
Gain Error[1]		E_G	V1=470mV, V2=660mV	--	±4	--	%
Gain Error Match[1]		E_{GM}	External 2.5V reference	--	±0.2	--	%
REFERENCE INPUT							
REFIN/OUT Input Voltage Range		V_{INR}	2.5V±8%	2.3	--	2.7	V
Input Impedance		I_{MIN}	--	3.7	--	--	kΩ
Input Capacitance		CIN	--	--	--	10	pF
ON-CHIP REFERENCE							
Reference Error		E_R	Nominal 2.5V	--	--	200	mV
Temperature Coefficient		T_C		--	30	60	ppm/°C
CLKIN							
Input Clock Frequency		C_{LKIN}	Note all specifications for CLKIN of 3.58MHz	1	--	4	MHz
LOGIC INPUTS[3]							
Input High Voltage		V_{INH}	V_{DD}=5V±5%	2.4	--	--	V
Input Low Voltage		V_{INL}	V_{DD}=5V±5%	--	--	0.8	V
Input Current		I_{IN}	Typically 10nA, V_{IN}=0V to V_{DD}	--	--	±3	μA
Input Capacitance		C_{IN}		--	--	10	pF
LOGIC OUTPUTS[3]							
F1 and F2	Output High Voltage	V_{OH}	I_{SOURCE}=10mA,V_{DD}=5V	4.5	--	--	V
	Output Low Voltage	V_{OL}	I_{SINK}=10mA, V_{DD}=5V	--	--	0.5	V
CF and REVP	Output High Voltage	V_{OH}	I_{SOURCE}=5mA,V_{DD}=5V	4	--	--	V
	Output Low Voltage	V_{OL}	I_{SINK}=5mA, V_{DD}=5V	--	--	0.5	V

PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Symbol	Description
1	V_{DD}	Power Supply.
2	V_{1P}	Positive and Negative Inputs for Channel 1 (Current Channel). Channel 1 has a PGA and the gain selections are outlined in Table I. The maximum signal level at these pins is ±1V with respect to AGND.
3	V_{1N}	
4	V_{2N}	Negative and Positive Inputs for Channel 2 (Voltage Channel). The maximum differential input voltage is ±660mV for specified operation. The maximum signal level at these pins is ±1V with respect to AGND.
5	V_{2P}	
6	$\overline{RESET}$	Reset Pin for the SC3333. A logic low is valid.
7	$REF_{IN/OUT}$	Reference voltage input/output pin.
8	AGND	Analog ground.
9	SET	Channel 1 gain select pin. See table 1.
10	CLK_{IN}	3.58MHZ crystal oscillator input pin.
11	CLK_{OUT}	3.58MHZ crystal oscillator output pin.
12	REVP	State indication pin. While negative power or a potential miswriting occurs, it will be set to logic high.
13	DGND	Digital ground.
14	CF	Calibration Frequency Logic Output..
15	F2	Low Frequency Logic Outputs. They can be used to directly drive a stepper motor or electromechanical impulse counter.
16	F1	

TIMIING CHARACTERISTICS[1,2]

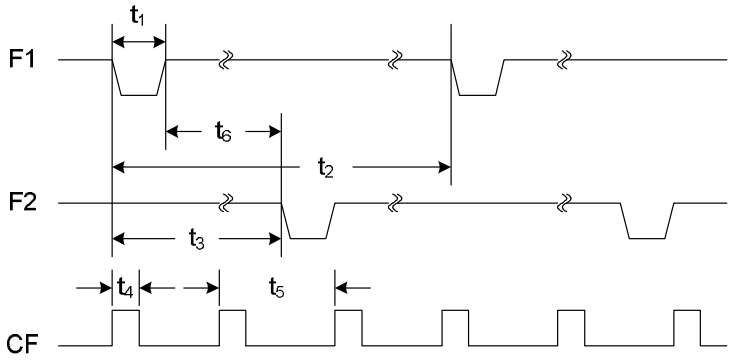
(V_{DD}=5V±5%, A_{GND}=D_{GND}=0V, On-chip Reference, C_{LKIN}=3.58MHZ, T_{MIN} to T_{MAX}=-40°C~+85°C.)

Parameter	Test Condition	Test Data	Units
t1[3]	F1 and F2 Pulse-width	275	ms
t2	F1 and F2 Pulse Period.	TBD	sec
t3	Time Between F1 Falling Edge and F2 Falling Edge	1/2 t2	sec
t4[3,4]	CF Pulse-width	90	ms
t5	CF Pulse Period.	TBD	sec
t6	Minimum Time Between F1 and F2 Pulse	CLKIN/4	sec

NOTE: 1. Sample tested during initial release and after any redesign or process change that may after this parameter.

2. See the following figure.

3. The pulse-widths of F1, F2 and CF are not fixed for higher output frequencies.



Timing Diagram for Frequency outputs

Timing Diagram for Frequency Outputs shows a timing diagram for the various frequency outputs of the SC3333. The low frequency outputs, F1 and F2 can drive electromechanical counters and two phase stepper motors directly. As the figure show, the F1 and F2 outputs provide two alternating low going pulses. The pulse width (t1) is set at 275ms and the time between the falling edges of F1 and F2 (t3) is approximately half the period of F1 (t2). If however the period of F1 and F2 falls below 550 ms (1.81Hz) the pulse width of F1 and F2 is set to half of their period. The frequency of F1 and F2 corresponds to the input voltages, and F=（13.6*V1*V2*G）/ $VREF^2$， The values of G can be set by consumers, and the selection of G please refer to the table I , V1 and V2 are the rms value of the two inputs, VREF is the voltage of reference, whose value is 2.5±0.2v when the internal bandgap reference of SC3333 is valid.

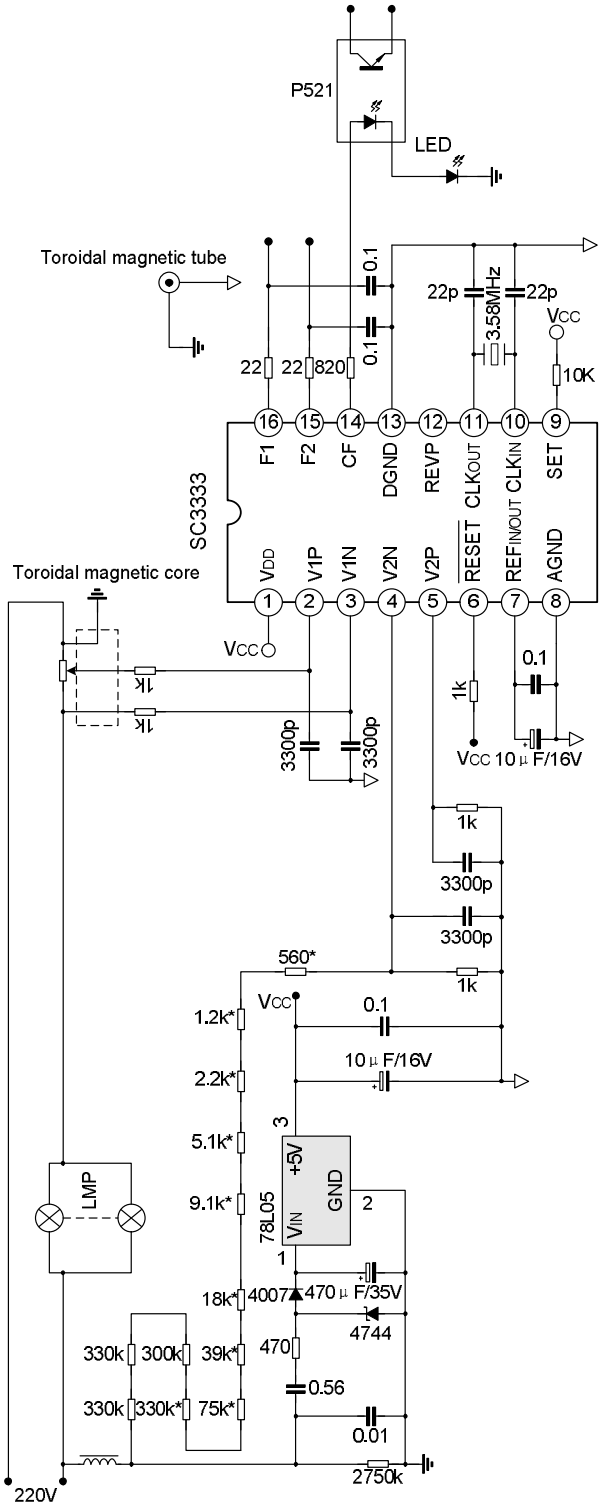
The high frequency output, CF is intended for calibration and supplies instantaneous real power. CF produces a 90ms wide active high pulse (t4) at a frequency proportional to active power. As in the case of F1 and F2, if the period of CF (t5) falls below 180ms, the CF pulse-width is set to half the period.

APPENDIX

Table I. gain selection for channel 1

SET	Gain	Maximum Differential Signal
0	1	±470mV
1	16	±30mV

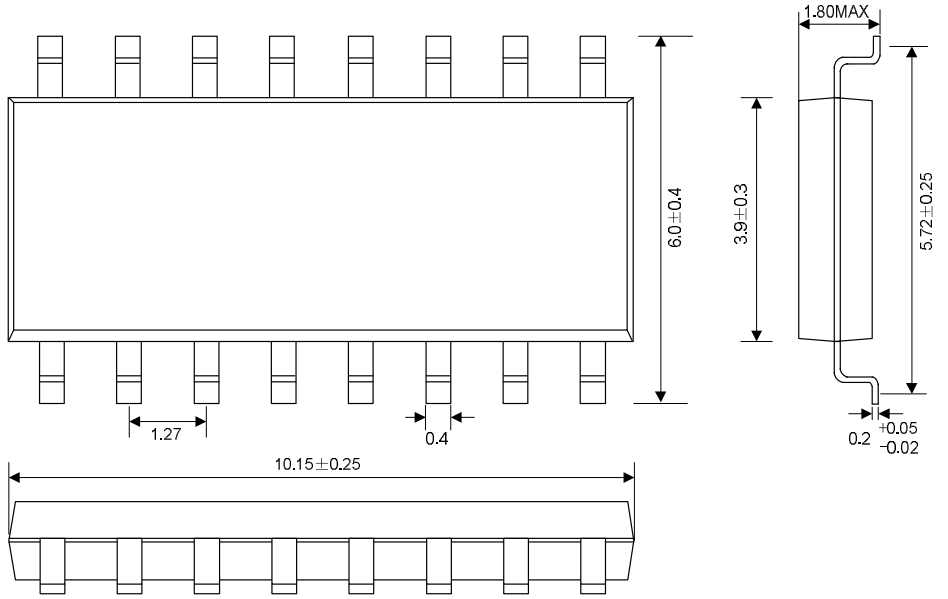
TYPICAL APPLICATION CIRCUIT



These resistors with * symbol used to adjust the precision of meters.

PACKAGE OUTLINE

SOP-16-225-1.27 UNIT: mm



HANDLING MOS DEVICES:

Electrostatic charges can exist in many things. All of our MOS devices are internally protected against electrostatic discharge but they can be damaged if the following precautions are not taken:

- Persons at a work bench should be earthed via a wrist strap.
- Equipment cases should be earthed.
- All tools used during assembly, including soldering tools and solder baths, must be earthed.
- MOS devices should be packed for dispatch in antistatic/conductive containers.

ATTACHMENT

Revision History

Data	REV	Description	Page
2006.12.22	1.0	Original	
2008.04.29	1.1	Modify the "TYPICAL APPLICATION CIRCUIT "	

Note: Silan reserves the right to make changes without notice in this specification for the improvement of the design and performance. Silan will supply the best possible product for customers.