New Product



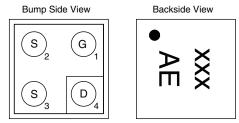
Si8809EDB

Vishay Siliconix

P-Channel 20 V (D-S) MOSFET

PRODUCT SUMMARY						
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)			
	0.090 at V_{GS} = - 4.5 V	- 2.6				
- 20	0.119 at V _{GS} = - 2.5 V	- 2.3	6 nC			
	0.155 at V _{GS} = - 1.8 V	- 2.0				

MICRO FOOT



Device Marking: xxx = Date/Lot Traceability Code AE

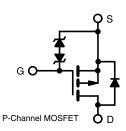
Ordering Information: Si8809EDB-T2-E1 (Lead (Pb)-free and Halogen-free)

FEATURES

- TrenchFET[®] Power MOSFET
- Ultra Small 0.8 mm x 0.8 mm Outline
- Ultra Thin 0.357 mm Height
- Typical ESD Protection 1000 V HBM
- **High Speed Switching**
- Material categorization: For definitions of compliance please see www.vishay.com/doc?99912

APPLICATIONS

- Portable Devices such as Cell Phones, Smart Phones, Tablet PCs and Media Players
 - Load Switch
 - Battery Switch



Parameter		Symbol	Limit	Unit	
Drain-Source Voltage		V _{DS}	- 20	V	
Gate-Source Voltage		V _{GS}	± 8		
	T _A = 25 °C		- 2.6 ^a		
Continuous Drain Current (T ₁ = 150 °C)	T _A = 70 °C		- 2.1 ^a		
Continuous Drain Current $(T_j = 150 \text{ C})$	T _A = 25 °C	I _D	- 1.9 ^b		
	T _A = 70 °C		- 1.5 ^b	А	
Pulsed Drain Current (t = 300 µs)		I _{DM}	- 13		
Continuous Source-Drain Diode Current	T _A = 25 °C		- 0.7 ^a		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	- 0.4 ^b		
	T _A = 25 °C		0.9 ^a		
Maximum Dawar Dissinction	T _A = 70 °C		0.6 ^a	w	
Maximum Power Dissipation	T _A = 25 °C	P _D	0.5 ^b	VV	
	T _A = 70 °C		0.3 ^b		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150	°C	
Soldering Recommendations (Peak Tempera		260	·U		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{a, d}	t≤5 s	D	105	135	°C/W	
Maximum Junction-to-Ambient ^{b, e}		R _{thJA}	200	260	0/10	

Notes:

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.

b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.

Refer to IPC/JEDEC (J-STD-020), no manual or hand soldering. C.

d. Maximum under steady state conditions is 185 °C/W.

e. Maximum under steady state conditions is 330 °C/W.

Document Number: 63301 S12-1620-Rev. B, 09-Jul-12

For technical questions, contact: pmostechsupport@vishav.com

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RoHS COMPLIANT HALOGEN FREE

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit
Static		· · · · · · · · · · · · · · · · · · ·		1	<u> </u>	I
Drain-Source Breakdown Voltage	V _{DS}	$V_{GS} = 0, I_D = -250 \ \mu A$	- 20			V
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L _ 250 uA		- 9		
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	- I _D = - 250 μΑ		2.1		mV/°C
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = -250 \ \mu A$	- 0.4		- 0.9	V
Cata Cauraa Laskana	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$			± 1	μA
Gate-Source Leakage		$V_{DS} = 0 V, V_{GS} = \pm 8 V$			± 10	
Zarra Casta Malta na Dunin Cuurant		$V_{DS} = -20 V, V_{GS} = 0 V$			- 1	
Zero Gate Voltage Drain Current	IDSS	V_{DS} = - 20 V, V_{GS} = 0 V, T_{J} = 55 °C			- 10	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \leq$ - 10 V, V_{GS} = - 4.5 V	- 5			Α
		$V_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -1.5 \text{ A}$		0.075	0.090	Ω
Drain-Source On-State Resistance ^a	R _{DS(on)}	$V_{GS} = -2.5 \text{ V}, \text{ I}_{D} = -1.5 \text{ A}$		0.097	0.119	
		V _{GS} = - 1.8 V, I _D = - 0.5 A		0.125	0.155	
Forward Transconductance ^a	9 _{fs}	V _{DS} = - 10 V, I _D = - 1.5 A		8		S
Dynamic ^b		· · · · · · · · · · · · · · · · · · ·		1	<u> </u>	
-	Q _g Q _{gs}	$V_{DS} = -10 \text{ V}, V_{GS} = -8 \text{ V}, I_{D} = -1.5 \text{ A}$		9.8	15	nC
Total Gate Charge		$V_{DS} = -10 \text{ V}, \text{ V}_{GS} = -4.5 \text{ V}, \text{ I}_{D} = -1.5 \text{ A}$		6	10	
Gate-Source Charge				0.8		
Gate-Drain Charge	Q _{gd}			1.85		1
Gate Resistance	Rg	f = 1 MHz		10		Ω
Turn-On Delay Time	t _{d(on)}			15	30	- ns
Rise Time	t _r	V_{DD} = - 10 V, R_{L} = 3.7 Ω		20	40	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1.5 A, V_{GEN} = - 4.5 V, R_g = 1 Ω		30	60	
Fall Time	t _f			10	20	
Turn-On Delay Time	t _{d(on)}			10	20	
Rise Time	t _r	V_{DD} = - 10 V, R_{L} = 3.7 Ω		10	20	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ - 1.5 A, V_{GEN} = - 8 V, R_g = 1 Ω		25	50	
Fall Time t _f				7	15	
Drain-Source Body Diode Characteristic	s	· · · · · · · · · · · · · · · · · · ·				
Continuous Source-Drain Diode Current	ntinuous Source-Drain Diode Current I_S $T_C = 25 \degree C$				- 0.7	^
Pulse Diode Forward Current	I _{SM}				- 13	A
Body Diode Voltage	V _{SD}	$I_{\rm S}$ = - 1.5 A, $V_{\rm GS}$ = 0		- 0.8	- 1.2	V
Body Diode Reverse Recovery Time	t _{rr}			20	40	ns
Body Diode Reverse Recovery Charge	Reverse Recovery Charge Q_{rr} $I_F = -1.5 M$			10	20	nC
Reverse Recovery Fall Time t _a		dl/dt = 100 A/µs, T _J = 25 °C		15		
Reverse Recovery Rise Time	t _b	1 1		5		ns

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %

b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

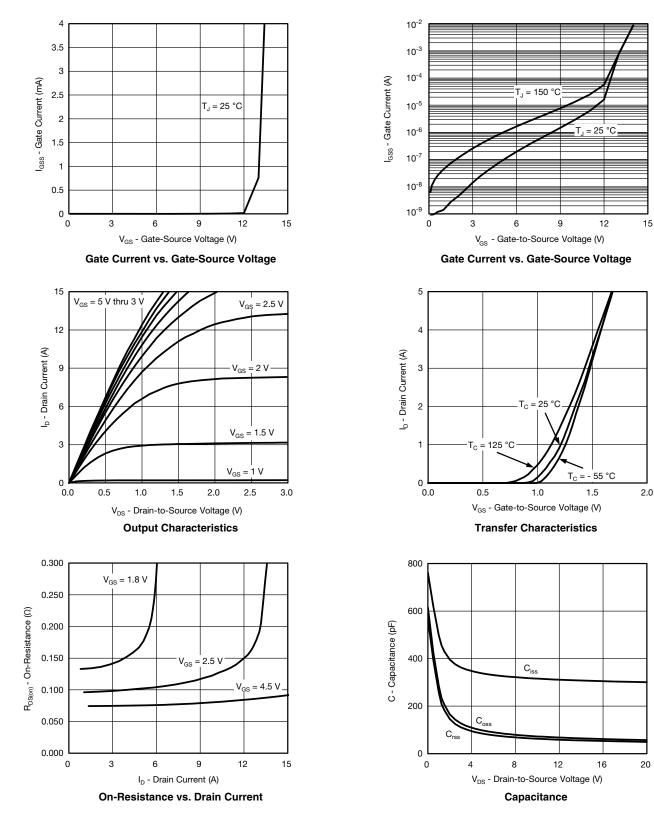
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



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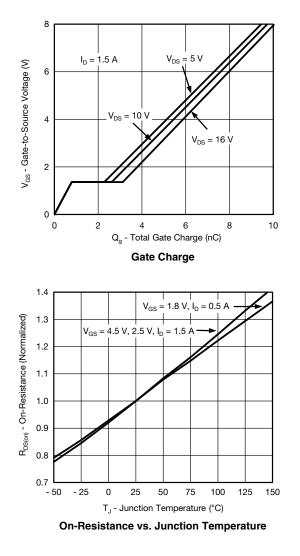
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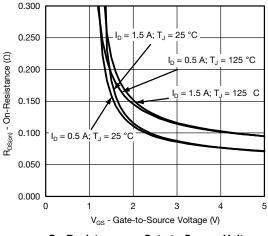
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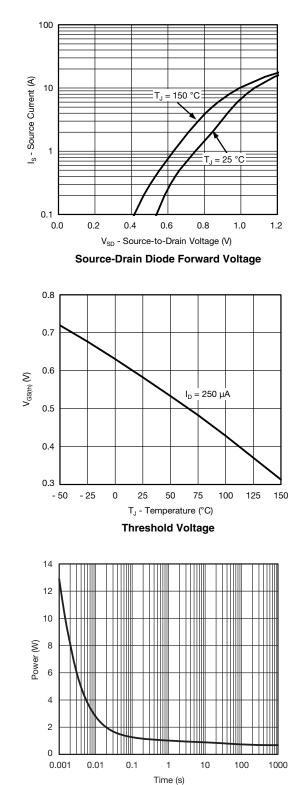


TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)





On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power (Junction-to-Ambient)

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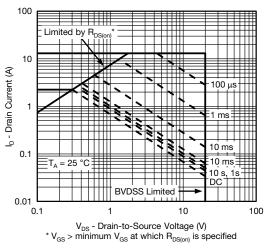
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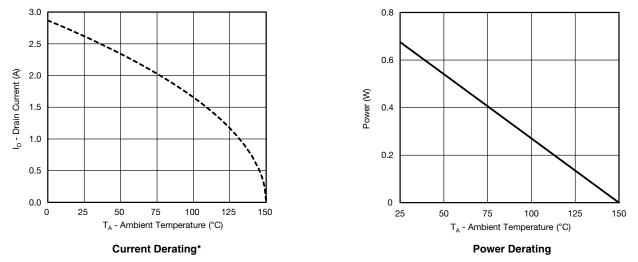


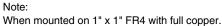
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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



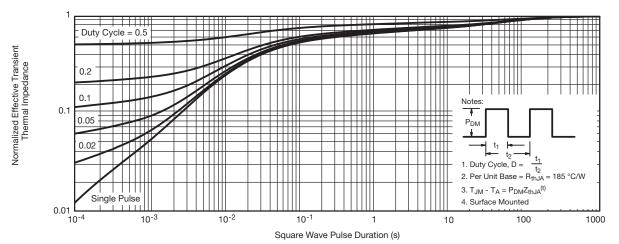


* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-ambient thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

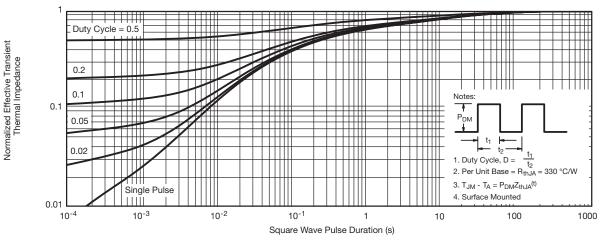


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TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with maximum copper)



Normalized Thermal Transient Impedance, Junction-to-Ambient (on 1" x 1" FR4 board with minimum copper)

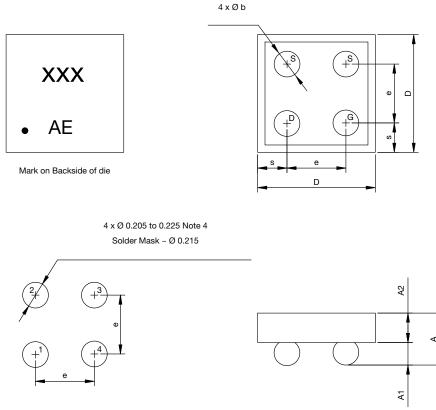
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PACKAGE OUTLINE

MICRO FOOT 0.8 mm x 0.8 mm: 4-BUMP (2 x 2, 0.4 mm PITCH)



Recommended Land

Notes (unless otherwise specified):

1. All dimensions are in millimeters.

2. Four (4) solder bumps are lead (Pb)-free 95.5Sn/3.5Ag/0.7Cu with diameter Ø 0.165 mm to Ø 0.185 mm.

3. Backside surface is coated with a Ti/Ni/Ag layer.

4. Non-solder mask defined copper landing pad.

5. • is location of pin 1.

Dim.	Millimeters ^a			Inches			
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Α	0.314	0.357	0.400	0.0124	0.0141	0.0157	
A ₁	0.127	0.157	0.187	0.0050	0.0062	0.0074	
A ₂	0.187	0.200	0.213	0.0074	0.0079	0.0084	
b	0.165	0.175	0.185	0.0064	0.0068	0.0072	
е		0.400			0.0157		
S	0.180	0.200	0.220	0.0070	0.0078	0.0086	
D	0.760	0.800	0.840	0.0299	0.0314	0.0330	

Notes:

a. Use millimeters as the primary measurement.

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