# Si52146

# PCI-EXPRESS GEN 1, GEN 2, & GEN 3 SIX OUTPUT CLOCK GENERATOR

## Features

- PCI-Express Gen 1, Gen 2, & Gen 3 compliant
- Low power push-pull type differential output buffers
- Integrated resistors on differential clocks
- Dedicated output enable pin for each clock
- Hardware selectable spread control
- Six PCI-Express clocks
- 25 MHz crystal input or clock input
- $I^2C$ support with readback capabilities
- Triangular spread spectrum profile for maximum electromagnetic interference (EMI) reduction
- Industrial temperature: –40 to 85 °C
- 3.3 V Power supply
- 32-pin QFN package


**Ordering Information:**
See page 18

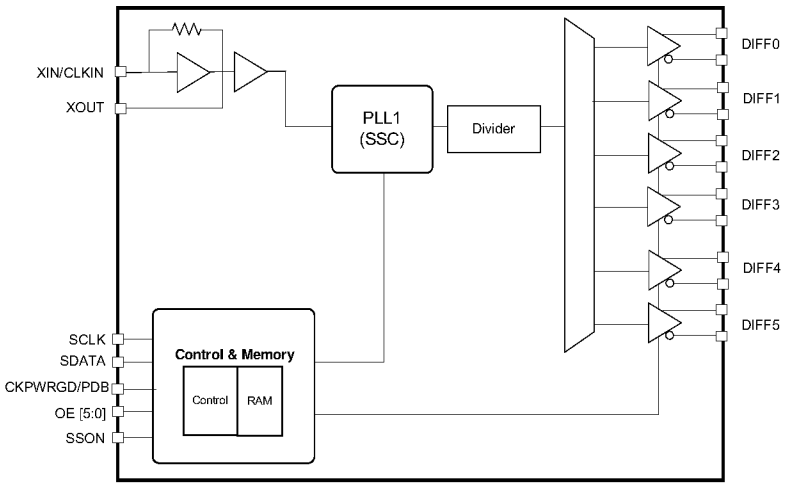
## Applications

- Network attached storage
- Multi-function printer
- Wireless access point
- Routers

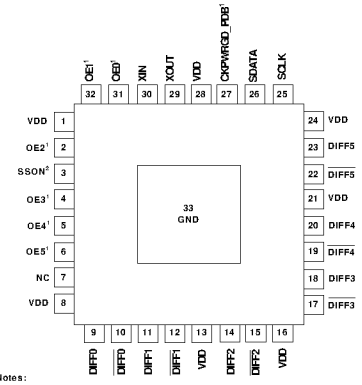
## Description

The Si52146 is a spread-controlled PCIe clock generator that can source six PCIe clocks simultaneously. The device has six hardware inputs for enabling the respective outputs on the fly while powered on along with the spread control hardware pin to enable Spread for EMI reduction.

## Functional Block Diagram




## Pin Assignments




Patents pending

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# 1. Electrical Specifications

### Table 1. DC Electrical Specifications

| Parameter | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| 3.3 V Operating Voltage | VDD core | 3.3 ±5% | 3.135 | 3.3 | 3.465 | V |
| 3.3 V Input High Voltage | $V_{IH}$ | Control input pins | 2.0 | — | $V_{DD}$ + 0.3 | V |
| 3.3 V Input Low Voltage | $V_{IL}$ | Control input pins | $V_{SS}$ – 0.3 | — | 0.8 | V |
| Input High Voltage | $V_{IHI2C}$ | SDATA, SCLK | 2.2 | — | — | V |
| Input Low Voltage | $V_{ILI2C}$ | SDATA, SCLK | — | — | 1.0 | V |
| Input High Leakage Current | $I_{IH}$ | Except internal pull-down resistors, $0 < V_{IN} < V_{DD}$ | — | — | 5 | µA |
| Input Low Leakage Current | $I_{IL}$ | Except internal pull-up resistors, $0 < V_{IN} < V_{DD}$ | –5 | — | — | µA |
| 3.3 V Output High Voltage (SE) | $V_{OH}$ | $I_{OH}$ = –1 mA | 2.4 | — | — | V |
| 3.3 V Output Low Voltage (SE) | $V_{OL}$ | $I_{OL}$ = 1 mA | — | — | 0.4 | V |
| High-impedance Output Current | $I_{OZ}$ | | –10 | — | 10 | µA |
| Input Pin Capacitance | $C_{IN}$ | | 1.5 | — | 5 | pF |
| Output Pin Capacitance | $C_{OUT}$ | | — | — | 6 | pF |
| Pin Inductance | $L_{IN}$ | | — | — | 7 | nH |
| Power Down Current | $I_{DD\_PD}$ | | — | — | 1 | mA |
| Dynamic Supply Current | $I_{DD\_3.3V}$ | All outputs enabled. Differential clocks with 5” traces and 2 pF load. | — | — | 60 | mA |

## Table 2. AC Electrical Specifications

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Crystal** | | | | | | |
| Long-term Accuracy | $L_{ACC}$ | Measured at $V_{DD}/2$ differential | — | — | 250 | ppm |
| **Clock Input** | | | | | | |
| CLKIN Duty Cycle | $T_{DC}$ | Measured at $V_{DD}/2$ | 47 | — | 53 | % |
| CLKIN Rise and Fall Times | $T_R/T_F$ | Measured between 0.2 $V_{DD}$ and 0.8 $V_{DD}$ | 0.5 | — | 4.0 | V/ns |
| CLKIN Cycle to Cycle Jitter | $T_{CCJ}$ | Measured at VDD/2 | — | — | 250 | ps |
| CLKIN Long Term Jitter | $T_{LTJ}$ | Measured at VDD/2 | — | — | 350 | ps |
| Input High Voltage | $V_{IH}$ | XIN/CLKIN pin | 2 | — | VDD+0.3 | V |
| Input Low Voltage | $V_{IL}$ | XIN/CLKIN pin | — | — | 0.8 | V |
| Input High Current | $I_{IH}$ | XIN/CLKIN pin, VIN = VDD | — | — | 35 | uA |
| Input Low Current | $I_{IL}$ | XIN/CLKIN pin, 0 < VIN <0.8 | –35 | — | — | uA |
| **DIFF at 0.7 V** | | | | | | |
| DIFF Duty Cycle | $T_{DC}$ | Measured at 0 V differential | 45 | — | 55 | % |
| Any DIFF Clock Skew from the Earliest Bank to the Latest Bank | $T_{SKEW(window)}$ | Measured at 0 V differential | — | — | 50 | ps |
| DIFF Cycle to Cycle Jitter | $T_{CCJ}$ | Measured at 0 V differential | — | 35 | 50 | ps |
| Output PCIe Gen1 REFCLK Phase Jitter | $RMS_{GEN1}$ | Includes PLL BW 1.5–22 MHz, ζ = 0.54, Td=10 ns, Ftrk=1.5 MHz with BER = 1E-12 | 0 | 40 | 108 | ps |
| Output PCIe Gen2 REFCLK Phase Jitter | $RMS_{GEN2}$ | Includes PLL BW 8–16 MHz, Jitter Peaking = 3 dB, ζ = 0.54, Td=12 ns), Low Band, F < 1.5 MHz | 0 | 2 | 3.0 | ps |
| Output PCIe Gen2 REFCLK Phase Jitter | $RMS_{GEN2}$ | Includes PLL BW 8–16 MHz, Jitter Peaking = 3 dB, ζ = 0.54, Td=12 ns), High Band, 1.5 MHz < F < Nyquist | 0 | 2 | 3.1 | ps |
| Output Phase Jitter Impact—PCIe Gen3 | $RMS_{GEN3}$ | Includes PLL BW 2–4 MHz, CDR = 10 MHz) | 0 | 0.5 | 1.0 | ps |
| DIFF Long Term Accuracy | $L_{ACC}$ | Measured at 0 V differential | — | — | 100 | ppm |
| DIFF Rising/Falling Slew Rate | $T_R/T_F$ | Measured differentially from ±150 mV | 1 | — | 8 | V/ns |
| Voltage High | $V_{HIGH}$ | | — | — | 1.15 | V |
| Voltage Low | $V_{LOW}$ | | –0.3 | — | — | V |
| Crossing Point Voltage at 0.7 V Swing | $V_{OX}$ | | 300 | — | 550 | mV |
| **Enable/Disable and Setup** | | | | | | |
| Clock Stabilization from Power-up | $T_{STABLE}$ | | — | — | 1.8 | ms |
| Stopclock Set-up Time | $T_{SS}$ | | 10.0 | — | — | ns |

### Table 3. Absolute Maximum Conditions

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Main Supply Voltage | $V_{DD\_3.3V}$ | Functional | — | — | 4.6 | V |
| Input Voltage | $V_{IN}$ | Relative to $V_{SS}$ | –0.5 | — | 4.6 | $V_{DC}$ |
| Temperature, Storage | $T_S$ | Non-functional | –65 | — | 150 | °C |
| Temperature, Operating Ambient | $T_A$ | Functional | –40 | — | 85 | °C |
| Temperature, Junction | $T_J$ | Functional | — | — | 150 | °C |
| Dissipation, Junction to Case | $Ø_{JC}$ | JEDEC (JESD 51) | — | — | 17 | °C/W |
| Dissipation, Junction to Ambient | $Ø_{JA}$ | JEDEC (JESD 51) | — | — | 35 | °C/W |
| ESD Protection (Human Body Model) | $ESD_{HBM}$ | JEDEC (JESD 22-A114) | 2000 | — | — | V |
| Flammability Rating | UL-94 | UL (Class) | | V–0 | | |
| Moisture Sensitivity Level | MSL | JEDEC (J-STD-020) | | 2 | | |

**Note:** While using multiple power supplies, the voltage on any input or I/O pin cannot exceed the power pin during power-up. Power supply sequencing is not required.

# 2. Functional Description

## 2.1. Crystal Recommendations

The clock device requires a parallel resonance crystal. Substituting a series resonance crystal causes the clock device to operate at the wrong frequency and violates the ppm specification. For most applications there is a 300 ppm frequency shift between series and parallel crystals due to incorrect loading.

**Table 4. Crystal Recommendations**

| Frequency (Fund) | Cut | Loading | Load Cap | Shunt Cap (max) | Motional (max) | Tolerance (max) | Stability (max) | Aging (max) |
|---|---|---|---|---|---|---|---|---|
| 25 MHz | AT | Parallel | 12–15 pF | 5 pF | 0.016 pF | 35 ppm | 30 ppm | 5 ppm |

### 2.1.1. Crystal Loading

Crystal loading plays a critical role in achieving low ppm performance. To realize low ppm performance, use the total capacitance the crystal sees to calculate the appropriate capacitive loading (CL).

Figure 1 shows a typical crystal configuration using the two trim capacitors. It is important that the trim capacitors are in series with the crystal. It is not true that load capacitors are in parallel with the crystal and are approximately equal to the load capacitance of the crystal.

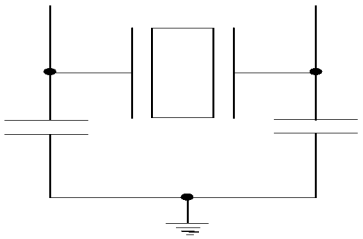


**Figure 1. Crystal Capacitive Clarification**

### 2.1.2. Calculating Load Capacitors

In addition to the standard external trim capacitors, consider the trace capacitance and pin capacitance to calculate the crystal loading correctly. Again, the capacitance on each side is in series with the crystal. The total capacitance on both side is twice the specified crystal load capacitance (CL). Trim capacitors are calculated to provide equal capacitive loading on both sides.

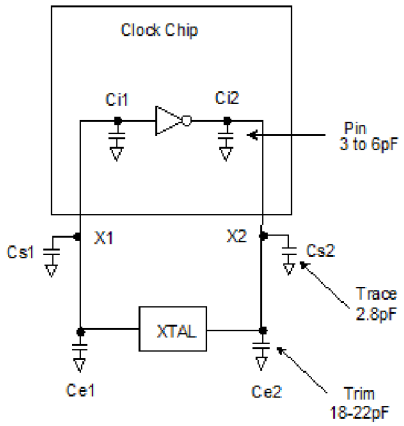



**Figure 2. Crystal Loading Example**

Use the following formulas to calculate the trim capacitor values for Ce1 and Ce2.

**Load Capacitance (each side)**

$$Ce = 2 \times CL - (Cs + Ci)$$

**Total Capacitance (as seen by the crystal)**

$$CLe = \frac{1}{\left(\frac{1}{Ce1 + Cs1 + Ci1} + \frac{1}{Ce2 + Cs2 + Ci2}\right)}$$

- CL: Crystal load capacitance
- CLe: Actual loading seen by crystal using standard value trim capacitors
- Ce: External trim capacitors
- Cs: Stray capacitance (terraced)
- Ci : Internal capacitance (lead frame, bond wires, etc.)

## 2.2. CKPWRGD_PDB (Power down) Clarification

The CKPWRGD_PDB pin is a dual-function pin. During initial power up, the pin functions as CKPWRGD. Upon the first powerup if the CKPWRGD is low, the device outputs will be disabled, but the crystal oscillator and $I^2C$ logics are active. Once CKPWRGD has been sampled high by the clock chip, the pin assumes a PDB functionality. When the pin has assumed a PDB functionality and the pin is pull low, the device will be placed in standby mode.

## 2.3. PDB (Power down) Assertion

The PDB pin is an asynchronous active low input used to disable all clocks in a glitch free manner. All outputs will be driven low in power down mode. In power down mode, all outputs, the crystal oscillator and the $I^2C$ logic are disabled.

## 2.4. PDB Deassertion

When a valid rising edge on CKPWRGD/PDB pin is applied, all outputs are enabled in a glitch free manner within two to six output clock cycle.

## 2.5. OE Clarification

The OE pins are active high inputs used to enable and disable the output clocks. To enable the output clock, the OE pin needs to be logic high and the $I^2C$ output enable bit needs to be logic high. There are two methods to disable the output clocks: the OE is pulled to a logic low, or the $I^2C$ enable bit is set to a logic low. The OE pins is required to be driven at all time and even though it has an internally 100 kΩ resistor.

## 2.6. OE Assertion

The OE signals are active high input used for synchronous stopping and starting the DIFF output clocks respectively while the rest of the clock generator continues to function. The assertion of the OE signal by making it logic high causes stopped respective DIFF output to resume normal operation. No short or stretched clock pulses are produced when the clock resumes. The maximum latency from the assertion to active outputs is no more than two to six output clock cycles.

## 2.7. OE Deassertion

When the OE pin is deasserted by making its logic low, the corresponding DIFF output is stopped cleanly, and the final output state is driven low.

## 2.8. SSON Clarification

SSON is an active input used to enable –0.5% spread on all DIFF outputs. When sampled high, –0.5% spread is enabled on all DIFF outputs. When sampled low, the DIFF output frequencies are non-spread.

## 3. Test and Measurement Setup

This diagram shows the test load configuration for the differential clock signals.

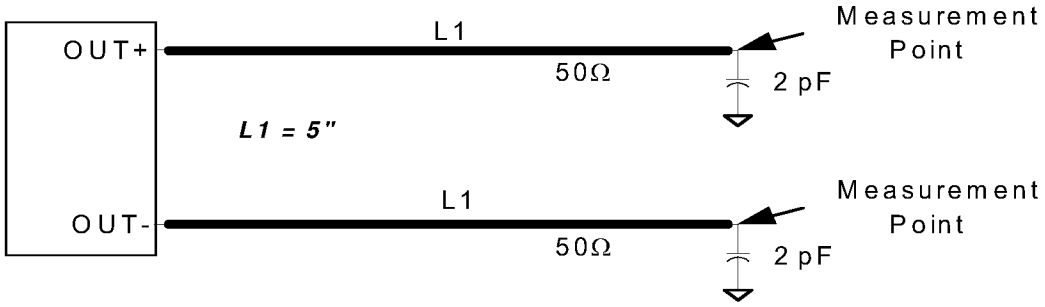



**Figure 3. 0.7 V Differential Load Configuration**

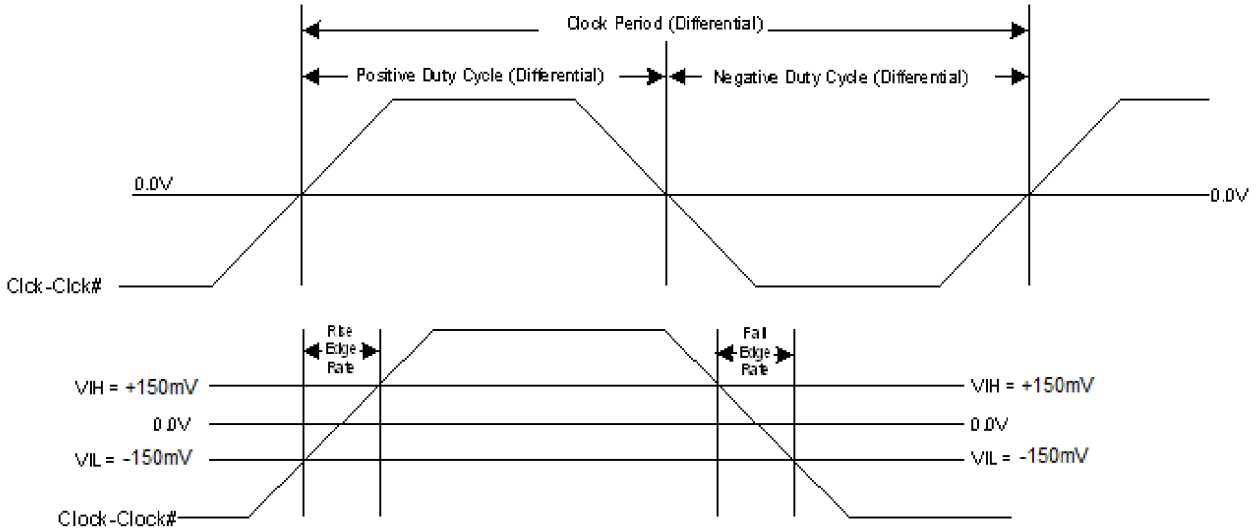



**Figure 4. Differential Output Signals (for AC Parameters Measurement)**

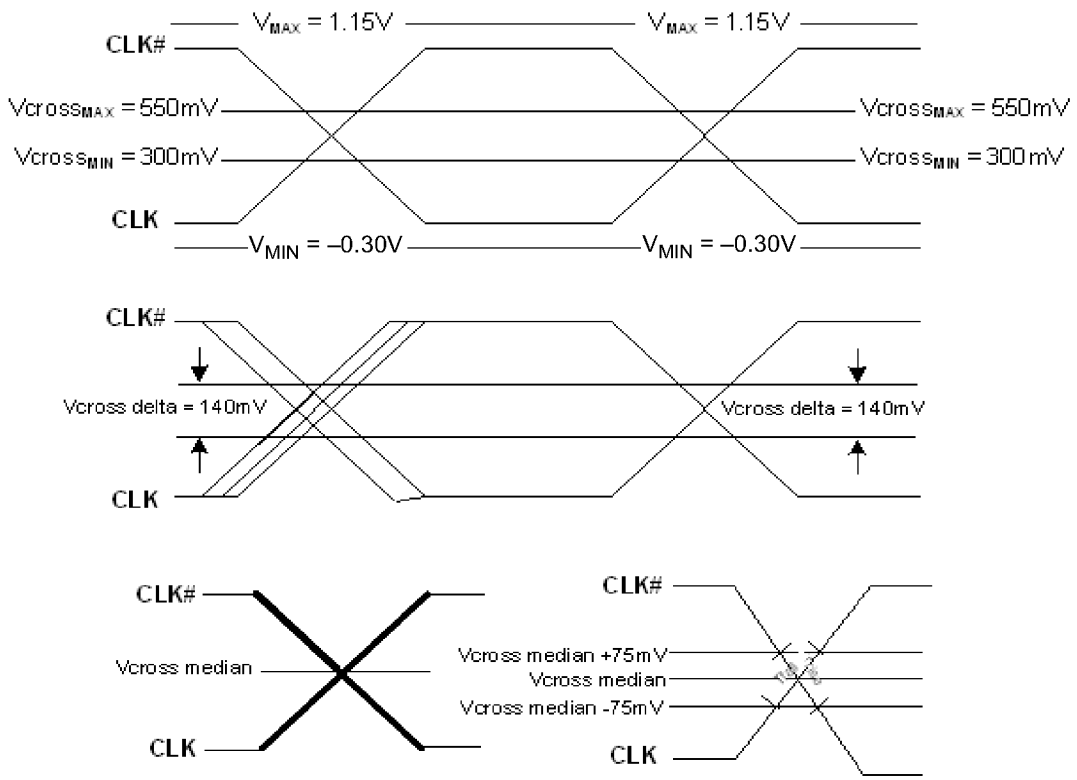



**Figure 5. Single-ended Measurement for Differential Output Signals (for AC Parameters Measurement)**

# 4. Control Registers

## 4.1. Serial Data Interface

To enhance the flexibility and function of the clock synthesizer, a two-signal serial interface is provided. Through the Serial Data Interface, various device functions, such as individual clock output buffers are individually enabled or disabled. The registers associated with the Serial Data Interface initialize to their default setting at power-up. The use of this interface is optional. Clock device register changes are normally made at system initialization, if any are required. The interface cannot be used during system operation for power management functions.

## 4.2. Data Protocol

The clock driver serial protocol accepts byte write, byte read, block write, and block read operations from the controller. For block write/read operation, access the bytes in sequential order from lowest to highest (most significant bit first) with the ability to stop after any complete byte is transferred. For byte write and byte read operations, the system controller can access individually indexed bytes. The offset of the indexed byte is encoded in the command code described in Table 1 on page 4.

The block write and block read protocol is outlined in Table 5 while Table 6 outlines byte write and byte read protocol. The slave receiver address is 11010110 (D6h).

**Table 5. Block Read and Block Write Protocol**

| Block Write Protocol | | Block Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address—7 bits | 8:2 | Slave address—7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code—8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Byte Count—8 bits | 20 | Repeat start |
| 28 | Acknowledge from slave | 27:21 | Slave address—7 bits |
| 36:29 | Data byte 1–8 bits | 28 | Read = 1 |
| 37 | Acknowledge from slave | 29 | Acknowledge from slave |
| 45:38 | Data byte 2–8 bits | 37:30 | Byte Count from slave—8 bits |
| 46 | Acknowledge from slave | 38 | Acknowledge |
| .... | Data Byte/Slave Acknowledges | 46:39 | Data byte 1 from slave—8 bits |
| .... | Data Byte N–8 bits | 47 | Acknowledge |
| .... | Acknowledge from slave | 55:48 | Data byte 2 from slave—8 bits |
| .... | Stop | 56 | Acknowledge |
| | | .... | Data bytes from slave/Acknowledge |
| | | .... | Data Byte N from slave—8 bits |
| | | .... | NOT Acknowledge |
| | | .... | Stop |

**Table 6. Byte Read and Byte Write Protocol**

| Byte Write Protocol | | Byte Read Protocol | |
|---|---|---|---|
| **Bit** | **Description** | **Bit** | **Description** |
| 1 | Start | 1 | Start |
| 8:2 | Slave address–7 bits | 8:2 | Slave address–7 bits |
| 9 | Write | 9 | Write |
| 10 | Acknowledge from slave | 10 | Acknowledge from slave |
| 18:11 | Command Code–8 bits | 18:11 | Command Code–8 bits |
| 19 | Acknowledge from slave | 19 | Acknowledge from slave |
| 27:20 | Data byte–8 bits | 20 | Repeated start |
| 28 | Acknowledge from slave | 27:21 | Slave address–7 bits |
| 29 | Stop | 28 | Read |
| | | 29 | Acknowledge from slave |
| | | 37:30 | Data from slave–8 bits |
| | | 38 | NOT Acknowledge |
| | | 39 | Stop |

## Control Register 0. Byte 0

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00000000

| Bit | Name | Function |
|---|---|---|
| 7:0 | Reserved | |

## Control Register 1. Byte 1

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | | | | DIFF0_OE | | DIFF1_OE | | DIFF2_OE |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00010101

| Bit | Name | Function |
|---|---|---|
| 7:5 | Reserved | |
| 4 | DIFF0_OE | **Output Enable for DIFF0.**<br>0: Output disabled.<br>1: Output Enabled. |
| 3 | Reserved | |
| 2 | DIFF1_OE | **Output Enable for DIFF1.**<br>0: Output disabled.<br>1: Output enabled. |
| 1 | Reserved | |
| 0 | DIFF2_OE | **Output Enable for DIFF2.**<br>0: Output disabled.<br>1: Output enabled. |

## Control Register 2. Byte 2

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIFF3_OE | DIFF4_OE | DIFF5_OE | | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 11100000

| Bit | Name | Function |
|---|---|---|
| 7 | DIFF3_OE | **Output Enable for DIFF3.**<br>0: Output disabled.<br>1: Output enabled. |
| 6 | DIFF4_OE | **Output Enable for DIFF4.**<br>0: Output disabled.<br>1: Output enabled. |
| 5 | DIFF5_OE | **Output Enable for DIFF5.**<br>0: Output disabled.<br>1: Output enabled. |
| 4:0 | Reserved | |

## Control Register 3. Byte 3

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | Rev Code[3:0] | | | | Vendor ID[3:0] | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00001000

| Bit | Name | Function |
|---|---|---|
| 7:4 | Rev Code[3:0] | **Program Revision Code.** |
| 3:0 | Vendor ID[3:0] | **Vendor Identification Code.** |

## Control Register 4. Byte 4

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | BC[7:0] | | | | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 00000110

| Bit | Name | Function |
|---|---|---|
| 7:0 | BC[7:0] | **Byte Count Register.** |

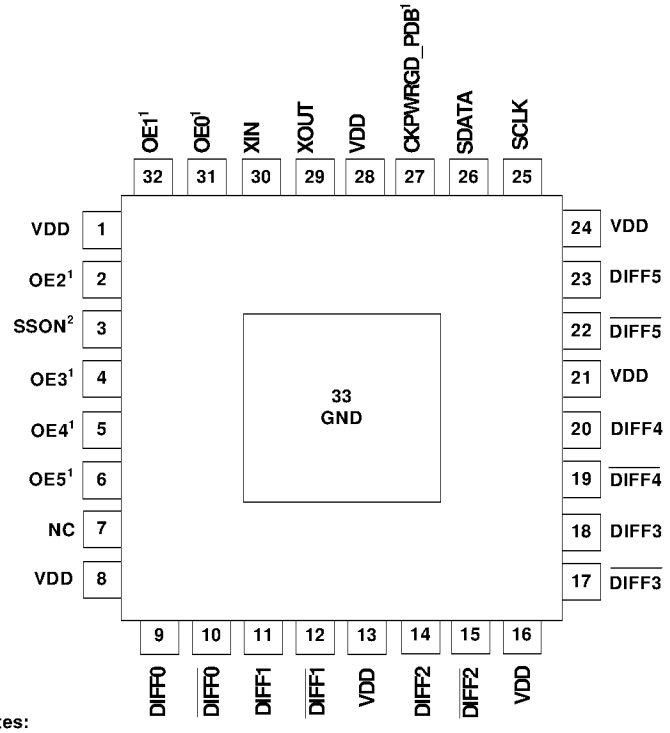
## Control Register 5. Byte 5

| Bit | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|
| Name | DIFF_Amp_Sel | DIFF_Amp_Cntl[2] | DIFF_Amp_Cntl[1] | DIFF_Amp_Cntl[0] | | | | |
| Type | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |

Reset settings = 11011000

| Bit | Name | Function |
|---|---|---|
| 7 | DIFF_Amp_Sel | **Amplitude Control for DIFF Differential Outputs.**<br>0: Differential outputs with Default amplitude.<br>1: Differential outputs amplitude is set by Byte 5[6:4]. |
| 6 | DIFF_Amp_Cntl[2] | **DIFF Differential Outputs Amplitude Adjustment.**<br>000: 300 mV 001: 400 mV 010: 500 mV 011: 600 mV<br>100: 700 mV 101: 800 mV 110: 900 mV 111: 1000 mV |
| 5 | DIFF_Amp_Cntl[1] | |
| 4 | DIFF_Amp_Cntl[0] | |
| 3:0 | Reserved | |

## 5. Pin Descriptions: 32-Pin QFN




**Notes:**
1. Internal 100 kohm pull-up.
2. Internal 100 kohm pull-down.

**Table 7. Si52146 32-Pin QFN Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 1 | VDD | PWR | 3.3 V power supply |
| 2 | OE2 | I,PU | 3.3 V input to disable DIFF2 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 3 | SSON | I, PD | 3.3 V-tolerant input for enabling –0.5% spread on DIFF clocks (internal 100 kΩ pull-down) |
| 4 | OE3 | I,PU | 3.3 V input to disable DIFF3 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 5 | OE4 | I,PU | 3.3 V input to disable DIFF4 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 6 | OE5 | I,PU | 3.3 V input to disable DIFF5 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 7 | NC | NC | No connect |
| 8 | VDD | PWR | 3.3 V power supply |
| 9 | DIFF0 | O, DIF | 0.7 V, 100 MHz differential clock |
| 10 | $\overline{\text{DIFF0}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 11 | DIFF1 | O, DIF | 0.7 V, 100 MHz differential clock |

**Table 7. Si52146 32-Pin QFN Descriptions**

| Pin # | Name | Type | Description |
|---|---|---|---|
| 12 | $\overline{\text{DIFF1}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 13 | VDD | PWR | 3.3 V power supply |
| 14 | DIFF2 | O, DIF | 0.7 V, 100 MHz differential clock |
| 15 | $\overline{\text{DIFF2}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 16 | VDD | PWR | 3.3 V power supply |
| 17 | $\overline{\text{DIFF3}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 18 | DIFF3 | O, DIF | 0.7 V, 100 MHz differential clock |
| 19 | $\overline{\text{DIFF4}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 20 | DIFF4 | O, DIF | 0.7 V, 100 MHz differential clock |
| 21 | VDD | PWR | 3.3 V power supply |
| 22 | $\overline{\text{DIFF5}}$ | O, DIF | 0.7 V, 100 MHz differential clock |
| 23 | DIFF5 | O, DIF | 0.7 V, 100 MHz differential clock |
| 24 | VDD | PWR | 3.3 V power supply |
| 25 | SCLK | I | SMBus compatible SCLOCK |
| 26 | SDATA | I/O | SMBus compatible SDATA |
| 27 | CKPWRGD_PDB | I, PU | 3.3 V CMOS input. A real-time active low input for asserting power down (PDB) and disabling all outputs (internal 100 kΩ pull-up). |
| 28 | VDD | PWR | 3.3 V power supply |
| 29 | XOUT | O | 25.00 MHz crystal output, Float XOUT if using only CLKIN (clock input) |
| 30 | XIN/CLKIN | I | 25.00 MHz crystal input or 3.3 V, 25 MHz clock input |
| 31 | OE0 | I,PU | 3.3 V input to disable DIFF0 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 32 | OE1 | I,PU | 3.3 V input to disable DIFF1 (internal 100 kΩ pull-up). Refer to Table 1 on page 4 for OE specifications. |
| 33 | GND | GND | Ground for bottom pad of the IC. |

## 6. Ordering Guide

| Part Number | Package Type | Temperature |
|---|---|---|
| **Lead-free** | | |
| Si52146-A01AGM | 32-pin QFN | Industrial, –40 to 85 °C |
| Si52146-A01AGMR | 32-pin QFN—Tape and Reel | Industrial, –40 to 85 °C |

## 7. Package Outline

Figure 6 illustrates the package details for the Si52146. Table 8 lists the values for the dimensions shown in the illustration.

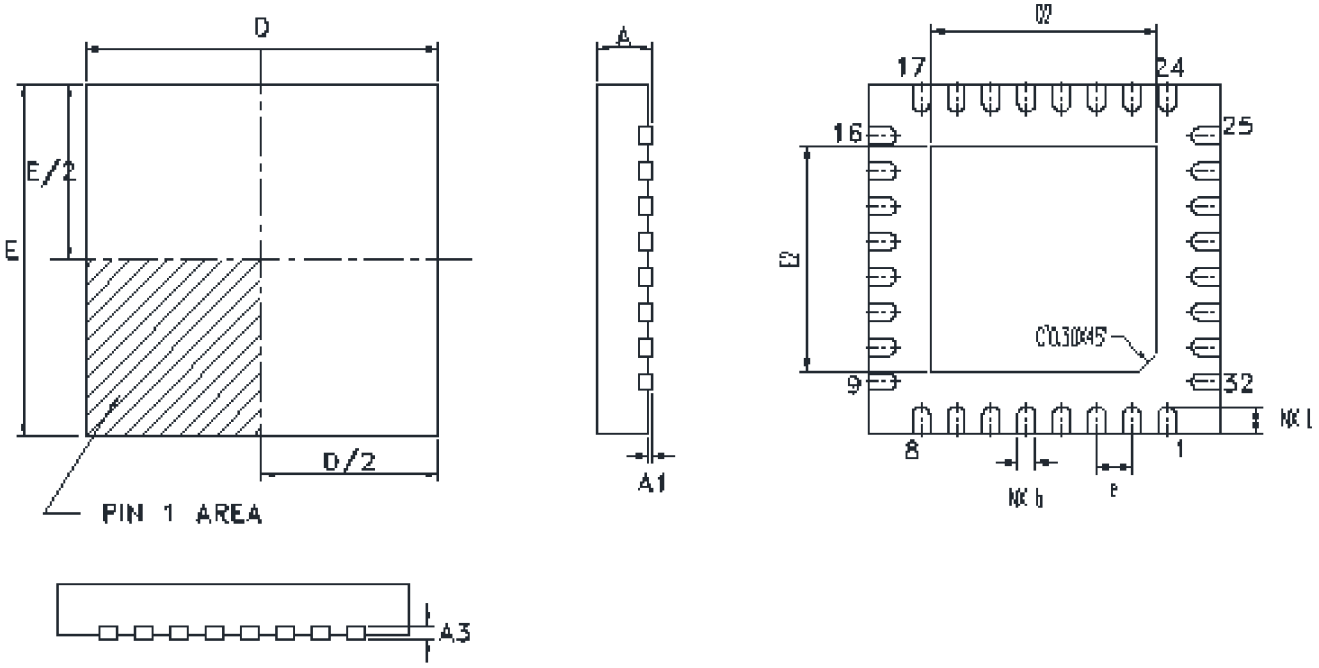



**Figure 6. 32-Pin Quad Flat No Lead (QFN) Package**

**Table 8. Package Diagram Dimensions**

| Symbol | Millimeters | | |
|---|---|---|---|
| | Min | Nom | Max |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.175 | 0.20 | 0.225 |
| b | 0.20 | 0.25 | 0.30 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.15 | 3.20 | 3.25 |
| e | 0.50 BSC | | |
| E | 4.90 | 5.00 | 5.10 |
| E2 | 3.15 | 3.20 | 3.25 |
| L | 0.30 | 0.40 | 0.50 |

**Notes:**

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.
4. Coplanarity less than 0.08 mm.
5. Terminal #1 identifier and terminal numbering convention conform to JESD 95-1 SPP-012.

## CONTACT INFORMATION

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