

# SANYO Semiconductors **DATA SHEET**

## LC875J64C LC875J56C LC875J48C

CMOS IC
ROM 64K/56K/48K byte, RAM 2048 byte on-chip
8-bit 1-chip Microcontroller

#### Overview

The SANYO LC875J64C/56C/48C are 8-bit microcomputer that, centered around a CPU running at a minimum bus cycle time of 83.3ns, integrates on a single chip a number of hardware features such as 64K/56K/48K byte ROM, 2048 byte RAM, sophisticated 16-bit timers/counters (may be divided into 8-bit timers), a 16-bit timer/counter (may be divided into 8-bit timers/counters or 8-bit PWMs), four 8-bit timers with a prescaler, a 16-bit timer with a prescaler (may be divided into 8-bit timers), a base timer serving as a time-of-day clock, a high-speed clock counter, a synchronous SIO interface (with automatic block transmission/reception capabilities), an asynchronous/synchronous SIO interface, a UART interface (full duplex), an 8-bit 11-channel AD converter, two 12-bit PWM channels, a system clock frequency divider, ROM correction function, and a 26-source 10-vector interrupt feature.

### **Features**

#### **■**ROM

65536 × 8-bits (LC875J64C)
 57344 × 8-bits (LC875J56C)
 49152 × 8-bits (LC875J48C)

#### **■**RAM

• 2048 × 9-bits (LC875J64C/56C/48C)

#### ■Minimum Bus Cycle

83.3ns (12MHz) V<sub>DD</sub>=3.0 to 5.5V
 125ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V
 500ns (2MHz) V<sub>DD</sub>=2.2 to 5.5V

Note: The bus cycle time here refers to the ROM read speed.

customer shall be solely responsible for the use.

- Any and all SANYO Semiconductor Co.,Ltd. products described or contained herein are, with regard to "standard application", intended for the use as general electronics equipment (home appliances, AV equipment, communication device, office equipment, industrial equipment etc.). The products mentioned herein shall not be intended for use for any "special application" (medical equipment whose purpose is to sustain life, aerospace instrument, nuclear control device, burning appliances, transportation machine, traffic signal system, safety equipment etc.) that shall require extremely high level of reliability and can directly threaten human lives in case of failure or malfunction of the product or may cause harm to human bodies, nor shall they grant any guarantee thereof. If you should intend to use our products for applications outside the standard applications of our customer who is considering such use and/or outside the scope of our intended standard applications, please
- Specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.

consult with us prior to the intended use. If there is no consultation or inquiry before the intended use, our

#### SANYO Semiconductor Co., Ltd.

TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110-8534 JAPAN

■Minimum Instruction Cycle Time

• 250ns (12MHz)  $V_{DD}=3.0 \text{ to } 5.5 \text{V}$ • 375ns (8MHz) V<sub>DD</sub>=2.5 to 5.5V V<sub>DD</sub>=2.2 to 5.5V • 1.5µs (2MHz)

#### **■**Ports

• Normal withstand voltage I/O ports

Ports whose I/O direction can be designated in 1-bit units 46 (P1n, P2n, P70 to P73, P80 to P86, PBn, PCn, PWM2, PWM3, XT2)

Ports whose I/O direction can be designated in 4-bit units

8 (P0n) • Normal withstand voltage input port 1 (XT1)

2 (CF1, CF2) • Dedicated oscillator ports • Reset pins  $1(\overline{RES})$ 

• Power pins 6 (VSS1 to 3, VDD1 to 3)

#### **■**Timers

• Timer 0: 16-bit timer/counter with two capture registers.

Mode 0: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) × 2 channels

Mode 1: 8-bit timer with an 8-bit programmable prescaler (with two 8-bit capture registers) + 8-bit counter (with two 8-bit capture registers)

Mode 2: 16-bit timer with an 8-bit programmable prescaler (with two 16-bit capture registers)

Mode 3: 16-bit counter (with two 16-bit capture registers)

• Timer 1: 16-bit timer/counter that supports PWM/toggle outputs

Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)

Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels

Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from the lower-order 8-bits)

Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (The lower-order 8-bits can be used as PWM)

- Timer 4: 8-bit timer with a 6-bit prescaler
- Timer 5: 8-bit timer with a 6-bit prescaler
- Timer 6: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 7: 8-bit timer with a 6-bit prescaler (with toggle output)
- Timer 8: 16-bit timer

Mode 0: 8-bit timer with an 8-bit prescaler  $\times$  2 channels

Mode 1: 16-bit timer with an 8-bit prescaler

- \* Timer 8 is not supported in this version of Emulator. Please use on-chip-debugger (only supported in flash-ROM version) for debugging when developing software.
- Base Timer
  - 1) The clock is selectable from the subclock (32.768kHz crystal oscillation), system clock, and timer 0 prescaler
  - 2) Interrupts programmable in 5 different time schemes

### ■High-speed Clock Counter

- 1) Can count clocks with a maximum clock rate of 20MHz (at a main clock of 10MHz).
- 2) Can generate output real-time.

#### **■**SIO

- SIO0: 8-bit synchronous serial interface
  - 1) LSB first/MSB first mode selectable
  - 2) Built-in 8-bit baudrate generator (maximum transfer clock cycle = 4/3 tCYC)
  - 3) Automatic continuous data transmission (1 to 256 bits, specifiable in 1 bit units, suspension and resumption of data transmission possible in 1 byte units)
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

#### **■**UART

- Full duplex
- 7/8/9 bit data bits selectable
- 1 stop bit (2-bit in continuous data transmission)
- Built-in baudrate generator
- ■AD Converter: 8-bits × 11 channels
- ■PWM: Multifrequency 12-bit PWM × 2 channels
- ■Remote Control Receiver Circuit (sharing pins with P73, INT3, and T0IN)
  - Noise rejection function (noise filter time constant selectable from 1 tCYC, 32 tCYC, and 128 tCYC)
- ■Watchdog Timer
  - External RC watchdog timer
  - Interrupt and reset signals selectable
- ■Clock Output Function
  - 1) Able to output selected oscillation clock 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, 1/64 as system clock.
- 2) Able to output oscillation clock of sub clock.

#### **■**Interrupts

- 26 sources, 10 vector addresses
  - 1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  - 2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address takes precedence.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4
4	0001BH	H or L	INT3/INT5/base timer
5	00023H	H or L	T0H/INT6
6	0002BH	H or L	T1L/T1H/INT7
7	00033H	H or L	SIO0/UART1 receive/T8L/T8H
8	0003BH	H or L	SIO1/UART1 transmit
9	00043H	H or L	ADC/T6/T7
10	0004BH	H or L	Port 0/T4/T5/PWM2, PWM3

- Priority levels X > H > L
- Of interrupts of the same level, the one with the smallest vector address takes precedence.
- IFLG (list of interrupt source flag function)
  - 3) Shows a list of interrupt source flags that caused a branching to a particular vector address (shown in the diagram above).
- ■Subroutine Stack Levels: 1024 levels (the stack is allocated in RAM)
- ■High-speed Multiplication/Division Instructions

16-bits × 8-bits (5 tCYC execution time)
 24-bits × 16-bits (12 tCYC execution time)
 16-bits ÷ 8-bits (8 tCYC execution time)
 24-bits ÷ 16-bits (12 tCYC execution time)

#### ■Oscillation Circuits

• RC oscillation circuit (internal): For system clock

• CF oscillation circuit: For system clock, with internal Rf

• Crystal oscillation circuit: For low-speed system clock, with internal Rf

• Frequency variable RC oscillation circuit (internal): For system clock

#### ■System Clock Divider Function

- Can run on low current.
- The minimum instruction cycle selectable from 300ns, 600ns, 1.2μs, 2.4μs, 4.8μs, 9.6μs, 19.2μs, 38.4μs, and 76.8μs (at a main clock rate of 10MHz).

#### ■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  - 1) Oscillation is not halted automatically.
  - 2) Canceled by a system reset or occurrence of an interrupt
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  - 1) The CF, RC, and crystal oscillators automatically stop operation.
  - 2) There are three ways of resetting the HOLD mode.
    - (1) Setting the reset pin to the low level.
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer.
  - 1) The CF and RC oscillators automatically stop operation.
  - 2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  - 3) There are four ways of resetting the X'tal HOLD mode.
    - (1) Setting the reset pin to the low level
    - (2) Setting at least one of the INT0, INT1, INT2, INT4, and INT5 pins to the specified level
    - (3) Having an interrupt source established at port 0
    - (4) Having an interrupt source established in the base timer circuit

#### ■ROM Correction Function

- Executes the correction program on detection of a match with the program counter value.
- Correction program area size : 128 bytes

### ■Package Form

QIP64E (14 × 14): Lead-free type
TQFP64J (10 × 10): Lead-free type

#### **■**Development Tools

• Evaluation chip: LC87EV690

• Emulator: EVA62S + ECB876600D + SUB875800 + POD64QFP or POD64SQFP

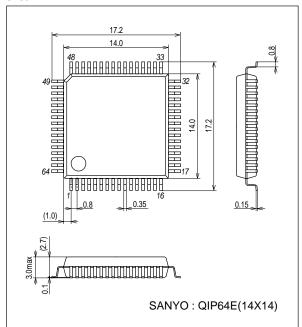
ICE-B877300 + SUB875800 + POD64QFP or POD64SQFP

• On-chip debugger: TCB87-TypeA or TCB87-TypeB + LC87F5JC8A

### **Package Dimensions**

unit: mm (typ)

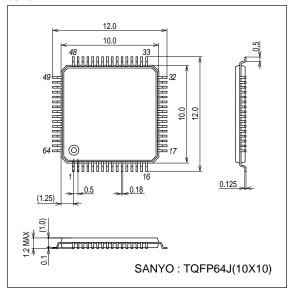
3159A



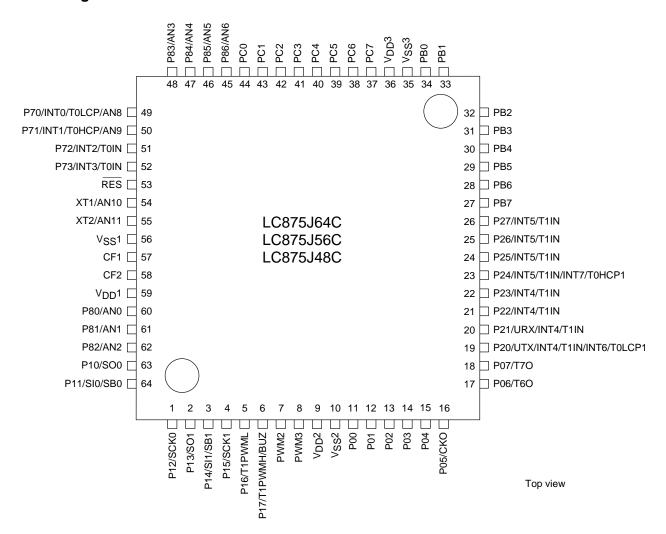
### **Package Dimensions**

unit: mm (typ)

3310

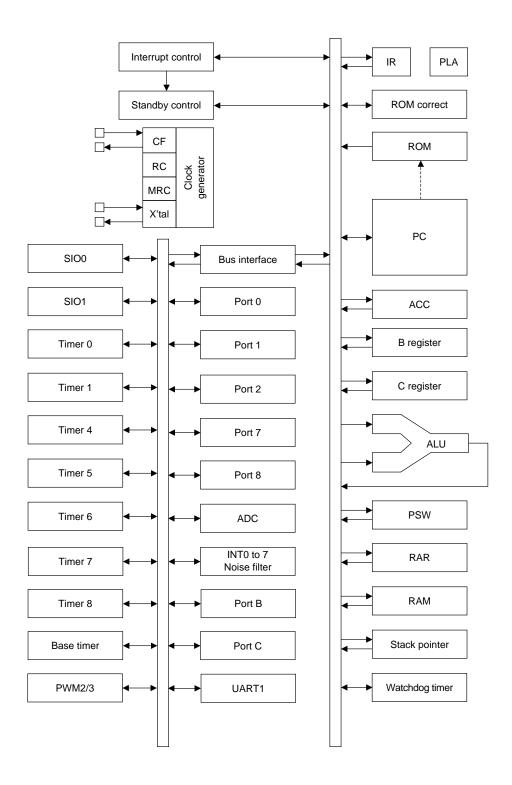


### **Pin Assignment**



SANYO: QIP64E(14×14) "Lead-free Type" SANYO: TQFP64J(10×10) "Lead-free Type"

### **System Block Diagram**



### **Pin Description**

III D0001	Puon								
Pin Name	I/O			De	scription				Option
V <sub>SS</sub> 1	-	- Power supply	pin						No
V <sub>SS</sub> 2									
V <sub>SS</sub> 3									
V <sub>DD</sub> 1	-	+ Power supply	/ pin						No
V <sub>DD</sub> 2									
V <sub>DD</sub> 3									
Port 0	I/O	• 8-bit I/O port							Yes
P00 to P07		I/O specifiable     Pull up resists		d d -ff : 4	hisisa				
		HOLD reset in		d on and off in 4-	bit units.				
		Port 0 interrup	•						
		Shared pins	ot input						
			utput (system clo	ck/can selected	from sub clock)				
		P06: Timer 6			,				
		P07: Timer 7							
Port 1	I/O	• 8-bit I/O port							Yes
P10 to P17		I/O specifiable	e in 1-bit units						
		Pull-up resistor	ors can be turned	d on and off in 1-	bit units.				
		Pin functions							
		P10: SIO0 da	•						
			ta input/bus I/O						
		P12: SIO0 clo							
		P13: SIO1 da	ta output ta input/bus I/O						
		P15: SIO1 da	•						
		P16: Timer 1F							
			PWMH output/be	eper output					
Port 2	I/O	• 8-bit I/O port							Yes
P20 to P27		I/O specifiable	e in 1-bit units						
. 20 10 1 21		Pull-up resistor	ors can be turned	d on and off in 1-	bit units.				
		Pin functions							
		P20: UART tr	ansmit						
		P21: UART re							
			•	•	1 event input/tin	ner 0L capture in	put/		
			imer 0H capture	-					
			-		1 event input/tin	ner 0L capture in	put/		
			imer 0H capture out/timer 0L capto	•					
			out/timer 0H capt	-					
		Interrupt ackno	-	aro i input					
		I Spi do Mio			Rising &			1	
			Rising	Falling	Falling	H level	L level		
		INT4	enable	enable	enable	disable	disable	1	
		1.1		enable	enable	disable	disable		
		INT5	enable	enable	eriable	aloablo	a.cab.c	1 1	
		INT5 INT6	enable	enable	enable	disable	disable		

Continued on next page.

Continued from preceding page.

Pin Name	I/O			Des	cription			Option	
Port 7	I/O	• 4-bit I/O port						No	
P70 to P73		I/O specifiabl	e in 1-bit units						
		<ul> <li>Pull-up resist</li> </ul>	ors can be turne	d on and off in 1-b	oit units.				
		<ul> <li>Shared pins</li> </ul>							
		P70: INT0 in	out/HOLD reset in	nput/timer 0L cap	ture input/watchd	og timer output			
		P71: INT1 in	out/HOLD reset in	nput/timer 0H cap	ture input				
	P72: INT2 input/HOLD reset input/timer 0 event input/timer 0L capture input/								
		High sp	eed clock counte	er input					
		P73: INT3 in	out (with noise file	ter)/timer 0 event	input/timer 0H ca	pture input			
		AD converter input port: AN8 (P70), AN9 (P71)							
		Interrupt acknow	wledge type		T	T	T 1		
			Rising	Falling	Rising & Falling	H level	L level		
		INT0	enable	enable	disable	enable	enable		
		INT1	enable	enable	disable	enable	enable		
		INT2	enable	enable	enable	disable	disable		
		INT3	enable	enable	enable	disable	disable		
Port 8	I/O	• 7-bit I/O port						No	
P80 to P86		I/O specifiabl	• I/O specifiable in 1-bit units						
		Shared pins							
		AD converte	input port : AN0	(P80) to AN6 (P8	36)				
PWM2, PWM3	I/O	PWM2 and P	WM3 output port	ts				No	
		General-purp	ose I/O available	•					
Port B	I/O	8-bit I/O port						Yes	
PB0 to PB7		I/O specifiabl	e in 1-bit units						
		·	ors can be turned	d on and off in 1-b	oit units.				
Port C	I/O	8-bit I/O port						Yes	
PC0 to PC7		I/O specifiabl							
		Pull-up resist	ors can be turne	d on and off in 1-b	oit units.				
RES	Input	Reset pin						No	
XT1	Input	• 32.768kHz cı	ystal oscillator in	put pin				No	
		Shared pins							
		General-purp	ose input port						
		AD converter	input port: AN10	)					
		Must be conne	cted to V <sub>DD</sub> 1 if r	not to be used.					
XT2	I/O	• 32.768kHz cı	ystal oscillator o	utput pin				No	
		Shared pins							
		General-purp	ose I/O port						
		AD converte	input port: AN1	I					
		1		ept open if not to	be used.				
CF1	Input	Ceramic reson	ator input pin					No	
CF2	Output	Ceramic reson	ator output pin					No	

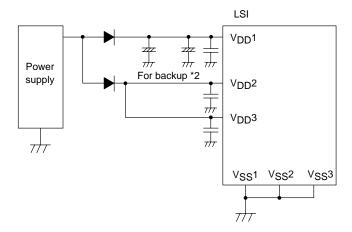
### **Port Output Types**

The table below lists the types of port outputs and the presence/absence of a pull-up resistor. Data can be read into any input port even if it is in the output mode.

Port Name	Option Selected in Units of	Option Type	Output Type	Pull-up Resistor
P00 to P07	1-bit	1	CMOS	Programmable (Note 1)
		2	Nch-open drain	No
P10 to P17	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable
P71 to P73	=	No	CMOS	Programmable
P80 to P86	=	No	Nch-open drain	No
PWM2, PWM3	-	No	CMOS	No
PB0 to PB7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
PC0 to PC7	1-bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
XT1	-	No	Input for 32.768kHz crystal oscillator (Input only)	No
XT2	-	No	Output for 32.768kHz crystal oscillator (Nch-open drain when in general-purpose output mode)	No

Note 1: Programmable pull-up resistors for port 0 are controlled in 4-bit units (P00 to 03, P04 to 07).

\*1: Connect the IC as shown below to minimize the noise input to the V<sub>DD</sub>1 pin. Be sure to electrically short the V<sub>SS</sub>1, V<sub>SS</sub>2, and V<sub>SS</sub>3 pins.



\*2: The internal memory is sustained by V<sub>DD</sub>1. If none of V<sub>DD</sub>2 and V<sub>DD</sub>3 are backed up, the high level output at the ports are unstable in the HOLD backup mode, allowing through current to flow into the input buffer and thus shortening the backup time.

Make sure that the port outputs are held at the low level in the HOLD backup mode.

**Absolute Maximum Ratings** at Ta = 25°C,  $V_SS1 = V_SS2 = V_SS3 = 0V$ 

	Parameter	Symbol	Pin/Remarks	Conditions			Specifi	cation	
		,			V <sub>DD</sub> [V]	min	typ	max	un
	ximum supply tage	V <sub>DD</sub> max	$V_{DD}1$ , $V_{DD}2$ , $V_{DD}3$	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3		-0.3		+6.5	
np	ut voltage	V <sub>I</sub> (1)	XT1, CF1			-0.3		V <sub>DD</sub> +0.3	
np	ut/output voltage	V <sub>IO</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C PWM2, PWM3, XT2			-0.3		V <sub>DD</sub> +0.3	\
	Peak output current	IOPH(1)	Ports 0, 1, 2 Ports B, C	CMOS output select Per 1 applicable pin		-10			
		IOPH(2)	PWM2, PWM3	Per 1 applicable pin		-20			
		IOPH(3)	P71 to P73	Per 1 applicable pin		-5			
	Mean output current	IOMH(1)	Ports 0, 1, 2 Ports B, C	CMOS output select Per 1 applicable pin		-7.5			
<u> </u>	(Note 1-1)	IOMH(2)	PWM2, PWM3	Per 1 applicable pin		-15			
บา		IOMH(3)	P71 to P73	Per 1 applicable pin		-3			
dinc	Total output	ΣΙΟΑΗ(1)	P71 to P73	Total of all applicable pins		-10			
High level output current	current	ΣΙΟΑΗ(2)	Port 1 PWM2, PWM3	Total of all applicable pins		-25			
Hig		ΣΙΟΑΗ(3)	Ports 0, 2	Total of all applicable pins		-25			
		ΣΙΟΑΗ(4)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins		-45			
		ΣΙΟΑΗ(5)	Port B	Total of all applicable pins		-25			
		ΣΙΟΑΗ(6)	Port C	Total of all applicable pins		-25			
		ΣΙΟΑΗ(7)	Ports B, C	Total of all applicable pins		-45			
	Peak output current	IOPL(1)	P02 to P07 Ports 1, 2 Ports B, C	Per 1 applicable pin				20	
		IOPL(2)	PWM2, PWM3 P00, P01	Per 1 applicable pin				30	
		IOPL(3)	Ports 7, 8 XT2	Per 1 applicable pin				10	n
ţ	Mean output current (Note 1-1)	IOML(1)	P02 to P07 Ports 1, 2 Ports B, C PWM2, PWM3	Per 1 applicable pin				15	
ut current		IOML(2)	P00, P01	Per 1 applicable pin				20	
utbut cr		IOML(3)	Ports 7, 8 XT2	Per 1 applicable pin				7.5	
Low level outp	Total output current	ΣIOAL(1)	Port 7 P83 to P86, XT2	Total of all applicable pins				15	
NO-		ΣIOAL(2)	P80 to P82	Total of all applicable pins				15	
		ΣIOAL(3)	Ports 7, 8 XT2	Total of all applicable pins				20	
		ΣIOAL(4)	Port 1 PWM2, PWM3	Total of all applicable pins				45	
		ΣIOAL(5)	Ports 0, 2	Total of all applicable pins				45	
		ΣIOAL(6)	Ports 0, 1, 2 PWM2, PWM3	Total of all applicable pins				80	
		ΣIOAL(7)	Port B	Total of all applicable pins				45	
		ΣIOAL(8)	Port C	Total of all applicable pins				45	
		ΣIOAL(9)	Ports B, C	Total of all applicable pins				80	
Pov	wer dissipation	Pd max	QIP64E (14 × 14)	Ta=-30 to +70°C				355	n
0-	orating ambient	Topr	TQFP64J (10 × 10)					255	
tem	erating ambient	Topr				-30		+70	c
	rage ambient nperature	Tstg				-55		+125	

Note 1-1: The mean output current is a mean value measured over 100ms.

Allowable Operating Conditions at Ta = -30 °C to +70 °C,  $V_SS1 = V_SS2 = V_SS3 = 0V$ 

	<u> </u>		7 . 00-	- טט	. 555		
Symbol	Pin/Remarks	Conditions			Specif	ication	ı
Symbol	1 III/IVerilaiks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
V <sub>DD</sub> (1)	$V_{DD}1=V_{DD}2=V_{DD}3$	0.245μs≤tCYC≤200μs		3.0		5.5	
		0.367μs≤tCYC≤200μs		2.5		5.5	
		1.47μs≤tCYC≤200μs		2.2		5.5	
VHD	V <sub>DD</sub> 1=V <sub>DD</sub> 2=V <sub>DD</sub> 3	RAM and register contents sustained in HOLD mode.		2.0		5.5	
V <sub>IH</sub> (1)	Ports 1, 2 P71 to P73 P70 port input/ interrupt side		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		V <sub>DD</sub>	
V <sub>IH</sub> (2)	Ports 0, 8, B, C PWM2, PWM3		2.2 to 5.5	0.3V <sub>DD</sub> +0.7		$V_{DD}$	
V <sub>IH</sub> (3)	Port 70 watchdog timer side		2.2 to 5.5	0.9V <sub>DD</sub>		V <sub>DD</sub>	V
V <sub>IH</sub> (4)	XT1, XT2, CF1 RES		2.2 to 5.5	0.75V <sub>DD</sub>		$V_{DD}$	
V <sub>IL</sub> (1)	Ports 1, 2 P71 to P73		4.0 to 5.5	V <sub>SS</sub>		0.1V <sub>DD</sub> +0.4	
	P70 port input/ interrupt side		2.2 to 4.0	V <sub>SS</sub>		0.2V <sub>DD</sub>	
V <sub>IL</sub> (2)	Ports 0, 8, B, C PWM2, PWM3		4.0 to 5.5	$V_{SS}$		0.15V <sub>DD</sub> +0.4	
			2.2 to 4.0	$V_{SS}$		0.2V <sub>DD</sub>	
V <sub>IL</sub> (3)	Port 70 watchdog timer side		2.2 to 5.5	V <sub>SS</sub>		0.8V <sub>DD</sub> -1.0	
V <sub>IL</sub> (4)	XT1, XT2, CF1 RES		2.2 to 5.5	V <sub>SS</sub>		0.25V <sub>DD</sub>	
tCYC			3.0 to 5.5	0.245		200	
			2.5 to 5.5	0.367		200	μs
			2.2 to 5.5	1.47		200	
FEXCF(1)	CF1	CF2 pin open     System clock frequency	3.0 to 5.5	0.1		12	
		division ratio=1/1	2.5 to 5.5	0.1		8	i
		• External system clock duty =50 ± 5%	2.2 to 5.5	0.1		2	
		CF2 pin open	3.0 to 5.5	0.2		24.4	
			2.5 to 5.5	0.2		16	
		division ratio=1/2	2.2 to 5.5	0.2		4	j
FmCF(1)	CF1, CF2	12MHz ceramic oscillation See Fig. 1.	3.0 to 5.5		12		MHz
FmCF(2)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		
FmCF(3)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.2 to 5.5		4		
FmRC		Internal RC oscillation	2.2 to 5.5	0.3	1.0	2.0	j
FmMRC		Frequency variable RC oscillation source oscillation	2.2 to 5.5		16		
	VHD  VIH(1)  VIH(2)  VIH(3)  VIH(4)  VIL(1)  VIL(2)  VIL(3)  VIL(4)  tCYC  FEXCF(1)  FmCF(1)  FmCF(2)  FmRC	VDD(1)         VDD1=VDD2=VDD3           VHD         VDD1=VDD2=VDD3           VIH(1)         Ports 1, 2             P71 to P73             P70 port input/             interrupt side           VIH(2)         Ports 0, 8, B, C             PWM2, PWM3           VIH(3)         Port 70 watchdog             timer side           VIH(4)         XT1, XT2, CF1             RES           VIL(1)         Ports 1, 2             P71 to P73             P70 port input/             interrupt side           VIL(2)         Ports 0, 8, B, C             PWM2, PWM3           VIL(3)         Port 70 watchdog             timer side           VIL(4)         XT1, XT2, CF1             RES           tCYC         TEXCF(1)           FEXCF(1)         CF1           FmCF(2)         CF1, CF2           FmCF(3)         CF1, CF2           FmRC         FmRC	Symbol	Symbol         Pin/Remarks         Conditions         Vpp [V]           VDD(1)         VDD1=VDD2=VDD3         0.245μsstCYC≤200μs         1.47μsstCYC≤200μs           VHD         VDD1=VDD2=VDD3         RAM and register contents sustained in HOLD mode.           VIH(1)         Ports 1, 2 P71 to P73 P70 port input/ interrupt side         2.2 to 5.5           VIH(2)         Ports 0, 8, B, C PVMM2, PVMM3         2.2 to 5.5           VIH(3)         Port 70 watchdog timer side         2.2 to 5.5           VIH(4)         XT1, XT2, CF1 RES         2.2 to 5.5           VIL(1)         Ports 1, 2 P71 to P73 P70 port input/ interrupt side         4.0 to 5.5           VIL(2)         Ports 0, 8, B, C PVM2, PVM3         2.2 to 4.0           VIL(3)         Port 70 watchdog timer side         2.2 to 5.5           VIL(4)         XT1, XT2, CF1 RES         2.2 to 5.5           ICYC         3.0 to 5.5         2.2 to 5.5           VIL(4)         XT1, XT2, CF1 RES         2.2 to 5.5           ICYC         3.0 to 5.5         2.5 to 5.5           ICYC         4.0 to 5.5         2.5 to 5.5           ICYC         5.5 to 5.5         2.2 to 5.5           ICYC         4.0 to 5.5         2.2 to 5.5           ICYC         5.0 to 5.5         2.2 to 5.5	Symbol   Pin/Remarks   Conditions   VDD [V]   min	Symbol   Pir/Remarks   Conditions   VoD [V]   min   typ	VpD(1)

Note 2-1: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-2: See Tables 1 and 2 for the oscillation constants.

### **Electrical Characteristics** at $Ta = -30^{\circ}C$ to $+70^{\circ}C$ , $V_SS1 = V_SS2 = V_SS3 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
i alametei	Symbol	Till/Itellians	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High level input current	I <sub>IH</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VDD (Including output Tr's off leakage current)	2.2 to 5.5			1	
	I <sub>IH</sub> (2)	XT1, XT2	For input port specification  VIN=VDD	2.2 to 5.5			1	
	I <sub>IH</sub> (3)	CF1	V <sub>IN</sub> =V <sub>DD</sub>	2.2 to 5.5			15	١.
Low level input current	I <sub>IL</sub> (1)	Ports 0, 1, 2 Ports 7, 8 Ports B, C RES PWM2, PWM3	Output disabled Pull-up resistor off VIN=VSS (Including output Tr's off leakage current)	2.2 to 5.5	-1			μА
	I <sub>IL</sub> (2)	XT1, XT2	For input port specification VIN=VSS	2.2 to 5.5	-1			
	I <sub>IL</sub> (3)	CF1	V <sub>IN</sub> =V <sub>SS</sub>	2.2 to 5.5	-15			
High level output	V <sub>OH</sub> (1)	Ports 0, 1, 2	I <sub>OH</sub> =-1mA	4.5 to 5.5	V <sub>DD</sub> -1			
voltage	V <sub>OH</sub> (2)	Ports B, C	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (3)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (4)	P71 to P73	I <sub>OH</sub> =-0.4mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (5)		I <sub>OH</sub> =-0.2mA	2.2 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (6)	PWM2, PWM3	I <sub>OH</sub> =-10mA	4.5 to 5.5	V <sub>DD</sub> -1.5			
	V <sub>OH</sub> (7)	1	I <sub>OH</sub> =-1.6mA	3.0 to 5.5	V <sub>DD</sub> -0.4			
	V <sub>OH</sub> (8)	1	I <sub>OH</sub> =-1mA	2.2 to 5.5	V <sub>DD</sub> -0.4			١.,
Low level output	V <sub>OL</sub> (1)	Ports 0, 1, 2	I <sub>OL</sub> =10mA	4.5 to 5.5			1.5	V
voltage	V <sub>OL</sub> (2)	Ports B, C	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (3)	PWM2, PWM3	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (4)	Ports 7, 8	I <sub>OL</sub> =1.6mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (5)	XT2	I <sub>OL</sub> =1mA	2.2 to 5.5			0.4	
	V <sub>OL</sub> (6)	P00, P01	I <sub>OL</sub> =30mA	4.5 to 5.5			1.5	
	V <sub>OL</sub> (7)	1	I <sub>OL</sub> =5mA	3.0 to 5.5			0.4	
	V <sub>OL</sub> (8)		I <sub>OL</sub> =2.5mA	2.2 to 5.5			0.4	
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 7	V <sub>OH</sub> =0.9V <sub>DD</sub>	4.5 to 5.5	15	35	80	Lo
	Rpu(2)	Ports B, C		2.2 to 5.5	18	50	150	kΩ
Hysteresis voltage	VHYS	RES Ports 1, 2, 7		2.2 to 5.5		0.1 V <sub>DD</sub>		٧
Pin capacitance	СР	All pins	For pins other than that under test:  VIN=VSS f=1MHz Ta=25°C	2.2 to 5.5		10		pF

## Serial Input/Output Characteristics at Ta = -30°C to +70°C, $V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$ 1. SIO0 Serial I/O Characteristics (Note 4-1-1)

		Parameter	Symbol	Pin/Remarks	Conditions			Speci	fication	
	r	arameter	Symbol	i iii/NeiiiaiKS	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
		Frequency	tSCK(1)	SCK0(P12)	See Fig. 6.		2			
	×	Low level pulse width	tSCKL(1)	-			1			
	Input clock	High level pulse width	tSCKH(1)			2.2 to 5.5	1			tCYC
Serial clock	In		tSCKHA(1)		Continuous data transmission/reception mode     See Fig. 6.     (Note 4-1-2)		4			1010
Serial		Frequency	tSCK(2)	SCK0(P12)	CMOS output selected     See Fig. 6.		4/3			
	ock	Low level pulse width	tSCKL(2)					1/2		tSCK
	Output clock	High level pulse width	tSCKH(2)			2.2 to 5.5		1/2		ISCK
	O		tSCKHA(2)		Continuous data transmission/reception mode     CMOS output selected     See Fig. 6.		tSCKH(2) +2tCYC		tSCKH(2) +(10/3) tCYC	tCYC
Serial input	Da	ta setup time	tsDI(1)	SB0(P11), SI0(P11)	Must be specified with respect to rising edge of SIOCLK.     See Fig. 6.		0.03			
Serial	Da	ta hold time	thDI(1)			2.2 to 5.5	0.03			
	Input clock	Output delay time	tdD0(1)	SO0(P10), SB0(P11)	Continuous data transmission/reception mode     (Note 4-1-3)				(1/3)tCYC +0.05	μs
Serial output	Input		tdD0(2)		• Synchronous 8-bit mode • (Note 4-1-3)	2.2 to 5.5			1tCYC +0.05	
Serik	Output clock		tdD0(3)		(Note 4-1-3)				(1/3)tCYC +0.05	

Note 4-1-1: These specifications are theoretical values. Add margin depending on its use.

Note 4-1-2: To use serial-clock-input in continuous trans/rec mode, a time from SIORUN being set when serial clock is "H" to the first negative edge of the serial clock must be longer than tSCKHA.

Note 4-1-3: Must be specified with respect to falling edge of SIOCLK. Must be specified as the time to the beginning of output state change in open drain output mode. See Fig. 6.

### 2. SIO1 Serial I/O Characteristics (Note 4-2-1)

		Dava	Compleal	Pin/Remarks	Conditions			Speci	fication	
		Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
	¥	Frequency	tSCK(3)	SCK1(P15)	See Fig. 6.		2			
	Input clock	Low level pulse width	tSCKL(3)				1			tCY
Serial clock	ū	High level pulse width	tSCKH(3)				1			С
Serial	¥	Frequency	tSCK(4)	SCK1(P15)	CMOS output selected     See Fig. 6.		2			
	Output clock	Low level pulse width	tSCKL(4)					1/2		tSCK
	õ	High level pulse width	tSCKH(4)					1/2		ISCK
Serial input	Da	ta setup time	tsDI(2)	SB1(P14), SI1(P14)	Must be specified with respect to rising edge of SIOCLK.     See Fig. 6.		0.03			
Serial	Da	ta hold time	thDI(2)				0.03			
Serial output	Ou	tput delay time	tdD0(4)	SO1(P13), SB1(P14)	Must be specified with respect to falling edge of SIOCLK.     Must be specified as the time to the beginning of output state change in open drain output mode.     See Fig. 6.				(1/3)tCYC +0.05	μѕ

Note 4-2-1: These specifications are theoretical values. Add margin depending on its use.

### Pulse Input Conditions at Ta = -30°C to +70°C, $V_SS1 = V_SS2 = V_SS3 = 0V$

Davastas	Cumahad	Pin/Remarks	Conditions			Specif	fication	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
High/low level	tPIH(1)	INT0(P70),	Interrupt source flag can be set.					
pulse width	tPIL(1)	INT1(P71),	Event inputs for timer 0 or 1					
		INT2(P72),	are enabled.					
		INT4(P20 to P23),		2.2 to 5.5	1			
		INT5(P24 to P27),						
		INT6(P20),						
		INT7(P24)						
	tPIH(2)	INT3(P73) when	Interrupt source flag can be set.					tCYC
	tPIL(2)	noise filter time	Event inputs for timer 0 are enabled.	2.2 to 5.5	2			icic
		constant is 1/1						
	tPIH(3)	INT3(P73) when	Interrupt source flag can be set.					
	tPIL(3)	noise filter time	Event inputs for timer 0 are enabled.	2.2 to 5.5	64			
		constant is 1/32						
	tPIH(4)	INT3(P73) when	Interrupt source flag can be set.					
	tPIL(4)	noise filter time	Event inputs for timer 0 are enabled.	2.2 to 5.5	256			
		constant is 1/128						
	tPIL(5)	RES	Resetting is enabled.	2.2 to 5.5	200			μs

### AD Converter Characteristics / Ta = -30 °C to +70 °C, $V_SS1 = V_SS2 = V_SS3 = 0V$

D	0	Dis /Dansada	O an altition o			Specifi	cation	
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit
Resolution	N	AN0(P80) to		3.0 to 5.5		8		bit
Absolute accuracy	ET	AN6(P86), AN8(P70),	(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD	AN9(P71), AN10(XT1),	AD conversion time=32×tCYC (when ADCR2=0) (Note 6-2)	4.5 to 5.5	15.68 (tCYC=		97.92 (tCYC=	
		AN11(XT2)			0.49µs)		3.06µs)	
					23.52		97.92	
				3.0 to 5.5	(tCYC=		(tCYC=	
					0.735μs)		3.06µs)	
			AD conversion time=64×tCYC		18.82		97.92	μs
			(when ADCR2=1) (Note 6-2)	4.5 to 5.5	(tCYC=		(tCYC=	
					0.294μs)		1.53µs)	
					47.04		97.92	
				3.0 to 5.5	(tCYC=		(tCYC=	
					0.735μs)		1.53µs)	
Analog input voltage range	VAIN			3.0 to 5.5	V <sub>SS</sub>		$V_{DD}$	V
Analog port	IAINH		VAIN=V <sub>DD</sub>	3.0 to 5.5			1	
input current	IAINL		VAIN=V <sub>SS</sub>	3.0 to 5.5	-1			μА

Note 6-1: The quantization error ( $\pm 1/2$ LSB) is excluded from the absolute accuracy value.

Note 6-2: The conversion time refers to the interval from the time the instruction for starting the converter is issued till the time the complete digital value corresponding to the analog input value is loaded in the required register.

 $\textbf{Consumption Current Characteristics} \ \, \text{at } Ta = -30^{\circ}C \ \, \text{to} \ \, +70^{\circ}C, \ \, V_{SS}1 = V_{SS}2 = V_{SS}3 = 0V$ 

Parameter	Symbol	Pin/	Conditions				ication									
	-,	Remarks		V <sub>DD</sub> [V]	min	typ	max	unit								
Normal mode consumption current (Note 7-1)	IDDOP(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	FmCF=12MHz ceramic oscillation mode FmX'tal=32.768kHz crystal oscillation mode System glock set to 12MHz eide	4.5 to 5.5		8	13.5									
	IDDOP(2)		System clock set to 12MHz side     Internal RC oscillation stopped     Frequency variable RC     oscillation stopped     1/1 frequency division ratio	3.0 to 3.6		4.5	8									
	IDDOP(3)		CF1=24MHz external clock FmX'tal=32.768kHz crystal oscillation mode System clock set to CF1 side	4.5 to 5.5		9.5	16									
	IDDOP(4)		Internal RC oscillation stopped     Frequency variable RC     oscillation stopped     1/2 frequency division ratio	3.0 to 3.6		5.2	8.8									
	IDDOP(5)		FmCF=8MHz     ceramic oscillation mode     FmX'tal=32.768kHz crystal	4.5 to 5.5		5.5	9									
	IDDOP(6)		oscillation mode  • System clock set to 8MHz side  • Internal RC oscillation stopped	3.0 to 3.6		3.1	5.6									
	IDDOP(7)		Frequency variable RC oscillation stopped     1/1 frequency division ratio	2.5 to 3.0		2.2	3.8	mA								
	IDDOP(8)		_	FmCF=4MHz     ceramic oscillation mode     FmX'tal=32.768kHz crystal	4.5 to 5.5		2	3.2								
	IDDOP(9)			_				oscillation mode  • System clock set to 4MHz side  • Internal RC oscillation stopped	3.0 to 3.6		1	2				
	IDDOP(10)				Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.7	1.4							
	IDDOP(11)		FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		0.55	2.1									
	IDDOP(12)		System clock set to internal RC oscillation     Frequency variable RC oscillation	3.0 to 3.6		0.3	1.4									
	IDDOP(14)		stopped     1/2 frequency division ratio     FmCF=0Hz (oscillation stopped)	2.2 to 3.0		0.2	1									
	IDDOP(14)		FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		1.2	3.5									
	IDDOP(16)				-			-		• Syster	Internal RC oscillation stopped     System clock set to 1MHz with frequency variable RC oscillation	3.0 to 3.6 2.2 to 3.0		0.65	1.6	
	• 1/2 frequency division     IDDOP(17)     • FmCF=0Hz (oscillation)		1/2 frequency division ratio     FmCF=0Hz (oscillation stopped)     FmX'tal=32.768kHz crystal	4.5 to 5.5		27	65									
	IDDOP(18)		oscillation mode  System clock set to 32.768kHz side Internal RC oscillation stopped	3.0 to 3.6		11	45	μА								
	IDDOP(19)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		7	32									

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

Continued on next page.

Continued from preceding page.

Parameter	Symbol	Pin/	Conditions		Specification				
	-,	Remarks		min	typ	max	uni		
HALT mode consumption current (Note 7-1)	IDDHALT(1)	V <sub>DD</sub> 1 =V <sub>DD</sub> 2 =V <sub>DD</sub> 3	HALT mode     FmCF=12MHz ceramic oscillation mode     FmX'tal=32.768kHz crystal oscillation mode     System clock set to 12MHz side	4.5 to 5.5		2.7	5.5		
	IDDHALT(2)		Internal RC oscillation stopped     Frequency variable RC oscillation stopped     1/1 frequency division ratio	3.0 to 3.6		1.4	3		
	IDDHALT(3)		HALT mode     CF1=24MHz external clock     FmX'tal=32.768kHz crystal oscillation mode     System clock set to CF1 side	4.5 to 5.5		3.6	7.4		
	IDDHALT(4)		Internal RC oscillation stopped Internal RC oscillation stopped Frequency variable RC oscillation stopped I/2 frequency division ratio	3.0 to 3.6		1.9	4.1		
	IDDHALT(5)		HALT mode     FmCF=8MHz ceramic oscillation mode	4.5 to 5.5		2	4.2		
	IDDHALT(6)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 8MHz side     Internal RC oscillation stopped	3.0 to 3.6		1.1	1.1     2.3       0.7     1.5		
	IDDHALT(7)		Frequency variable RC oscillation stopped     1/1 frequency division ratio	2.5 to 3.0		0.7		mA	
	IDDHALT(8)		HALT mode     FmCF=4MHz ceramic oscillation mode     FmYibal 20 700HHz caystal application mode	4.5 to 5.5			2.1		
	IDDHALT(9)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 4MHz side     Internal RC oscillation stopped	3.0 to 3.6			1.1		
	IDDHALT(10)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.3	0.3 0.7	-	
	IDDHALT(11)		HALT mode     FmCF=0Hz (oscillation stopped)	4.5 to 5.5		0.28			
	IDDHALT(12)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to internal RC oscillation	3.0 to 3.6		0.15	0.7		
	IDDHALT(13)	-	Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		0.1	0.1 0.5		
	IDDHALT(14)		HALT mode     FmCF=0Hz (oscillation stopped)	4.5 to 5.5		1	2.9		
	IDDHALT(15)		FmX'tal=32.768kHz crystal oscillation mode     Internal RC oscillation stopped     System clock set to 1MHz with	3.0 to 3.6		0.55	1.8		
	IDDHALT(16)		frequency variable RC oscillation  • 1/2 frequency division ratio	2.2 to 3.0		0.35	1.4		
	IDDHALT(17)		HALT mode     FmCF=0Hz (oscillation stopped)     Total to a result in the stopped in the st	4.5 to 5.5		19	50		
	IDDHALT(18)		FmX'tal=32.768kHz crystal oscillation mode     System clock set to 32.768kHz side     Internal RC oscillation stopped	3.0 to 3.6		6.2	30		
	IDDHALT(19)		Frequency variable RC oscillation stopped     1/2 frequency division ratio	2.2 to 3.0		3.6	20		
HOLD mode		V <sub>DD</sub> 1	• HOLD mode	4.5 to 5.5		0.015	10	μΑ	
consumption current	IDDHOLD(2)		CF1=V <sub>DD</sub> or open (external clock mode)	3.0 to 3.6		0.009	7		
ALI TOTAL	IDDHOLD(3)			2.2 to 3.0		0.006	6		
Fimer HOLD	IDDHOLD(4)		• Timer HOLD mode	4.5 to 5.5		16	45		
mode consumption	IDDHOLD(5)	1	CF1=V <sub>DD</sub> or open (external clock mode)     FmX'tal=32.768kHz crystal oscillation mode	3.0 to 3.6		5.5	25		
current	IDDHOLD(6)		· 1 · 1 · Cd · · · · · · · · · · · · · · · · ·	2.2 to 3.0		3	15		

Note 7-1: The consumption current value includes none of the currents that flow into the output Tr and internal pull-up resistors.

### **UART (Full Duplex) Operating Conditions** at Ta = -30°C to +70°C, $V_SS1 = V_SS2 = V_SS3 = 0V$

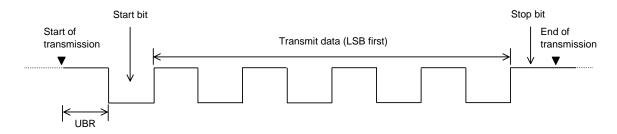
Doromotor	Symbol	Dia/Damania	Conditions		Specification				
Parameter	Symbol	Pin/Remarks	Conditions	V <sub>DD</sub> [V]	min	typ	max	unit	
Transfer rate	UBR	UTX(P20), URX(P21)		2.2 to 5.5	16/3		8192/3	tCYC	

Data length: 7, 8, and 9 bits (LSB first)

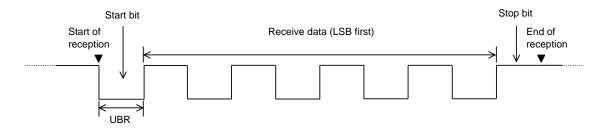
Stop bits: 1-bit (2-bit in continuous data transmission)

Parity bits: None

\*Example of Continuous 8-bit Data Transmission Mode Processing (First Transmit Data = 55H)



\*Example of Continuous 8-bit Data Reception Mode Processing (First Receive Data = 55H)



### Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator

Nominal	Vendor	Ossillator Name		Circuit	Constant		Operating Voltage	Oscillation Stabilization Time		Remarks
Frequency Name	Oscillator Name	C1 [pF]	C2 [pF]	Rf [Ω]	Rd1 [Ω]	Range [V]	typ [ms]	max [ms]		
12MHz	MURATA	CSTCE12M0G52-R0	(10)	(10)	Open	470	3.0 to 5.5	0.1	0.5	Internal C1, C2
8MHz	8MHz MURATA	CSTCE8M00G52-R0	(10)	(10)	Open	2.2k	2.7 to 5.5	0.1	0.5	Internal
8MHZ MURATA	CSTLS8M00G53-R0	(15)	(15)	Open	680	2.5 to 5.5	0.1	0.5	C1, C2	
4MHz MU	MUDATA	CSTCR4M00G53-R0		(15)	Open	3.3k	2.2 to 5.5	0.2	0.6	Internal
	MURATA	CSTLS4M00G53-B0	(15)	(15)	Open	3.3k	2.2 to 5.5	0.2	0.6	C1, C2

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after  $V_{DD}$  goes above the operating voltage lower limit (see Figure 4).

### Characteristics of a Sample Subsystem Clock Oscillator Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit with a Crystal Oscillator

Nominal Frequency	Vendor Name	Oscillator Name		Circuit (	Constant		Operating Voltage	Oscillation Stabilization Time			
			C3 [pF]	C4 [pF]	Rf [Ω]	Rd2 [Ω]	Range [V]	typ [s]	max [s]	Remarks	
32.768kHz	SEIKO EPSON	MC-306	18	18	Open	560k	2.2 to 5.5	1.4	3.0	Applicable CL value = 12.5pF	

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized after the instruction for starting the subclock oscillation circuit is executed and to the time interval that is required for the oscillation to get stabilized after the HOLD mode is reset (see Figure 4).

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

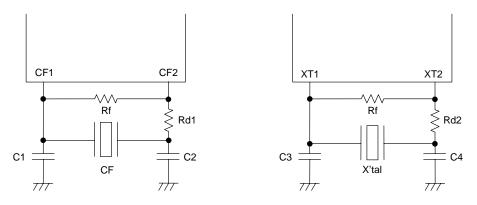


Figure 1 CF Oscillator Circuit

Figure 2 XT Oscillator Circuit

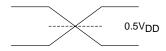
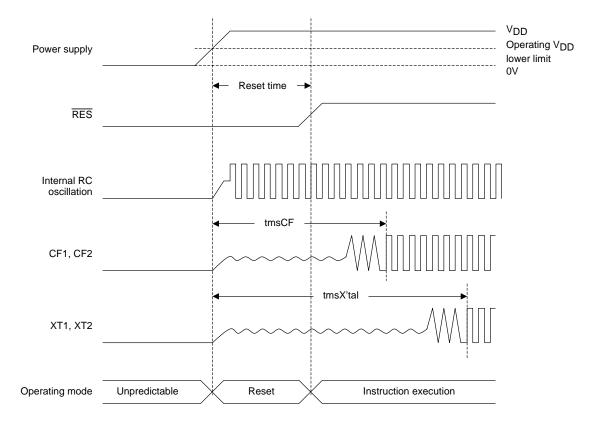
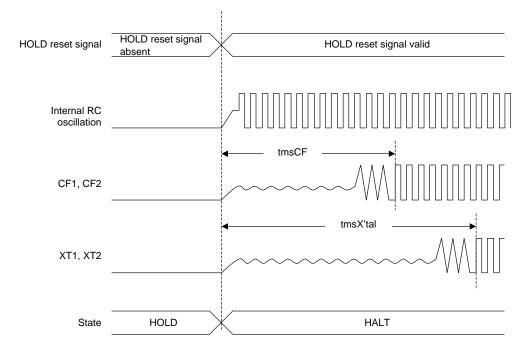


Figure 3 AC Timing Measurement Point

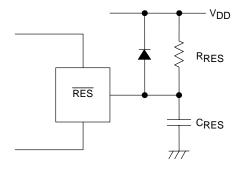


Reset Time and Oscillation Stabilizing Time



HOLD Reset Signal and Oscillation Stabilization Time

Figure 4 Oscillation Stabilization Times



#### Note:

Determine the value of  $C_{RES}$  and  $R_{RES}$  so that the reset signal is present for a period of 200 $\mu$ s after the supply voltage goes beyond the lower limit of the IC's operating voltage.

Figure 5 Reset Circuit

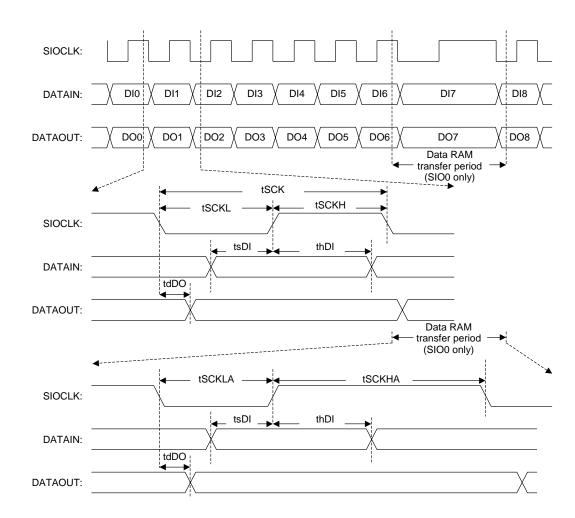


Figure 6 Serial I/O Output Waveforms

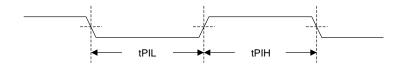


Figure 7 Pulse Input Timing Signal Waveform

- SANYO Semiconductor Co.,Ltd. assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all SANYO Semiconductor Co.,Ltd. products described or contained herein.
- SANYO Semiconductor Co.,Ltd. strives to supply high-quality high-reliability products, however, any and all semiconductor products fail or malfunction with some probability. It is possible that these probabilistic failures or malfunction could give rise to accidents or events that could endanger human lives, trouble that could give rise to smoke or fire, or accidents that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all SANYO Semiconductor Co.,Ltd. products described or contained herein are controlled under any of applicable local export control laws and regulations, such products may require the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written consent of SANYO Semiconductor Co.,Ltd.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the SANYO Semiconductor Co.,Ltd. product that you intend to use.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production.
- Upon using the technical information or products described herein, neither warranty nor license shall be granted with regard to intellectual property rights or any other rights of SANYO Semiconductor Co.,Ltd. or any third party. SANYO Semiconductor Co.,Ltd. shall not be liable for any claim or suits with regard to a third party's intellectual property rights which has resulted from the use of the technical information and products mentioned above.

This catalog provides information as of February, 2007. Specifications and information herein are subject to change without notice.