Document Title

128K x16 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0.0	Initial Draft	October 1, 1997	Preliminary
1.0	Finalize - Change operation voltage: Vcc=2.3~3.3V → Vcc=2.3~2.7V - Release operating current I_{CC}=2mA → 5mA I_{CC1} Read/Write=3/15mA → 5/20mA	August 27, 1998	Final

128K x16 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization:128Kx16
- Power Supply Voltage
  K6T2016S3M Family: 2.3~2.7V
- Low Data Retention Voltage : 2V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2 -400F

GENERAL DESCRIPTION

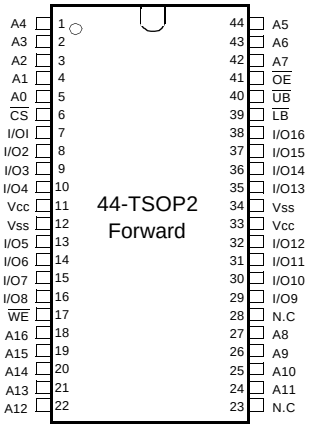
The K6T2016S3M families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and small package for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Produc Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2},Max)	
K6T2016S3M-B	Commercial(0~70°C)	2.3~2.7V	120[1]/150ns	10μA	45mA	44-TSOP2-F
K6T2016S3M-F	Industrial(-40~85°C)			15μA		

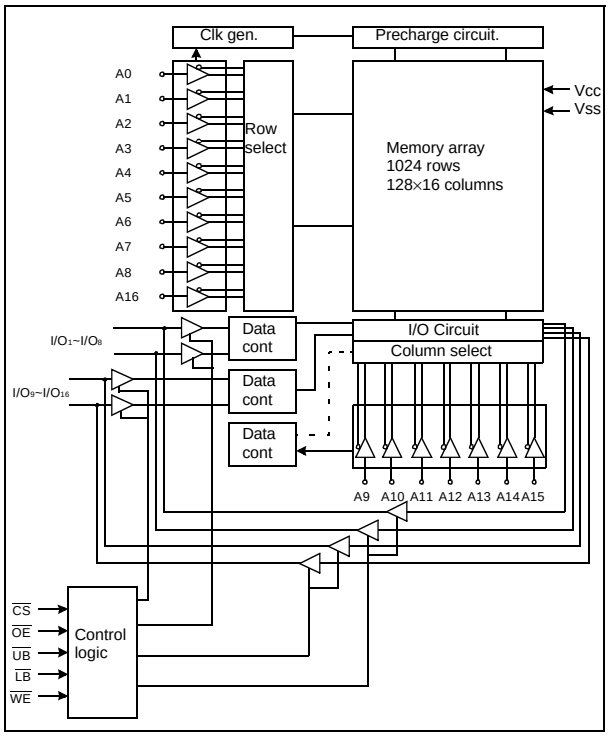
1. The parameter is measured with 30pF test load.

PIN DESCRIPTION



Name	Function	Name	Function
$\overline{CS}$	Chip Select Input	I/O_1~I/O_{16}	Data Inputs/Outputs
$\overline{OE}$	Output Enable Input	A_0~A_{16}	Address Inputs
$\overline{WE}$	Write Enable Input	Vcc	Power
$\overline{UB}$	Upper Block Select Input	Vss	Ground
$\overline{LB}$	Lower Block Select Input	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



PRODUCT LIST

Commercial Temperature Product(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
K6T2016S3M-TB12 K6T2016S3M-TB15	44-TSOP2, 120ns, 2.3~2.7V, LL 44-TSOP2, 150ns, 2.3~2.7V, LL	K6T2016S3M-TF12 K6T2016S3M-TF15	44-TSOP2, 120ns, 2.3~2.7V, LL 44-TSOP2, 150ns, 2.3~2.7V, LL

Note : LL - Low Low Standby Current

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	$\overline{LB}$	$\overline{UB}$	I/O1~8	I/O9~16	Mode	Power
H	X[1)]	X[1)]	X[1)]	X[1)]	High-Z	High-Z	Deselected	Standby
L	H	H	X[1)]	X[1)]	High-Z	High-Z	Output Disabled	Active
L	X[1)]	X[1)]	H	H	High-Z	High-Z	Output Disabled	Active
L	L	H	L	H	Dout	High-Z	Lower Byte Read	Active
L	L	H	H	L	High-Z	Dout	Upper Byte Read	Active
L	L	H	L	L	Dout	Dout	Word Read	Active
L	X[1)]	L	L	H	Din	High-Z	Lower Byte Write	Active
L	X[1)]	L	H	L	High-Z	Din	Upper Byte Write	Active
L	X[1)]	L	L	L	Din	Din	Word Write	Active

1. X means don't care. (Must be in low or high state)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	1.0	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6T2016S3M-L
		-40 to 85	°C	K6T2016S3M-P
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	K6T2016S3M Family	2.3	2.5	2.7	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	K6T2016S3M Family	2.0	-	Vcc+0.3[2)]	V
Input low voltage	V_{IL}	K6T2016S3M Family	-0.3[3)]	-	0.6	V

Note:
1. Commercial Product : T_A=0 to 70°C, otherwise specified
   Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : Vcc+1.0V in case of pulse width ≤ 20ns
3. Undershoot : -1.0V in case of pulse width ≤ 20ns
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	8	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	10	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply current	I_{CC}	I_{IO}=0mA, $\overline{CS}$=V_{IL}, V_{IN}=V_{IL} or V_{IH}, Read		-	-	5	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty I_{IO}=0mA, $\overline{CS}$≤0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V	Read	-	-	5	mA
			Write	-	-	20	
	I_{CC2}	Cycle time=Min, 100% duty		-	-	45	mA
Output low voltage	V_{OL}	I_{OL}=0.5mA at 2.3~2.7V		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-0.5mA		2.0	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS}$=V_{IH}, Other inputs=V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc		-	-	10[1)]	µA

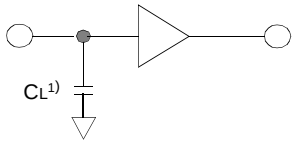
1. K6T2016S3M-I Family =15µA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V
Output load (See right) : C_L=100pF+1TTL
C_L[1)]=30pF+1TTL

1. Refer to AC CHARACTERISTICS



1. Including scope and jig capacitance

AC CHARACTERISTICS (V_{CC}=2.3~2.7V, K6T2016S3M-L Family : T_A=0 to 70°C, K6T2016S3M-I Family : T_A=-40 to 85°C)

Parameter List		Symbol	Speed Bins				Units
			120[1)]ns		150ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	120	-	150	-	ns
	Address access time	t_{AA}	-	120	-	150	ns
	Chip select to output	t_{CO}	-	120	-	150	ns
	Output enable to valid output	t_{OE}	-	60	-	75	ns
	Byte enable to valid output	t_{BA}	-	60	-	75	ns
	Chip select to low-Z output	t_{LZ}	20	-	20	-	ns
	Output enable to low-Z output	t_{OLZ}	10	-	10	-	ns
	$\overline{UB}$, $\overline{LB}$ enable to low-Z output	t_{BLZ}	10	-	10	-	ns
	Output hold from address change	t_{OH}	15	-	15	-	ns
	Chip disable to high-Z output	t_{HZ}	-	35	0	40	ns
	Output disable to high-Z output	t_{OHZ}	-	35	0	40	ns
	$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	-	35	0	40	ns
Write	Write cycle time	t_{WC}	120	-	150	-	ns
	Chip select to end of write	t_{CW}	100	-	120	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	100	-	120	-	ns
	$\overline{UB}$, $\overline{LB}$ valid to end of write	t_{BW}	100	-	120	-	ns
	Write pulse width	t_{WP}	80	-	100	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	30	0	40	ns
	Data to write time overlap	t_{DW}	50	-	60	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

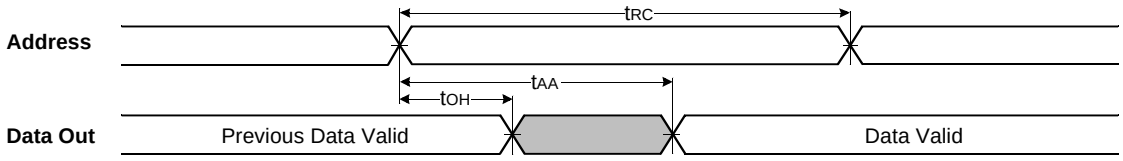
1. The parameter is measured with 30pF test load.

DATA RETENTION CHARACTERISTICS

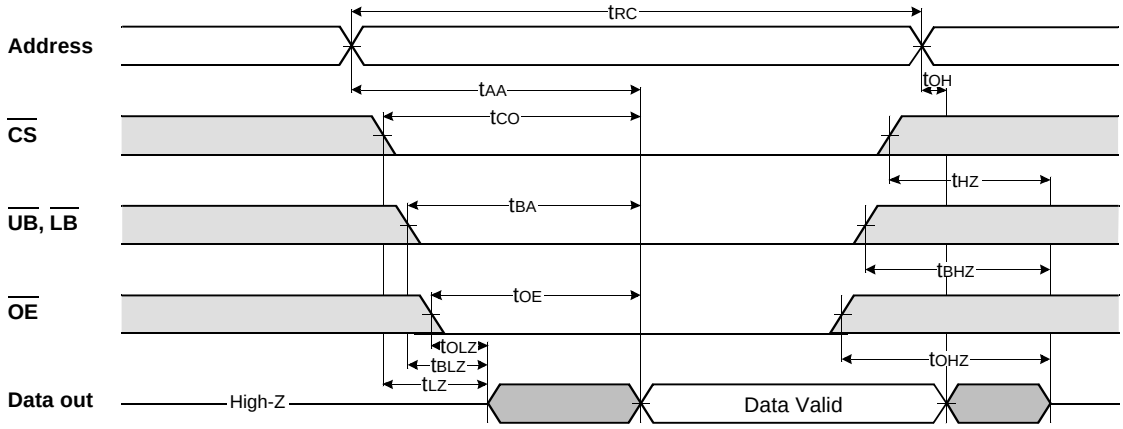
Item	Symbol	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS}$≥Vcc-0.2V	2.0	-	2.7	V
Data retention current	I_{DR}	Vcc=2.0V, $\overline{CS}$≥Vcc-0.2V	-	-	10	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH}, $\overline{UB}$ or/and $\overline{LB}$=V_{IL})



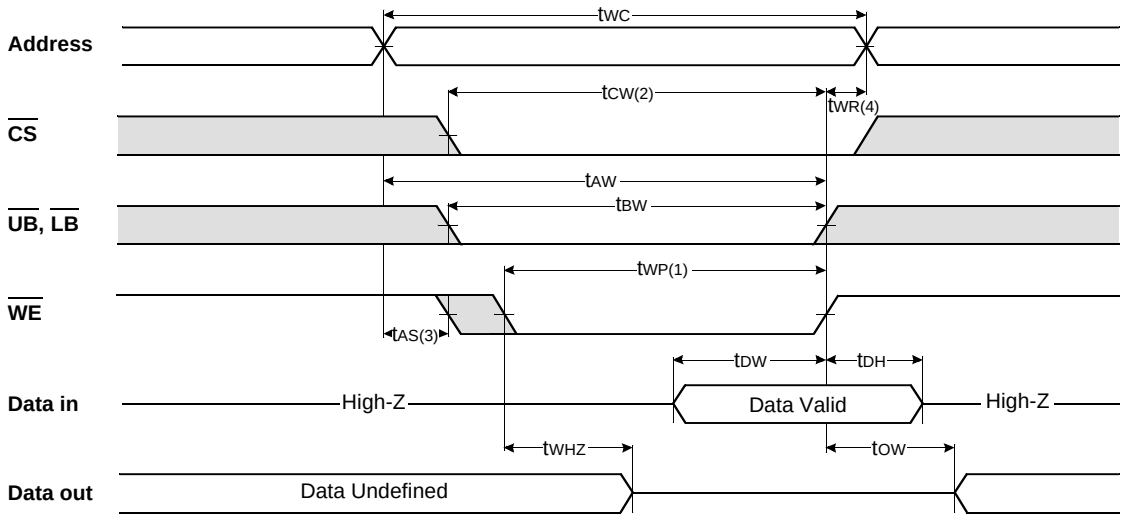
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



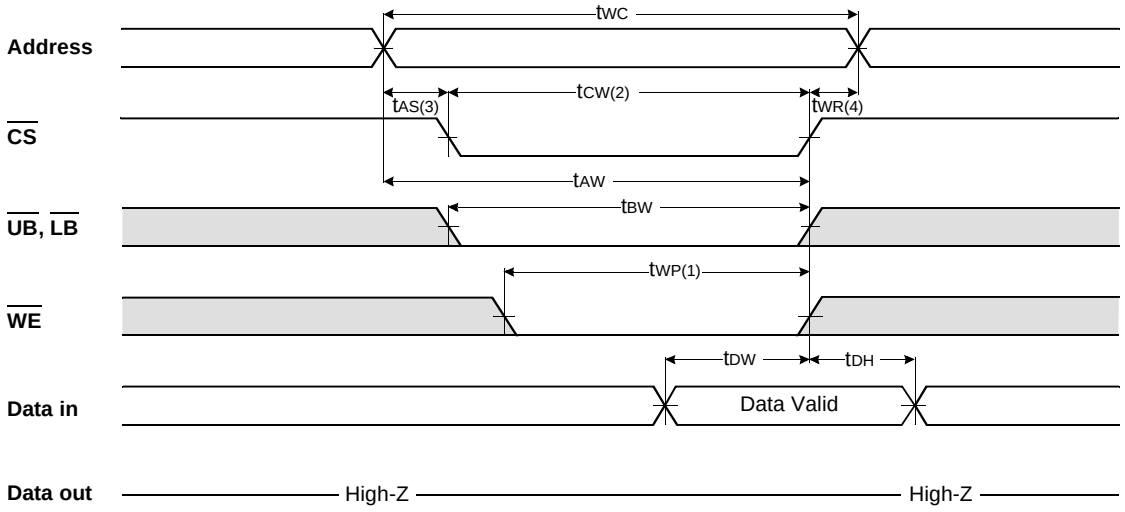
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

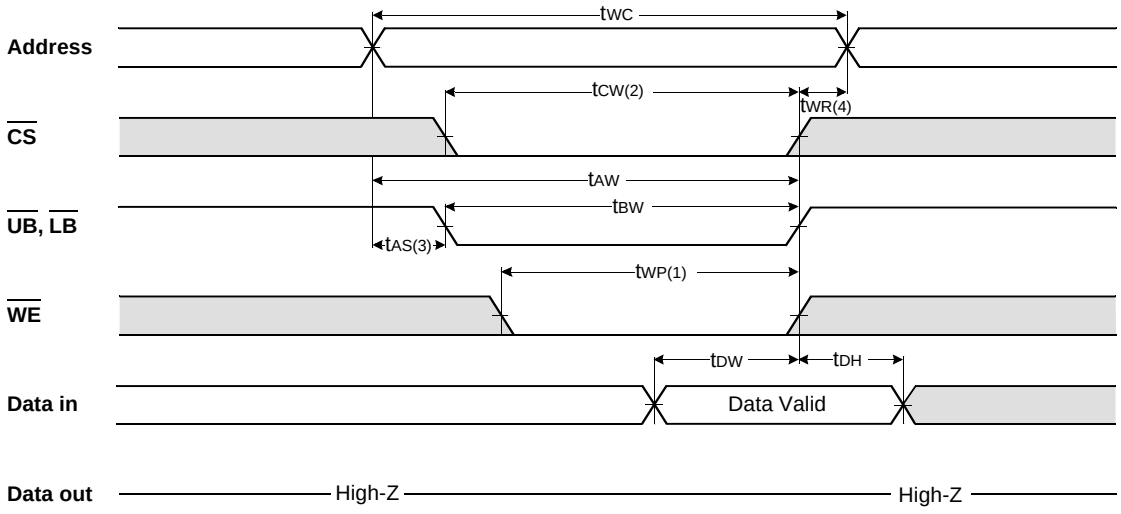
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) ($\overline{UB}$, $\overline{LB}$ Controlled)

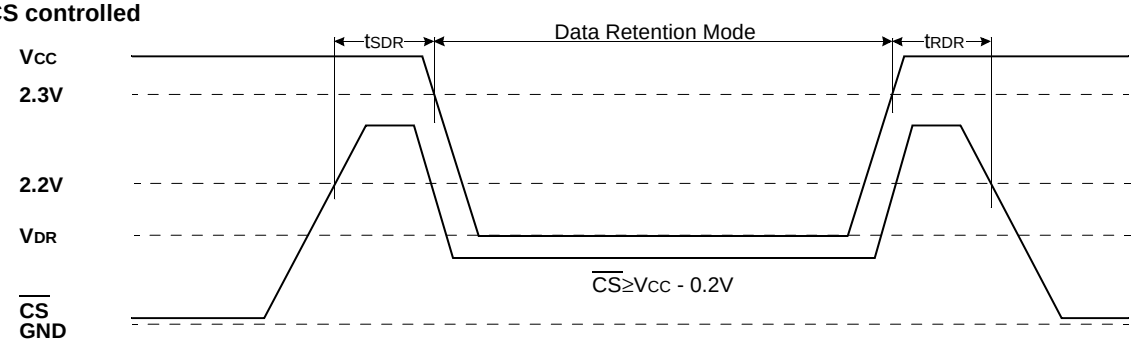


NOTES (WRITE CYCLE)

1. A write occurs during the overlap(t_{WP}) of low $\overline{CS}$ and low $\overline{WE}$. A write begins when $\overline{CS}$ goes low and $\overline{WE}$ goes low with asserting $\overline{UB}$ or $\overline{LB}$ for single byte operation or simultaneously asserting $\overline{UB}$ and $\overline{LB}$ for double byte operation. A write ends at the earliest transition when $\overline{CS}$ goes high and $\overline{WE}$ goes high. The t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS}$ going low to end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end or write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.

DATA RETENTION WAVE FORM

$\overline{CS}$ controlled



PACKAGE DIMENSIONS

Unit : millimeter(inch)

44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)