## Document Title

**1Mx8 bit Low Power and Low Voltage CMOS Static RAM**

## Revision History

| Revision No. | History | Draft Date | Remark |
|---|---|---|---|
| 0.0 | Initial draft | June 22, 1999 | Advance |
| 1.0 | Finalize<br>- Adopt New Code system.<br>- Improve $V_{IN}$, $V_{OUT}$ max. on 'ABSOLUTE MAXIMUM RATINGS' from 7.0V to $V_{CC}$+0.5V.<br>- Change Icc: from 12 to 10mA<br>- Change Icc1: from 10 to 12mA | February 29, 2000 | Final |

## *1Mx8 bit Low Power and Low Voltage CMOS Static RAM*

### FEATURES

- Process Technology: TFT
- Organization: 1M x8
- Power Supply Voltage: 4.5~5.5V
- Low Data Retention Voltage: 2.0V(Min)
- Three state output and TTL Compatible
- Package Type: 44-TSOP2-400F/R

### GENERAL DESCRIPTION

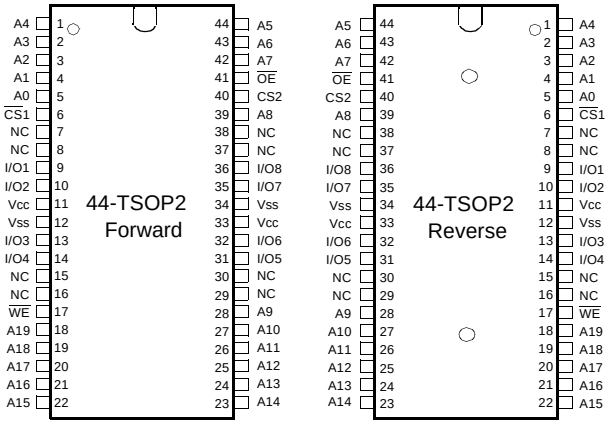
The K6T8008C2M families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support industrial operating temperature ranges for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

### PRODUCT FAMILY

| Product Family | Operating Temperature | Vcc Range | Speed | Power Dissipation | | PKG Type |
|---|---|---|---|---|---|---|
| | | | | Standby ($I_{SB1}$, Max) | Operating ($I_{CC2}$, Max) | |
| K6T8008C2M-B | Commercial(0~70°C) | 4.5~5.5V | 55[1]/70ns | 50µA | 70mA | 44-TSOP2-400F/R |
| K6T8008C2M-F | Industrial(-40~85°C) | | | 80µA | | |

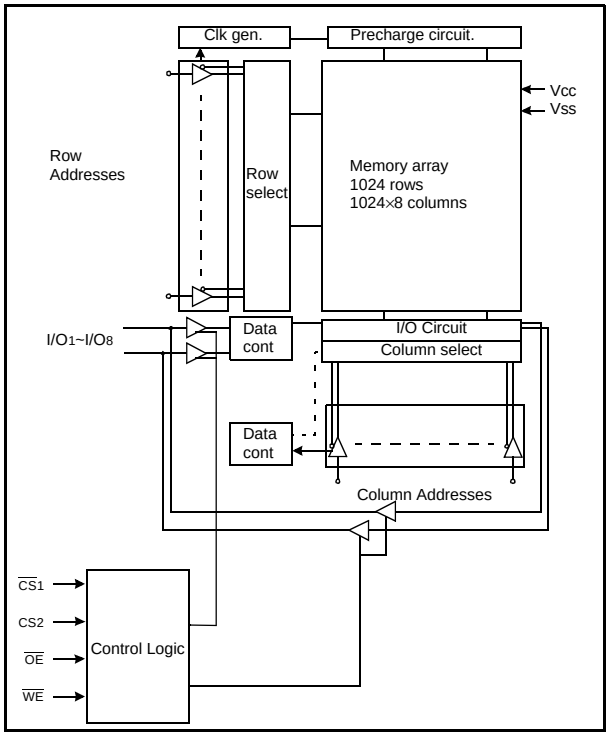
1. The parameter is measured with 50pF test load.

### PIN DESCRIPTION




| Name | Function | Name | Function |
|---|---|---|---|
| $\overline{CS}_1$, $CS_2$ | Chip Select Inputs | Vcc | Power |
| $\overline{OE}$ | Output Enable Input | Vss | Ground |
| $\overline{WE}$ | Write Enable Input | $A_0$~$A_{19}$ | Address Inputs |
| $I/O_1$~$I/O_8$ | Data Inputs/Outputs | NC | No Connect |

### FUNCTIONAL BLOCK DIAGRAM



## PRODUCT LIST

| Commercial Temperature Products(0~70°C) | | Industrial Temperature Products(-40~85°C) | |
|---|---|---|---|
| **Part Name** | **Function** | **Part Name** | **Function** |
| K6T8008C2M-TB55 | 44-TSOP2-F, 55ns, 5.0V, LL | K6T8008C2M-TF55 | 44-TSOP2-F, 55ns, 5.0V, LL |
| K6T8008C2M-TB70 | 44-TSOP2-F, 70ns, 5.0V, LL | K6T8008C2M-TF70 | 44-TSOP2-F, 70ns, 5.0V, LL |
| K6T8008C2M-RB55 | 44-TSOP2-R, 55ns, 5.0V, LL | K6T8008C2M-RF55 | 44-TSOP2-R, 55ns, 5.0V, LL |
| K6T8008C2M-RB70 | 44-TSOP2-R, 70ns, 5.0V, LL | K6T8008C2M-RF70 | 44-TSOP2-R, 70ns, 5.0V, LL |

## FUNCTIONAL DESCRIPTION

| $\overline{CS_1}$ | $CS_2$ | $\overline{OE}$ | $\overline{WE}$ | $I/O_{1\sim8}$ | Mode | Power |
|---|---|---|---|---|---|---|
| H | X | X | X | High-Z | Deselected | Standby |
| X | L | X | X | High-Z | Deselected | Standby |
| L | H | H | H | High-Z | Output Disabled | Active |
| L | H | L | H | Dout | Read | Active |
| L | H | X | L | Din | Write | Active |

Note: X means don't care. (Must be low or high state)

## ABSOLUTE MAXIMUM RATINGS[1)]

| Item | Symbol | Ratings | Unit | Remark |
|---|---|---|---|---|
| Voltage on any pin relative to Vss | $V_{IN}$, $V_{OUT}$ | -0.5 to $V_{CC}$+0.5V | V | - |
| Voltage on Vcc supply relative to Vss | $V_{CC}$ | -0.3 to 7.0 | V | - |
| Power Dissipation | $P_D$ | 1.0 | W | - |
| Storage temperature | $T_{STG}$ | -65 to 150 | °C | - |
| Operating Temperature | $T_A$ | 0 to 70 | °C | K6T8008C2M-B |
| | | -40 to 85 | °C | K6T8008C2M-F |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## RECOMMENDED DC OPERATING CONDITIONS[1)]

| Item | Symbol | Product | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Supply voltage | Vcc | K6T8008C2M Family | 4.5 | 5.0 | 5.5 | V |
| Ground | Vss | All Family | 0 | 0 | 0 | V |
| Input high voltage | $V_{IH}$ | K6T8008C2M Family | 2.2 | - | Vcc+0.5[2)] | V |
| Input low voltage | $V_{IL}$ | K6T8008C2M Family | -0.5[3)] | - | 0.8 | V |

Note:
1. Commercial Product: $T_A$=0 to 70°C, otherwise specified.
   Industrial Product: $T_A$=-40 to 85°C, otherwise specified.
2. Overshoot: $V_{CC}$+3.0V in case of pulse width ≤30ns.
3. Undershoot: -3.0V in case of pulse width ≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE[1)] (f=1MHz, $T_A$=25°C)

| Item | Symbol | Test Condition | Min | Max | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$=0V | - | 8 | pF |
| Input/Output capacitance | $C_{IO}$ | $V_{IO}$=0V | - | 10 | pF |

1. Capacitance is sampled, not 100% tested.

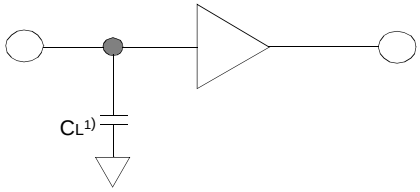
## DC AND OPERATING CHARACTERISTICS

| Item | Symbol | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Input leakage current | $I_{LI}$ | $V_{IN}$=Vss to Vcc | | -1 | - | 1 | µA |
| Output leakage current | $I_{LO}$ | $\overline{CS_1}$=$V_{IH}$, $CS_2$=$V_{IL}$ or $\overline{OE}$=$V_{IH}$ or $\overline{WE}$=$V_{IL}$, $V_{IO}$=Vss to Vcc | | -1 | - | 1 | µA |
| Operating power supply current | $I_{CC}$ | $I_{IO}$=0mA, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $\overline{WE}$=$V_{IH}$, $V_{IN}$=$V_{IH}$ or $V_{IL}$ | | - | - | 10 | mA |
| Average operating current | $I_{CC1}$ | Cycle time=1µs, 100%duty, $I_{IO}$=0mA, $\overline{CS_1}$≤0.2V, $CS_2$≥Vcc-0.2V, $V_{IN}$≤0.2V or $V_{IN}$≥Vcc-0.2V | | - | - | 12 | mA |
| | $I_{CC2}$ | Cycle time=Min, $I_{IO}$=0mA, 100% duty, $\overline{CS_1}$=$V_{IL}$, $CS_2$=$V_{IH}$, $V_{IN}$=$V_{IL}$ or $V_{IH}$ | | - | - | 70 | mA |
| Output low voltage | $V_{OL}$ | $I_{OL}$ = 2.1mA | | - | - | 0.4 | V |
| Output high voltage | $V_{OH}$ | $I_{OH}$ = -1.0mA | | 2.4 | - | - | V |
| Standby Current(TTL) | $I_{SB}$ | $\overline{CS_1}$=$V_{IH}$, $CS_2$=$V_{IL}$, Other inputs=$V_{IH}$ or $V_{IL}$ | | - | - | 3 | mA |
| Standby Current(CMOS) | $I_{SB1}$ | $\overline{CS}$≥Vcc-0.2V, Other inputs=0~Vcc | K6T8008C2M-B | - | - | 50 | µA |
| | | | K6T8008C2M-F | - | - | 80 | |

## AC OPERATING CONDITIONS

**TEST CONDITIONS**(Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
Input rising and falling time: 5ns
Input and output reference voltage: 1.5V
Output load(see right): $C_L$=100pF+1TTL
$C_L$=50pF+1TTL




1.Including scope and jig capacitance

## AC CHARACTERISTICS ($V_{CC}$=4.5~5.5V, Commercial product: $T_A$=0 to 70°C, Industrial product: $T_A$=-40 to 85°C)

| Parameter List | | Symbol | Speed Bins | | | | Units |
|---|---|---|---|---|---|---|---|
| | | | 55ns | | 70ns | | |
| | | | Min | Max | Min | Max | |
| Read | Read Cycle Time | $t_{RC}$ | 55 | - | 70 | - | ns |
| | Address Access Time | $t_{AA}$ | - | 55 | - | 70 | ns |
| | Chip Select to Output | $t_{CO}$ | - | 55 | - | 70 | ns |
| | Output Enable to Valid Output | $t_{OE}$ | - | 25 | - | 35 | ns |
| | Chip Select to Low-Z Output | $t_{LZ}$ | 10 | - | 10 | - | ns |
| | Output Enable to Low-Z Output | $t_{OLZ}$ | 5 | - | 5 | - | ns |
| | Chip Disable to High-Z Output | $t_{HZ}$ | 0 | 20 | 0 | 25 | ns |
| | Output Disable to High-Z Output | $t_{OHZ}$ | 0 | 20 | 0 | 25 | ns |
| | Output Hold from Address Change | $t_{OH}$ | 10 | - | 10 | - | ns |
| Write | Write Cycle Time | $t_{WC}$ | 55 | - | 70 | - | ns |
| | Chip Select to End of Write | $t_{CW}$ | 45 | - | 60 | - | ns |
| | Address Set-up Time | $t_{AS}$ | 0 | - | 0 | - | ns |
| | Address Valid to End of Write | $t_{AW}$ | 45 | - | 60 | - | ns |
| | Write Pulse Width | $t_{WP}$ | 40 | - | 50 | - | ns |
| | Write Recovery Time | $t_{WR}$ | 0 | - | 0 | - | ns |
| | Write to Output High-Z | $t_{WHZ}$ | 0 | 20 | 0 | 20 | ns |
| | Data to Write Time Overlap | $t_{DW}$ | 25 | - | 30 | - | ns |
| | Data Hold from Write Time | $t_{DH}$ | 0 | - | 0 | - | ns |
| | End Write to Output Low-Z | $t_{OW}$ | 5 | - | 5 | - | ns |

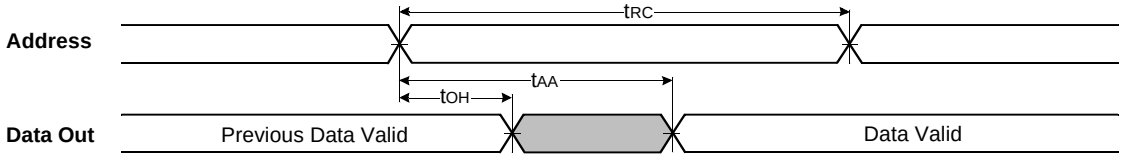
## DATA RETENTION CHARACTERISTICS

| Item | Symbol | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Vcc for data retention | $V_{DR}$ | $\overline{CS_1}$≥Vcc-0.2V1) | 2.0 | - | 5.5 | V |
| Data retention current | $I_{DR}$ | Vcc=3.0V, $\overline{CS_1}$≥Vcc-0.2V1) | - | - | 202) | µA |
| Data retention set-up time | $t_{SDR}$ | See data retention waveform | 0 | - | - | ms |
| Recovery time | $t_{RDR}$ | | 5 | - | - | |

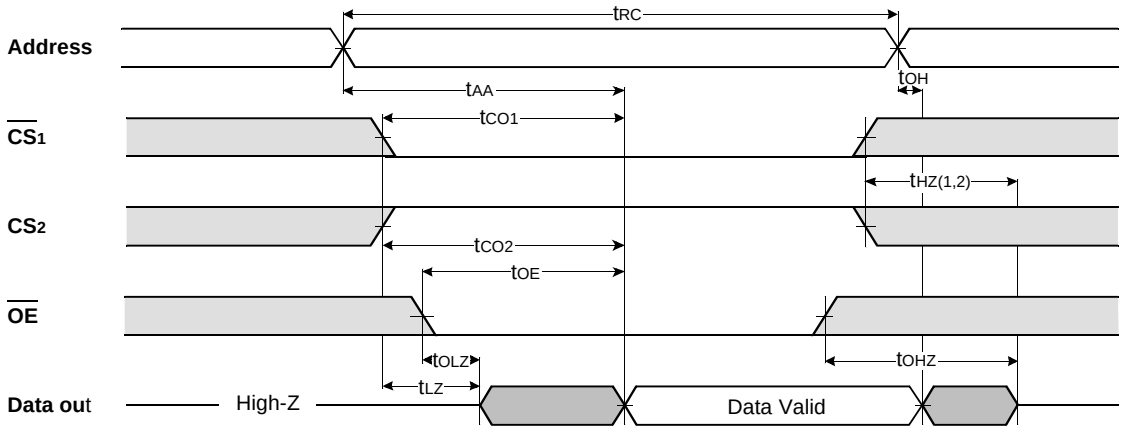
1. $\overline{CS_1}$≥Vcc-0.2V,$CS_2$≥Vcc-0.2V($\overline{CS_1}$ controlled) or $CS_2$≥Vcc-0.2V($CS_2$ controlled).
2. Industrial product=30µA

## TIMING DIAGRAMS

### TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=$V_{IL}$, $CS_2$=$\overline{WE}$=$V_{IH}$)



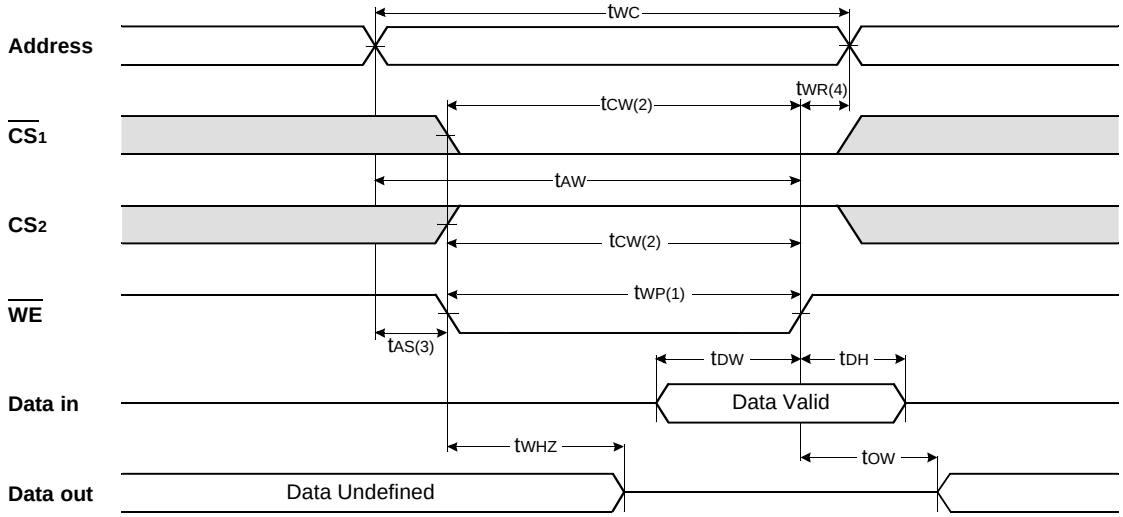

### TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=$V_{IH}$)



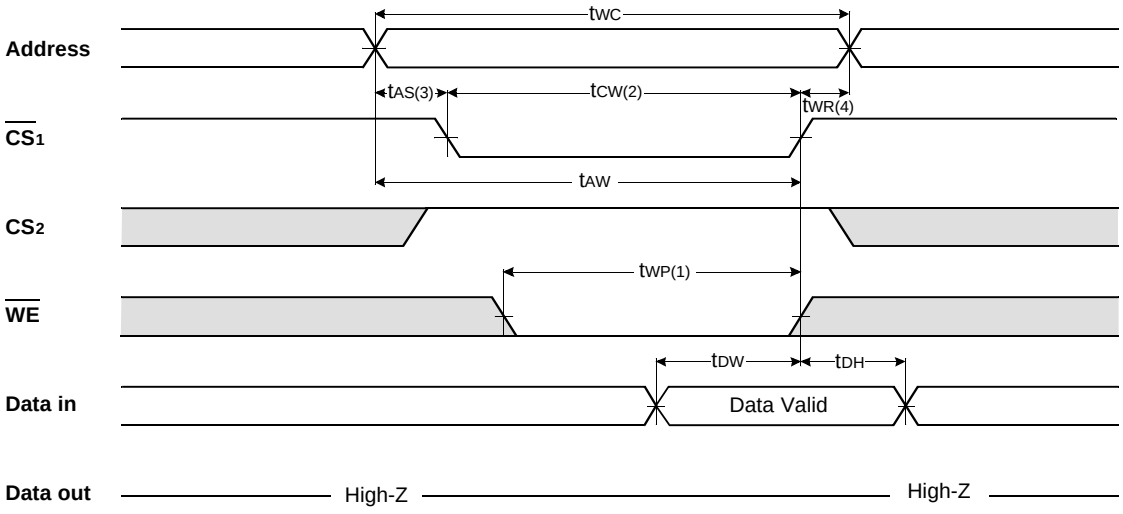

**NOTES** (READ CYCLE)

1. $t_{HZ}$ and $t_{OHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}$(Max.) is less than $t_{LZ}$(Min.) both for a given device and from device to device interconnection.

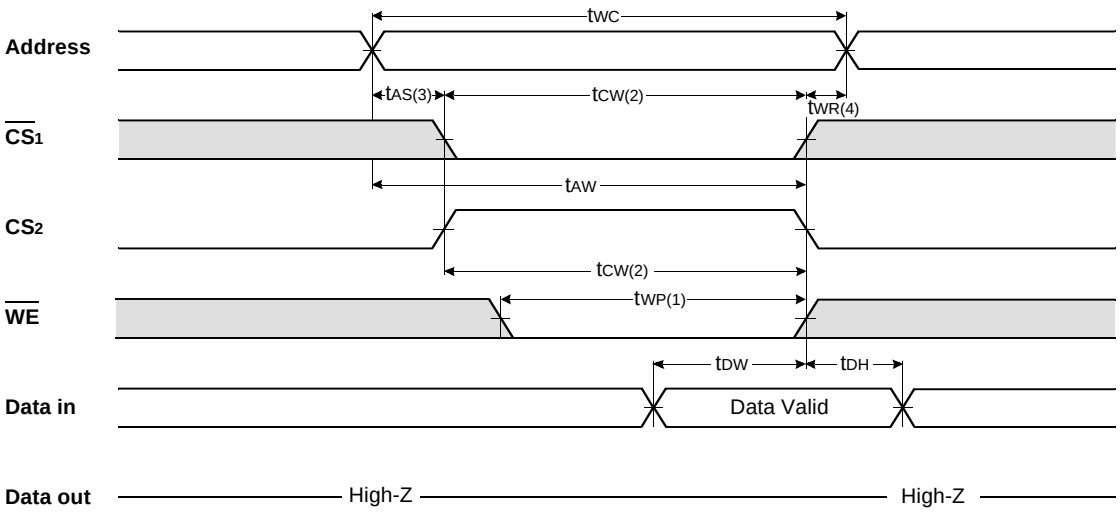
**TIMING WAVEFORM OF WRITE CYCLE(1)** ($\overline{WE}$ Controlled)




**TIMING WAVEFORM OF WRITE CYCLE(2)** ($\overline{CS_1}$ Controlled)



**TIMING WAVEFORM OF WRITE CYCLE(3)** ($CS_2$ Controlled)

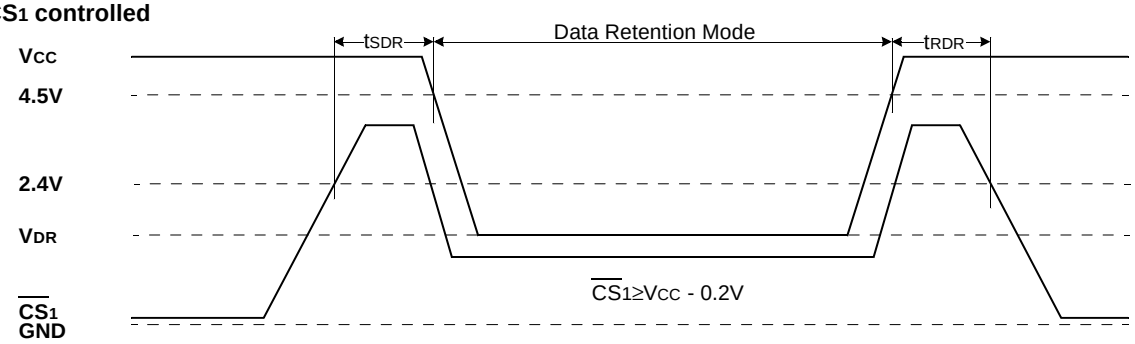



**NOTES** (WRITE CYCLE)

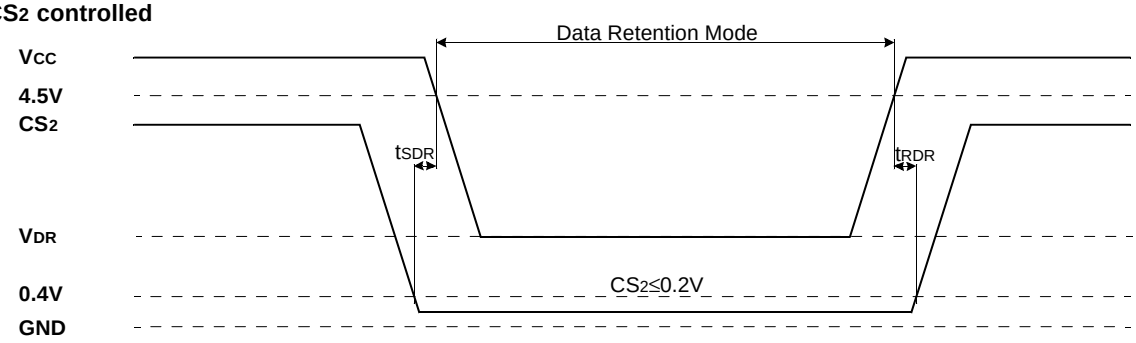
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high $CS_2$ and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, $CS_2$ going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, $CS_2$ going low and $\overline{WE}$ going high, $t_{WP}$ is measured from the begining of write to the end of write.
2. $t_{CW}$ is measured from the $\overline{CS_1}$ going low or $CS_2$ going high to the end of write.
3. $t_{AS}$ is measured from the address valid to the beginning of write.
4. $t_{WR}$ is measured from the end of write to the address change. $t_{WR}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR2}$ applied in case a write ends as $CS_2$ going to low.

## DATA RETENTION WAVE FORM

**$\overline{CS_1}$ controlled**



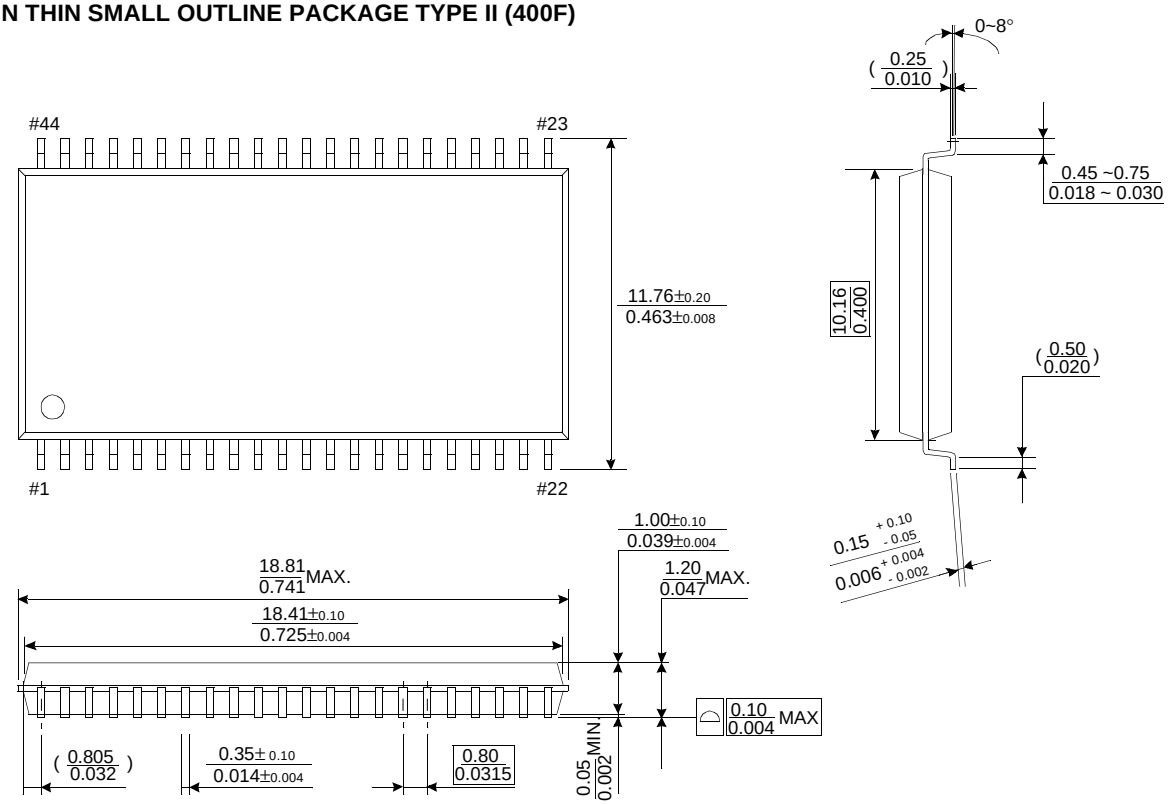

**$CS_2$ controlled**



## PACKAGE DIMENSIONS

Unit: millimeters(inches)

### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400F)




### 44 PIN THIN SMALL OUTLINE PACKAGE TYPE II (400R)