E4/STM-1/OC-3 ATM INTERFACE CIRCUITS S3015/S3016

FEATURES

- Complies with ANSI, Bellcore, and ITU-T specifications
- On-chip high-frequency PLL for clock generation and clock recovery
- On-chip analog circuitry for transformer driver and equalization
- Supports 139.264 Mbit/s (E4) and 155.52 Mbit/s (OC-3) transmission rates
- Supports 139.264 Mbit/s and 155.52 Mbit/s Coded Mark Inversion (CMI) interfaces
- Reference frequencies of 19.44 (OC-3) or 17.408 MHz (E4)
- Interface to both PECL and TTL logic
- Lock detect on clock recovery device
- Low jitter PECL interface
- 1.6W total typ power
- +5V only power supply
- Small 52 PQFP TEP package
- Supports both electrical and optical interfaces

APPLICATIONS

- ATM over SONET
- OC-3/STM-1 or E4-based transmission systems
- OC-3/STM-1 or E4 modules
- OC-3/STM-1 or E4 test equipment
- Section repeaters
- Add drop multiplexors
- Broadband cross-connects
- Fiber optic terminators
- Fiber optic test equipment

GENERAL DESCRIPTION

The S3015 transmitter and S3016 receiver derive high speed timing signals for SONET/SDH or PDH–based equipment. These circuits are implemented using AMCC's proven Phase Locked Loop (PLL) technology. Figures 1a and 1b show typical network applications.

The S3015 and S3016 each have an on-chip VCO which can be synchronized directly to the incoming data stream. The chipset can be used with a 19.44 MHz reference clock when operated in the SONET/SDH OC-3 mode. In E4 mode the chipset can be operated with a 17.408 MHz reference clock in support of existing system clocking schemes. On-chip coded-mark-inversion (CMI) encoding and decoding is provided for 139.264 Mbit/s and 155.52 Mbit/s interfaces.

The low jitter PECL interface guarantees compliance with the bit-error rate requirements of the Bellcore, ANSI, and ITU-T standards. The S3015/S3016 chipset is packaged in a .65mm pitch, compact 52-pin PQFP, offering designers a small package outline.

The S3015 and S3016 provide the major components on-chip for a coaxial cable interface, including analog transformer driver circuitry and equalization interface circuitry.

Figure 1a. Electrical Interface

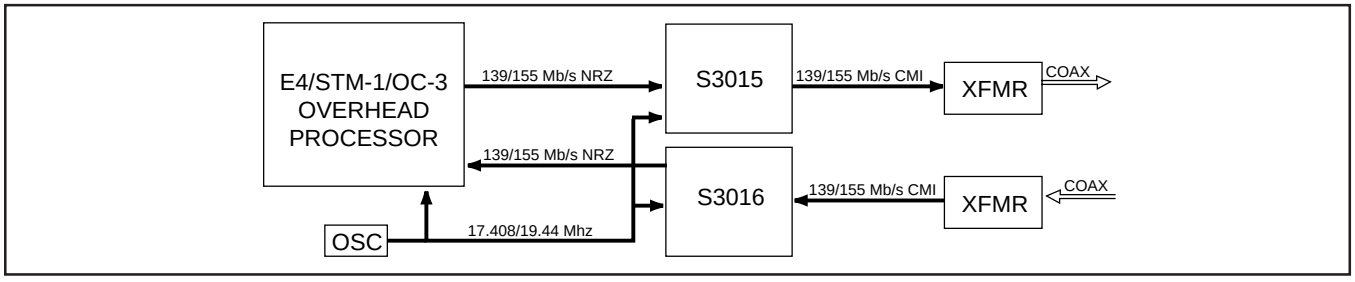
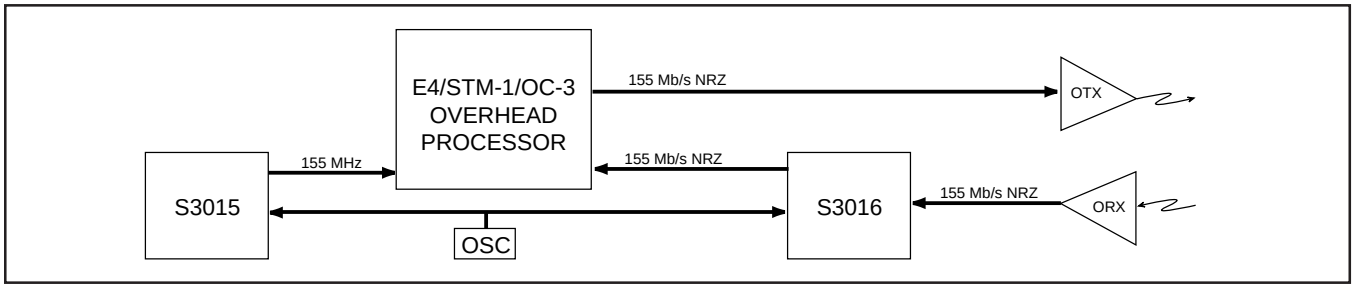


Figure 1b. Optical Interface



SONET/SDH OVERVIEW

Synchronous Optical Network (SONET) is a standard for connecting one fiber system to another at the optical level. SONET, together with the Synchronous Digital Hierarchy (SDH) administered by the ITU-T, form a single international standard for fiber interconnect between telephone networks of different countries. SONET is capable of accommodating a variety of transmission rates and applications.

The SONET standard is a layered protocol with four separate layers defined. These are:

- Photonic
- Section
- Line
- Path

Figure 2 shows the layers and their functions. Each of the layers has overhead bandwidth dedicated to administration and maintenance. The photonic layer simply handles the conversion from electrical to optical and back with no overhead. It is responsible for transmitting the electrical signals in optical form over the physical media. The section layer handles the transport of the framed electrical signals across the optical cable from one end to the next. Key functions of this layer are framing, scrambling, and error monitoring. The line layer is responsible for the reliable transmission of the path layer information stream carrying voice, data, and video signals. Its main functions are synchronization, multiplexing, and reliable transport. The path layer is responsible for the actual transport of services at the appropriate signaling rates.

Data Rates and Signal Hierarchy

Table 1 contains the data rates and signal designations of the SONET hierarchy. The lowest level is the basic SONET signal referred to as the synchronous transport signal level-1 (STS-1). An STS-*N* signal is made up of *N* byte-interleaved STS-1 signals. The optical counterpart of each STS-*N* signal is an optical carrier level-*N* signal (OC-*N*). The S3015/S3016 chipset supports OC-3 rates (155.52 Mbit/s).

Table 1. SONET Signal Hierarchy

Elec.	ITU-T	Optical	Data Rate (Mbit/s)
STS-1		OC-1	51.84
STS-3	STM-1	OC-3	155.52
STS-12	STM-4	OC-12	622.08
STS-24		OC-24	1244.16
STS-48	STM-16	OC-48	2488.32

Frame and Byte Boundary Detection

The SONET/SDH fundamental frame format for STS-3 consists of nine transport overhead bytes followed by Synchronous Payload Envelope (SPE) bytes. This pattern of 9 overhead and 261 SPE bytes is repeated nine times in each frame. Frame and byte boundaries are detected using the A1 and A2 bytes found in the transport overhead. (See Figure 3.)

For more details on SONET operations, refer to the ANSI SONET standard document.

Figure 3. SONET Structure

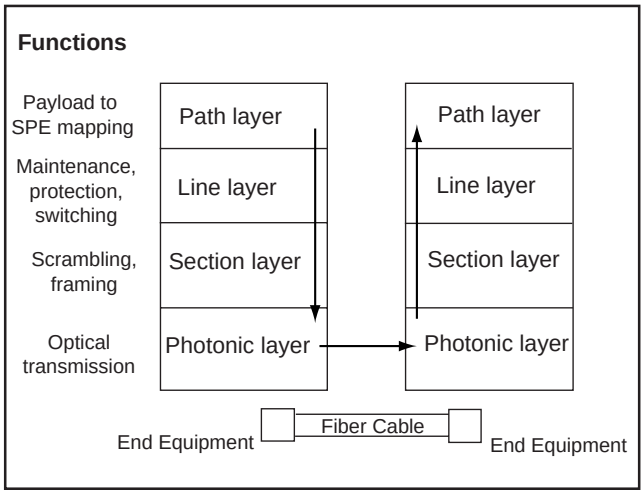
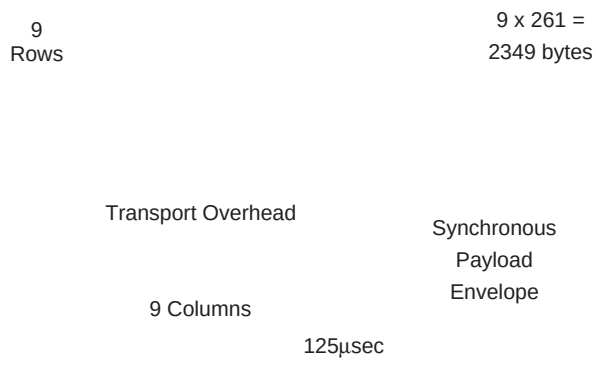


Figure 3. STS-3 Frame Format



S3015/S3016 OVERVIEW

The S3015 transmitter and the S3016 receiver can be used to implement the front end of STS-3, OC-3 or E4 equipment. The block diagrams in Figures 4 and 10 show the basic operation of both chips.

When serial data is present at the input of the transmitter, the S3015 VCO synchronizes directly to the incoming data, which is retimed for the purpose of optional CMI encoding. In the absence of incoming serial data, the S3015 operates as a clock synthesizer. In this mode, a crystal oscillator is connected to the TTL reference input and synthesized up to the 155 MHz output frequency. The S3016 receiver performs clock recovery by synchronizing its on-chip VCO directly to the incoming data stream.

The S3015 provides a PECL output for an optical interface and two transformer driver outputs for an electrical interface. One of these drivers is a monitor output. The S3016 provides a PECL input for an optical interface and an analog input for an electrical interface.

When the chipset is used in an electrical interface, the PECL output of the transmitter can be connected to the PECL input of the receiver to implement a diagnostic loopback mode for test. When the chipset is used in an optical interface, a transformer driver output of the transmitter can be connected to the analog input of the receiver to implement the loopback mode.

S3015 TRANSMITTER FUNCTIONAL DESCRIPTION

The S3015 transmitter chip performs the last stage of digital processing of a transmit SONET STS-3 or ITU-T E4 bit serial data stream. A Coded Mark Inversion (CMI) encoder can be enabled for encoding STS-3 electrical and E4 signals.

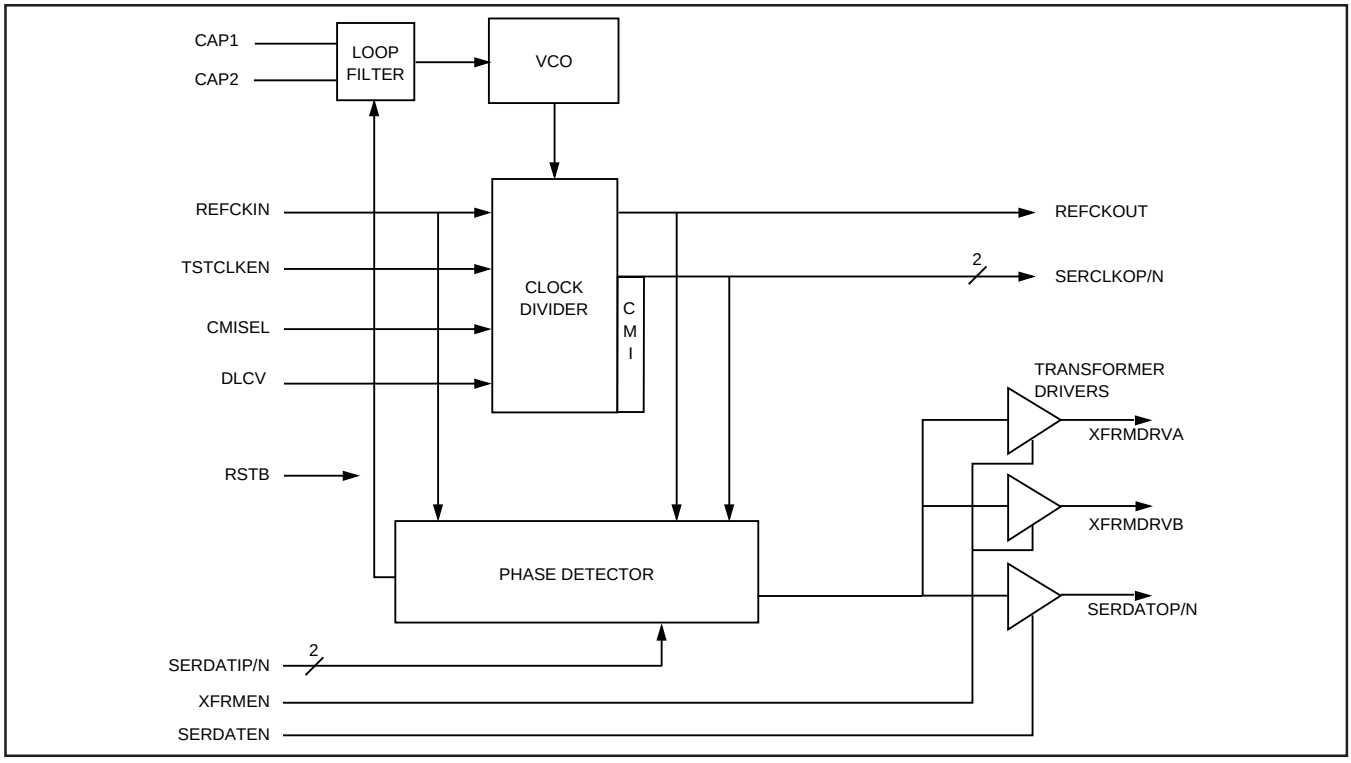
Clock Recovery

If serial data is present on the SERDATIP/N inputs, the clock is recovered from the serial data stream at 139.264 MHz or 155.52 MHz and synthesized to 278.528 MHz or 311.04 MHz to CMI encode the incoming data.

Optical and Electrical Interfaces

The digital data outputs (SERDATOP/N) are the PECL outputs for an optical interface and are to be connected to an electrical to optical converter, as shown in Figure 18. This data is also routed to two on-chip transformer drivers and sent out on XFRMDRVA and XFRMDRVB to drive the transformers of the electrical interface, as shown in Figure 20. These outputs are shut off when the reset is active, XFRMEN is active, or when the chip is in NRZ mode and the data inputs are in the logic zero state. The electrical characteristics for the transformer drivers are shown in Table 5.

Figure 4. S3015 OC3/STM-1/E4 Transmitter Functional Block Diagram



CMI Encoding

Coded Mark Inversion format (CMI) ensures at least one data transition per 1.5 bit periods, thus aiding the clock recovery process. Zeros are represented by a Low state for one half a bit period, followed by a High state for the rest of that bit period. Ones are represented by a steady Low or High state for a full bit period. The state of the ones bit period alternates at each occurrence of a one. Figure 5 shows an example of CMI-encoded data. The STS-3 electrical interface and the E4 interface are specified to have CMI-encoded data.

The CMI encoder on the S3015 accepts serial data from SERDATIP/N at 139.264 or 155.52 Mb/s. The data is then encoded into CMI format, and the result is shifted out with transitions at twice the basic data rate. The CMISEL input controls whether the CMI encoder is in the data path. A CMI code violation can be inserted for diagnostic purposes by activating the DLCV input. The DLCV input is sampled on every cycle of the serial clock to allow a single or multiple line code violations to be inserted. This violation is either an inverted zero code or an inversion of the alternating ones logic level, depending on the state of the data. Subsequent one codes take into account the induced violation to avoid error multiplication.

Jitter Generation

Jitter Generation is defined as the amount of jitter at the OC-3 or E-4 output of equipment. Jitter generation for OC-3 shall not exceed 0.01 UI rms when measured using a highpass filter with a 12 kHz cutoff frequency.

For STM-1 and E4, the jitter generated shall not exceed the specifications shown in Figure 6.

In order to meet the SONET, STM-1 E4 jitter specifications as shown in Figure 6, the SERDATIP/N serial data input must meet the jitter characteristics as shown in Figure 7.

Figure 5. CMI Encoded Data

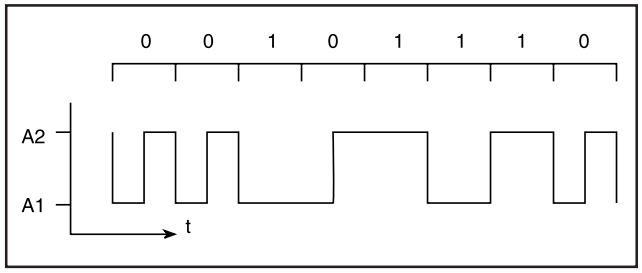
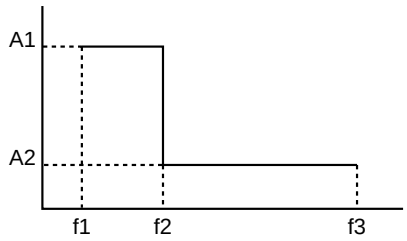


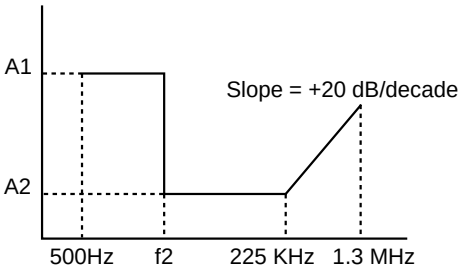
Figure 6. Jitter Generation Specifications Compliant to G.823 and G.825



	f1(Hz)	f2(KHz)	f3(MHz)	A1	A2
OC-3	—	—	—	.01(1)	.01(1)
STM-1	500	65	1.3	1.5(2)	.15(2)
E4	200	10	3.5	1.5(2)	.075(2)

1. UI rms
2. UI p–p

Figure 7. S3015 Maximum Allowable Input Jitter



	f2(KHz)	A1	A2
OC-3	—	.005(1)	.005(1)
STM-1	65	1.45(2)	.10(2)
E4	10	1.45(2)	.025(2)

1. UI rms
2. UI p–p

Figure 8. Mask of a pulse corresponding to a binary 0 Compliant to G.703

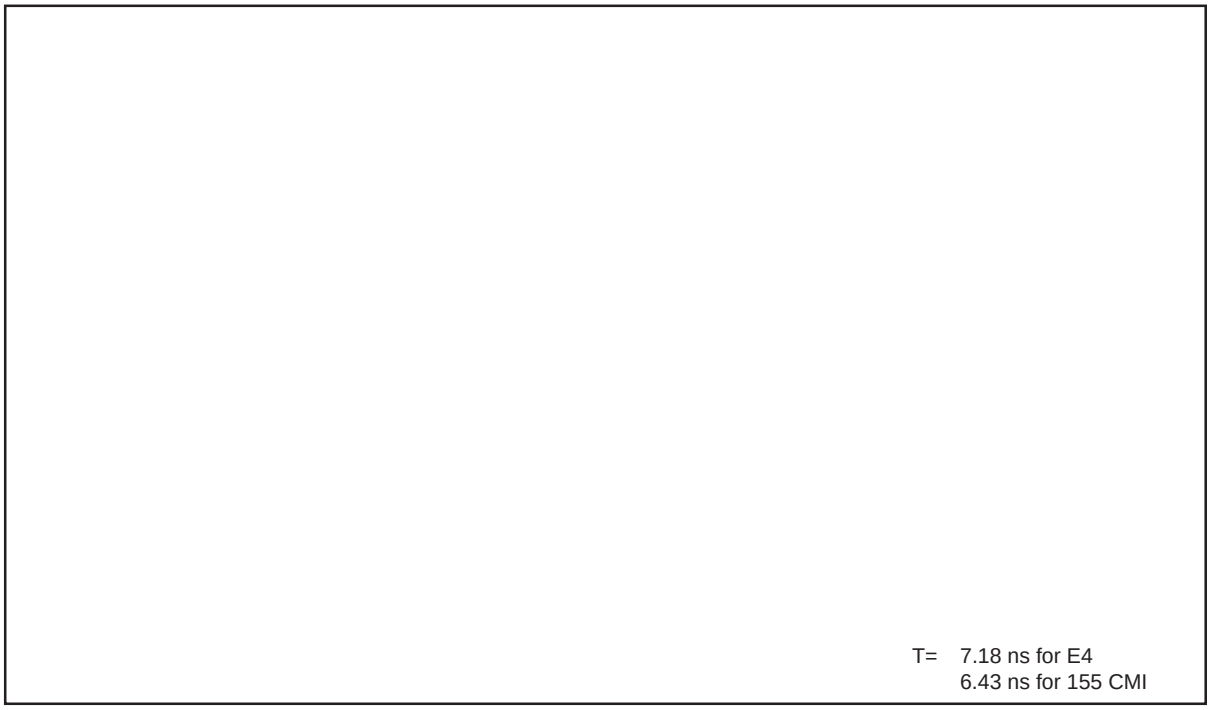
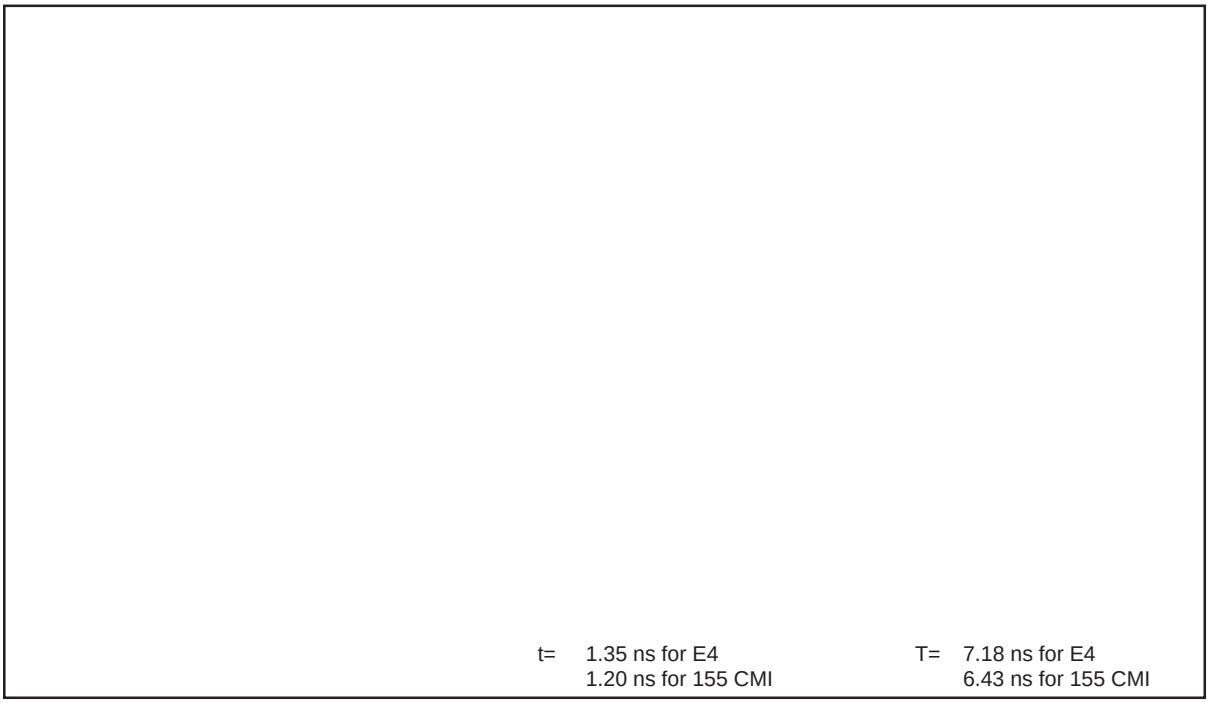


Figure 9. Mask of a pulse corresponding to a binary 1 Compliant to G.703



Notes:
1. The maximum “steady state” amplitude should not exceed the 0.55 V limit. Overshoots and other transients are permitted to fall into the dotted area, bounded by the amplitude levels 0.55 V and 0.6 V, provided that they do not exceed the steady state level by more than 0.05 V. The possibility of relaxing the amount by which the overshoot may exceed the steady state level is under study.
2. For the purpose of these masks, the rise time and decay time should be measured between -0.4 V and 0.4 V, and should not exceed 2 ns.
3. The inverse pulse in Figure 9 will have the same characteristics, noting that the timing tolerances at the zero level of the negative and positive transitions are ±0.1 ns and ±0.5 ns respectively.

S3016 RECEIVER FUNCTIONAL DESCRIPTION

The S3016 receiver provides the first stage of digital processing of a receive SONET STS-3 or ITU-T E4 serial bit stream. A Coded Mark Inversion (CMI) decoder can be enabled for decoding STS-3 electrical and E4 signals.

Clock recovery is performed on the incoming scrambled NRZ or CMI–coded data stream. A reference clock is required for phase locked loop start-up and proper operation under loss of signal conditions. An integral prescaler and phase locked loop circuit is used to multiply this reference frequency to the nominal bit rate.

Clock Recovery

The Clock Recovery function, as shown in the block diagram in Figure 10, generates a clock that is frequency matched to the incoming data baud rate at the SERDATIP/N differential inputs. The clock is phase aligned by a PLL so that it samples the data in the center of the data eye pattern.

The phase relationship between the edge transitions of the data and those of the generated clock are compared by a phase/frequency discriminator. Output pulses from the discriminator indicate the required direction of phase corrections. These pulses are smoothed by an integral loop filter. The output of the loop filter controls the frequency of the Voltage Controlled Oscillator (VCO), which generates the recovered clock. Frequency stability without incoming data is guaranteed by an alternate reference input (REFCKIN) to which the PLL locks when data is lost.

When the test clock enable (TSTCLKEN) input is set high, the clock recovery block is disabled. The reference clock (REFCKIN) is used as the bit rate clock input in place of the recovered clock. This feature is used for functional testing of the device.

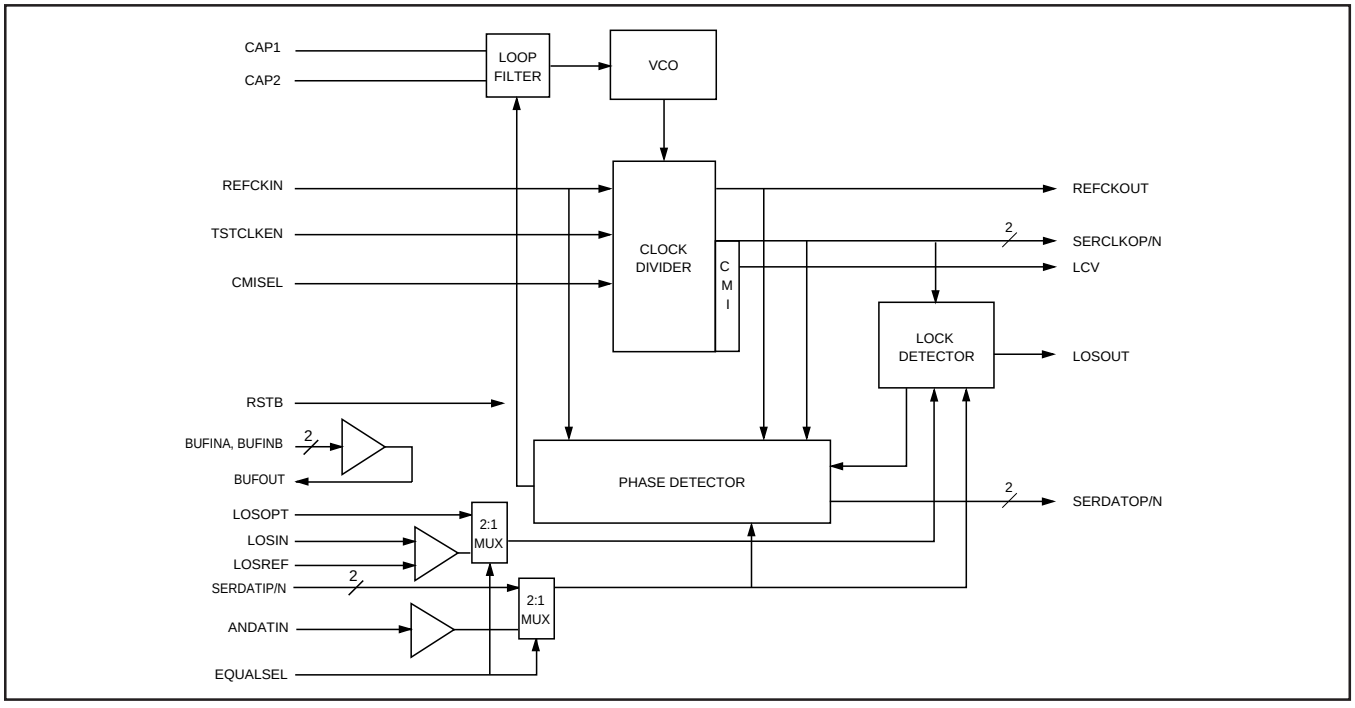
The loop filter transfer function is optimized to enable the PLL to track the jitter, yet tolerate the minimum transition density expected in a received SONET or E4 data signal. This transfer function yields a typical capture time of 16 µs for random incoming NRZ data.

The total loop dynamics of the clock recovery PLL yield a jitter tolerance which exceeds the minimum tolerance proposed for OC-3/STM-1/E4 equipment by the Bellcore and ITU-T documents, shown in Figure 13.

Optical and Electrical Interfaces

The digital data inputs (SERDATIP/N) are the PECL inputs from an optical to electrical converter, as shown in Figure 16. The data input for the coaxial interface is ANDATIN, which is the serial data input from the equalizer circuit and should be connected as shown in Figure 17. The EQUALSEL input is used to select either SERDATIP/N or ANDATIN.

Figure 10. S3016 OC-3/STM-1/E4 Receiver Functional Block Diagram



CMI Decoding

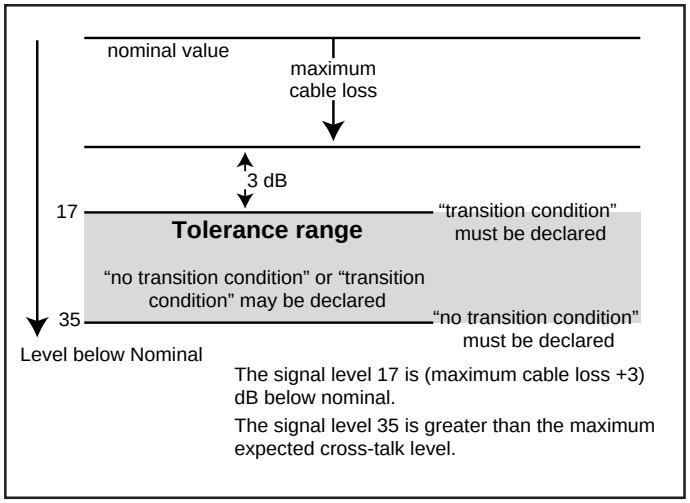
The CMI decoder block on the S3016 accepts serial data from the SERDATIP/N input at the rate of 139.264 or 155.52 Mb/s. The incoming CMI data, which has transitions that represent this data rate (the clock associated with this data would be running at twice this rate), is then decoded from CMI to NRZ format.

Loss of Signal

The clock recovery circuit monitors the incoming data stream for loss of signal. If the incoming encoded data stream has had no transitions continuously for 96 to 224 recovered clock cycles, loss of signal is declared and the PLL will switch from locking onto the incoming data to locking onto the reference clock per the requirements of G.775. Alternatively, the loss-of signal (LOSIN) input can force a loss-of-signal condition. This signal is compared internally against the LOSREF input reference voltage. This input can be set to meet the conditions shown in Figure 11. If the zero to peak signal level drops below the LOSREF/20 voltage level for more than 96 to 224 bit intervals, a loss of signal condition will be indicated on the LOSOUT pin and the PLL will change its reference from the serial data stream to the reference clock. When the peak input voltage is greater than LOSREF/10, the loss of signal condition will be deasserted and the PLL will recover the clock from the serial data inputs.

In NRZ mode, a logic low level on the LOSOPT input will cause the PLL to change its reference to the reference clock. This pin should be driven by a PECL compatible level signal detect signal from the fiber optic receiver.

Figure 11. Criteria for determination of transition conditions. Compliant to G.775.



Serial Clock Output to Data Output Timing

The serial data is clocked out on the falling edge of SERCLKOP. (See Figure 12.) This timing is valid in both NRZ and CMI modes.

Input Jitter Tolerance

Input jitter tolerance is defined as the peak to peak amplitude of sinusoidal jitter applied on the input signal that causes an equivalent 1 dB optical/electrical power penalty. OC-3 and E-4 input jitter tolerance requirements are shown in Figure 13.

The S3016 PLL complies with the minimum jitter tolerance for clock recovery proposed for SONET/SDH equipment defined by the Bellcore TA-NWT-000253 standard when used as shown in Figure 13. The S3016 PLL also complies with the minimum jitter tolerance for clock recovery as defined in the ITU-T E4 specification when used as shown in Figure 17.

Figure 12. S3016 Clock to Data Timing

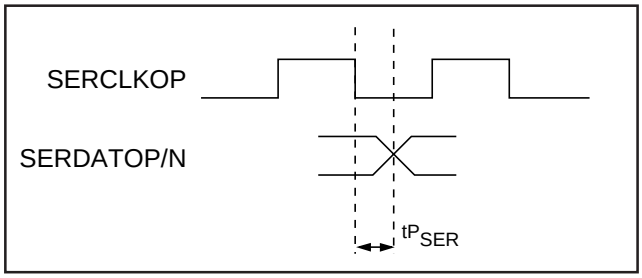
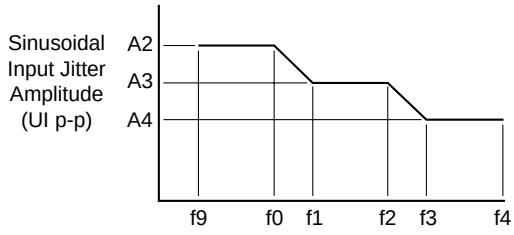


Figure 13. Clock Recovery Jitter Tolerance Compliant to G.823 and G.825



	f9 (Hz)	f0 (Hz)	f1 (Hz)	f2 (KHz)	f3 (KHz)	f4 (MHz)	A2	A3	A4
OC-3	10	30	300	6.5	65	—	15	1.5	.15
STM-1 (Optical)	0.125	19.3	500	6.5	65	1.3	39[1]	1.5	0.15
STM-1 (Electrical)	0.125	19.3	500	3.25	65	1.3	39[1]	1.5	0.075
E4	TBD	TBD	200	0.5	65	1.3	15	1.5	0.075

Note:
1. Only tested to 20 due to test equipment limitation.

Reference Clock Input

The reference clock input seen in Figure 10 provides backup reference clock signals to the clock recovery block when the clock recovery block detects a loss of signal condition. It contains a counter that divides the clock output from the clock recovery block down to the same frequency as the reference clock REFCKIN.

OTHER OPERATING MODES

Diagnostic Loopback

When the chipset is used in an electrical interface, the serial data output (SERDATOP/N) of the transmitter can be connected the serial data input (SERDATIP/N) of the receiver to implement a loopback test for diagnostic purposes, as shown in Figure 14. In this mode, SERDATEN on the transmitter and EQUALSEL on the receiver are both held low. LOSOPT on the receiver is held high or not connected.

Test Mode

The Test Clock Enable (TSTCLKEN) inputs on both chips provide access to the PLL.

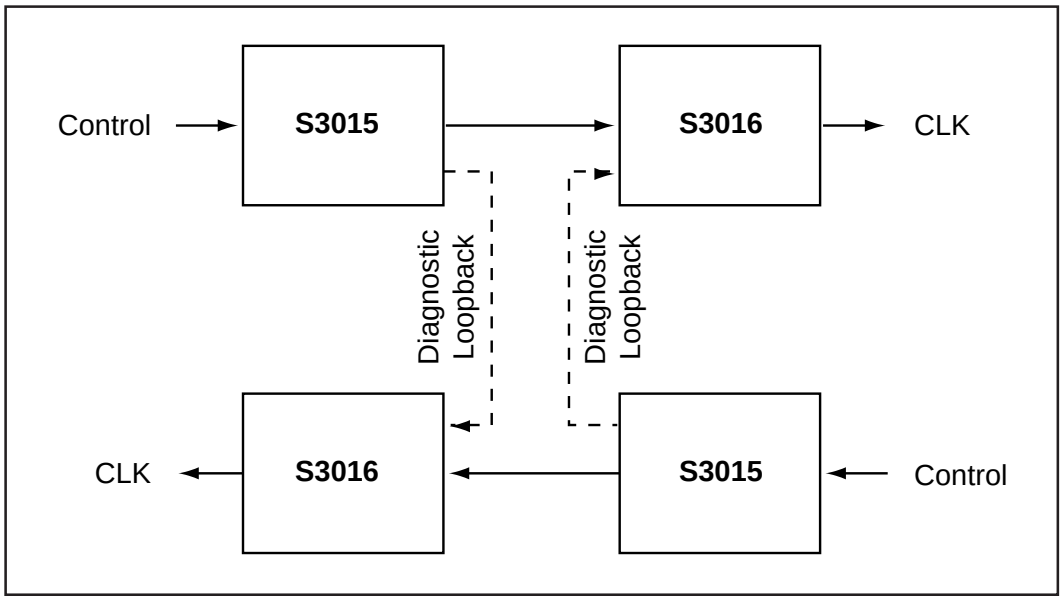
The PLL-generated clock source on both the S3015 and S3016 can be bypassed by setting TSTCLKEN high. In this mode, an externally generated clock source must be applied at the REFCLKIN input.

Clock Synthesis

In the Clock Synthesis mode, the S3015 synthesizes the E4 (139.264 MHz) clock from a 17.408 MHz crystal oscillator or the STS-3/STM-1 (155.52 MHz) clock from a 19.44 MHz crystal oscillator. In this mode, a crystal oscillator is connected to the TTL reference input and synthesized up to the output frequency.

The S3015 PLL complies with jitter generation for clock synthesis proposed for SONET/SDH equipment defined by the Bellcore TA-NWT-000253 standard, when used with a crystal reference source as defined in Table 4.

Figure 14. Loopback Diagram



S3015 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
REFCKIN	TTL	I	10	Reference clock. Input used as the reference for the internal bit clock frequency synthesizer.
TSTCLKEN	TTL	I	35	Test clock enable signal, active high, that enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Set low for normal operation.
DLCV	Single--ended PECL	I	34	Diagnostic line code violation, set high to force a CMI line code violation. DLCV is only active in CMI mode. DLCV is sampled on the falling edge of SERCLKOP.
CMISEL	TTL	I	33	CMI select, used to select CMI or NRZ. A logic high selects CMI mode. A logic low selects NRZ mode. Both the SERDATOP/N and the XFRMDRV outputs are controlled by CMISEL.
RSTB	TTL	I	24	Reset input for the device, active low. Initializes the device to a known state. When active, all data outputs are held low. Clock outputs are still active during reset.
CAP1 CAP2	–	I	1 52	The loop filter capacitor is connected to these pins. The capacitor value should be 0.1µf ±10% tolerance, X7R dielectric. 50 V is recommended (16 V is acceptable).
SERDATIP SERDATIN	Diff. PECL	I	45 46	Serial data in. The clock is recovered from transitions on these inputs. No phase relationship to REFCKIN is required.
XFRMEN	TTL	I	23	Transformer driver enable used to enable the transformer driver outputs. A logic low enables XFRMDRVA and XFRMDRVB. A logic high turns off the transformer driver outputs.
SERDATEN	TTL	I	5	Serial data enable, used to enable the serial data outputs. A logic low enables SERDATOP/N. A logic high turns off the serial data outputs.
SERDATOP SERDATON	Diff. PECL	O	7 6	Serial data out signal. In NRZ mode, this signal is the delayed version of the incoming data stream (SERDATIP/N) updated on the falling edge of Serial Clock Out (SERCLKOP). In CMI mode, this signal is the CMI-encoded version of SERDATIP/N.
SERCLKOP SERCLKON	Diff. PECL	O	29 30	Serial clock out signal that is a 155 MHz clock that is phase-aligned with Serial Data Out (SERDATO) in NRZ mode. In CMI mode, SERCLKOP/N cannot be used.
REFCKOUT	TTL	O	11	Single-ended TTL reference clock output.

S3015 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
XFRMDRVA	Analog	O	20	Transformer driver A, used to drive the transformer of the electrical interface. For E4 operation, this output should be connected per Figure 19 to provide the correct G.703 compatible output levels from the transformer when connected to the specified 75Ω cable.
XFRMDRVB	Analog	O	21	Transformer driver B, used to drive the monitor transformer of the electrical interface. This output should be connected per Figure 20 to provide the correct output levels from the transformer when connected to the specified 75Ω cable.
AVEE	0V	–	2, 22, 39, 42, 43	Analog 0V
AVCC	+5V	–	3, 19, 38, 40, 48	Analog +5V
ECLVCC		–	4, 9, 12, 15, 25, 28, 31,37	
ECLVEE	0V	–	8, 32, 36	Digital 0V
TTLGND	GND	–	13, 27	
TTLVCC	+5V	–	14, 26	TTL Power Supply (+5V if TTL)
NC	–	–	16, 17, 18, 41, 44, 47, 49, 50, 51	No Connection

S3016 Pin Assignment and Descriptions

Pin Name	Level	I/O	Pin #	Description
BUFINA BUFINB	Analog	I	22 23	Buffer inputs to the equalizer network buffer circuit. This circuit provides a high impedance load to the transformer termination network in order to comply with the required return loss specifications. These pins should be connected as shown in Figure 17. These pins are electrically equivalent.
ANDATIN	Analog	I	16	Analog serial data input from the equalizer circuit. It must be connected to the output of the equalizer circuit as shown in Figure 17. When the S3016 is used with a fiber optic receiver, this input should be left open and the SERDATIP/N inputs should be used.
EQUALSEL	TTL	I	33	Equalization select used to select SERDATIP/N or ANDATIN. A logic high selects ANDATIN.
REFCKIN	Single-ended TTL	I	10	Input used as the reference for the VCO when the input data signal is lost.
SERDATIP SERDATIN	Diff. PECL	I	45 46	Serial data in. Clock is recovered from transitions on these inputs when selected by EQUALSEL.
TSTCLKEN	TTL	I	35	Test clock enable signal, active high, that enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL.
CMISEL	TTL	I	32	CMI Select used to select CMI or NRZ. A logic high selects CMI mode. Either ANDATIN or SERDATIN may be used as inputs to the CMI decoder.
RSTB	TTL	I	34	Reset input for the device, active low. Initializes the device to a known state, shuts off SERCLKOP/N, and forces the PLL to acquire to the reference clock. A reset of at least 16 ms should be applied at power-up and whenever it is necessary to reacquire to the reference clock. The S3016 will also reacquire to the reference clock if the serial data is held quiescent (constant ones or constant zeros) or LOSIN or LOSOPT are activated for at least 224 bit intervals.

S3016 Pin Assignment and Descriptions (Continued)

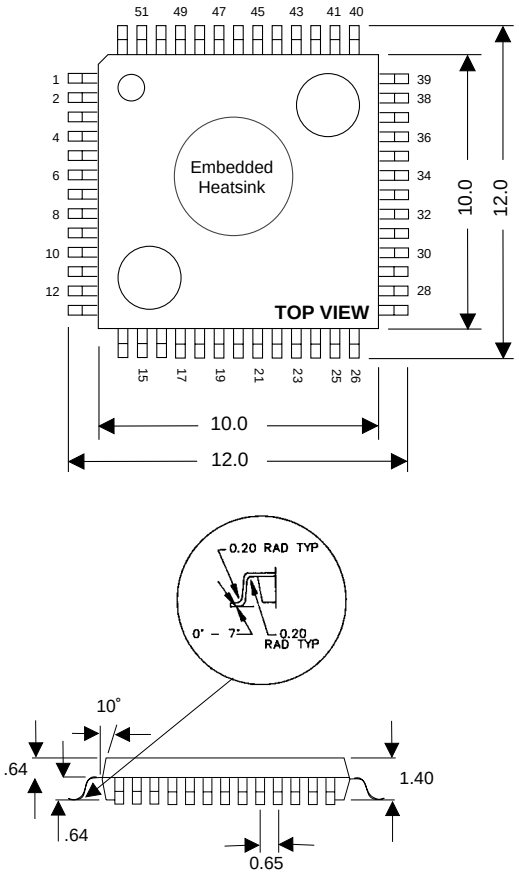
Pin Name	Level	I/O	Pin #	Description
LOSIN	Analog	I	18	Loss of signal in. A single-ended input that indicates a loss of received signal. When the signal level at LOSIN drops below the voltage level set by LOSREF for greater than 96 to 224 bit intervals, the data on Serial Data Out (SERDATOP/N) will be forced to a constant low, and the PLL will change its reference from the serial data stream to the reference clock. This input is to be driven by the external bandpass filter and peak detect circuit as shown in Figure 17. This signal must be used to assure correct automatic reacquisition to serial data following an interruption and subsequent reconnection of the data path. This will assure that the PLL does not "wander" out of reacquisition range when no signal is applied. When LOSIN is inactive, data on the SERDATIP/N pins will be processed normally.
LOSOPT	PECL	I	4	Loss of optical signal input, active low. It has the same functionality as LOSIN, except that it is used in optical mode instead of electrical. It should be driven by the external optical receiver module to indicate a loss of received optical power.
LOSREF	Analog	I	19	Loss of signal reference that sets the comparator levels for LOSIN. (See Table 6.)
CAP1 CAP2	–	I	1 52	The loop filter capacitor is connected to these pins. The capacitor value should be 0.1µf ±10% tolerance, X7R dielectric. 50 V is recommended.
LOSOUT	TTL	O	5	Loss of signal out, active low. Clock recovery indicator. Set high when the internal clock recovery has locked onto the incoming datastream. LOSOUT is an asynchronous output. This output is deasserted when there is no incoming serial data input or when the received signal has dropped below the reference voltage set by LOSREF for more than 96 to 224 bit intervals. In this case, the PLL locks to the reference clock.
SERDATOP SERDATON	Diff. PECL	O	6 7	Serial NRZ data out signal. It can be either a delayed version of the NRZ data input (NRZ mode) or the decoded CMI data (CMI mode). SERDATOP/N is updated on the falling edge of SERCLKOP/N per Figure 12.
SERCLKOP SERCLKON	Diff. PECL	O	28 29	Serial clock out signal that is phase-aligned with Serial Data Out (SERDATOP). (See Figure 12 and Table 3 for timing.)
LCV	Single-ended PECL	O	31	Line code violation that is set high to indicate that the current bit contains a CMI line code violation in CMI mode. LCV is updated on the falling edge of SERCLKOP/N per Figure 12. In NRZ mode, this is a test output.

S3016 Pin Assignment and Descriptions (Continued)

Pin Name	Level	I/O	Pin #	Description
BUFOUT	Analog	O	20	Buffer output of the equalizer network buffer circuit. This circuit provides a low impedance driver to the equalizer circuit. This pin should be connected as shown in Figure 17 to drive the equalizer network.
REFCKOUT	TTL	O	11	Single-ended TTL reference clock output (19.44 MHz).
AVEE	0V	–	2, 17, 21, 39, 42, 43	Analog 0V
AVCC	+5V	–	3, 15, 24, 38, 40, 48	Analog +5V
ECLVEE	0V	–	8, 36	Digital 0V
ECLVCC	+5V	–	9, 12, 25, 30, 37	Digital +5V
TTLGND	GND	–	13, 27	TTL Ground
TTLVCC	+5V	–	14, 26	TTL Power Supply (+5V if TTL)
NC	–	–	41, 44, 47, 49, 50, 51	No Connection

Figure 15. 52-Pin PQFP Package and Heatsink

DW0045-29



All dimensions nominal in mm.

Absolute Maximum Ratings

PARAMETER	MIN	TYP	MAX	UNIT
Case Temperature under Bias	–55		125	°C
Junction Temperature under Bias	–55		150	°C
Storage Temperature	–65		150	°C
Voltage on VCC with Respect to GND	–0.5		+7.0	V
Voltage on Any TTL Input Pin	–0.5		+5.5	V
Voltage on Any PECL Input Pin	VCC-3		VCC	V
TTL Output Sink Current			20	mA
TTL Output Source Current			10	mA
High Speed PECL Output Source Current			50	mA
Static Discharge Voltage		500		V

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNIT
Ambient Temperature under Bias	-40		85	°C
Junction Temperature under Bias	-10		+125	°C
Voltage on VCC with Respect to GND	4.75	5.0	5.25	V
Voltage on Any TTL Input Pin	0		VCC	V
Voltage on Any PECL Input Pin	VCC-2		VCC	V
S3015 ICC		141	240	mA
S3016 ICC		180	240	mA

Table 2. S3015/S3016 Clock Recovery Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
Nominal VCO Center Frequency		622.08		MHz	Given REFCKIN = VCO ÷ 32
OC–3/STS–3 Lock Range		+8, -12		%	With respect to fixed reference frequency
Acquisition Lock Time [1]			64	µsec	With device already powered up and valid REFCLK
Reference Clock Input Duty Cycle	30		70	% of UI	
Reference Clock Rise & Fall Times			5.0	ns	10% to 90% of amplitude
PECL Output Rise & Fall Times			850	ps	10% to 90%, 50Ω load, 5 pf cap
Reference Clock Frequency Tolerance	-100		100	ppm	
tP_{SER} SERCLKOP Falling to SERDATO Valid Prop Delay	100		500	ps	See Figure 13

1. Specification based on design values. Not tested.

Table 3. S3015 Clock Synthesis Mode Performance Specifications

Parameter	Min	Typ	Max	Units	Condition
PECL Data Output Jitter (S3015 SERDATOP/N) OC–3/STS–3			64	ps (rms)	In CSU mode, given • 56 ps rms jitter on REFCKIN in 12KHz to 1 MHz band
E4–STS–3 CMI			32		• 28 ps rms jitter on REFCKIN in 12KHz to 1 MHz band
Reference Clock Frequency Tolerance Clock Synthesis	-20		+20	ppm	Required to meet SONET output jitter generation specification

Table 4. Electrical Characteristics for Transformer Driver (1)

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

Parameter	Min	Typ	Max	Units	Condition
Operating Frequency		155		MHz	270 Ω || 3pF load
VSWR (2)		1.3:1	1.5:1		75 Ω A.C. Coupled Termination

1. For output waveform characteristics, see Figures 8 and 9.
2. Up to 250 MHz.

Table 5. Electrical Characteristics for ANDATIN Input

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak to Peak Input Voltage Range	V_{iptp}				1.3	V
Common-Mode Rejection Ratio	CMRR(1)		40			dB
Power-Supply Rejection Ratio	PSRR(1)		40			dB
Input Sensitivity	S_{IN}	T_A = MIN to MAX	110			mV
DC offset at input (2)					V_{CC} - 1V	V

1. Up to 300 KHz
2. Signal is undefined if left floating

Table 6. Electrical Characteristics for LOSIN Input

(V_{CC} = +5V, T_A = +25°C, input AC coupled unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Peak to Peak Input Voltage Range	V_{iptp}				1.1	V
Common-Mode Rejection Ratio	CMRR(1)		40			dB
Power-Supply Rejection Ratio	PSRR(1)			35		dB
Signal Level for LOS detected (3)		T_A = MIN to MAX	LOS-REF/30	LOS-REF/20	LOS-REF/10	V/V
Signal Level for LOS cleared (3)		T_A = MIN to MAX	LOS-REF/15	LOS-REF/10	LOS-REF/5	V/V
Hysterisis between "trans. cond." and "no trans. cond." (2)			4	6		dB

1. Up to 300 KHz
2. LOSREF >0.5 volts
3. LOS detected and LOS cleared will maintain 2:1 ratio ±5%.

Below are typical operating conditions:

Voltage Applied at LOSREF	Compare Voltage #1	Compare Voltage #2	Hysterisis
1.4 Volts	140 mV ± 0.6dB	70 mV ± 1dB	6dB +1.6 -1.4dB
0.7 Volts	70 mV ± 1dB	35 mV ± 1.6dB	6dB +2.7 -2.0dB
0.3 Volts	30 mV ± 1.6dB	15 mV ± 3.5dB	6dB +6.0 -3.7dB

Table 7. Electrical Characteristics for BUFIN, BUFOUT

At V_{CC} = +5VDC, R_{LOAD} = 75Ω a.c. coupled and T_A = 25˚C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS (BUFOUT) Voltage Output			± 0.6	± 0.8		V
Output Resistance			1	3	8	Ω
TRANSFER CHARACTERISTICS Gain (BUFIN to BUFOUT)(1)			.85	.93	1.1	V/V
VSWR (2)	VSWR	With 75 ohm AC coupled termination		1.3:1	1.5:1	
Harmonic Distortion (2)	HD	Input = 0.3V p-p Input = 0.6V p-p Input = 1.2V p-p	35 30 25	40 35 30		dBc
DC Input Bias		Input externally AC coupled	Vcc - 0.85			V
DC Output Bias		Output externally AC coupled	Vcc - 2.5			V

1. Up to 300 MHz
2. Up to 250 MHz

Thermal Management

Device	Power	Θja Still Air w/DW0045-29	Max Still Air[1] w/DW0045-29
S3015/S3016	1.25W	37.5˚C/W	85˚C

1. Max ambient temperature permitted in still air to maintain T_j <130˚C.

TTL Input/Output DC Characteristics

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}[1]	Input LOW Voltage			0.8	Volts	Guaranteed Input LOW Voltage
V_{IH}[1]	Input HIGH Voltage	2.0			Volts	Guaranteed Input HIGH Voltage
I_{IL}	Input LOW Current	-400.0			µA	V_{CC} = MAX, V_{IN} = 0.5V
I_{IH}	Input HIGH Current			50.0	µA	V_{CC} = MAX, V_{IN} = 2.7V
I_I	Input HIGH current at Max. VCC			1.0	mA	V_{CC} = MAX, V_{IN} = 5.5V
I_{OS}	Output Short Circuit Current	-100.0		-25.0	mA	V_{CC} = MAX, V_{OUT} = 0.5V
V_{IK}	Input Clamp Diode Voltage	-1.2			Volts	V_{CC} = MIN, I_{IN} = -18 ma
V_{OL}	Output LOW Voltage			0.5	Volts	V_{CC} = MIN, I_{OL} = 8 ma
V_{OH}	Output HIGH Voltage	2.7			Volts	V_{CC} = MIN, I_{OH} = -1 ma

1. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

PECL Input/Output DC Characteristics

(T_A = -40°C to +85°C, V_{CC} = 5 V ±5%)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -1.441	Volts	Guaranteed Input LOW Voltage for single-ended inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.225		V_{CC} -0.570	Volts	Guaranteed Input HIGH Voltage for single-ended inputs
V_{IL}	Input LOW Voltage	V_{CC} -2.000		V_{CC} -0.700	Volts	Guaranteed Input LOW Voltage for differential inputs
V_{IH}	Input HIGH Voltage	V_{CC} -1.750		V_{CC} -0.450	Volts	Guaranteed Input HIGH Voltage for differential inputs
V_{ID}	Input Diff. Voltage	0.250	0.500	1.400	Volts	Differential Input Voltage
I_{IH}	Input High Current	-0.500		20.000	µA	V_{ID} = 500mV
I_{IL}	Input Low Current	-0.500		20.000	µA	V_{ID} = 500mV
V_{OL}	Output LOW Voltage	V_{CC} -2.000		V_{CC} -1.500	Volts	50 ohm termination to V_{CC} -2V
V_{OH}	Output HIGH Voltage	V_{CC} -1.110		V_{CC} -0.670	Volts	50 ohm termination to V_{CC} -2V
V_{OD}	Output Diff. Voltage	0.390		1.330	Volts	Differential Output Voltage

1. These conditions will be met with no airflow.
2. When not used, tie the positive differential PECL pin to VCC and the negative differential ECL pin to ground via a 3.9K resistor.

Figure 16. Differential ECL Input and Output Applications

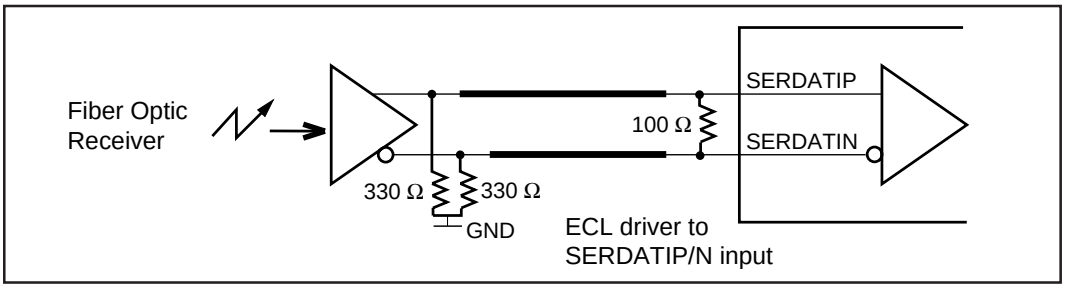


Figure 17. S3016 Transformer Input Application

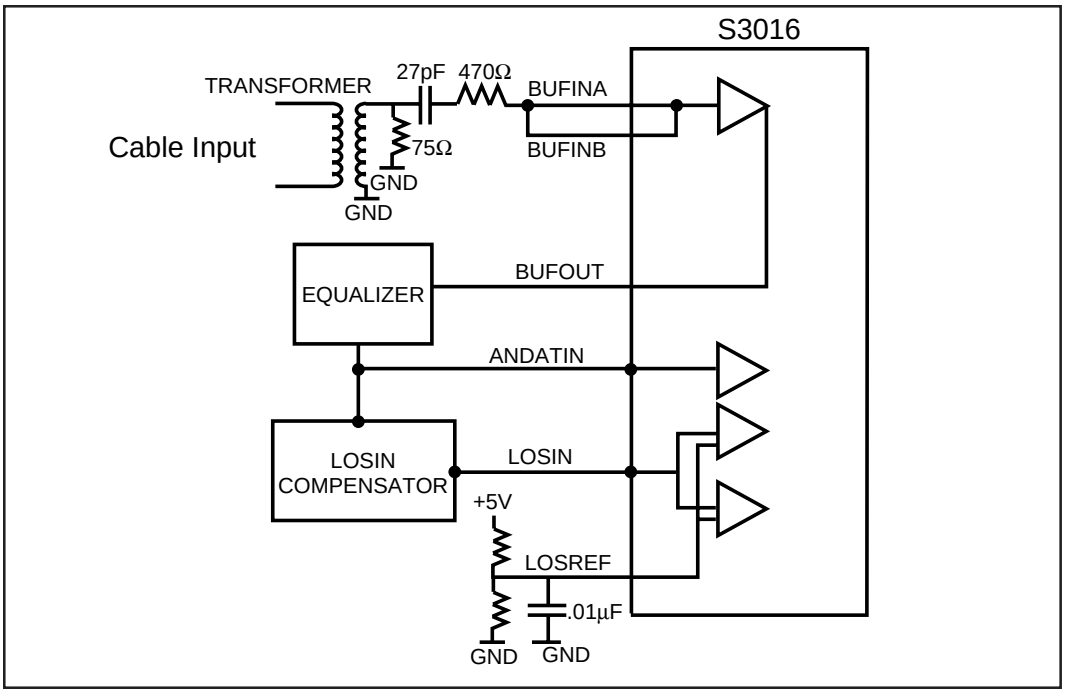


Figure 18. S3015 Differential ECL Output Application

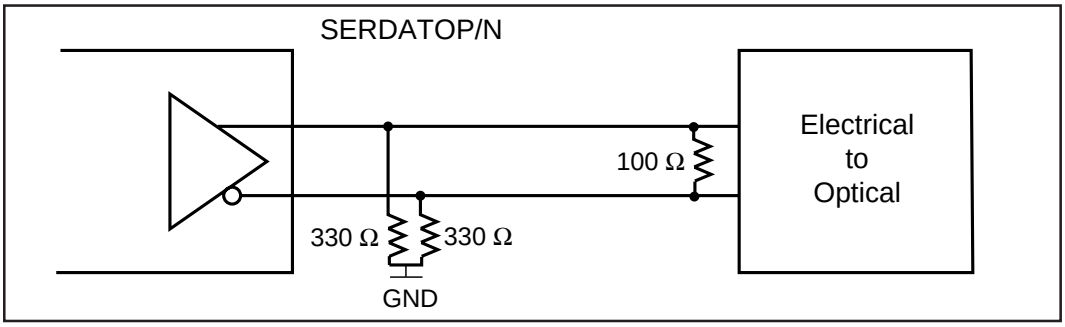


Figure 19. S3015 Transformer Output Application

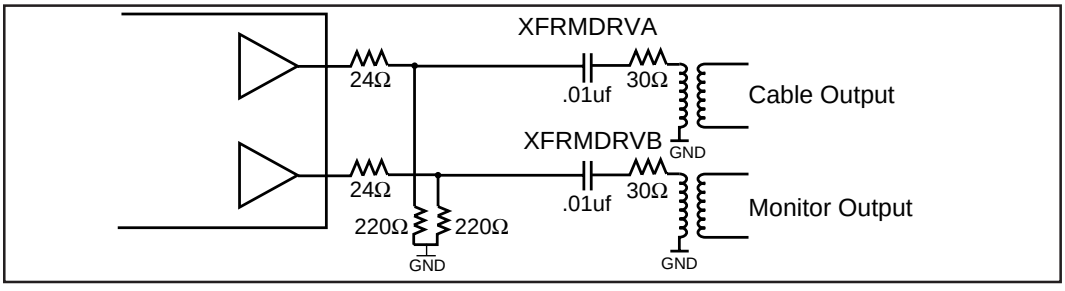


Figure 20. OC3 Application

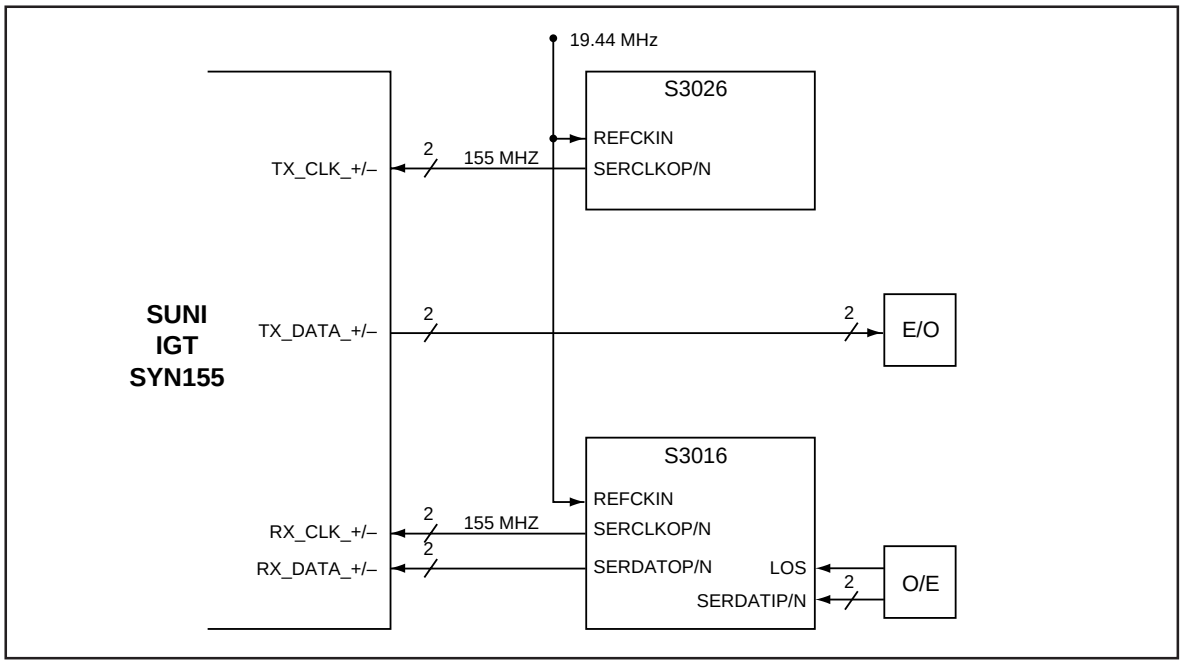


Figure 21. STM-1 CMI, E4 Application

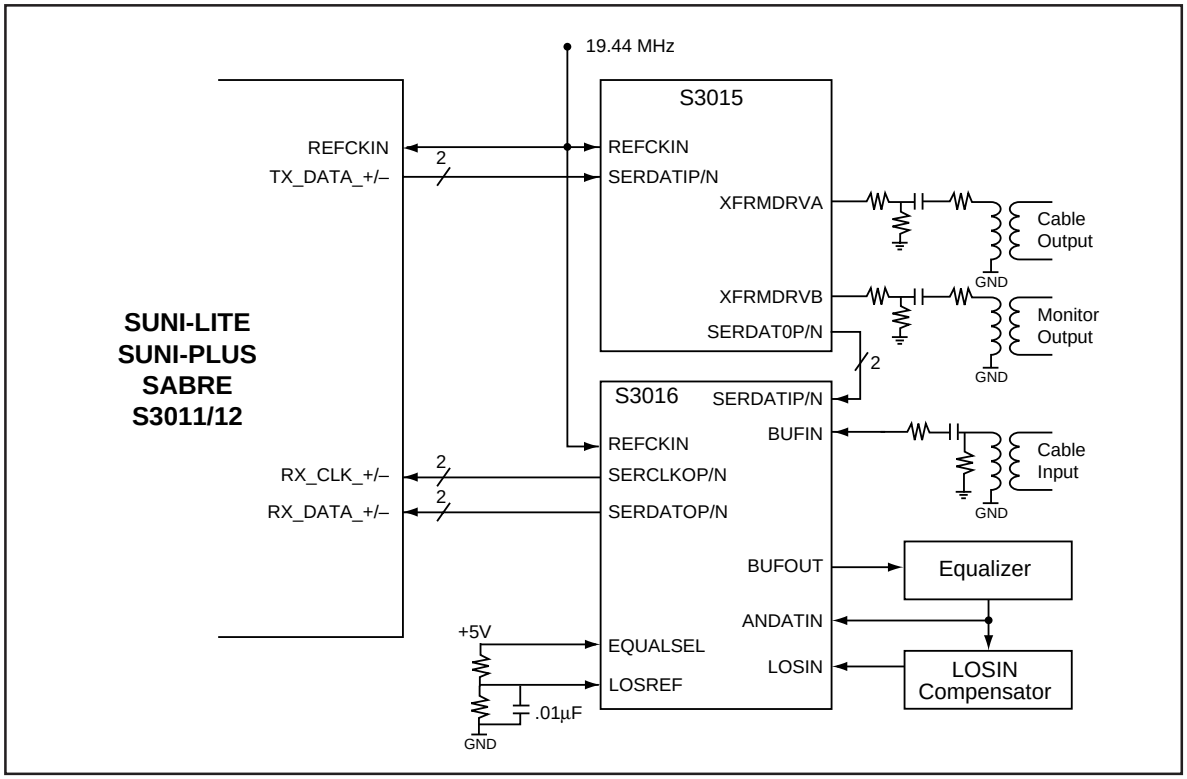


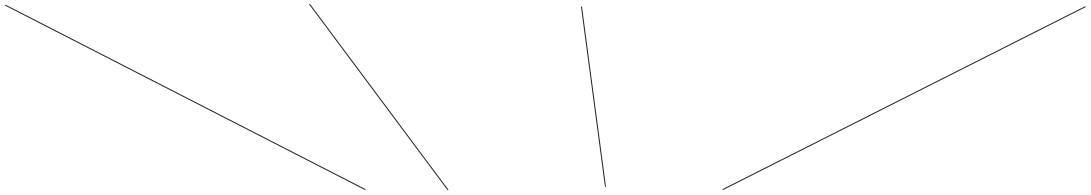
Table 8. Suggested Interface Devices

Processor Interface		
PMC PM5345	SUNI	Saturn User Network Interface
PMC PM5346	SUNI-Lite	Saturn User Network Interface
PMC PM5347	SUNI-Plus	Saturn User Network Interface
IGT WAC-013-A		SONET LAN ATM Processor
TRANSWITCH SYN155		155 Mbit/s Synchronizer
TI SABRE TDC 1500		155 Mbit/s Processor
AMCC S3011/12		SONET/SDH/ATM 0C3 Transmitter & Receiver
Electrical Interface		
Mini-Circuits	MCL TXI-R5	Wideband RF Transformer (Surface Mount)
Mini-Circuits	MCL TO-75	Wideband RF Transformer (Through-Hole)
Optical Interface		
HP HFBR-520x	155 Mbit/s	Fiber Optic Transceiver
CTS ODL-1408X	155 Mbit/s	Fiber Optic Transceiver
Sumitomo SDM4123-XC	155 Mbit/s	Fiber Optic Transceiver
AMP 269039-1	155 Mbit/s	Fiber Optic Transceiver

Ordering Information

GRADE	TRANSMITTER		
S – Industrial/ commercial	3015	A – 52 TQFP TEP w/DW0045-29 heatsink unattached	H0 – No Heatsink

GRADE	RECEIVER		
S – Industrial/ commercial	3016	A – 52 TQFP TEP w/DW0045-29 heatsink unattached	H0 – No Heatsink



X XXXX X / XX

Grade Part number Package H0 for no heatsink (identifier not marked on part)

ISO 9001 CERTIFIED

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