FEATURES

- Functionally compliant with ANSI X3T9.3 Fibre Channel physical, transmission, and signaling protocol standards
- Supports Fibre Channel data transmission rates of 1062.5, 531.25, and 265.625 Mbit/s
- S2030 transmitter incorporates phase-locked loop (PLL) providing clock synthesis from low-speed reference
- S2031 receiver PLL provides clock and data recovery
- On-chip 8B/10B encoding and decoding
- 16-bit parallel TTL interface
- Low-jitter serial ECL interface
- Lock detect outputs
- Link and local loopback
- Interfaces with coax, twisted pair, or fiber optics

APPLICATIONS

High-speed data communications

- Supercomputer
- Mainframe
- Workstation
- Frame buffer
- Switched networks
- Data broadcast environments
- Proprietary extended backplanes

GENERAL DESCRIPTION

The S2030 and S2031 fibre channel transmitter and receiver pair are designed to perform high-speed serial data transmission over fiber optic or coaxial cable interfaces conforming to the requirements of the ANSI X3T9.3 Fibre Channel specification. The chipset is selectable to 1062.5, 531.25, and 265.625 Mbit/s data rates. It features a 16-bit data word, which is expandable to 20 bits in raw mode with the encoding bypassed.

The chipset performs parallel-to-serial and serial-to-parallel conversion, encoding/decoding functions, framing, and primitive signal/sequence generation and identification. The S2030 on-chip PLL synthesizes the high-speed clock from a low-speed reference. The S2031 on-chip PLL synchronizes directly to incoming digital signals, while simultaneously retiming and regenerating the data stream. The transmitter and receiver each support differential ECL-compatible I/O for fiber optic component interfaces, to minimize crosstalk and maximize data integrity. Local and link loopback modes allow for system diagnostics. The chips require +5V and –5.2V power supplies, and dissipate approximately 3.5 watts each.

Figure 1 shows a typical network configuration incorporating the chipset.

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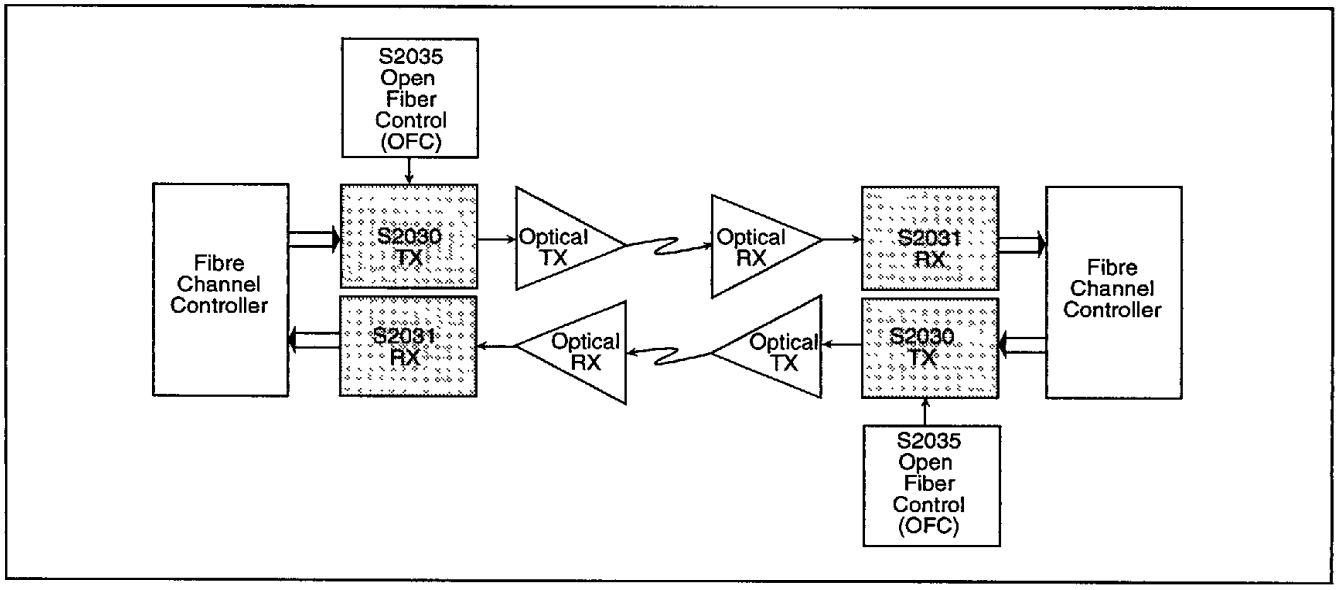
Figure 1. Typical Network Configuration



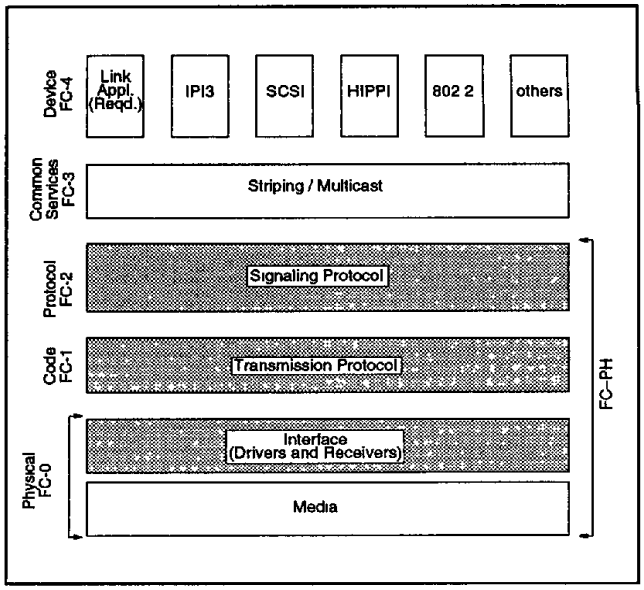
FIBRE CHANNEL OVERVIEW

Fibre Channel is a high-performance serial link supporting its own as well as higher-level protocols associated with networking standards such as the High-Performance Parallel Interface (HIPPI), Intelligent Peripheral Interface (IPI), Small Computer System Interface (SCSI), and others. Fibre Channel is capable of replacing the HIPPI, IPI, and SCSI physical interfaces with a protocol-efficient alternative that provides performance improvements in both distance and speed. Fibre Channel standards are organized in layers, as seen in Figure 2. The S2030/S2031 chipset implements the physical portion, the transmission protocol, and the link start-up elements of the signaling protocol, shown as shaded blocks in the diagram.

The Fibre Channel is optimized for movement of large blocks of data such as those used in file transfers between processors (supercomputer, mainframe, etc.), storage systems (disk and tape), communications, and output-only devices such as laser printers and frame buffers.

Basics of the Fibre Channel specification are covered in the following sections. For details on Fibre Channel transmission and signaling protocol, refer to the ANSI X3T9.3 Fibre Channel Standard document.

Figure 2. Fibre Channel Organization



Physical Layer

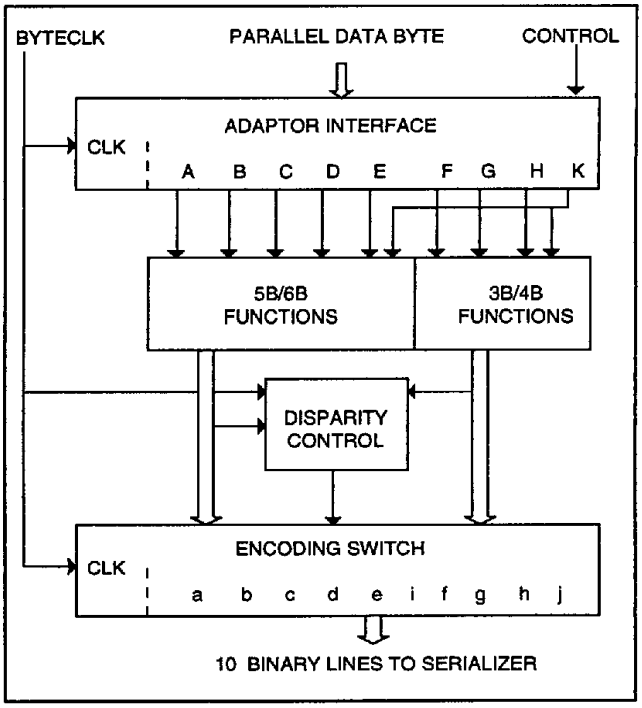
The lowest level of the Fibre Channel standard defines the physical link in the Fibre Channel system, including the fiber, connectors, and optical parameters for a variety of data rates. A serial copper version is also defined for limited distance applications. The standard supports serial data streams at data rates of 132.813, 265.625, 531.25, and 1062.5 Mbit/s at a system bit error rate (BER) of less than 10^{-12}.

Transmission Protocol

The Fibre Channel transmission protocol includes serial encoding and decoding rules, special characters, and error control. It uses the 8B/10B transmission code, in which information to be transmitted is encoded 8 bits at a time into a 10-bit transmission character (see Figure 3)[1]. Information received is recovered 10 bits at a time and those transmission characters used for data ("D"-type) are decoded into one of the correct 256 8-bit combinations.

Refer to the Fibre Channel standard for the complete listing of valid data characters. Some of the remaining transmission characters ("K"-type) are used for functions associated with control signals related to protocol management. Table 1 specifies the valid special characters. Codes detected at the receiver that are not D- or K-type are flagged as errors.

Figure 3. 8B/10B Encoding



1. A.X. Widmer and P.A. Franaszek, "A Byte-Oriented DC Balanced (0,4) 8B/10B Transmission Code," IBM Research Report RC 9391, May 1982.

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The characters defined by this transmission code ensure that short run lengths and enough transitions are present in the serial bit stream to make clock recovery possible at the receiver. The encoding also greatly increases the likelihood of detecting any single or multiple bit errors that may occur during transmission and reception of data.

Signaling Protocol

Fibre Channel signaling protocol includes the frame structure and byte sequences portrayed in Figure 4. The protocol also defines *ordered sets*, four-byte transmission words containing data and special characters which have a special meaning. Ordered sets provide the ability to obtain bit and word synchronization, which also establishes word boundary alignment. An ordered set always begins with the special character K28.5, with the precise format dependent on the running disparity (RD) status of the previous bit streams. Three ordered set types are defined in the signaling protocol: frame delimiters, primitive signals, and primitive sequences. Tables 2, 3, and 4 specify the ordered sets defined for use by the standard.

A *frame delimiter* is an ordered set that immediately precedes or follows the contents of a frame. Separate and distinct delimiters identify the start and end of a frame. A frame is composed of a start-of-frame (SOF) delimiter, frame content, and an end-of-frame (EOF) delimiter.

A *primitive signal* is an ordered set designated by the standard to have a special meaning. The two primitive signals are Idle and Receiver Ready (R_RDY).

A *primitive sequence* is an ordered set that is transmitted repeatedly and continuously to indicate specific conditions within a port or conditions encountered by the receiver logic of a port. When a primitive sequence is received and recognized, a corresponding primitive sequence or idle is transmitted in response. The primitive sequences supported by the standard are Offline (OLS), Not Operational (NOS), Link Reset (LR), and Link Reset Response (LRR).

Figure 4. General Frame Format

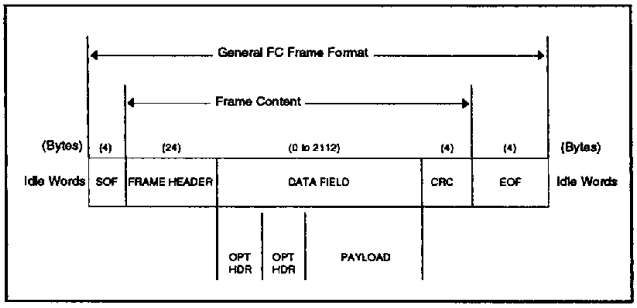

Table 1. Valid Special Characters

Special Code Name	Current RD – abcdei fghj	Current RD + abcdei fghj	Notes
K28.0	001111 0100	110000 1011	Reserved
K28.1	001111 1001	110000 0110	Reserved
K28.2	001111 0101	110000 1010	Reserved
K28.3	001111 0011	110000 1100	Reserved
K28.4	001111 0010	110000 1101	Reserved
K28.5	001111 1010	110000 0101	
K28.6	001111 0110	110000 1001	Reserved
K28.7	001111 1000	110000 0111	Reserved
K23.7	111010 1000	000101 0111	Reserved
K27.7	110110 1000	001001 0111	Reserved
K29.7	101110 1000	010001 0111	Reserved
K30.7	011110 1000	100001 0111	Reserved

Table 2. Frame Delimiter Functions

Delimiter Function	Beginning RD	Ordered Set
SOF Connect Class 1 (SOFc1)	Negative	K28.5 D21.5 D23.0 D23.0
SOF Initiate Class 1 (SOFi1)	Negative	K28.5 D21.5 D23.2 D23.2
SOF Normal Class 1 (SOFn1)	Negative	K28.5 D21.5 D23.1 D23.1
SOF Initiate Class 2 (SOFi2)	Negative	K28.5 D21.5 D21.2 D21.2
SOF Normal Class 2 (SOFn2)	Negative	K28.5 D21.5 D21.1 D21.1
SOF Initiate Class 3 (SOFi3)	Negative	K28.5 D21.5 D22.2 D22.2
SOF Normal Class 3 (SOFn3)	Negative	K28.5 D21.5 D22.1 D22.1
SOF Fabric (SOFf)	Negative	K28.5 D21.5 D24.2 D24.2
EOF Terminate (EOFt)	Negative	K28.5 D21.4 D21.3 D21.3
	Positive	K28.5 D21.5 D21.3 D21.3
EOF Disconnect-Terminate (EOFdt)	Negative	K28.5 D21.4 D21.4 D21.4
	Positive	K28.5 D21.5 D21.4 D21.4
EOF Abort (EOFa)	Negative	K28.5 D21.4 D21.7 D21.7
	Positive	K28.5 D21.5 D21.7 D21.7
EOF Normal (EOFn)	Negative	K28.5 D21.4 D21.6 D21.6
	Positive	K28.5 D21.5 D21.6 D21.6
EOF Disconnect-Terminate-Invalid (EOFdti)	Negative	K28.5 D10.4 D21.4 D21.4
	Positive	K28.5 D10.5 D21.4 D21.4
EOF Normal-Invalid (EOFni)	Negative	K28.5 D10.4 D21.6 D21.6
	Positive	K28.5 D10.5 D21.6 D21.6

Explanation:
SOF—Start-of-frame delimiter
EOF—End-of-frame delimiter

Table 3. Primitive Signals

Primitive Signal	Beginning RD	Ordered Set
Idle Word	Negative	K28.5 D21.4 D21.5 D21.5
Receiver Ready (R_RDY)	Negative	K28.5 D21.4 D10.2 D10.2

Table 4. Primitive Sequences

Primitive Sequence	Beginning RD	Ordered Set
Offline (OLS)	Negative	K28.5 D21.1 D10.4 D21.2
Not_Operational (NOS)	Negative	K28.5 D21.2 D31.5 D5.2
Link_Reset_(LR)	Negative	K28.5 D9.2 D31.5 D9.2
Link_Reset_Response (LRR)	Negative	K28.5 D21.1 D31.5 D9.2

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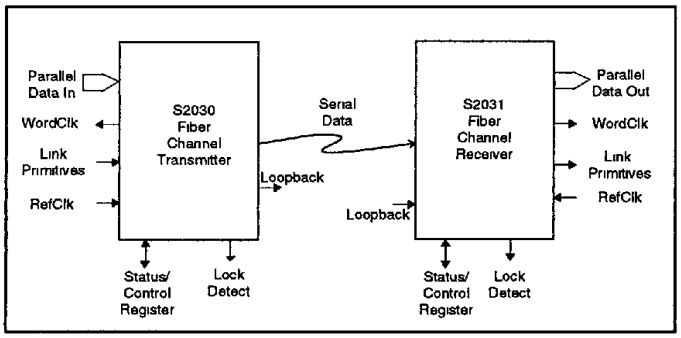
S2030/S2031 OVERVIEW

The S2030 transmitter and S2031 receiver generate control, handshaking, encoding/decoding, framing signals, and link start-up procedures to implement a Fibre Channel interface. The frame header and CRC are handled as data. Operation of the S2030/S2031 chips is straightforward, as depicted in Figure 5. The sequence of operations is as follows:

Transmitter
1. 16-bit parallel input
2. 8B/10B encoding
3. Parallel-to-serial conversion
4. Serial output

Receiver
1. Clock and data recovery from serial input
2. Serial-to-parallel conversion
3. Frame detection
4. 10B/8B decoding
5. 16-bit parallel output

Figure 5. Interface Diagram



Internal clocking and control functions are transparent to the user. Details of data timing can be seen in Figure 6.

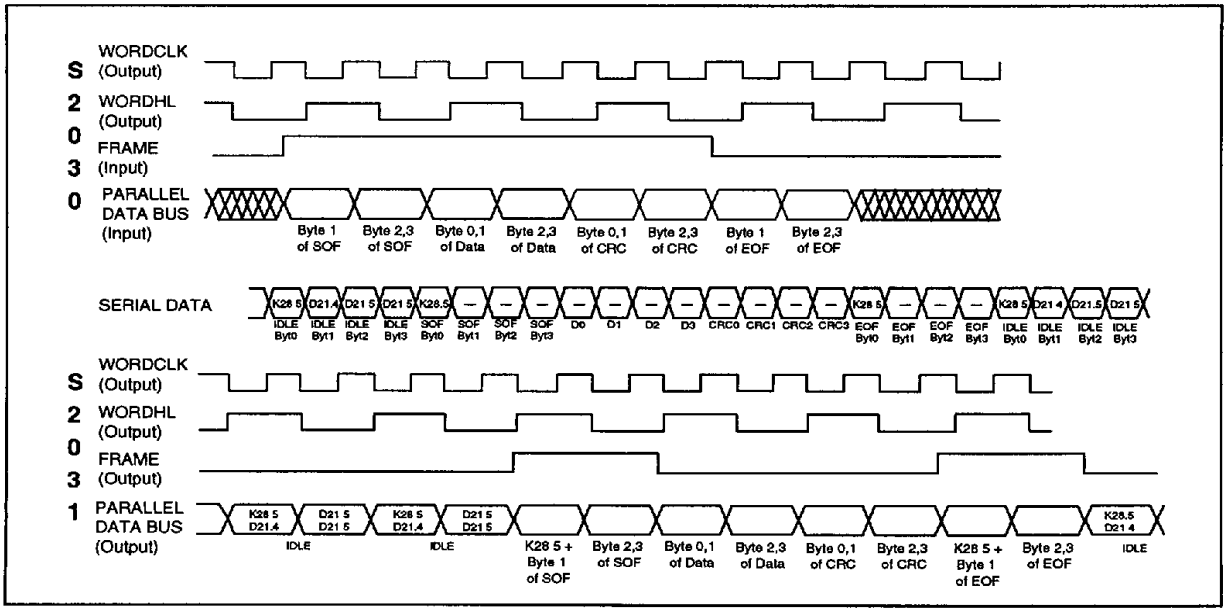
A bidirectional 8-bit control/status port is used to read chip status and write control information to the chip. A lock detect feature is provided on both chips, which indicates that the PLL is locked (synchronized) to the data stream. The transmitter generates the appropriate primitive signal and sequences based on its Link Primitive inputs. The receiver identifies the ordered sets received and decodes them on its Link Primitive outputs.

A raw data mode is also provided that bypasses the 8B/10B encoder and allows user-defined coding schemes. See the section **Other Operating Modes** on page 3-50.

Loopback Modes

Both local and link loopback operating modes are supported by the chipset. Local loopback provides capability for performing offline testing of the interface to ensure the integrity of the serial channel before enabling the transmission medium. It also allows for system diagnostics. Link loopback provides a means for link testing and can also be used to implement a repeater function, with clock jitter and data distortion determining the number of repeaters allowed. See the section **Other Operating Modes** on page 3-50.

Figure 6. Interface Timing



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Fiber Optic Modules

AMCC recommends the Force, Inc. Models T/R or Finisar FTM/FRM-850 digital fiber optics modules to handle optical signal transmission/receiving. Force, Inc. can be reached at P.O. Box 2045, Christiansburg, VA, 24073, Phone (703) 382-0462, Fax (703) 381-0392. Finisar Corp. can be reached at 3515 Edison Way, Menlo Park, CA 94025. Telephone (415) 364-2722, Fax (-3041).

S2030 TRANSMITTER

Architecture/Functional Description

The S2030 transmitter chip is designed to implement the ANSI X3T9.3 Fibre Channel specification transmit functions through the physical, transmission, and portions of the signaling protocol layers. A block diagram showing the basic chip operation is shown in Figure 7. (An Open Fiber Control circuit for laser-based systems is offered as a separate device by AMCC.)

In its working state, the S2030 continuously transmits an encoded bit stream onto its data channel depending on the state of the FRAME, LKPRIM<2:0>, LSRSFT, and TXFAIL inputs. The S2030 enters the failure state if TXFAIL goes high, and sends the NOS sequence. Similarly, if LSRSFT goes high the device goes into the off-line state and sends the OLS sequence.

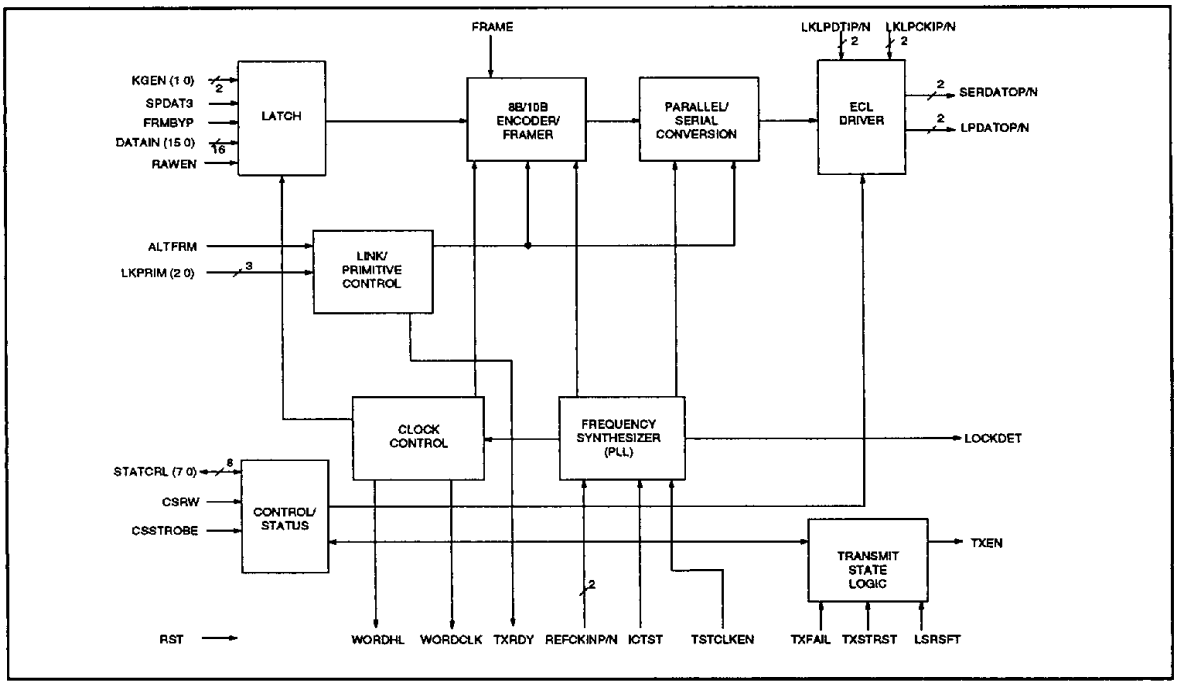
When FRAME is in the high state and a 16 bit byte pair has been latched into the S2030 by WORDCLK, the data is byte multiplexed, encoded, serialized, and shifted out onto the serial link. At the transitions of FRAME the upper byte of the input byte pair is replaced by the K28.5 framing character. It is assumed that the user will place the required D characters in the lower byte of that word and both bytes of the following word/byte pair to form a frame delimiter sequence (Please refer to Table 2 and to the ANSI X3T9.3 Fibre Channel standard document.) The WORDCLK and WORDHL outputs are provided to properly synchronize the byte pair and word pair inputs to the S2030. The encoder can be bypassed when the RAWEN input is held high, providing a simple 20 bit parallel to serial conversion function.

The chip is programmable to operate at the Fibre Channel data rates of 1062.5, 531.25, and 265.625 Mbit/s. Speed is selected through the control register. Clock synthesis from a 53.125 or 26.5625 MHz reference input is performed on-chip

8B/10B Encoder/Framer

The encoder accepts byte-wide data from the input register and multiplexer, performs the 8B/10B encoding function, and converts from a parallel to serial bit stream. The S2030 generates the K28.5 special character or an alternate K28.1 special character to correctly frame the data. In addition the KGEN<1:0> inputs can be used to generate any of the K-characters allowed by the Fibre Channel standard.

Figure 7. S2030 Block Diagram



Raw Data Mode

If the RAWEN input is held high, the encoder and the internal primitive sequence generator are bypassed. The 16 data inputs are combined with four additional inputs normally associated with the encoding function to form a 20 bit data channel. This data is clocked in, multiplexed, directly serialized, and shifted out of the device.

Control Register

The control register establishes the transmitter chip operating mode. It is written via the Status/Control (STATCRL <7:0>) data bus. Encoder enable/disable, data rate, loopback, NRZI and Offline modes are all controlled through this register. Multiplexing of the control and status registers onto the STATCRL <7:0> bus is controlled by the CSRW input pin. The control information is written to the Control register on the rising edge of the CSSTROBE signal as shown in Figure 18. Figure 9 depicts the configuration of the control register.

Transmitter State Diagram

The transmitter state machine is implemented in accordance with the requirements of Paragraphs 12.3 and 12.4 of the Fibre Channel specification. Inputs to the state machine are the input signals LSRSFT, TXFAIL, and TXSTRST, as well as Control Register bit 0 (Offline). The transmitter state diagram is shown in Figure 8. The Failure state is entered when the TXFAIL input is active. This state is "trapping" to the extent that the transmitter remains in the Failure state after TXFAIL goes inactive. As required by the Standard, the external intervention of a Control Register Offline command or a full reset is required to return to the Not Enabled state.

Figure 8. S2030 State Diagram

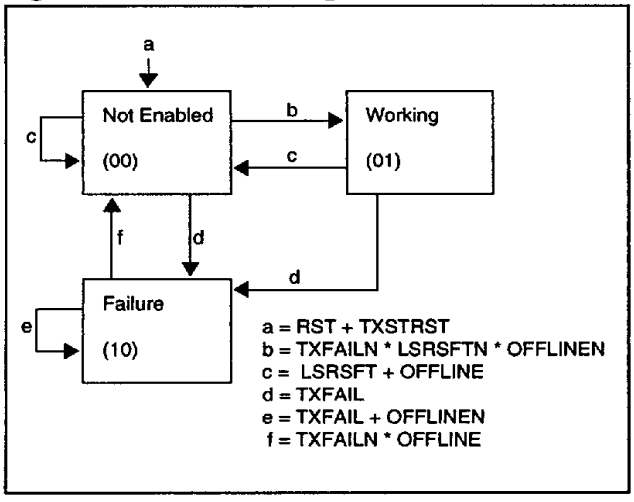
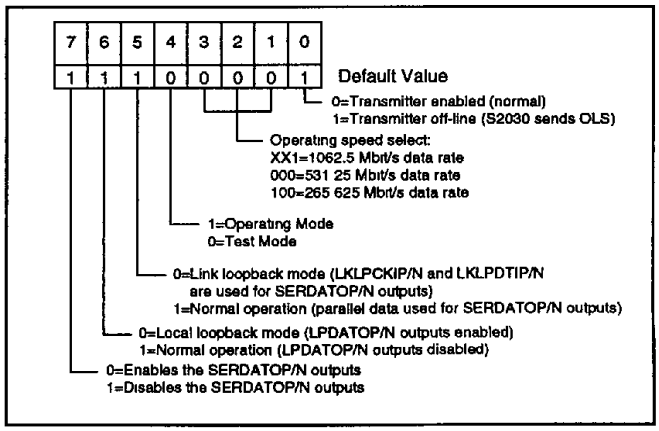


Figure 9. S2030 Control Register Configuration



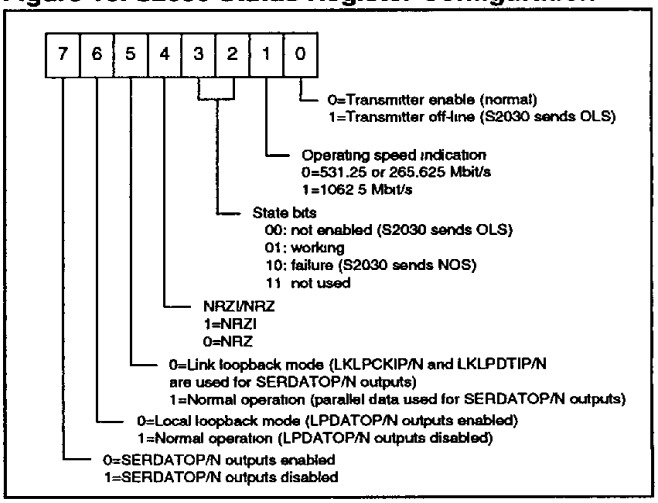
Status Register

The status register indicates the operational status of the S2030. It contains the transmitter state and the bypass and loopback indicators. It contains the transmitter state as described above and in the Fibre Channel specification. The Status data is multiplexed onto the STATCRL<7:0> bus as controlled by the CSRW input pin. The CSSTROBE signal is the actual gating signal for the status data as shown in Figure 19. The bit configuration of the status register is shown in Figure 10.

Frequency Synthesizer (PLL)

The S2030 lock detect function indicates the state of the phase-locked loop (PLL) clock synthesis unit. The S2030 will obtain phase and frequency lock within 2500 bit times after the start of receiving reference clock inputs (per the Fibre Channel specification). Upon acquisition and maintaining of lock, the LOCKDET output will go high. If lock is lost then LOCKDET will go low.

Figure 10. S2030 Status Register Configuration



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Test Functions

The S2030 has a testability input to aid in functional testing of the device. The TSTCLKEN input allows the internal voltage-controlled oscillator (VCO) to be bypassed and the reference clock substituted. This allows full functional testing of the digital portion of the chip or bypassing the internal synthesized clock with an external clock source. (See the section **Other Operating Modes** on page 3-50.)

Reference Clock Input

The reference clock input must be supplied with a differential ECL crystal clock source with 100 PPM tolerance. See Table 8 for reference clock frequencies and corresponding data transmission rates.

Link/Primitive Control

The primitive signals and sequences (IDLE, R_RDY, OLS, NOS, LR and LRR) are generated as indicated to the S2030 via the Link Primitive (LKPRIM <2:0>) inputs (See Table 5). These pins may be driven directly from the S2031 receiver chip to automatically execute the link start-up procedure defined in the Fibre Channel transmission specification. Link primitive operation requires FRAME, KGEN1, and KGEN0 to remain low (inactive). If LKPRIM<2:0> is set to 000, the S2030 will output a continuous logic zero on the serial data outputs when FRAME is low. (Please note: This is *not* the same as an encoded D0.0.) See the section Other Operating Modes on page 3-50 for details on link initialization.

Table 5. LKPRIM Input Definitions

LKPRIM <2:0> Inputs	Primitive
000	Burst mode
001 or 111	Idle word
010	*R_RDY
011	OLS
100	NOS
101	LR
110	LRR

* Not used for Link initialization

S2030 TRANSMITTER PIN DESCRIPTIONS

Input/Output Signals

Status/Control [STATCRL] <7:0>. TTL. Bidirectional 8-bit data bus for the control or status registers. Direction is controlled by the CSRW input. Please refer to Figure 18 and Figure 19 for detailed timing relationships of these signals.

Input Signals

K. Char Gen/Expanded Data Path [KGEN] <1:0>. TTL. When the S2030 is operating in the "encoded mode" (RAWEN = 0), bit 1 is used to specify data (D) or control (K) for parallel data bits 0–7. Bit 0 is used to specify data or control for parallel data bits 8–15. These bits need to be driven low when FRAME is Low for correct LKPRIM operation. When the chip operates in the "raw" mode (RAWEN = 1), bypassing the 8B/10B encoder, these 2 bits are combined with the DATAIN bits. (See Table 7.)

Expanded Data Path [SPDAT3]. TTL. When the S2030 operates in the "raw" mode, bypassing the 8B/10B encoder, this bit is combined with the DATAIN bits. See Table 7.) In encoded mode, it has no function.

Frame Bypass [FRMBYP]. TTL. In the encoded mode (RAWEN = 0), a high will cause the S2030 to encode data on the 16-bit data bus [DATAIN] for transmission, ignoring the FRAME, ALTFRM, and LKPRIM <2:0> inputs. When the S2030 operates in the "raw" mode (RAWEN = 1), bypassing the 8B/10B encoder, this bit is combined with the DATAIN bits. (See Table 7.)

Control/Status Read/Write [CSRW]. TTL. If CSSTROBE is low and CSRW is high, the status register data is enabled onto the STATCRL bus. When CSRW is low, data input to the STATCRL bus will be used as control register data and clocked in on the rising edge of CSSTROBE. (Please refer to Figures 18 and 19.)

Control/Status Strobe [CSSTROBE]. TTL. Clocks the control register on the rising edge when CSRW is Low.

Parallel Data In [DATAIN] <15:0>. TTL. Active High. 16-bit data bus which accepts input data from the subsystem.

Reset [RST]. TTL. Active Low. Master reset input. Puts the S2030 into the Not Enabled state (S2030 sends OLS.)

Reference Clock [REFCKINP/N]. Diff. ECL. Reference clock used by the PLL for frequency acquisition. The reference clock must be 53.125 MHz for 1062.5 or 531.25 Mbit/s operation, and 26.5625 MHz for 265.625 Mbit/s operation. Used for clock input when Test Clock Enabled.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the reference clock to be used in place of the VCO for testing. Allows a means of testing the functions of the chip without the use of the PLL. Also allows the bypassing of the on-chip synthesized serial clock.

Laser Safety [LSRSFT]. TTL. Active High. Forces the S2030 to the "not enabled" state.

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Transmitter Failure [TXFAIL]. TTL. Active High. Forces the S2030 to the failure state (S2030 sends NOS).

Frame [FRAME]. TTL. Rising edge forces the K28.5 signal or the alternate K28.1 signal to be transmitted to initiate a frame. Falling edge forces K28.5 or K28.1 to be transmitted to end frame. See Figure 20.

Link Primitive [LKPRIM] <2:0>. TTL. Encoded bits indicating the type of link primitive to be transmitted when FRAME is low. (See Table 5.)

Alternate Frame [ALTFRM]. TTL. Active High. Indicates the transmission of a K28.1 character in place of the K28.5 in the SOF, EOF, and Idles.

Tx State Reset [TXSTRST]. TTL. Active High. Forces the S2030 into the Not Enabled state (S2030 sends OLS).

Link Loop Data Inputs [LKLPDTIP/N]. Diff. ECL. Retimed serial data inputs. In general, these inputs come from the S2031 and provide a means of looping the data out of the S2030 without processing, other than retiming.

Link Loop Clock Inputs [LKLPCKIP/N]. Diff. ECL. Recovered clock input from the S2031. Provides a means of looping the data out of the S2030 without processing, other than retiming.

IC Test [ICTST]. TTL. Tie to ground.

Raw Mode Enable [RAWEN]. TTL. Active High. When high, puts the chip into the "raw" mode, enabling the 20-bit data path, and bypassing the 8B/10B encoder. When low, the chip is in the encoded mode, uses the 16-bit data path, and encodes this data with the 8B/10B encoder. This input affects the usage of the KGEN1, KGEN0, SPDAT3, and FRMBYP inputs. (See Table 7.)

Output Signals

Word Clock [WORDCLK]. TTL. Word clock for encoder. The encoder operates synchronously to this clock.

Lock Detect [LOCKDET]. TTL. Active High. Indicates that the PLL VCO is locked to the REFCKINP/N signal.

Local Loopback Data [LPDATOP/N]. Diff. ECL. Serial data to the S2031 used for loopback test.

Serial Data Out [SERDATOP/N]. Diff. ECL. Serial data to the fiber optic transmitter.

Transmitter Ready [TXRDY]. TTL. Active High. Indicates to the subsystem that Idle sequences are being transmitted. Means that the transmitter is ready to transmit data.

Transmitter Enable [TXEN]. TTL. Active High. Used to enable the optical or electrical driver. Goes low if S2030 is not in the working state.

Word H/L [WORDHL]. TTL. Active High. Word clock divided by two. The Frame input should be valid on the rising edge of WORDHL to guarantee correct word boundaries.

S2031 RECEIVER

Architecture/Functional Description

The S2031 receiver chip is designed to implement the ANSI X3T9.3 Fibre Channel Specification Receiver functions through the Fibre Channel physical, transmission, and portions of the signaling protocol layers. A block diagram showing the basic chip function is provided in Figure 11.

Whenever a signal is present, the S2031 attempts to achieve synchronization on both bit and transmission-word boundaries of the received encoded bit stream. When word synchronization is achieved, the S2031 enters the Synchronization Acquired state and provides the decoded data on its parallel outputs. A synchronization failure on either a bit or transmission-word boundary causes a loss-of-synchronization (LOS) error.

The S2031 accepts serial encoded data from a fiber optic or coaxial interface and decodes the SOF characters, data bits, and EOF characters. Clock recovery is performed on-chip, with the output data presented to the Fibre Channel transmission layer as 16-bit parallel data. The chip is programmable to operate at the Fibre Channel specified operating frequencies of 1062.5, 531.25, and 265.625 Mbit/s. Speed is selected through the control register.

Decoder

The decoder accepts a serial bit stream, does serial to byte-wide parallel conversion, and performs the 10B/8B decoding function. The S2031 recognizes the K28.5 symbol, or an alternate programmable K28.1 special character, to correctly frame the data.

Control Register

The control register establishes the chip operating mode. It is written via the Control/Status (STATCRL <7:0>) data bus. Framing mode, data rate, loopback mode, NRZI mode, are all controlled through this register. Multiplexing of the control and status registers onto the STATCRL<7:0> bus is controlled by the CSRW input pin. The control information is actually written to the Control register on the rising edge of the CSSTROBE signal as shown in Figure 18. Figure 13 depicts the bit configuration of the control register word.

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Receiver State Diagram

The receiver state machine is implemented in accordance with the requirements of Paragraphs 12.1 and 12.2 of the Fibre Channel specification. Inputs to the state machine are the external input signals RST, RXSTRST, SIGLOS and the internal signals from the Sync detection and SYNCLOST sequencer. The SYNCLOST sequencer implements the loss of sync procedure described in Paragraph 12.1.3.1 of the Fibre Channel specification. The establishment of bit synchronization (indicated by LOCKDET = 1) and the detection of three successive properly formatted primitive sequences containing the selected K-characters will set the Sync Acquired (10) state and arm the 5 state SYNCLOST sequencer. The sequencer counts the number of Ordered Sets or Primitive Sequences received that contain errors and are separated by less than two non-errored Ordered Sets. The detection of two successive non-errored Ordered Sets reduces the count by one. If the error count rises to four, SYNCLOST is set and the receiver state machine is forced to the Loss of Sync (00) state. Loss of Sync is also set if bit synchronization is lost, either through SIGLOS active, or by the failure of the runlength and density checks. The receiver will recover to the Sync Acquired state only if bit and word synchronization are reestablished and three error-free Ordered Sets are again detected. No external intervention is required to reacquire sync. The assertion of RST or RXSTRST will force and hold the Reset (01) state. The receiver state diagram and the SYNCLOST Sequencer state diagram is shown in Figure 12.

Figure 12. S2031 State Diagrams

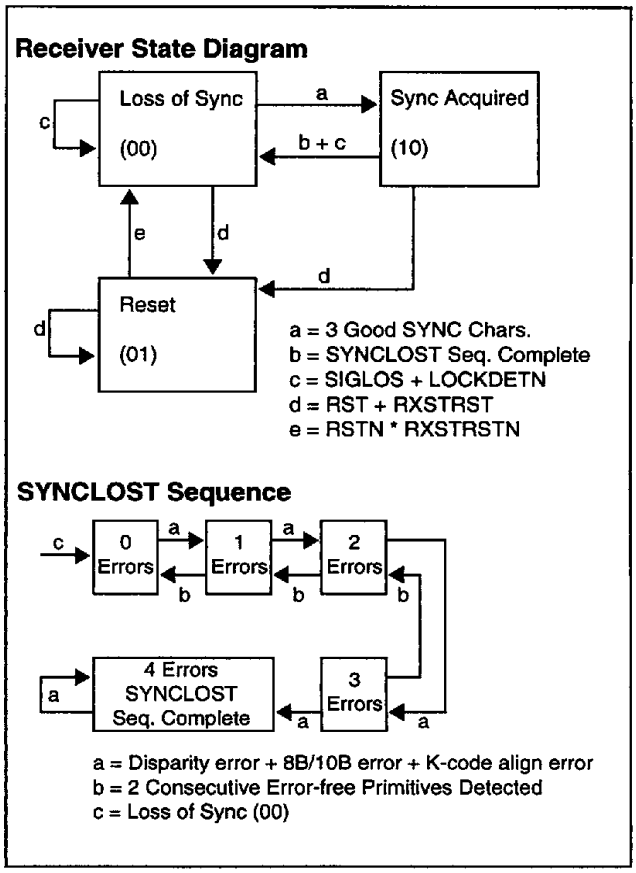


Figure 11. S2031 Block Diagram

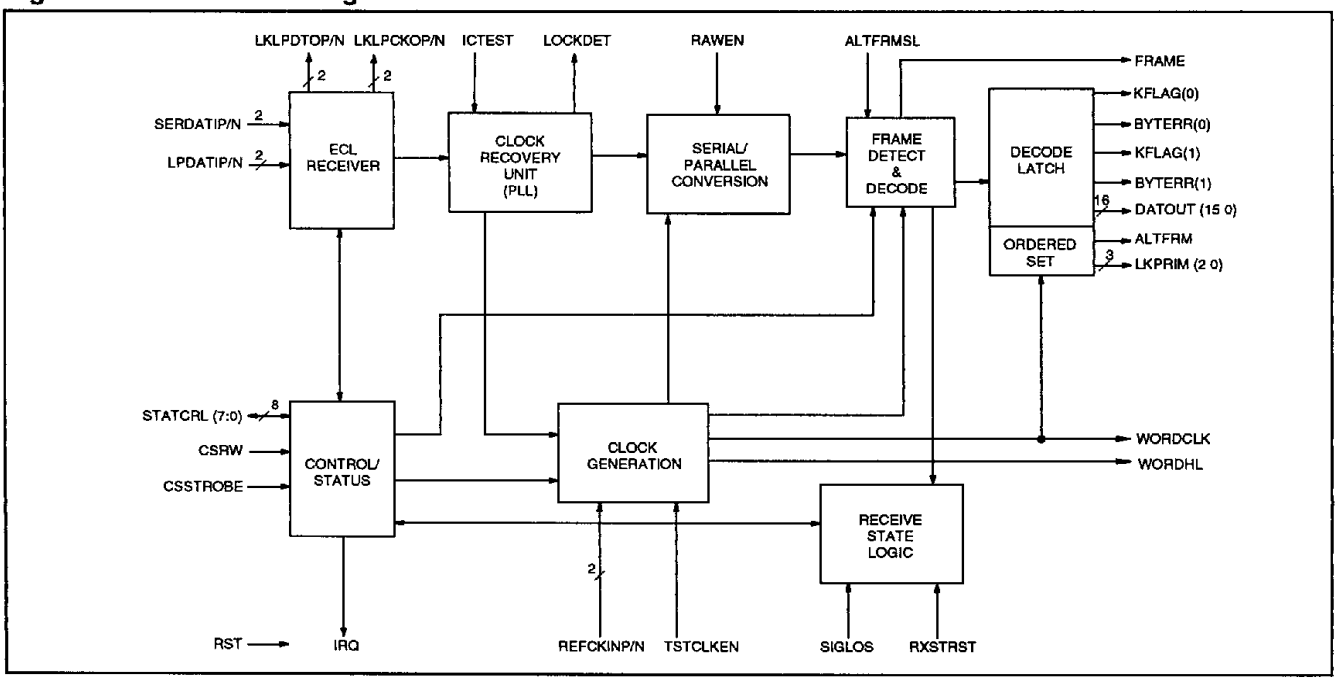


Figure 13. S2031 Control Register Configuration

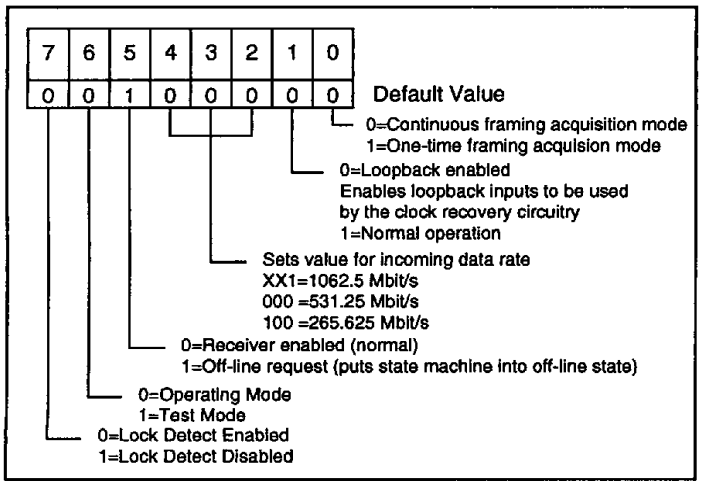
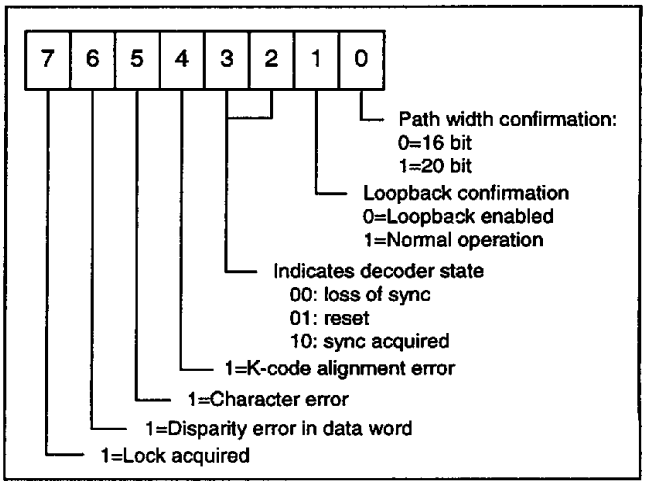


Figure 14. S2031 Status Register Configuration



Status Register

The status register contains information to be read by the Fibre Channel signaling protocol layer. It indicates the operational status of the S2031. If any of the error bits in the status register are set active, the IRQ flag will be raised indicating an error condition has occurred. The status register indicates disparity errors, illegal 8B/10B words, special character alignment errors and the decoder bypass and loopback states. It contains the receiver state as described above and in the Fibre Channel specification. The Status data is multiplexed onto the STATCRL<7:0> bus as controlled by the CSRW input pin. The CSSTROBE signal is the actual gating signal for the status data as shown in Figure 19. The bit configuration of the status register is shown in Figure 14.

Lock Detect

The lock detect function on the S2031 has been optimized for the anticipated needs of Fibre Channel systems. In general, the Clock Recovery macro decides whether to acquire lock to the serial data inputs or the reference clock inputs using a simple state machine. This state machine makes its decisions based on the run length and transition density of the serial data inputs. If the serial data has a run length less than 64 bit times and a transition density greater than 12.5%, the run length and transition density checks are satisfied and the lock detect signal goes high after approximately 2000 serial clock cycles. (The 2000 serial clock cycles are required to guarantee that the recovered clock is centered in the eye opening of the received data.) During the 2000 serial clock cycle time, the serial data is sent out of the CRU, but exhibits a BER which initially exceeds the 10^{-12} requirement.

If at any time during the reception of data the run length or transition density checks are violated, the state machine forces the VCO to lock to the reference clock. The lock detect signal goes low when this occurs. This is required to guarantee that the VCO maintains the correct frequency in the absence of data.

The internal lock detect state machine can be disabled through bit 7 of the control register. When the lock detect state machine is disabled, the LOCKDET output will be held inactive and the PLL will remain locked to the reference clock regardless of the run length or transition density of the incoming serial bit stream.

In any transfer of PLL control from the serial data to the reference clock, the WORDCK output remains phase continuous and glitch free assuring the integrity of downstream clocking.

Initialization

For operation at 531.25 Mbit/s, the Default values of the Control register during a 20 ms reset (RST=0) allow the VCO to properly lock to the 53 MHz reference. The default values enable the run length and density detection functions of the lock detect state machine. For operation at 1062.5 Mbit/s a Control register write can select the operating speed (XX1 on bits 4, 3 and 2) and enable the lock detect (bit 7).

For 265.625 Mbit/s operation, two write cycles of the Control Register are required. Since the Default Values at reset select 531.25 Mbit/s mode (assuming 53 MHz reference), but 265.625 Mbit mode requires a 26 MHz reference, reset places the VCO at its lowest frequency.

A Control Register write with 100 in bits 4, 3 and 2, and 1 in bit 7 disables lock detect and allows the VCO to properly lock to the 26 MHz reference. After at least 20 ms a second Control Register write with bit 7 set to zero will enable lock detect, and thus normal operation.

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Reference Clock Input

The reference clock input must be supplied with a differential ECL crystal clock source with 100 PPM tolerance. See Table 9 for reference clock frequencies and corresponding data transmission rates.

Delimiter/Primitive Decoding

The primitive signals and sequences (IDLE, OLS, NOS, LR, and LRR) are decoded and indicated to the Fibre Channel signaling protocol layer via the link primitive (LKPRIM) outputs. (See Table 6.) These pins may be used to directly drive the transmitter chip to execute the link start-up procedure defined in the Fibre Channel specification. The primitive signal and sequence ordered sets are also output to the Fibre Channel signaling protocol layer via the parallel data bus.

Table 6. LKPRIM Output Definitions

Primitive	LKPRIM <2:0> Outputs
No primitive received	111
LRR	001
Unused	010
NOS or off line state	011
Fail state	100
OLS	101
LR	110
Idle	111

S2031 RECEIVER PIN DESCRIPTIONS

Input/Output Signals

Control/Status [STATCRL] <7:0>. TTL. Bidirectional 8 bit data bus for the control or status registers. Direction is controlled by the CSRW input. Please refer to Figure 18 and Figure 19 for detailed timing relationships of these signals.

Input Signals

Control/Status Enable [CSRW]. TTL. If CSSTROBE is low and CSRW is high, the status register data is enabled onto the STATCRL bus. When CSRW is low, control register data will be clocked on the rising edge of CSSTROBE.

Reset [RST]. TTL. Active Low. Master reset input. Causes S2031 to output the Offline primitive on the LKPRIM Lines.

Serial Data [SERDATIP/N]. Diff. ECL. Serial data from the fiber optic receiver.

Loopback Data [LPDATIP/N]. Diff. ECL. Serial data from the S2030 used for loopback test.

Reference Clock [REFCKINP/N]. Diff. ECL. Reference clock used by the PLL for initial frequency acquisition. The reference clock must be 53.125 MHz for both 1062.5 and 531.25 Mbit/s operation, and 26.5625 MHz for 265.625 Mbit/s operation. Used as clock input when Test Clock Enable active.

Test Clock Enable [TSTCLKEN]. TTL. Active High. Enables the REFCKINP/N to be used in place of the VCO for testing.

Signal Loss [SIGLOS]. TTL. Active High. Indicates a loss of signal from the fiber optic receiver. This input will cause the state machine to enter the Loss of Sync state. This signal will also force the PLL to acquire frequency lock to the reference clock in order to maintain downstream clocking in the absence of data.

Control/Status Strobe [CSSTROBE]. TTL. Clocks the control register on the rising edge when CSRW is low.

Alternate Frame Select [ALTFRMSL]. TTL. When high a K28.1 special character will be used for framing. When low a K28.5 special character will be used for framing.

Rx State Reset [RXSTRST]. TTL. Active High. Forces the S2031 into the Reset state.

Raw Mode Enable [RAWEN]. TTL. When high enables the 20-bit data path, bypassing the decoder. (See Table 7.)

IC Test [ICTEST]. TTL. Tie to ground.

Output Signals

Interrupt Request [IRQ]. TTL. Active High. Indicates an error has occurred which can be read from the status register.

Parallel Data Out [DATOUT] <15:0>. TTL. 16-bit data bus which outputs 16-bit parallel data to the subsystem. Data is decoded from the serial or loop data input.

K Character Flag/Expanded Data Path [KFLAG] <1:0>. TTL. Active High. Indicates the decoded data byte is a special character (K byte). (See Table 1.) When the S2031 is operating in the "encoded mode" (RAWEN = 0), KFLAG0 is used to indicate whether decoded control (K) or data (D) information is being output on parallel data bits 15–8. KFLAG1 provides the same indication for parallel data bits 7–0. Control information is indicated whenever KFLAG0 or KFLAG1 is high; a low indicates data. Also used for the expanded data path in Raw Mode. (See Table 7.)

Byte Error Flag/Expanded Data Path [BYTERR] <1:0>. TTL. Active High. Indicates the received byte contained a character or disparity error. Also used for the expanded data path in Raw Mode. (See Table 7.)

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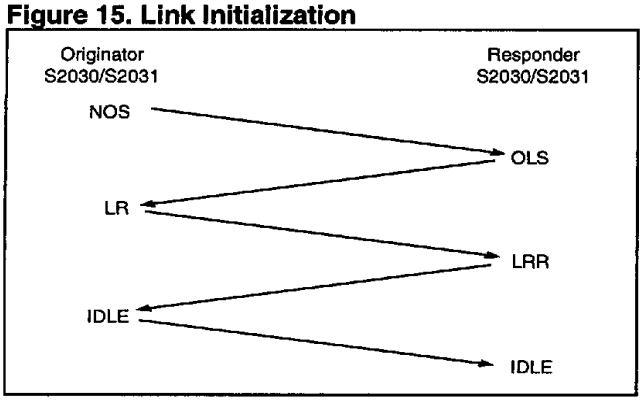
Figure 15. Link Initialization



Word Clock [WORDCLK]. TTL. Word clock for data bus. Data is valid on the rising edge.

Link Primitive [LKPRIM] <2:0>. TTL. Encoded bits indicating the type of link primitive received. (See Table 6.)

Alternate Frame [ALTFRM]. TTL. Indicates the reception of a K28.1 character when ALTFRMSL is low. Indicates the reception of K28.5 character when ALTFRMSL is high.

Link Loop Data Outputs [LKLPDTOP/N]. Diff. ECL. Serial data outputs retimed by the onboard clock and data recovery unit from the serial data input.

Link Loop Clock Outputs [LKLPCKOP/N]. Diff. ECL. Recovered clock output from the serial data input.

Lock Detect [LOCKDET]. TTL. Active High. Indicates that the S2031 has achieved bit synchronization (PLL lock). When bit sync is lost, the S2031 outputs the Offline primitive, the IRQ line is asserted and bit 7 of the status register is low.

Frame [FRAME]. TTL. Active High. Indicates that the receiver has received a framing special character. Either a K28.5 or a K28.1 can be used for framing as set by the ALTFRMSL pin.

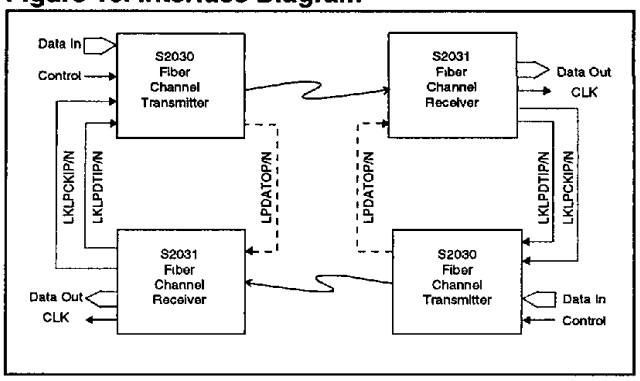
Word H/L [WORDHL]. TTL. Active High. Word clock divided by two. The rising edge of WORDHL indicates the beginning of a primitive sequence, or a 4 byte data word.

OTHER OPERATING MODES

Link Initialization

Link initialization is required after power-on or Reset in accordance with Fibre Channel Specifications. Table 4 defines the primitive sequences used, and Figure 15 defines the link initialization protocol implemented by the S2030/S2031 chipset. At the conclusion of link initialization, both should be transmitting and receiving Idles. If at any time the Frame input is activated, the data present on the data bus will be transmitted in lieu of the Link Primitive.

Figure 16. Interface Diagram



Raw Mode

Encoder and decoder raw data mode functions are provided per the Fibre Channel specification. An NRZI conversion is also available. In raw mode the data bus is expanded to form a 20-bit word. Raw mode is enabled by setting the RAWEN pin high.

Loopback Modes

Two types of loopback mode are supported: local loopback and link loopback. (See Figure 16.) The local loopback mode requires a S2030 and a S2031. When enabled, serial encoded data from the S2030 transmitter is sent to the S2031 receiver, where the clock is extracted and the data is decoded. The parallel data is then sent to the subsystem for verification. This loopback mode provides the capability to perform offline testing of the interface to guarantee the integrity of the serial channel before enabling the transmission medium, and also allows system diagnostics.

The link loopback mode provides a means for link testing. When link loopback mode is enabled, the transmitter accepts serial clock and data from the receiver chip. The serial data is reclocked using the link loopback clock to minimize distortion, and then transmitted via the serial data output pins. Link loopback can also be used to implement a repeater function, with clock jitter and data distortion determining the number of repeaters allowed.

Test Modes

Other chip test modes are available. The control interface test mode allows testing of the control interface via loopback of the control register bits to the status register.

The Test Clock Enable pin provides a PLL bypass mode that can be used for operating the digital area of the chip. In this mode clock signals are input through the reference clock pins. This can be used for testing the device during the manufacturing process, during an off-line self-test, or if an external clock source is preferred.

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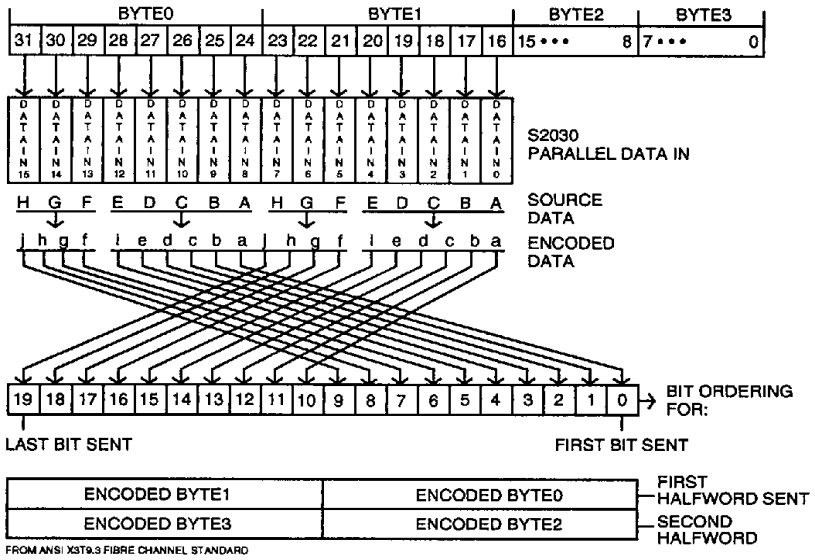
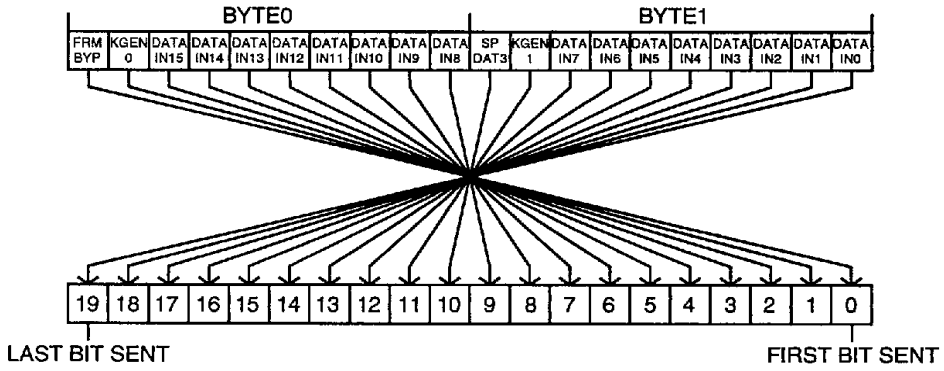
Table 7. Transmit/Receive Bit Order

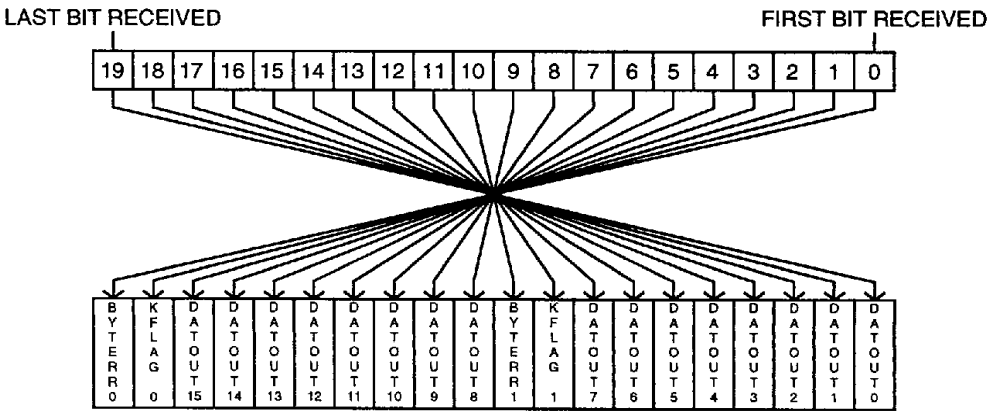
Encoded Mode



Raw Mode Transmit



Raw Mode Receive



S2030 TRANSMITTER PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	ECL GND	26	ECL GND	51	PLLVEE3	76	ECL GND
2	NC	27	VCC	52	REFCKINP	77	STATCRL0
3	DATAIN15	28	VCC	53	PLLGND3	78	STATCRL1
4	DATAIN14	29	NC	54	REFCKINN	79	STATCRL2
5	DATAIN13	30	TTL GND	55	PLLVEE4	80	TTL GND
6	DATAIN12	31	ALTFRM	56	PLLVEE4	81	STATCRL3
7	ECL GND	32	FRAME	57	SERDATOP	82	VEE
8	DATAIN11	33	LKPRIM0	58	PLLGND4	83	CSSTROBE
9	DATAIN10	34	LKPRIM1	59	SERDATON	84	CSRW
10	DATAIN9	35	LKPRIM2	60	LPDATOP	85	STATCRL4
11	WORDCLK	36	VEE	61	PLLGND4	86	VEE
12	VEE	37	TXFAIL	62	LPDATON	87	STATCRL5
13	VEE	38	ECL GND	63	PLLGND2	88	ECL GND
14	WORDHL	39	LSRSFT	64	LKLPCKIP	89	STATCRL6
15	DATAIN8	40	VEE	65	NC	90	VEE
16	DATAIN7	41	TXSTRST	66	LKLPCKIN	91	STATCRL7
17	DATAIN6	42	TXEN	67	NC	92	RAWEN
18	DATAIN5	43	TXRDY	68	NC	93	SPDAT3
19	ECL GND	44	VEE	69	LKLPDTIP	94	KGEN1
20	DATAIN4	45	ICTST	70	PLLVEE2	95	FRMBYP
21	DATAIN3	46	TTL GND	71	LKLPDTIN	96	TTL GND
22	DATAIN2	47	RST	72	PLLVEE0	97	KGEN0
23	DATAIN1	48	TSTCLKEN	73	PLLGND0	98	VCC
24	DATAIN0	49	LOCKDET	74	PLLGND1	99	VCC
25	ECL GND	50	ECL GND	75	PLLVEE1	100	ECL GND

S2031 RECEIVER PINOUT

PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME	PIN NO.	NAME
1	ECLGND	26	ECLGND	51	PLLVEE3	76	ECLGND
2	DNC	27	VCC	52	REFCKINP	77	STATCRL0
3	DATOUT7	28	VCC	53	PLLGND3	78	STATCRL1
4	DATOUT6	29	WORDHL	54	REFCKINN	79	STATCRL2
5	DATOUT5	30	TTL GND	55	PLLVEE4	80	TTL GND
6	DATOUT4	31	ALTFRM	56	PLLVEE4	81	STATCRL3
7	ECLGND	32	FRAME	57	LKLPDTON	82	VEE
8	DATOUT3	33	LKPRIM0	58	PLLGND4	83	CSSTROBE
9	DATOUT2	34	LKPRIM1	59	LKLPDTOP	84	CSRW
10	DATOUT1	35	LKPRIM2	60	LKLPCKON	85	STATCRL4
11	WORDCLK	36	VEE	61	PLLGND4	86	VEE
12	VEE	37	ALTFRMSL	62	LKLPCKOP	87	STATCRL5
13	VEE	38	ECLGND	63	PLLGND2	88	ECLGND
14	PAROUT	39	RXSTRST	64	SERDATIN	89	STATCRL6
15	DATOUT0	40	VEE	65	NC	90	VEE
16	DATOUT15	41	RAWEN	66	SERDATIP	91	STATCRL7
17	DATOUT14	42	ICTEST	67	NC	92	IRQ
18	DATOUT13	43	SIGLOS	68	NC	93	BYTERR1
19	ECLGND	44	VEE	69	LPDATIN	94	KFLAG1
20	DATOUT12	45	TESTRST	70	PLLVEE2	95	BYTERR0
21	DATOUT11	46	TTL GND	71	LPDATIP	96	TTL GND
22	DATOUT10	47	RST	72	PLLVEE0	97	KFLAG0
23	DATOUT9	48	TSTCLKEN	73	PLLGND0	98	VCC
24	DATOUT8	49	LOCKDET	74	PLLGND1	99	VCC
25	ECLGND	50	ECLGND	75	PLLVEE1	100	ECLGND

Power Supply Connections:

VCC	+5V	ECL GND	0V	NC	No Connect
VEE	–4.5V/–5.2V	PLLGND	0V	DNC	Do Not Connect
TTL GND	0V	PLLVEE	–4.5V/–5.2V	TESTRST	0V

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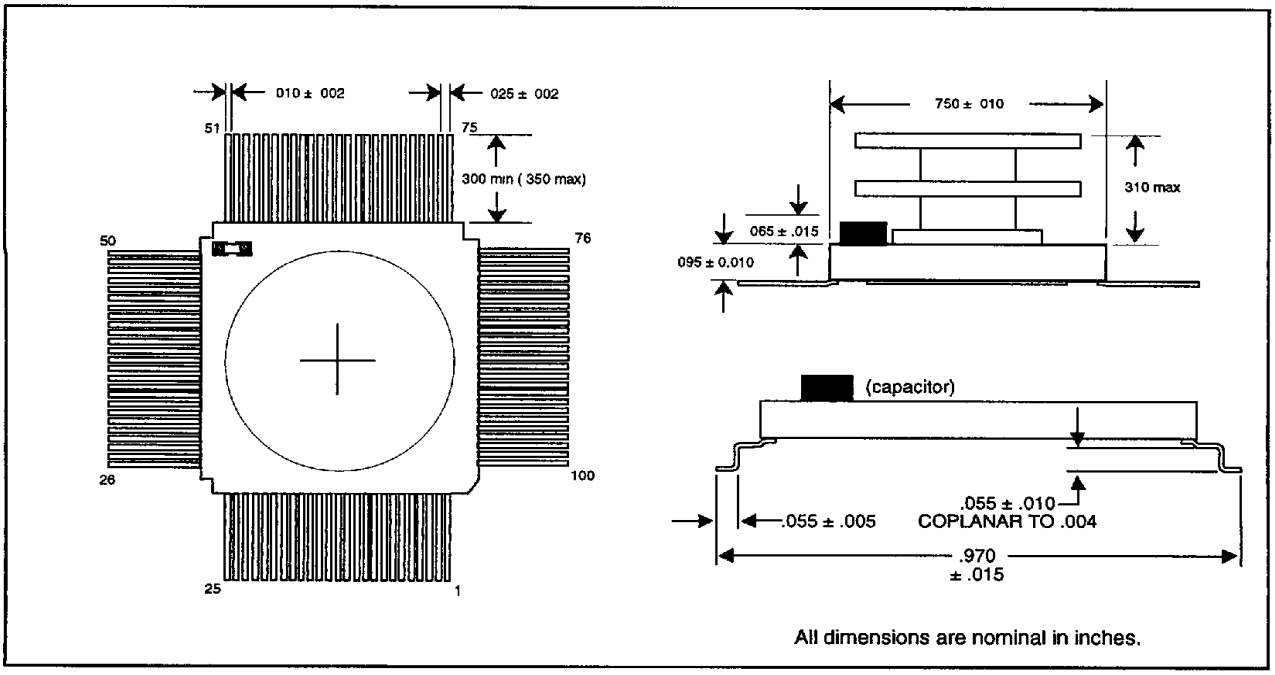
Figure 17. 100-pin LDCC Package



3

ABSOLUTE MAXIMUM RATINGS

ECL Supply Voltage V_{EE}	–8.0VDC
ECL Input Voltage	GND to –3V
ECL Output Source Current (continuous)	–50mA DC
TTL Supply Voltage V_{CC}	7.0V
TTL Input Voltage	5.5V
Operating Junction Temperature T_J	+130°C
Storage Temperature	–65° to +150°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	NOM	MAX	UNITS
ECL Supply Voltage (V_{EE})	–4.2	–4.5/–5.2	–5.46	V
TTL Supply Voltage (V_{CC})	4.75	5.0	5.25	V
TTL Output Current Low (I_{OL})			8	mA
Ambient Temperature	0		70	°C
Junction Temperature			130	°C
S2030 $-I_{CC}$ $-I_{EE}$		93 –548	127 –745	mA mA
S2031 $-I_{CC}$ $-I_{EE}$		168 –526	239 –736	mA mA

ECL INPUT/OUTPUT DC CHARACTERISTICS

Symbol	Parameter	Test Conditions	Signal Name	Min	Max	Unit
V_{IL}[1]	Input LOW Voltage	Guaranteed Input LOW Voltage for all differential inputs		-0.85	-2.00	Volts
V_{IH}[1]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all differential inputs		-0.60	-1.75	Volts
V_{ID}[1,2,6]	Input DIFF Voltage	Guaranteed Input DIFF Voltage for all differential inputs		0.25	1.40	Volts
V_{IL}	Input LOW Current	V_{EE} =MAX, V_{IL}=-1.55V	LKLPDTIP/N[4], LKLPCKIP/N[4], SERDATIP/N[5], LPDATIP/N[5],	-4.40	-5.80	mA
		V_{EE} =MAX, V_{IL}=-1.55V	REFCLKINP/N[4,5]	-1.00	20.00	uA
V_{IH}	Input HIGH Current	V_{EE} =MAX, V_{IH}=-1.05V	LKLPDTIP/N[4], LKLPCKIP/N[4], SERDATIP/N[5], LPDATIP/N[5],	4.40	5.80	mA
		V_{EE} =MAX, V_{IH}=-1.05V	REFCLKINP/N[4,5]	-1.00	20.00	uA
V_{OL}[3,7]	Output LOW Voltage	100Ω between differential outputs		-0.90	-2.50	Volts
V_{OH}[3,7]	Output HIGH Voltage	100Ω between differential outputs		-0.50	-2.10	Volts
V_{OD}[2,3]	Output DIFF Voltage	100Ω between differential outputs		0.40	1.00	Volts

1. Differential ECL Inputs
2. V_{ID} and V_{OD} represent differential voltage swing specifications.
3. Source Terminated Differential ECL Compatible Outputs
4. S2030 Signals
5. S2031 Signals
6. When not used, tie the positive differential ECL pin to ground and the negative differential ECL pin to VEE via a 3.9K resistor.
7. These levels are fully compatible with standard ECL 10K/100K levels at either VEE=–4.5V or –5.2V.

TTL INPUT/OUTPUT DC CHARACTERISTICS [1]

Symbol	Parameter	Test Conditions	Min	Max	Unit
V_{IL}[2]	Input LOW Voltage	Guaranteed Input LOW Voltage for all inputs		0.8	Volts
V_{IH}[2]	Input HIGH Voltage	Guaranteed Input HIGH Voltage for all inputs	2.0		Volts
I_{IL}	Input LOW Current	V_{CC} =MAX, V_{IN}=0.5V	-400.0		uA
I_{IH}	Input HIGH Current	V_{CC} =MAX, V_{IN}=2.7V		50.0	uA
I_{I}	Input HIGH Current at Max VCC	V_{CC} =MAX, V_{IN}=5.25V		1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} =MAX, V_{OUT}=0.5V	-25.0	-100.0	mA
I_{OZL}	Output Three-State Current LOW-Output Macro	V_{CC} =MAX, V_{OL} =0.4V	-50.0	50.0	uA
I_{OZH}	Output Three-State Current HIGH-Output Macro	V_{CC} =MAX, V_{OH} =2.4V	-50.0	50.0	uA
V_{IK}	Input Clamp Diode Voltage	V_{CC} =MIN, V_{IN}=-18.0mA	-1.2		Volts
V_{OL}	TTL Output LOW Voltage	V_{CC} =MIN, V_{OL} =8mA		0.5	Volts
V_{OH}	TTL Output HIGH Voltage	V_{CC} =MIN, V_{OH}=-1.0mA	2.4		Volts

1. Typical limits are at 25°C, V_{cc} = 5.0V.
2. These input levels provide a zero noise immunity and should only be tested in a static, noise-free environment.
3. These conditions will be met with a 70°C ambient airflow of 400 LFPM.

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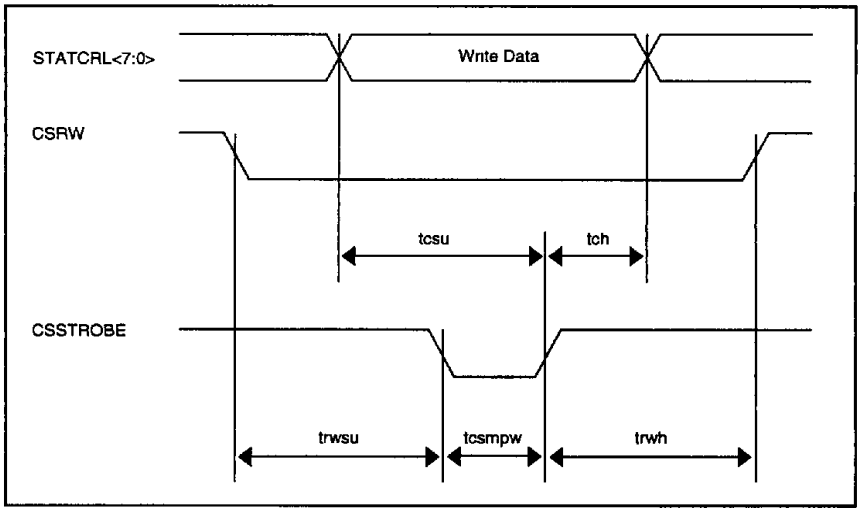
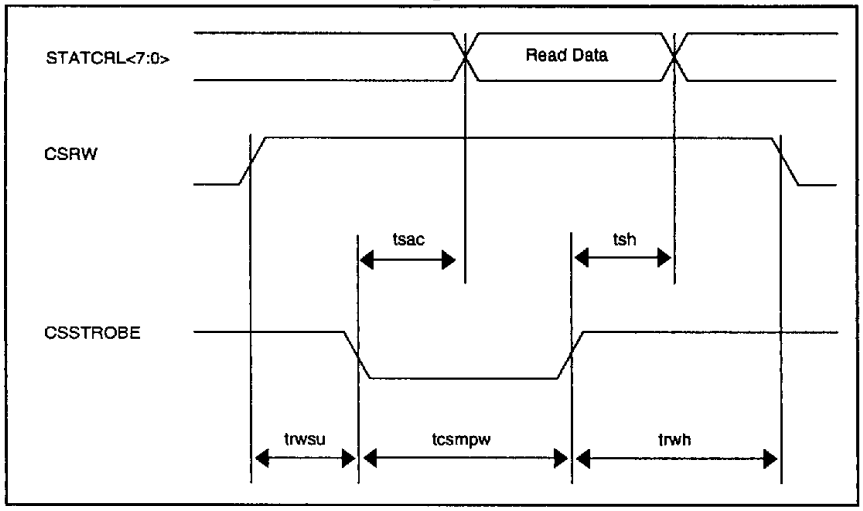
Figure 18. S2030/S2031 Control Register Write Access



Symbol	Description	Min	Max	Units
trwsu	CSRW setup time before CSSTROBE goes low	5		ns
trwh	CSRW hold time after CSSTROBE rising edge	5		ns
tcsu	STATCRL<7:0> setup time before CSSTROBE rising edge	5		ns
tch	STATCRL<7:0> hold time after CSSTROBE rising edge	5		ns
tcsmpw	CSSTROBE minimum pulse width	15		ns

Figure 19. S2030/S2031 Status Register Read Access



Symbol	Description	Min	Max	Units
trwsu	CSRW setup time before CSSTROBE goes low	5		ns
trwh	CSRW hold time after CSSTROBE rising edge	5		ns
tsac	Time to STATCRL<7:0> valid after CSSTROBE goes low		10	ns
tsh	STATCRL<7:0> hold time after CSSTROBE rising edge		2	ns
tcsmpw	CSSTROBE minimum pulse width	15		ns

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Figure 20. Transmitter Timing Diagram

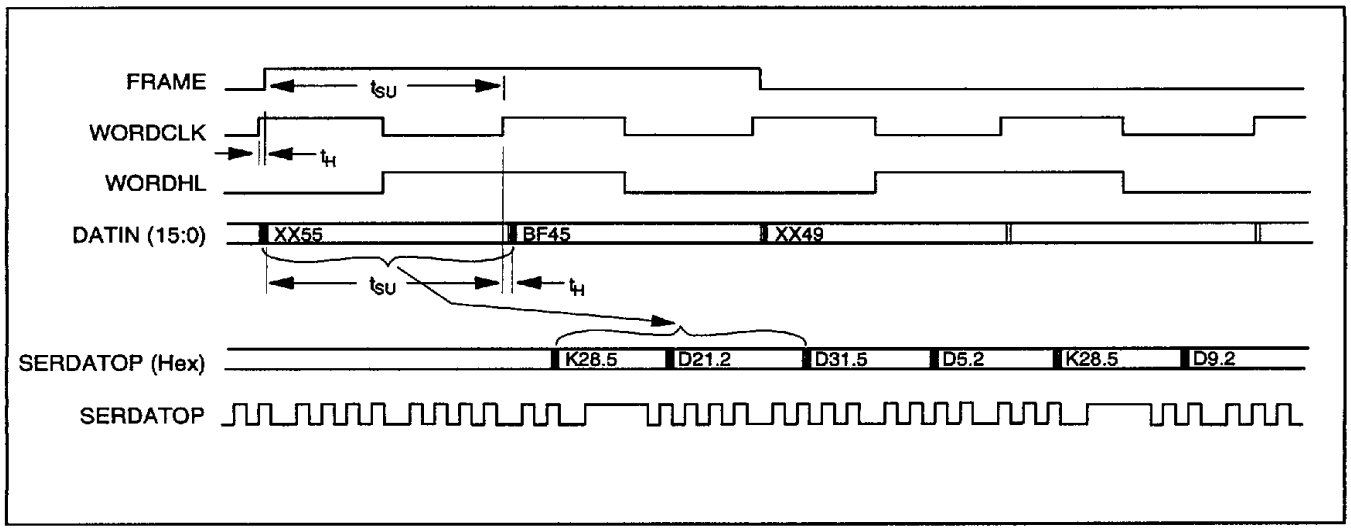

Table 8. Transmitter Timing Table

Symbol	Description	Data Transmission Rate			Units
		1062.5 Mbit/s	531.25 Mbit/s	265.625 Mbit/s	
t_{SU}	Setup time, minimum	1	1	1	ns
t_H	Hold time, minimum	2	2	2	ns
f_{WDCK}	Word clock frequency	53.125	26.5625	13.28125	MHz
f_{WDHL}	Word high/low frequency	26.5625	13.28125	6.64063	MHz
f_{REF}	Reference clock frequency	53.125	53.125	26.5625	MHz

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Figure 21. Receiver Timing Diagram (Receiving Ordered Sets)

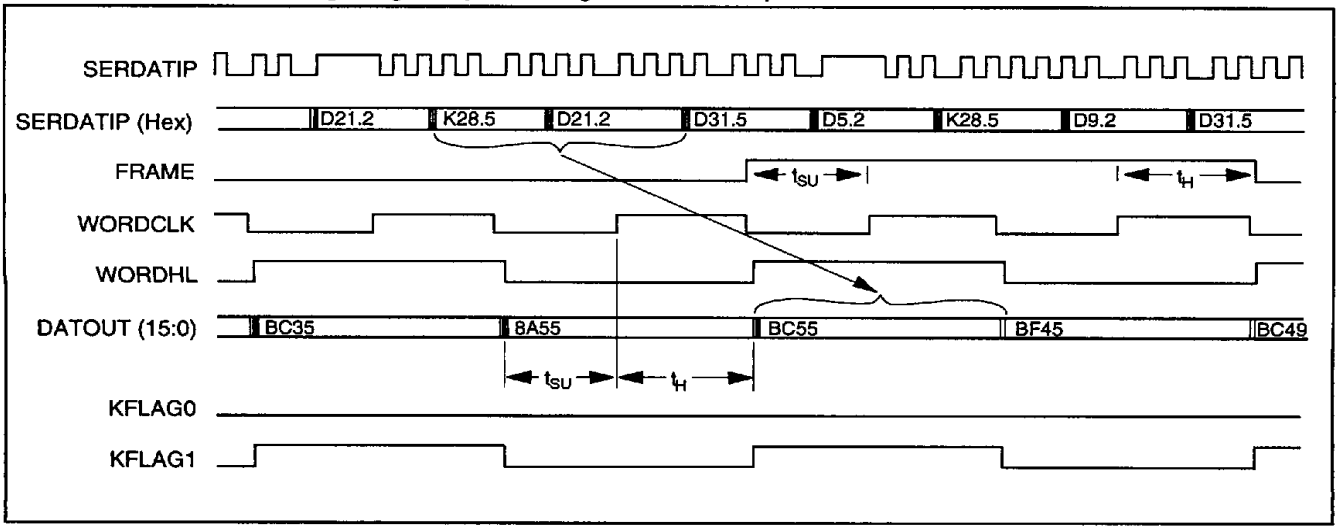
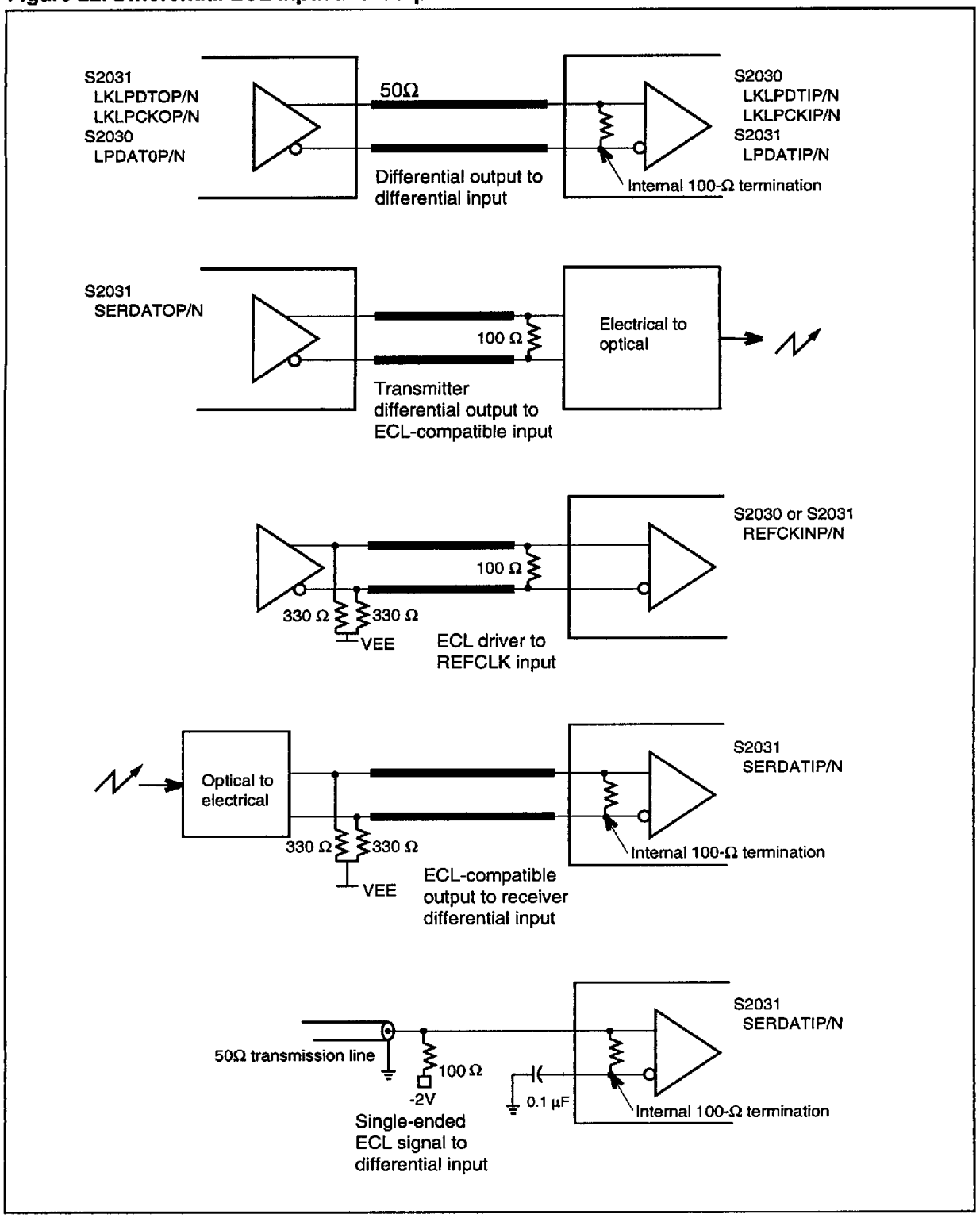


Table 9. Receiver Timing Table

Symbol	Description	Data Transmission Rate			Units
		1062.5 Mbit/s	531.25 Mbit/s	265.625 Mbit/s	
t_{SU}	Setup time, minimum	5	5	5	ns
t_H	Hold time, minimum	5	5	5	ns
f_{WDCK}	Word clock frequency	53.125	26.5625	13.28125	MHz
f_{WDHL}	Word high/low frequency	26.5625	13.28125	6.64063	MHz
f_{REF}	Reference clock frequency	53.125	53.125	26.5625	MHz

Figure 22. Differential ECL Input and Output Termination



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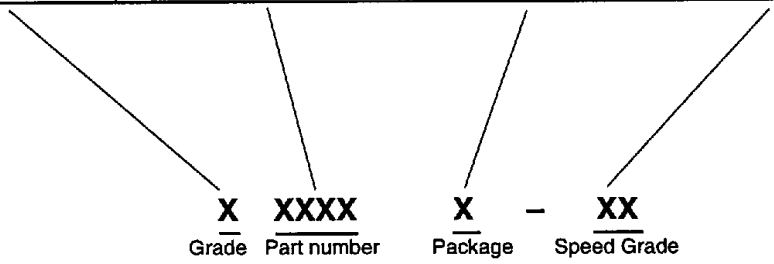
Ordering Information

GRADE	TRANSMITTER	PACKAGE	SPEED GRADE
S—commercial	2030	A–100 LDCC with straight leads B–Die C–100 LDCC leadformed with heatsink unattached	2–265.625 Mbit/s 5–531.25 Mbit/s 10–1062.5 Mbit/s

GRADE	RECEIVER	PACKAGE	SPEED GRADE
S—commercial	2031	A–100 LDCC with straight leads B–Die C–100 LDCC leadformed with heatsink unattached	2–265.625 Mbit/s 5–531.25 Mbit/s 10–1062.5 Mbit/s



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