# S-2510A

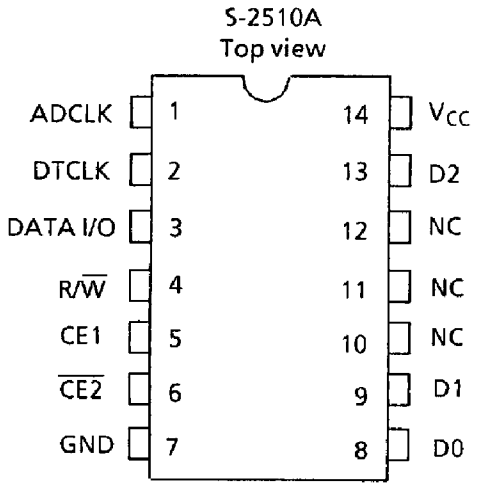
## 2560-bit CMOS static RAM

The S-2510A is a 2560-bit complete CMOS static RAM. Addresses and data are input or output in serial for easy interfacing, so it is suitable for expansion of telephone memories.

## ■ Features

- Low standby current:
  0.01 μA typ. 0.25 μA max. $V_{CC}$ = 1.5 V
- Low data retention voltage: 1.0 V min.
- Wide operating voltage range:
  1.16 V to 5.5 V
- Interface is available for connecting only 4 pins
- Data length is set by D0, D1, and D2
- 14-pin DIP package

## ■ Pin Assigmment




| | |
|---|---|
| ADCLK | Address clock |
| DTCLK | Data clock |
| DATA I/O | Data input/output |
| R/$\overline{W}$ | Read/write |
| CE1 | Chip enable1 |
| $\overline{CE2}$ | Chip enable2 |
| $V_{CC}$ | Power supply voltage (+5V) |
| GND | Ground |

**Figure 1**

## ■ Block Diagram

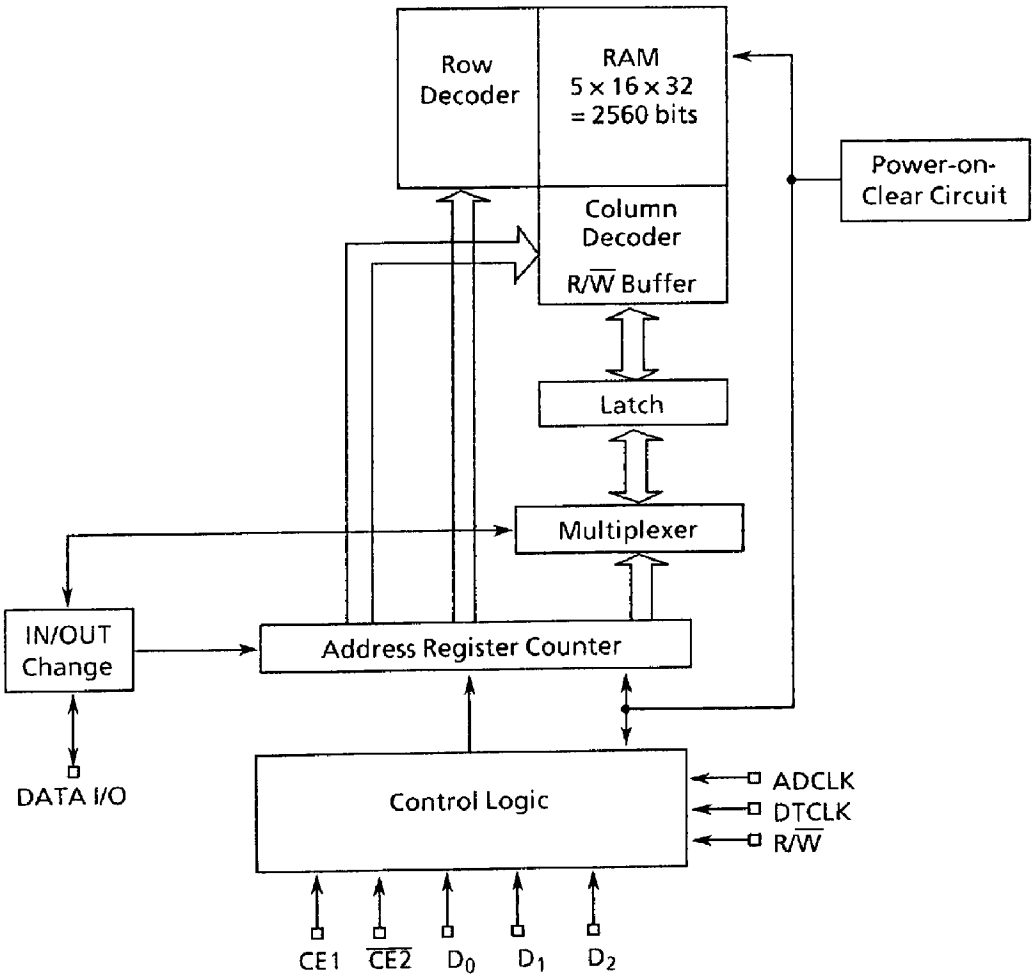



Figure 2

## ■ Absolute Maximum Ratings

Table 1

| Item | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Storage temperature | $T_{stg}$ | | – 40 to + 125 | °C |
| Storage temperature under bias | $T_{bias}$ | | – 30 to + 75 | °C |
| Power supply voltage | $V_{CC}$ | | 6.0 | V |
| Input voltage | $V_{IN}$ | All input pins | $V_{SS}$ – 0.3 to $V_{CC}$ + 0.3 | V |
| Output voltage | $V_{OUT}$ | DATA I/O | $V_{SS}$ – 0.3 to $V_{CC}$ + 0.3 | V |
| Power dissipation | $P_D$ | Ta = 25°C | 300 | mW |

## ■ Recommended Operating Conditions

Table 2

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | Ta = 25°C | 1.16 | — | 5.5 | V |
| High level input voltage | $V_{IH}$ | Ta = 25°C | 0.8 × $V_{CC}$ | — | $V_{CC}$ | V |
| Low level input voltage | $V_{IL}$ | Ta = 25°C | $V_{SS}$ | — | 0.2 × $V_{CC}$ | V |
| Operating temperature | $T_{opr}$ | | −30 | — | 75 | °C |

## ■ Electrical Characteristics

### 1. DC characteristics

Table 3

($Ta = 25°C, V_{SS} = 0\ V$)

| Item | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Data retention voltage | $V_{DR}$ | | 1.0 | — | — | V |
| Standby current | $I_{SB}$ | $V_{CC}$ = 1.5 V | — | 0.01 | 0.25 | µA |
| | | $V_{CC}$ = 5.5 V | — | 5.0 | 50.0 | µA |
| Operating current consumption (No load when read) | $I_{CC}$ | $V_{CC}$ = 1.5 V, f = 10 kHz | — | — | 2.0 | µA |
| | | $V_{CC}$ = 5.0 V, f = 10 kHz | — | — | 10.0 | µA |
| | | $V_{CC}$ = 3.0 V, f = 200 kHz | — | — | 50.0 | µA |
| | | $V_{CC}$ = 5.0 V, f = 500 kHz | — | — | 200.0 | µA |
| Low level output current | $I_{OL}$ | $V_{CC}$ = 1.5 V, $V_{OL}$ = 0.1 V | 25 | — | — | µA |
| | | $V_{CC}$ = 5.0 V, $V_{OL}$ = 0.4 V | 250 | — | — | µA |
| High level output current | $I_{OH}$ | $V_{CC}$ = 1.5 V, $V_{OH}$ = 1.4 V | — | — | −25 | µA |
| | | $V_{CC}$ = 5.0 V, $V_{OH}$ = 4.6 V | — | — | −250 | µA |
| Low level output leakage current | $I_{OFFL}$ | $V_{CC}$ = 5.5 V, $V_{OFFL}$ = 0 V | −1.0 | −0.01 | — | µA |
| High level output leakage current | $I_{OFFH}$ | $V_{CC}$ = 5.5 V, $V_{OFFH}$ = 5.5 V | — | 0.01 | 1.0 | µA |
| Low level input leakage current | $I_{IL}$ | $V_{CC}$ = 5.5 V, $V_{OFFL}$ = 0 V | −1.0 | −0.01 | — | µA |
| High level input leakage current | $I_{IH}$ | $V_{CC}$ = 5.5 V, $V_{OFFH}$ = 5.5 V | — | 0.01 | 1.0 | µA |

## 2. AC characteristics

**Table 4**

| Item | Symbol | $V_{CC}$ = 1.2 V | $V_{CC}$ = 3.0 V | $V_{CC}$ = 5.0 V |
|---|---|---|---|---|
| Maximum operating frequency* | $f_{MAX}$ | 35 kHz | 200 kHz | 500 kHz |
| DTCLK lead time | $t_{PDT}$ | 3.0 µs min. | 0.5 µs min. | 0.2 µs min. |
| Initialize time<br>CE initialize lead time | $t_{INIT}$<br>$t_{CE1\&2}$ | 9.0 µs min. | 1.5 µs min. | 0.6 µs min. |
| Hold time after CE initialization | $t_{CE1'\&2'}$ | 3.0 µs min. | 0.5 µs min. | 0.2 µs min. |
| Read/write changeable time | $t_{RWA}$,$t_{RWB}$ | 9.0 µs min. | 1.5 µs min. | 0.6 µs min. |
| Dummy clock delay time | $t_{DUMMY}$ | 12.0 µs min. | 2.0 µs min. | 0.8 µs min. |
| DATA I/O off time when read | $t_{RD}$ | 12.0 µs min | 2.0 µs min. | 0.8 µs min. |
| ADCLK delay time | $t_{ADR}$,$t_{DT}$ | 6.0 µs min. | 1.0 µs min. | 0.4 µs min. |
| Change timing of D0, D1, and D2 | $t_{DLA}$,$t_{DLB}$ | 9.0 µs min. | 1.5 µs min. | 0.6 µs min. |
| Data output delay time | $t_{RDT}$ | 3.0 µs max. | 0.5 µs max. | 0.2 µs max. |

* Frequency of ADCLK or DTCLK
Load capacitance of DATA I/O: 100 pF

### (1) Initialize

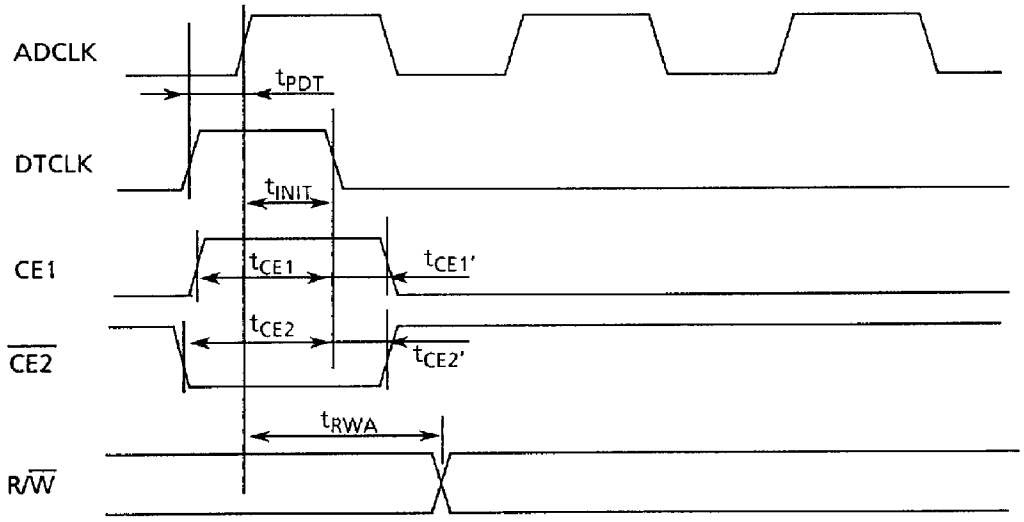



**Figure 3**

(2) Address finish

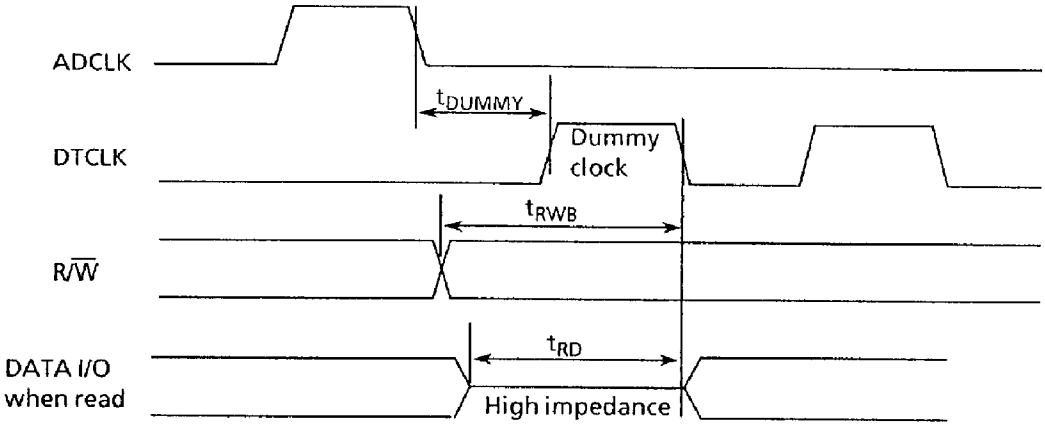



Figure 4

(3) Address (data) input

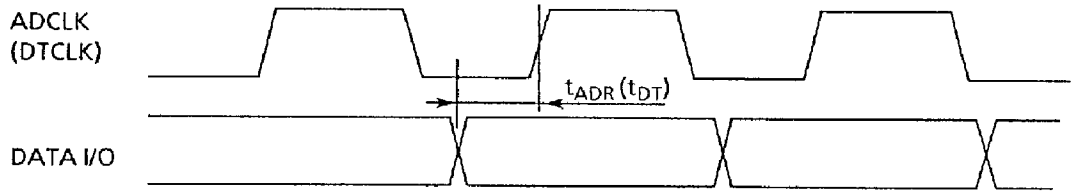



Figure 5

(4) Change of D0, D1, and D2

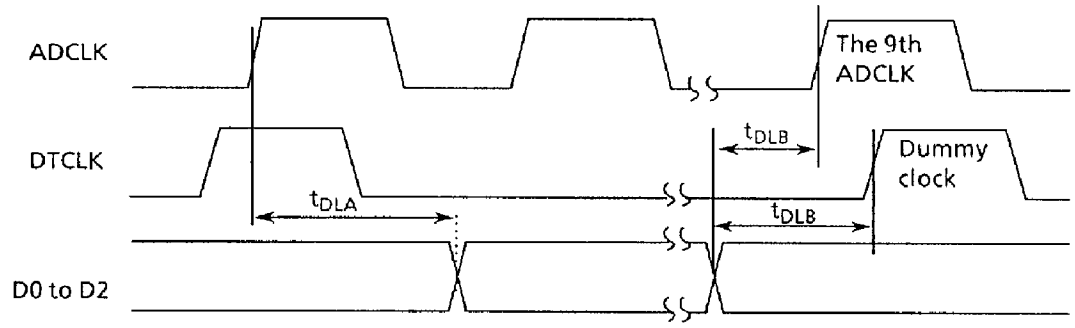



Figure 6

(5) Read

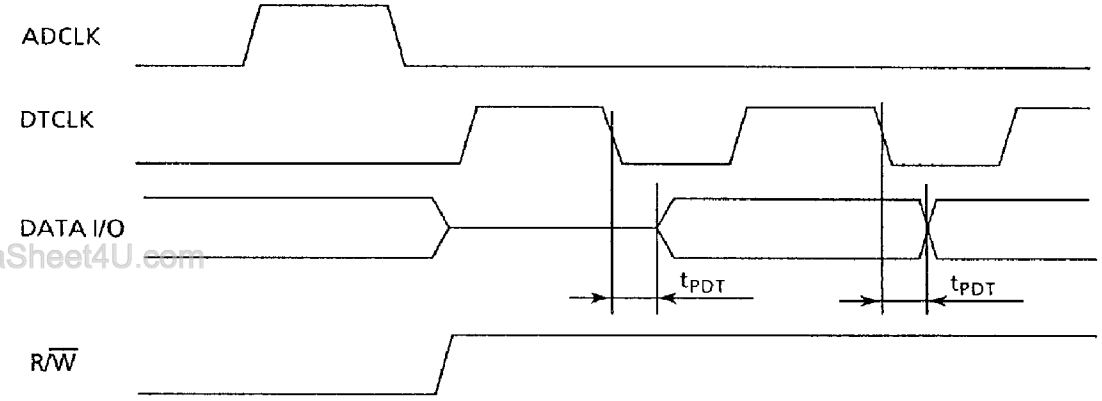



Figure 7

## ■ Pin Function

| No. | Signal | Functions |
|---|---|---|
| 1 | ADCLK | Clock input pin for transmitting addresses.<br>Addresses are fetched, synchronized with rise of ADCLK. By transmitting ADCLK synchronized with DTCLK, memory is initialized to be in address receivable status. When address is finished, DTCLK can be accessed after 1 clock of ADCLK has been sent. |
| 2 | DTCLK | Clock input pin for transmitting data.<br>Data are fetched, synchronized with rise of DTCLK when write. After being fetched for specified data length, data are written into the memory in a timing between DTCLKs. After address input, the first DTCLK becomes the dummy clock to indicate that address is completed. R/$\overline{W}$ becomes effective, synchronized with rise of the dummy clock.<br>Data read from the memory are output to DATA I/O synchronized with fall of the dummy clock when read. |
| 3 | DATA I/O | Address input, or data I/O pin.<br>When read, initialize before fall of the dummy clock to return DATA I/O to high impedance. |
| 4 | R/$\overline{W}$* | Read/write selection pin. It is not the write clock of negative logic.<br>Do not change its level during DTCLK send when address input. |
| 5<br>6 | CE1*<br>$\overline{CE2}$* | Chip enable pins.<br>They are latched synchronized with clock at initialization. Clock and data are receivable when pins are in enable state.<br>Note: Standby current does not change even in enable state. |
| 7 | GND | Connect to GND. |
| 8<br>9<br>10 | D0*<br>D1*<br>D2* | Data width selection pin.<br>There are seven data widths you can select as in the table below. |

| D0 | D1 | D2 | Data width × word | Valid address data width |
|---|---|---|---|---|
| 0 | 0 | 0 | 8-bit × 256 | 8 bits |
| 1 | 0 | 0 | 8-bit × 256 | 8 bits |
| 0 | 1 | 0 | 2-bit × 1024 | 10 bits |
| 1 | 1 | 0 | 3-bit × 512 | 9 bits |
| 0 | 0 | 1 | 4-bit × 512 | 9 bits |
| 1 | 0 | 1 | 5-bit × 512 | 9 bits |
| 0 | 1 | 1 | 6-bit × 256 | 8 bits |
| 1 | 1 | 1 | 7-bit × 256 | 8 bits |

| No. | Signal | Functions |
|---|---|---|
| 11<br>12<br>13 | NC | Non connection. |
| 14 | $V_{CC}$ | Positive power supply. Connect to between1.16 V to 5.5 V. |

* CE1 and $\overline{CE2}$ are latched at power on or at initialization, and keep their state until the next initialization. They have no effect unless they change at initialization.
The levels of R/$\overline{W}$, D0, D1, and D2 are fetched through the buffer.
Set the level of R/$\overline{W}$ before the rise of the first DTCLK (dummy clock) after initialization.
D0, D1, and D2 can change from initialization to the rise of the ninth ADCLK. If output ADCLK is less than nine, set their levels before the rise of dummy clock. Usually, they are fixed to power supply or GND.

## ■ Operation

1. Initialize

When power is turnd on, the power-on-clear circuit starts operation; memory, address counter and controller are initialized, and the states of CE1 and $\overline{CE2}$ are read. DATA I/O becomes high impedance. When ADCLK and DTCLK are detected to have been high, address counter and controller are reinitialized, and the states of CE1 and $\overline{CE2}$ are reread. Then, after chip enable, memory receives external input.

At initialization, set that rise of DTCLK is earlier than rise of ADCLK as shown in Figure 8.

When memory is initialized in read or write state, perform the initialization after data for set data width is read or written, that is, DTCLK is output for set data width.

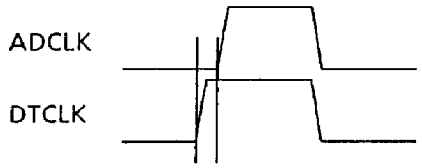



**Figure 8 Initialize**

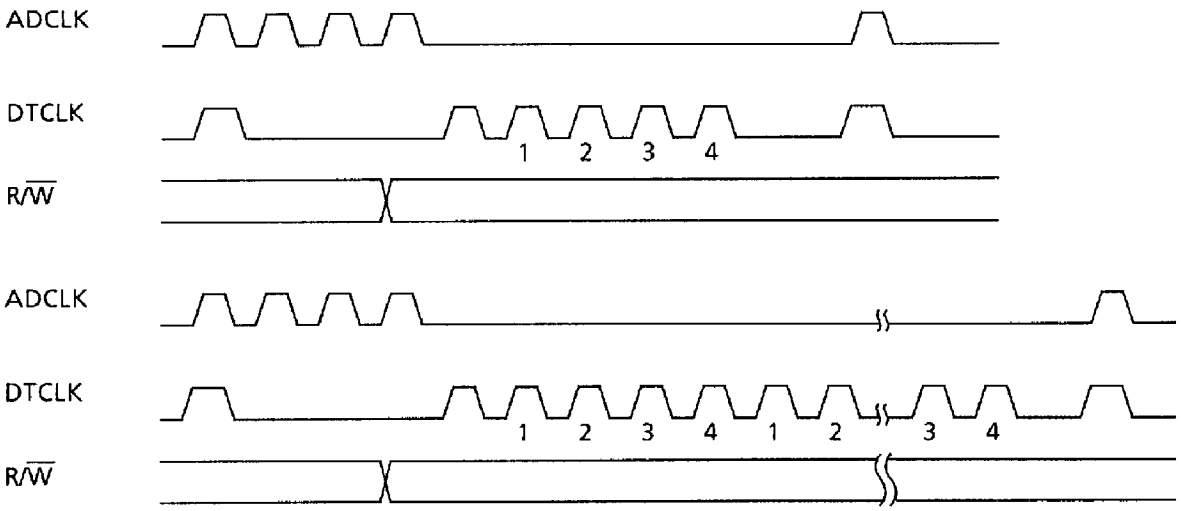



**Figure 9 Example of initialize: when data width is 4 bits**

2. Address set

Address is set after initialization.
Addresses are input from DATA I/O synchronized with ADCLK. Input addresses are fetched at rise of ADCLK. The last input bit becomes the MSB of addresses. When addresses are input over the valid address data width, address data over the width are ignored. Address is valid from initialization by ADCLK and DTCLK until rise of DTCLK.

[ Note ] Input 1-bit (1-ADCLK) or more address.

Figure 11 shows examples of address set in case of 8-bit address width.

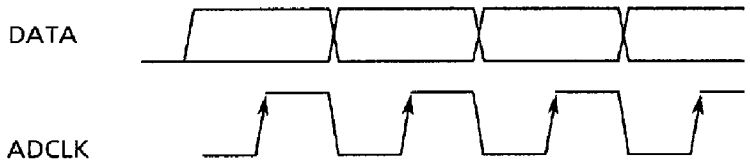
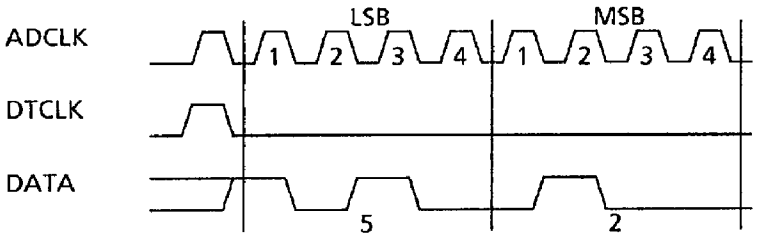


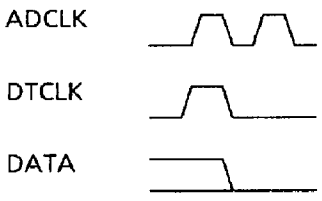

**Figure 10 Address read**

When inputting address $25_H$




The following abbreviations are available.

When inputting address $00_H$




When inputting address $90_H$

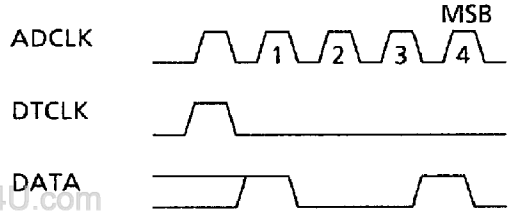





**Figure 11 Examples of address set: when valid address data width is 8 bits**

3. Write

After address set, level of R/$\overline{W}$ is sent to the S-2510A.

When R/$\overline{W}$ is low, the S-2510A goes into write mode and DATA I/O becomes the input pin. Data is input from DATA I/O synchronized with DTCLK after dummy clock, and is read at rise of DTCLK. Read data is stored temporarily in latch until bit number of data amounts to data width, then it is written in memory. Therefore if 2-bit data (2 DTCLKs after dummy clock) is sent when data width is 4 bits, the data is not written in memory. By sending DATA I/O and DTCLK continuously, address is automatically incremented and data is continuously written in memory.

Figures 12 to 14 show examples of write timing.

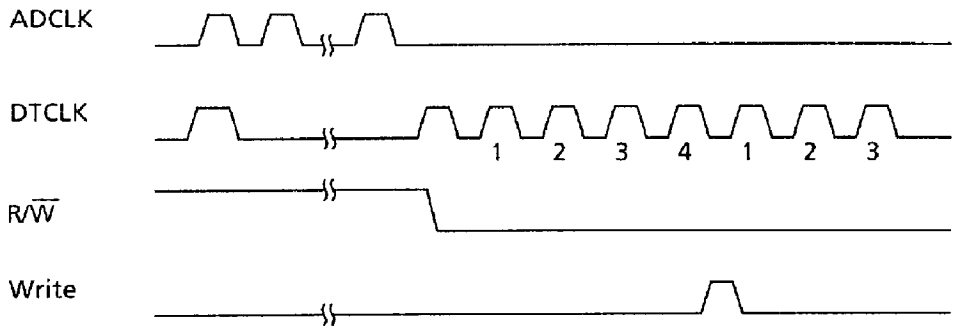



**Figure 12 Write timing: when data width is 4 bits**

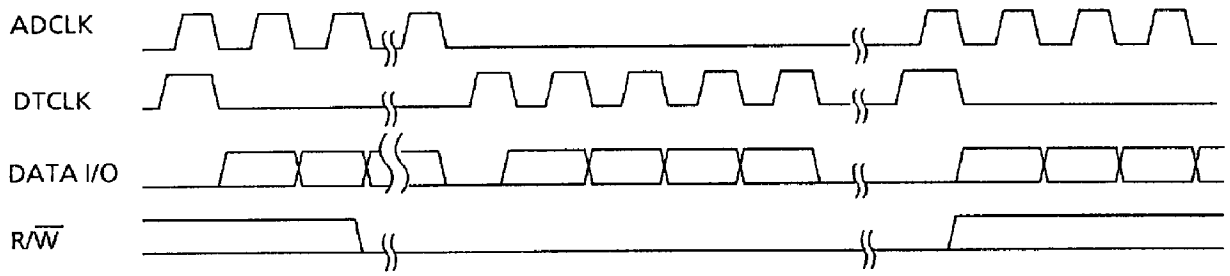



**Figure 13 R/$\overline{W}$ switch timing when write: when data width is 4 bits**

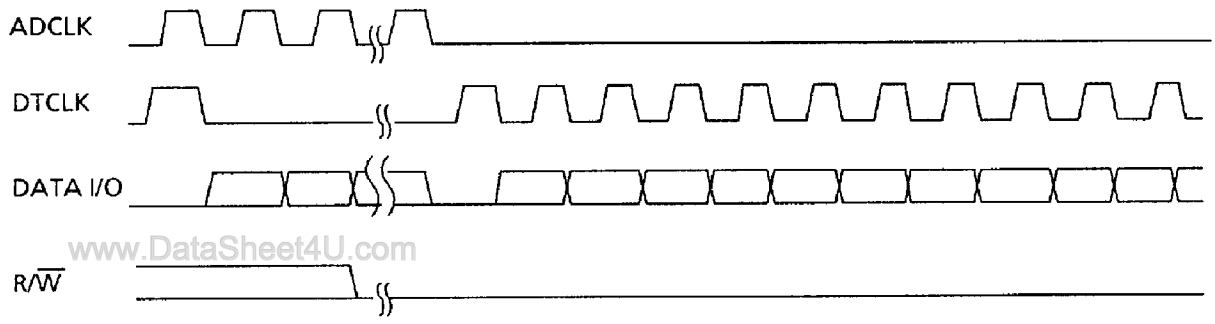





**Figure 14 R/$\overline{W}$ switch timing when write: continuous writing**

4. Read

After address set, level of R/$\overline{W}$ is sent to the S-2510A.

When R/$\overline{W}$ is high, the S-2510A goes into read mode. Data is output at fall of dummy clock. Address is automatically incremented by outputting DTCLK to read data continuously.
When DATA I/O returns to high impedance from read mode, initialization is performed by ADCLK and DTCLK after data read for set data width is completed.

Figures 15 and 16 show examples of read timing.

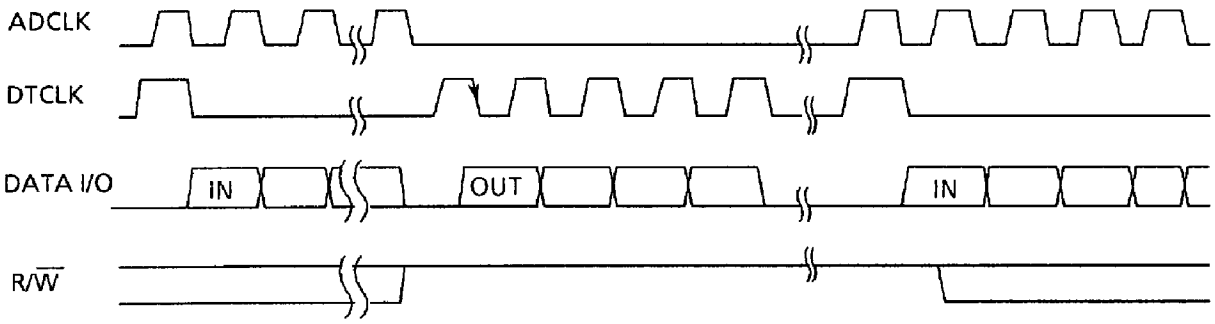



**Figure 15 R/$\overline{W}$ switch timing when read: when data width is 4 bits**

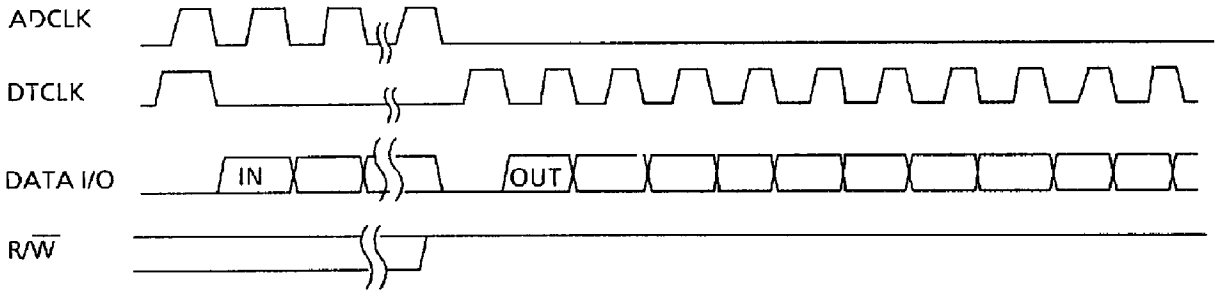



**Figure 16 R/$\overline{W}$ switch timing when read: continuous reading**

5. Conclusion

Operation from initialization to read or write is illustrated in the following timing chart.

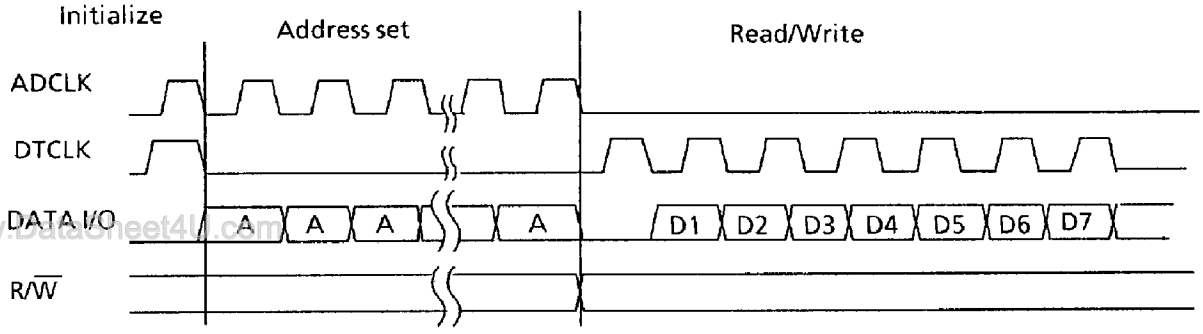





**Figure 17 Operation timing**

## ■ Dimensions (Unit:mm)

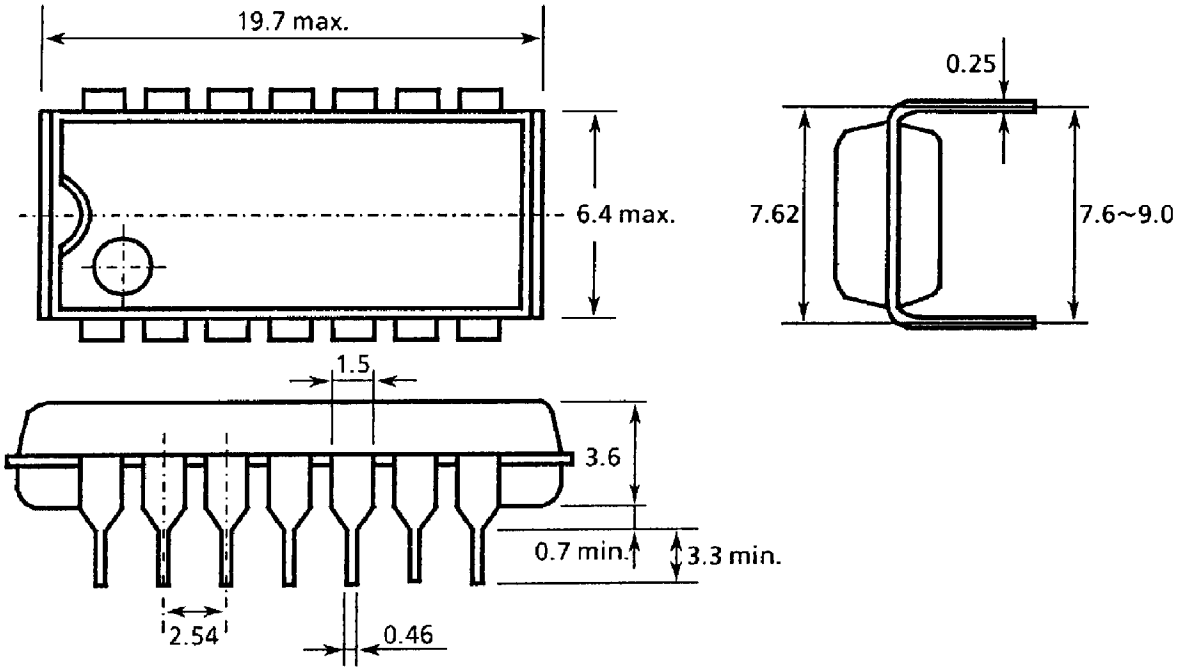
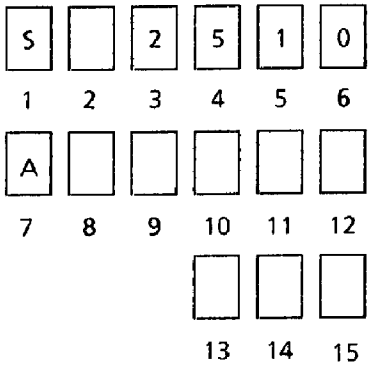



Figure 18

## ■ Markings




1 : S

2, 8, 9 : Blank

3 to 7 : Product name

10 to 12 : Lot No.

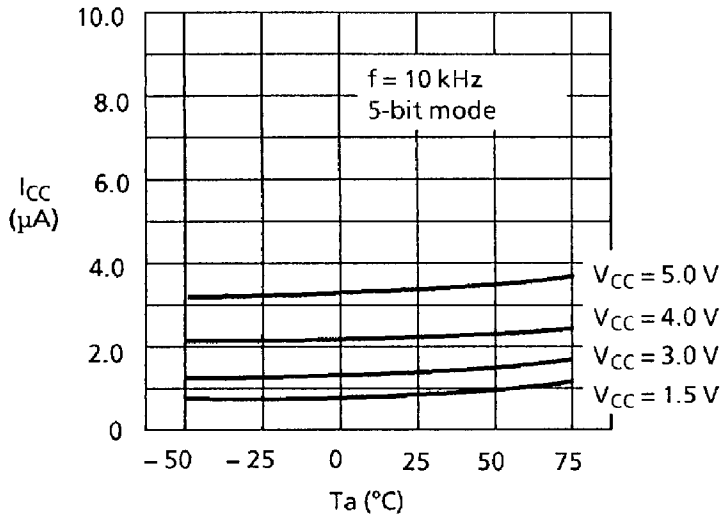
13 : Assembly mark

14 : Last column of year

15 : Manufacturing month : January = 1, February = 2, March = 3, April = 4,
May = 5, June = 6, July = 7, August = 8, September = 9
October = X, November = Y, December = Z

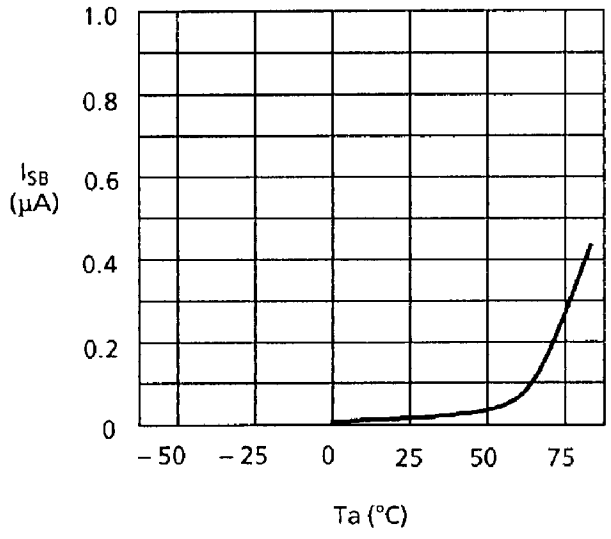
## ■ Characteristics

1. Operating current consumption ($I_{CC}$) – Ambient temperature (Ta)

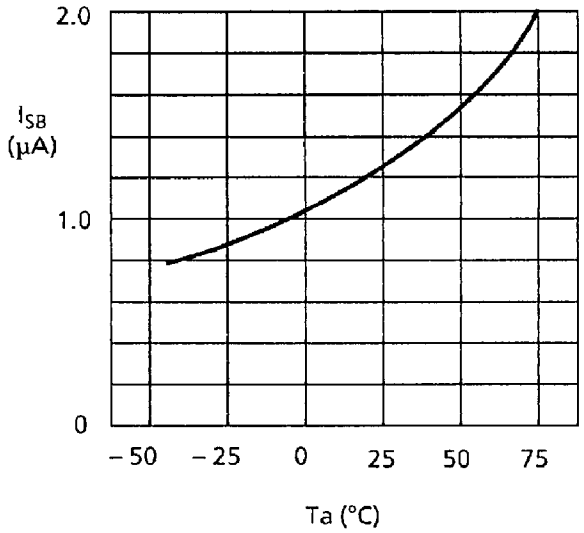



2. Standby current ($I_{SB}$) – Ambient Temperature (Ta)

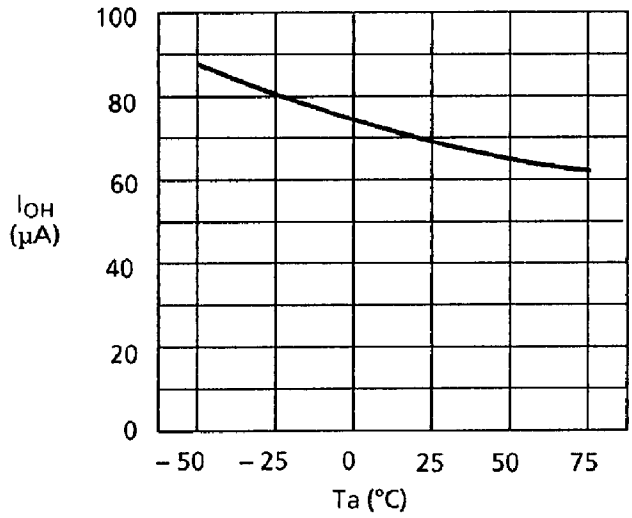
2.1 $V_{CC}$ = 1.5 V




2.2 $V_{CC}$ = 5.0 V



3. High level output current ($I_{OH}$) – Ambient temperature (Ta)




4. Low level output current ($I_{OL}$) – Ambient temperature (Ta)