SH7450
Renesas Microcomputer

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1. Overview

1.1 Features

The SH7450 is a single-chip RISC microcontroller based on a Renesas original RISC CPU core. It provides an extensive set of peripheral functions necessary for implementing application systems integrated on the same chip.

The CPU used in the SH7450 features a RISC (reduced instruction set computer) instruction set and adopts a superscalar architecture to radically increase instruction execution speed. It uses the Renesas SH-4A as the CPU core and can implement high-performance/high-functionality systems at low cost, even for real-time control and other applications that require high-speed performance and could not be implemented with earlier microcontrollers.

The SH7450 includes 32 Kbytes of instruction cache and 32 Kbytes of operand cache. Either copy-back or write-through can be selected for the operand cache. It furthermore includes a memory management unit (MMU) that can access a 4 GB address space. It includes a 4-entry fully associative TLB for instructions and a 64-entry fully associative TLB for both instruction and operands.

The SH7450 also includes 8 Kbytes of IL memory, 16 Kbytes of OL memory and 512 Kbytes of SuperHyway RAM (SHwy RAM) as internal SRAM. The IL and OL memory units are capable of high-speed access and can be used as system stack area or as a permanently resident area for the core block for functions that require high performance.

The SH7450 provides a direct RAM interface function (DRI) that transfers parallel data directly to internal SHwy RAM and can transfer data input from, for example, an image sensor, to internal SHwy RAM.

The SH7450 integrates on the same chip a wide range of peripheral functions necessary for system construction. These include a floating point unit (FPU), large-capacity ROM and RAM blocks, a direct memory access controller (DMAC), several types of timer, the Renesas serial peripheral interface (RSPI), a user break controller (UBC), a RAM monitor function, a serial communications interface with FIFO (SCIF), a control area network (CAN), A/D converters (ADC), a DAC interface function, an interrupt controller (INTC), and I/O ports.

The SH7450 can connect with external memory or peripheral ICs using an external memory access function. This can significantly reduce total system costs.

The SH7450 is a F-ZTAT™ (Flexible Zero Turn Around Time) version device that includes built-in flash memory. Programs can be downloaded or erased either using a ROM programmer or with software. This means that the user can reload software with the SH7450HM mounted on a board.

Note: F-ZTAT is a trademark of Renesas Technology Corp.

1.1.1 Applications

Automobile equipment control (driver-assist systems, etc.)

1.1.2 Specifications Overview

Table 1.1 provides an overview of the SH7450 specifications.

Table 1.1 Specifications Overview

Item	Description
CPU	• Renesas original Super-H architecture • Compatibility at the object code level between the SH-1, SH-2, SH-3, and SH-4. • 32-bit internal data bus • General-purpose register file 16 32-bit general-purpose registers (and 8 32-bit shadow registers) 7 32-bit control registers 4 32-bit system registers Register banks for rapid interrupt response • RISC type instruction set (upwards compatible with the SH series) Instruction length: fixed 16-bit length for improved code efficiency Load/store architecture Delayed branch instructions Conditional execution Instruction set based on the C programming language • Two-instruction simultaneous execution superscalar architecture, including FPU • Instruction execution time: a maximum of two instructions per cycle • Address space: 4 GB • Address space identifier (ASID): 8 bits for 256 virtual address spaces • Built-in multiplier • Eight stage pipeline • Harvard architecture

Item	Description
FPU	• Built-in floating point coprocessor (FPU) • Single precision (32 bits) and double precision (64 bits) support • Supports IEEE 754 standard data formats and exceptions • Rounding mode: round to nearest and round toward zero • Handling unnormalized numbers: truncating towards zero, generating an interrupt to conform to the IEEE 754 standard • Floating point registers: 32 bits × 16 registers × 2 banks (16 standard precision or 8 double precision) × 2 banks • 32-bit CPU-FPU floating point communication register (FPUL) • Supports an FMAC (multiply and accumulate) instruction • Supports the FDIV (division) and FSQRT (square root) instructions • Supports the FLDI0/FLD1 (load the constants 0 or 1) instructions • Instruction execution times Latency (FADD/FSUB): 3 cycles (standard precision), 5 cycles (double precision) Latency (FMAC/FMUL): 5 cycles (standard precision), 7 cycles (double precision) Pitch (FADD/FSUB): 1 cycle (standard precision), 1 cycle (double precision) Pitch (FMAC/FMUL): 1 cycle (standard precision), 3 cycles (double precision) Note: FMAC is only supported for single precision. • 3D graphics instructions (single precision only) Four-dimensional vector transformation and matrix operation (FTRV), 4 cycles (pitch), 8 cycles (latency) Four-dimensional vector inner product (FIPR), 1 cycle (pitch), 5 cycles (latency) • 11-stage pipeline
Memory management unit (MMU)	• 4 GB address space, 256 address space identifiers (ASID: 8 bits) • Single virtual memory mode and multiple virtual memory mode • Supports multiple page sizes: 1 Kbyte, 4 Kbytes, 8 Kbytes, 64 Kbytes, 256 Kbytes, 1 Mbyte, 4 Mbytes, and 64 Mbytes. • Four-entry fully associative TLB for instructions • 64-entry fully associative TLB for instructions and operands • Supports both software based replacement methods and random counter based replacement algorithms • The TLB content can be accessed directly with address mapping • Access rights check function
Cache memory	• Instruction memory (IC) 32 Kbytes, 4-way set associative 256 entries/ways, 32-byte block length Low-power function (way prediction structure) • Operand cache (OC) 32 Kbytes, 4-way set associative 256 entries/ways, 32-byte block length • Single stage copy-back buffer, single stage write-through buffer Store queue (32 bytes × 2 entries)

Item	Description
IL memory	• 8-Kbyte high-speed access RAM • Two-page structure • Allows access from three ports: provides the following three read/write ports. SuperHyway bus Cache/RAM internal bus Instruction bus • Allows CPU access to 8, 16, 32, and 64-bit operands • Allows accesses in 8, 16, 32, and 64-bit, as well as 16 and 32-byte, units by external requests
OL memory	• 16-Kbyte high-speed access RAM • 4-page structure • Allows access from three ports: provides the following three read/write ports. SuperHyway bus Cache/RAM internal bus Operand bus • Allows CPU access to 8, 16, 32, and 64-bit operands • Allows accesses in 8, 16, 32, and 64-bit, as well as 16 and 32-byte, units by external requests
ROM	• 2-Mbyte flash memory: SH74504 • 1.5-Mbyte flash memory: SH74513
RAM	• 512-Kbyte SRAM
Operating modes	• Operating modes Single-chip mode ROM enabled extended mode • On-board programming modes User mode Boot mode User boot mode • Processing states Reset state Instruction execution state
User break controller (UBC)	• Supports debugging with a user break interrupt • Two break channels • The address, data value, access type, and data size can all be used as break conditions. • Supports a sequential break function
Clock generator (CPG)	• Main clock selection circuit: the EXTAL pin input clock frequency multiplied by 12 • Clock operating modes CPU clock (Ick): 240 MHz maximum SHwy clock (SHck): 80 MHz maximum Peripheral clock (Pck): 40 MHz maximum Peripheral A clock (PAck): 80 MHz maximum FlexRay clock (FRck): 80 MHz maximum • Input clock frequency: 20 MHz
Bus state controller (BSC)	• External memory access mode (can be directly connected to SRAM or ROM) • Bus widths: 8, 16, and 32 bits • Supports access to linear address spaces of up to 64 Mbytes for each of the CS0 to CS2 spaces

Item	Description
Watchdog timer (WDR)	• One channel • Supports both watchdog timer mode, in which the SH7450HM is reset internally by a counter overflow and interval timer mode, in which interrupts are generated • In watchdog timer mode, the overflow signal is output from the chip. Also, the microcontroller itself can be reset.
Interrupt controller (INTC)	• Interrupt priority • External interrupts: 15 levels • Internal peripheral interrupts: 30 levels
Direct memory access controller (DMAC)	• 6 channels (DMA0 to DMA5) + 6 channels (DMA6 to DMA11) • Transfer data size: 1 byte, 2 bytes (word), 4 bytes (long word), 16 bytes, 32 bytes • Maximum number of transfers: 16,777,216 • Transfer address method: dual address • Transfer modes: cycle stealing mode 1, cycle stealing mode 2, or burst mode • Transfer request sources: automatic request (software request), on-chip peripheral module request (SCIF, RSPI, IIC3, ATU-IIIS, ADC, DRI), and external request (DMA0 to DMA3 only) • Channel priority: either fixed channel priority or round robin can be selected for DMA0 to DMA5 and DMA6 to DMA11. • The priority between DMA0 to DMA5 and DMA6 to DMA11 is fixed to round robin.
Advanced timer unit IIIS (ATU-IIIS)	• 62 channels • Provides timer A (6 channels × 2 systems), timer F (4 channels), timer G (6 channels), and timer TOU (8 channels × 5 systems)
Timer unit (TMU)	• Three auto-reload 32-bit timer channels • Each channel can select one of five counter input clocks: one of 5 peripheral clocks (Pck/4, Pck/16, Pck/64, Pck/256, or Pck/1024) (Note: Pck is the peripheral clock)
Built-in FIFO serial communications interface (SCIF)	• Four channels • Transmit and receive FIFOs each with 16 bytes • Supports both asynchronous and synchronous modes • Supports full-duplex communication • The transfer clock can be selected from either an internal clock from a baud rate generator or an external clock input to the SCK pin • Maximum transfer rate: 10 MHz (design target value)
Renesas serial peripheral interface (RSPI)	• Three channels • Synchronous serial communication • Supports both master and slave modes • Programmable bit length, clock polarity, and clock phase • Supports sequential iterative execution of transfer operations • Supports both MSB first and LSB first transfer • Maximum transfer rate: 10 MHz (design target value)
I^2C interface (IIC)	• One channel • Supports the Philips proposed I^2C bus (Inter IC Bus) interface standard • Master and slave functions
Controller area network (CAN)	• Five channels • 64 mailboxes

Item	Description
A/D converter (ADC)	• Two modules • 12 bits, 24 channels (AD0: 16 channels, AD1: 8 channels) • Provides three conversion modes Continuous scan mode Single cycle scan mode A/D conversion value summation mode (performs an A/D conversion of the same channel 2 to 4 times and adds the converted values) • Conversion times When AVCC = 5 V: 1.25 µs When AVCC = 3.3 V: 10 µs • Accuracy When AVCC = 5 V: T.B.D. When AVCC = 3.3 V: T.B.D.
Parallel DAC control (PDAC)	• One channel • 10-bit parallel output • This is a parallel DAC control circuit that controls an external 10-bit D/A converter • Generates modulation A, modulation B, and modulation C output waveforms.
Direct RAM input interface (DRI)	• Three channels • Acquisition timing adjustment function • Decimation control function • Acquisition period: 40 MHz (design target value)
Direct RAM output interface (DRO)	• One channel • Reads SHwy RAM and outputs parallel data to off-chip circuits • Data width: 8 or 16 bits • Transfer speed: 10 MHz
Parallel selector (PSEL)	• One channel • This is a parallel selector circuit that periodically changes the external selector outputs • This module is activated by an activation event and stopped by either a stop command or a termination event • 4-bit selector output • Two clock output systems and one clear signal output
FlexRay	• Two channels: SH74504 • None: SH74513
AUD RAM monitor function (AUDR)	• Functions for reading/writing memory mapped modules connected to an internal or external bus • Parallel 4-bit data input and output • Transfer frequency: 12.5 MHz maximum
I/O ports	• Number of ports: 166 • Built-in input threshold value switching function (0.35, 0.5, or 0.7 × Vcc)
Module stop function	• Supports the module stop function for the PDAC, PSEL, DRI, and DRO modules.
User debugging interface	• H-UDI (User Debugging Interface) • AUD (Advanced User Debugger) Note: The AUD module is not included in the mass production versions of the chip. It is only supported in the EVA chip version.

Item	Description
Supply voltage	• Internal logic voltage: 1.5 V +0.15 V, -0.1 V • I/O voltage: 3.3 V ±0.3 V or 5.0 V ±0.5 V
Operating temperature	• Ta = -40 to +125°C
Package	• PRBG0292GB-A (0.8 mm pitch)

1.2 Product Line Overview

Table 1.2 lists the SH7450 products.

Table 1.2 Products

Product	Model	ROM Capacity	RAM Capacity	Package	FlexRay
SH74504	R5F74504KBG	2 Mbytes	IL memory: 8 Kbytes, OL emory: 16 Kbytes, and SHwyRAM: 512 Kbytes	PRBG0292GB-A	Yes
SH74513	R5F74513KBG	1.5 Mbytes			No

1.3 Block Diagram

Figure 1.1 shows the SH7450 block diagram

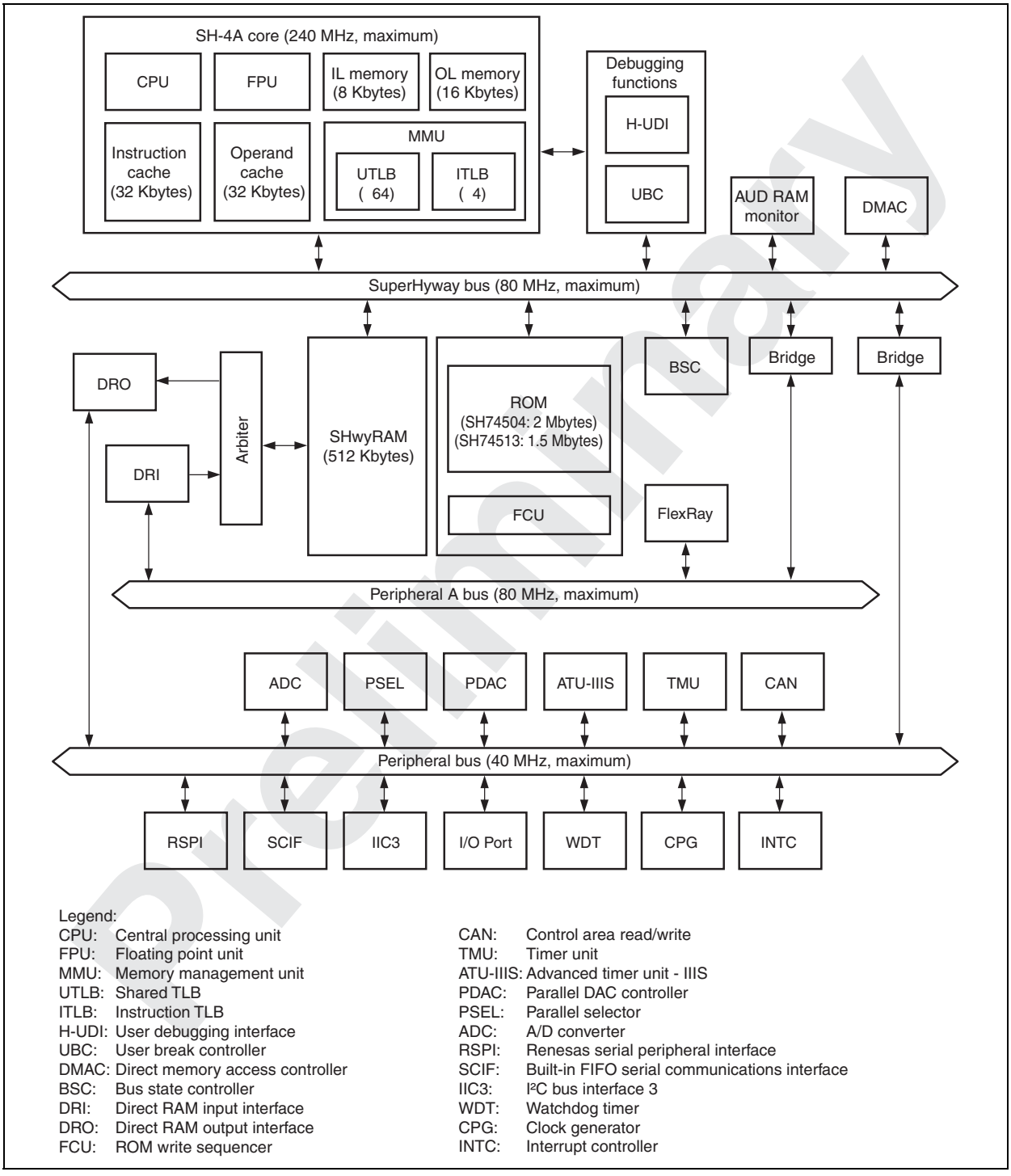
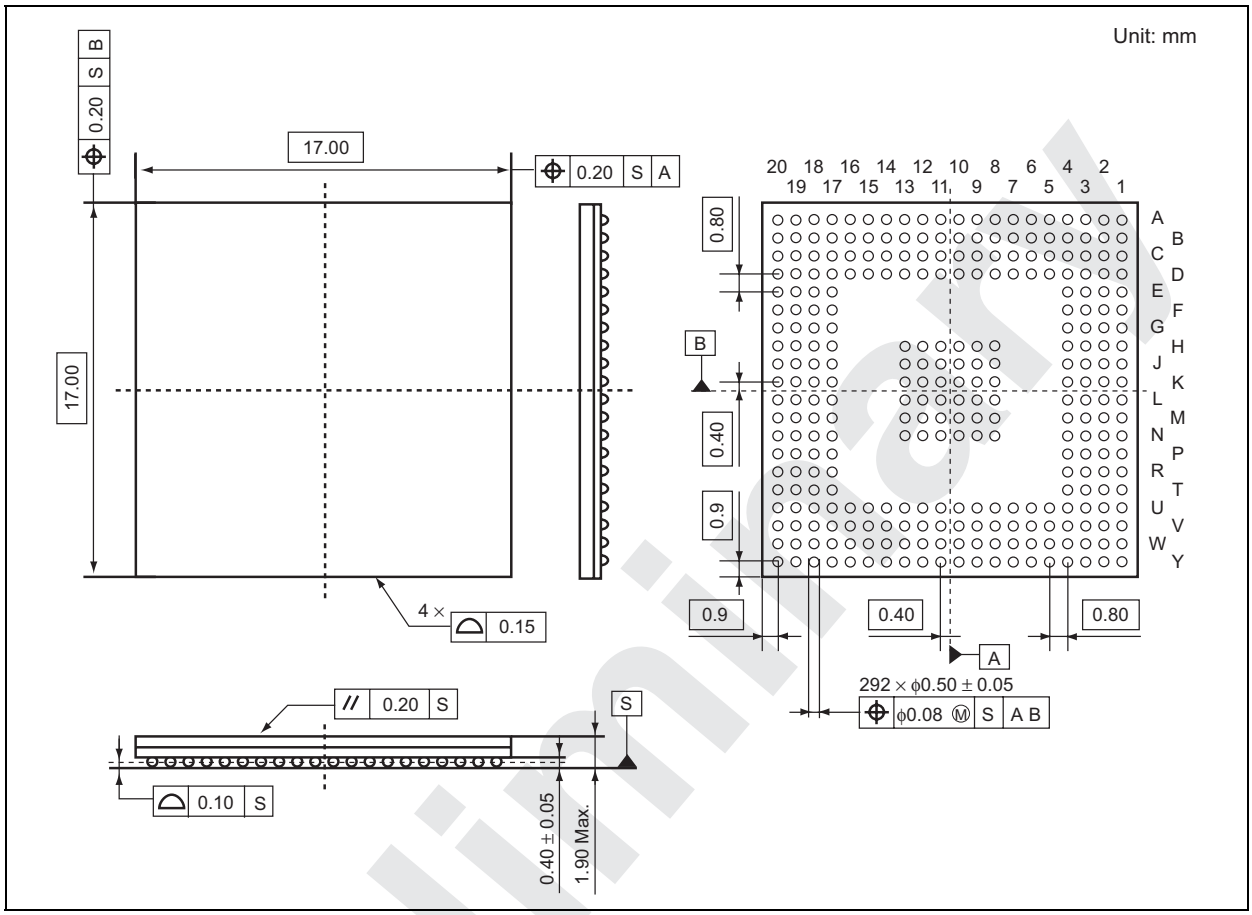


Figure 1.1 Block Diagram

Package Dimension



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