

HD74BC373A

Octal D Type Transparent Latches With 3 State Outputs

REJ03D0283-0300Z (Previous ADE-205-009A (Z)) Rev.3.00 Jul.16.2004

Description

The HD74BC373A provides high drivability and operation equal to or better than high speed bipolar standard logic IC by using Bi-CMOS process. The device features low power dissipation that is about 1/5 of high speed bipolar logic IC, when the frequency is 10 MHz. The device has eight D type latches with three state outputs in a 20 pin package. When the latch enable input is high, the Q outputs will follow the D inputs. When the latch enable goes low, data at the D inputs will be retained at the outputs until latch enable returns high again. When a high logic level is applied to the output control input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

Features

- Input/Output are at high impedance state when power supply is off.
- Built in input pull up circuit can make input pins be open, when not used.
- TTL level input
- Wide operating temperature range input pins $Ta = -40 \text{ to} + 85^{\circ}\text{C}$
- Ordering Information

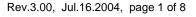
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74BC373AFPEL	SOP-20 pin (JEITA)	FP-20DAV	FP	EL (2,000 pcs/reel)
HD74BC373ATELL	TSSOP-20 pin	TTP-20DAV	Т	ELL (2,000 pcs/reel)

Note: Please consults the sales office for the above package availability.

Function Table

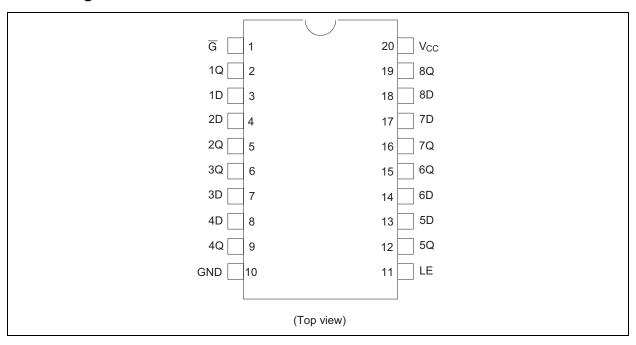
	Inputs		
G	LE	D	Output Q
Н	Х	Х	Z
L	Н	L	L
L	Н	Н	Н
L	L	Х	No change

H : High levelL : Low levelX : ImmaterialZ : High impedance





Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply voltage	V _{cc}	-0.5 to +7.0	V
Input diode current	I _{IK}	±30	mA
Input voltage	V _{IN}	-0.5 to +7.5	V
Output voltage	V _{OUT}	-0.5 to +7.5	V
Off state output voltage	$V_{OUT(off)}$	-0.5 to +5.5	V
Storage temperature	Tstg	-65 to +150	\mathcal{C}

Note: 1. The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

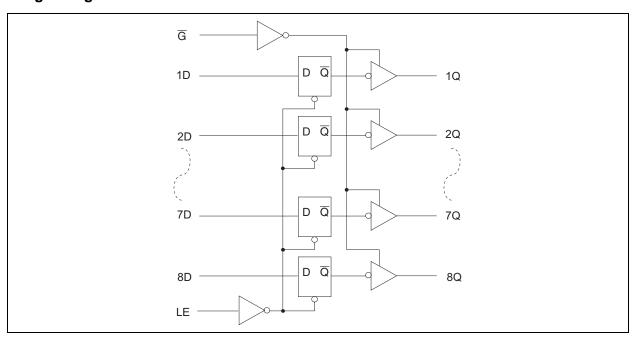
Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	V _{cc}	4.5	5.0	5.5	V
Input voltage	V _{IN}	0	_	V _{cc}	V
Output voltage	V _{out}	0	_	V _{cc}	V
Operating temperature	Topr	-40	_	85	°C
Input rise/fall time*1	t _r , t _f	0	_	8	ns/V

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

Logic Diagram



Electrical Characteristics ($Ta = -40^{\circ}C$ to $+85^{\circ}C$)

Item	Symbol	V _{cc} (V)	Min	Max	Unit	Test Conditions
Input voltage	V _{IH}		2.0	_	V	
	V_{IL}		_	0.8	V	
Output voltage	V _{OH}	4.5	2.4		V	$I_{OH} = -3 \text{ mA}$
		4.5	2.0		V	$I_{OH} = -15 \text{ mA}$
	V_{OL}	4.5	_	0.4	V	I _{OL} = 24 mA
		4.5	_	0.5	V	$I_{OL} = 48 \text{ mA}$
Input diode voltage	V _{IK}	4.5	_	-1.2	V	$I_{IN} = -18 \text{ mA}$
Input current	I ₁	5.5	_	-250	μA	$V_{IN} = 0 V$
		5.5	_	1.0	μA	V _{IN} = 5.5 V
		5.5	_	100	μΑ	V _{IN} = 7.0 V
Short circuit output current*1	Ios	5.5	-100	-225	mA	V _{IN} = 0 or 5.5 V
Off state output current	I _{OZH}	5.5	_	50	μΑ	$V_0 = 2.7 \text{ V}$
	I _{OZL}	5.5	_	-50	μΑ	$V_0 = 0.5 \text{ V}$
Supply current	I _{CCL}	5.5	_	29.5	mA	V _{IN} = 0 or 5.5 V
						All outputs is "L"
	I _{CCH}	5.5	_	2.5	mA	V _{IN} = 0 or 5.5 V
						All outputs is "H"
	I _{CCZ}	5.5		2.5	mA	V _{IN} = 0 or 5.5 V
						All outputs is "Z"
	I _{CCT} *2	5.5	_	1.5	mA	$V_{IN} = 3.4 \text{ or } 0.5 \text{ V}$

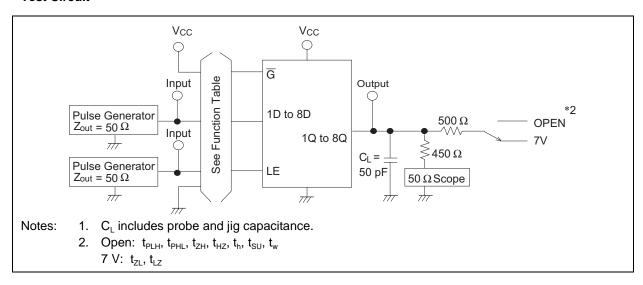
Notes: 1. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

Switching Test Method ($C_L = 50 \text{ pF}$)

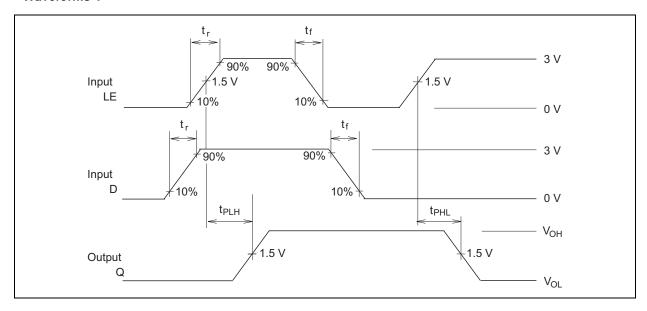
			Ta =	25℃	Ta = -40	0 to 85℃		
			$V_{CC} = 5.0 \text{ V}$ $V_{CC} = 5.0 \text{ V} \pm 10\%$					
Item		Symbol	Min	Max	Min	Max	Unit	Test Conditions
Propagation	$D\toQ$	t _{PLH}	3.0	8.0	3.0	10.0	ns	See under figure
delay time		t _{PHL}	3.0	8.0	3.0	10.0		
	$LE \to Q$	t _{PLH}	3.0	8.0	3.0	10.0	ns	
		t _{PHL}	3.0	8.0	3.0	10.0		
Output enable tim	ne	t_{ZH}	3.0	9.0	3.0	11.0	ns	
		t_{ZL}	3.0	9.0	3.0	11.0		
Output disable time		t _{HZ}	3.0	8.0	3.0	10.0	ns	
		t _{LZ}	3.0	8.0	3.0	10.0		
Setup time		t _S (H)	2.0	_	2.0	_	ns	
		t _S (L)	2.0	_	2.0	_		
Hold time		t _h (H)	2.0	_	2.0	_	ns	
		t _h (L)	2.0	_	2.0	_		
Pulse width		t _w	6.0	_	6.0	_	ns	
Input capacitanse	9	C _{IN}	3.0(Typ)	•	_		pF	$V_{IN} = V_{CC}$ or GND
Output capacitan	ce	Co	15.0(Typ)		_		pF	$V_0 = V_{CC}$ or GND

^{2.} When input by the TTL level, it shows $\rm I_{\rm CC}$ increase at per one input pin.

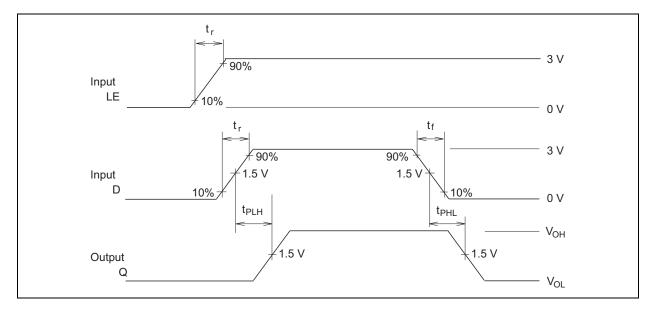
Test Circuit



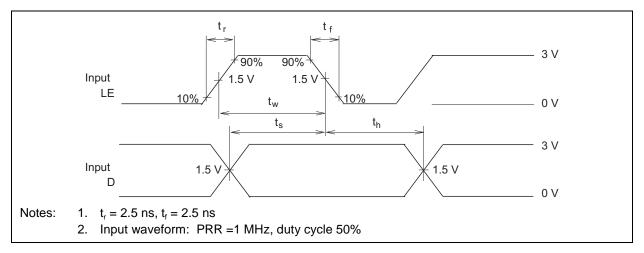
Waveforms-1



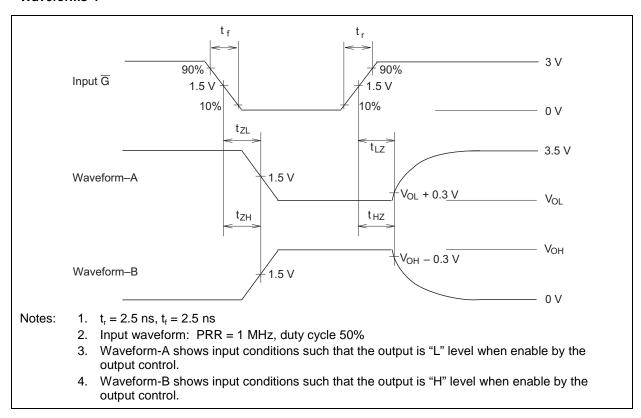
Waveforms-2



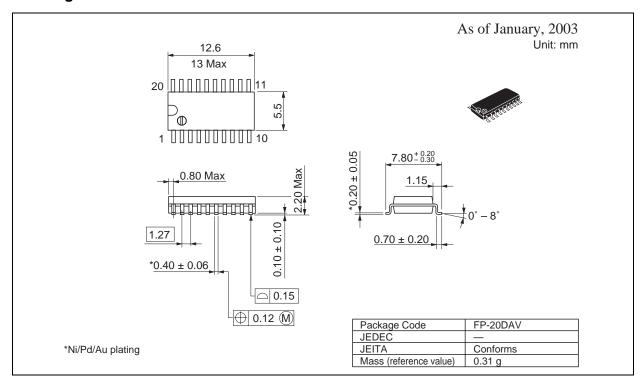
Waveforms-3

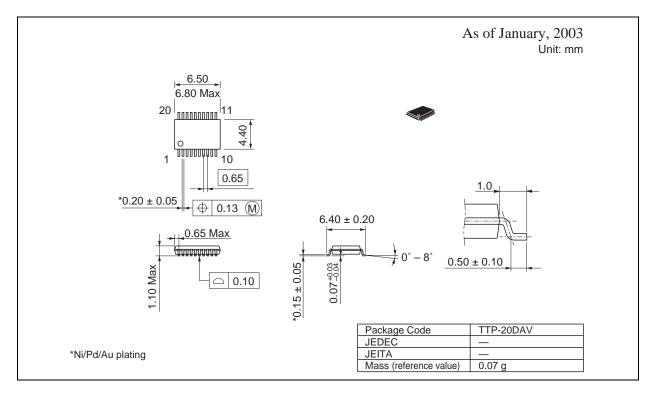


Waveforms-4



Package Dimensions





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