V91F565U24QB
128M x 72 HIGH PERFORMANCE
FULLY BUFFERED DIMM (FBDIMM)

Features

- 240-pin DDR2 fully buffered, dual in-line memory module (FBDIMM)
- ECC detect and channel error reports to host memory controller
- Fast data transfer rate: PC2-4200(DDR2-533), or PC2-5300(DDR2-667)
- 3.2 Gb/s and 4.0 Gb/s link transfer rates
- High-speed, differential, Point-to-Point link between host memory controller and AMB
  10 pair southbound (data transfer to FBDIMM)
  14 pair northbound (data transfer from FBDIMM)
- High-density scaling with up to 8 dual-rank modules per channel
- Support SMBus protocol interface for access to the AMB configuration register
- Full Host Control of the DDR2 DRAMs
- Automatic DDR2 DRAM bus and channel calibration
- Transparent Mode for DRAM Test Support
- MBIST and IBIST test functions
- RoHS Compliant Products
- JEDEC standard 1.8V ± 0.1V power supply
- VDDQ=1.8V ± 0.1V
- VCC=1.5V for advanced memory buffer (AMB)
- Gold edge contacts
- Serial Presence Detect (SPD) with EEPROM

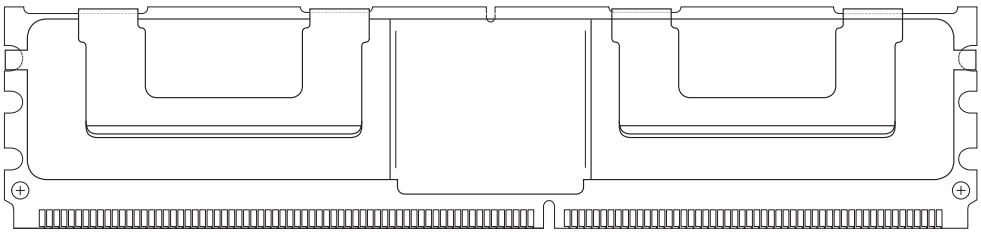
Description

The V91F565U24QB memory module is organized as 134,217,728 x 72 bits in a 240 pin fully buffered ECC memory module. The 128M x 72 memory module uses 18 ProMOS 64M x 8 DDR2 SDRAMs. The x72 modules are ideal for use in high performance computer systems where increased memory density and fast access times are required.

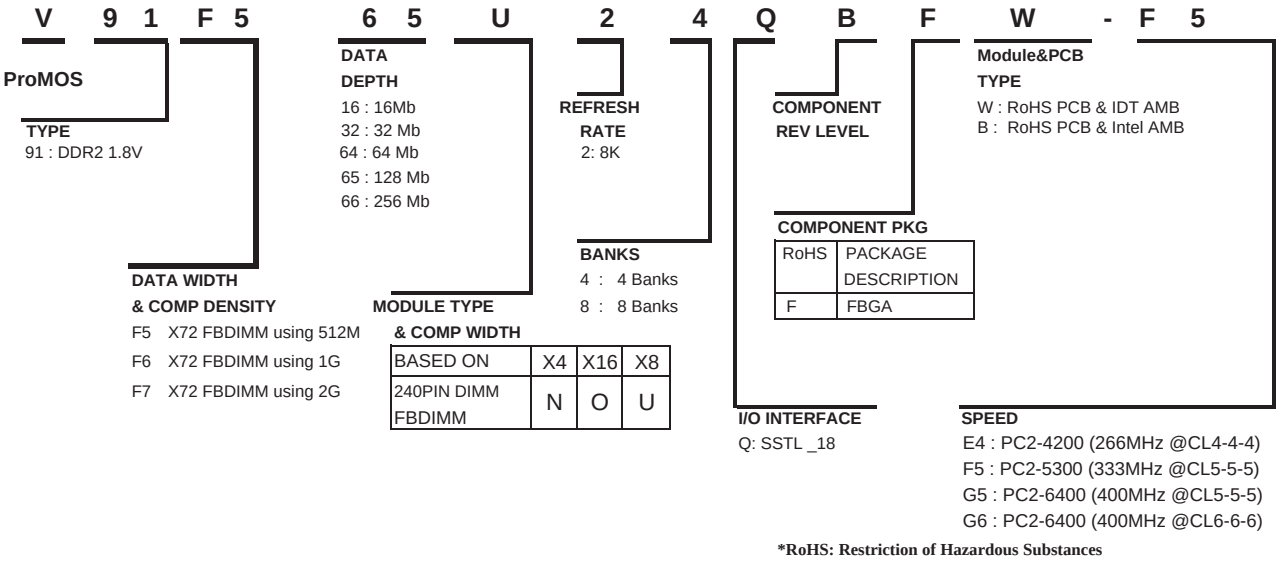
Speed Grade

	DDR2-533 PC2-4200 (E4)	DDR2-667 PC2-5300 (F5)	Units
Bandwith @CL=3	400	400	Mbps
Bandwith @CL=4	533	533	Mbps
Bandwith @CL=5	533	667	Mbps
CL-tRCD-tRP	4-4-4	5-5-5	tCK

240-PIN FBDIMM



Part Number Information

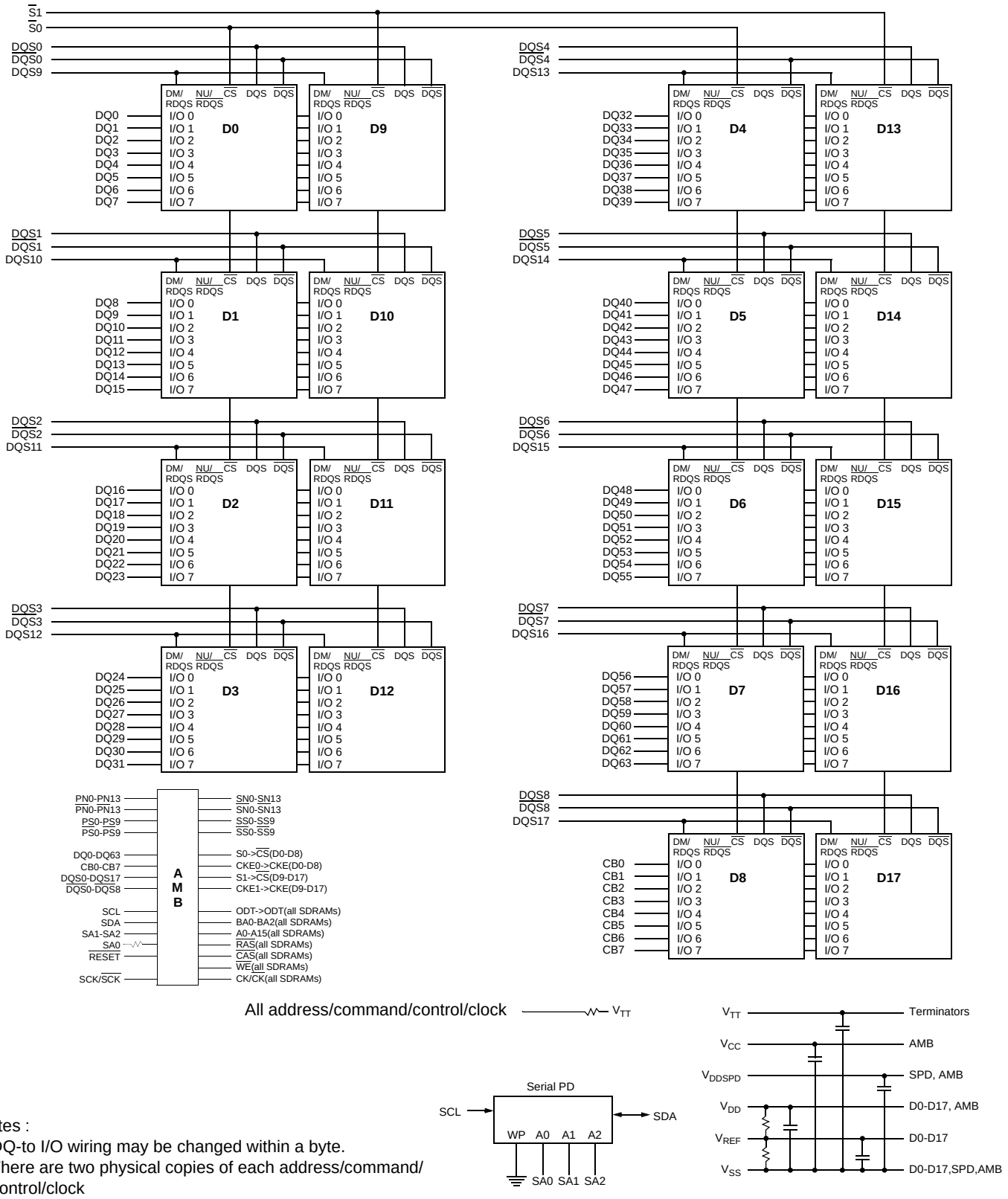


***RoHS: Restriction of Hazardous Substances**

Block Diagram

Functional Block Diagram: 1GB, 128Mx72 Module

(populated as 2 rank of x8 DDR2 SDRAMs)



Notes :

1. DQ-to I/O wiring may be changed within a byte.
2. There are two physical copies of each address/command/ control/clock

Pin Configuration (front/back side)

DDR2 240 Pin FBDIMM Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front	Pin	Front
1	V_{DD}	121	V_{DD}	31	PN3	151	SN3	61	$\overline{PN9}$	181	SN9	91	$\overline{PS9}$	211	$\overline{SS9}$
2	V_{DD}	122	V_{DD}	32	$\overline{PN3}$	152	$\overline{SN3}$	62	V_{SS}	182	V_{SS}	92	V_{SS}	212	V_{SS}
3	V_{DD}	123	V_{DD}	33	V_{SS}	153	V_{SS}	63	PN10	183	SN10	93	PS5	213	SS5
4	V_{SS}	124	V_{SS}	34	PN4	154	SN4	64	$\overline{PN10}$	184	$\overline{SN10}$	94	$\overline{PS5}$	214	$\overline{SS5}$
5	V_{DD}	125	V_{DD}	35	$\overline{PN4}$	155	$\overline{SN4}$	65	V_{SS}	185	V_{SS}	95	V_{SS}	215	V_{SS}
6	V_{DD}	126	V_{DD}	36	V_{SS}	156	V_{SS}	66	PN11	186	SN11	96	PS6	216	SS6
7	V_{DD}	127	V_{DD}	37	PN5	157	SN5	67	$\overline{PN11}$	187	$\overline{SN11}$	97	$\overline{PS6}$	217	$\overline{SS6}$
8	V_{SS}	128	V_{SS}	38	$\overline{PN5}$	158	$\overline{SN5}$	68	V_{SS}	188	V_{SS}	98	V_{SS}	218	V_{SS}
9	V_{CC}	129	V_{CC}	39	V_{SS}	159	V_{SS}	KEY				99	PS7	219	SS7
10	V_{CC}	130	V_{CC}	40	PN13	160	SN13	69	V_{SS}	189	V_{SS}	100	$\overline{PS7}$	220	$\overline{SS7}$
11	V_{SS}	131	V_{SS}	41	$\overline{PN13}$	161	$\overline{SN13}$	70	PS0	190	SS0	101	V_{SS}	221	V_{SS}
12	V_{CC}	132	V_{CC}	42	V_{SS}	162	V_{SS}	71	$\overline{PS0}$	191	$\overline{SS0}$	102	PS8	222	SS8
13	V_{CC}	133	V_{CC}	43	V_{SS}	163	V_{SS}	72	V_{SS}	192	V_{SS}	103	$\overline{PS8}$	223	$\overline{SS8}$
14	V_{SS}	134	V_{SS}	44	RFU*	164	RFU*	73	PS1	193	SS1	104	V_{SS}	224	V_{SS}
15	V_{TT}	135	V_{TT}	45	RFU*	165	RFU*	74	$\overline{PS1}$	194	$\overline{SS1}$	105	RFU**	225	RFU**
16	VID1	136	VID0	46	V_{SS}	166	V_{SS}	75	V_{SS}	195	V_{SS}	106	RFU**	226	RFU**
17	$\overline{RESET}$	137	DNU/M_Test	47	V_{SS}	167	V_{SS}	76	PS2	196	SS2	107	V_{SS}	227	V_{SS}
18	V_{SS}	138	V_{SS}	48	PN12	168	SN12	77	$\overline{PS2}$	197	$\overline{SS2}$	108	V_{DD}	228	SCK
19	RFU**	139	RFU**	49	$\overline{PN12}$	169	$\overline{SN12}$	78	V_{SS}	198	V_{SS}	109	V_{DD}	229	$\overline{SCK}$
20	RFU**	140	RFU**	50	V_{SS}	170	V_{SS}	79	PS3	199	SS3	110	V_{SS}	230	V_{SS}
21	V_{SS}	141	V_{SS}	51	PN6	171	SN6	80	$\overline{PS3}$	200	$\overline{SS3}$	111	V_{DD}	231	V_{DD}
22	PN0	142	SN0	52	$\overline{PN6}$	172	$\overline{SN6}$	81	V_{SS}	201	V_{SS}	112	V_{DD}	232	V_{DD}
23	$\overline{PN0}$	143	$\overline{SN0}$	53	V_{SS}	173	V_{SS}	82	PS4	202	SS4	113	V_{DD}	233	V_{DD}
24	V_{SS}	144	V_{SS}	54	PN7	174	SN7	83	$\overline{PS4}$	203	$\overline{SS4}$	114	V_{SS}	234	V_{SS}
25	PN1	145	SN1	55	$\overline{PN7}$	175	$\overline{SN7}$	84	V_{SS}	204	V_{SS}	115	V_{DD}	235	V_{DD}
26	$\overline{PN1}$	146	$\overline{SN1}$	56	V_{SS}	176	V_{SS}	85	V_{SS}	205	V_{SS}	116	V_{DD}	236	V_{DD}
27	V_{SS}	147	V_{SS}	57	PN8	177	SN8	86	RFU*	206	RFU*	117	V_{TT}	237	V_{TT}
28	PN2	148	SN2	58	$\overline{PN8}$	178	$\overline{SN8}$	87	RFU*	207	RFU*	118	SA2	238	VDDSPD
29	$\overline{PN2}$	149	$\overline{SN2}$	59	V_{SS}	179	V_{SS}	88	V_{SS}	208	V_{SS}	119	SDA	239	SA0
30	V_{SS}	150	V_{SS}	60	PN9	180	SN9	89	V_{SS}	209	V_{SS}	120	SCL	240	SA1
								90	PS9	210	SS9				

RFU = Reserved Future Use.
* These pin positions are reserved for forwarded clocks to be used in future module implementations
** These pin positions are reserved for future architecture flexibility

1. The following signals are CRC bits and thus appear out of the normal sequence : PN12/$\overline{PN12}$, SN12/$\overline{SN12}$, PN13/$\overline{PN13}$, SN13/$\overline{SN12}$, PS9/$\overline{PS9}$, SS9/$\overline{SS9}$.

Pin Description

Pin Name	Type	Pin Description	Pin Numbers
SCK	Input	System Clock Input, positive line	228
$\overline{SCK}$	Input	System Clock Input, negative line	229
PN[13:0]	Output	Primary northbound Data, positive lines	22, 25, 28, 31, 34, 37, 40, 48, 51, 54, 57, 60, 63, 66
$\overline{PN}$[13:0]	Output	Primary northbound Data, negative lines	23, 26, 29, 32, 35, 38, 41, 49, 52, 55, 58, 61, 64, 67
PS[9:0]	Input	Primary Southbound Data, positive lines	70, 73, 76, 79, 82, 90, 93, 96, 99, 102
$\overline{PS}$[9:0]	Input	Primary Southbound Data, negative lines	71, 74, 77, 80, 83, 91, 94, 97, 100, 103
SN[13:0]	Output	Secondary Northbound Data, positive lines	142, 145, 148, 151, 154, 157, 160, 168, 171, 174, 177, 180, 183, 186
$\overline{SN}$[13:0]	Output	Secondary Northbound Data, negative lines	143, 146, 149, 152, 155, 158, 161, 16, 172, 175, 178, 181, 184, 187
SS[9:0]	Input	Secondary Southbound Data, positive lines	190, 193, 196, 199, 202, 210, 213, 216, 219, 222
$\overline{SS}$[9:0]	Input	Secondary Southbound Data, negative lines	191, 194, 197, 200, 203, 211, 214, 217, 220, 223
SCL	Input	Serial Presence Detect (SPD) Clock Input	120
SDA	Input	SPD Data Input / Output	119
SA[2:0]	Input	SPD Address Inputs, also used to slelect the DIMM number in the AMB	118, 239, 240
VID[1:0]	NC	Voltage ID : These pins must be unconnected for DDR2 - based Fully Buffered DIMMs VID[0] is V_{DD} value : OPEN = 1.8 V, GND = 1.5 V ; VID[1] is V_{CC} value : OPEN = 1.5V, GND = 1.2V	16, 136
RESET	Input	AMB reset signal	17
RFU	RFU	Reserved for Future Use	19, 20, 44, 45, 86, 87, 105, 106, 139, 140, 164, 165, 206, 207, 225, 226
V_{CC}	PWR	AMB Core Power and AMB Channel Interface Power (1.5 Volt)	9, 10, 12, 13, 129, 130, 132, 133
V_{DD}	PWR	DRAM Power and AMB DRAM I/O Power (1.8Volt)	1, 2, 3, 5, 6, 7, 108, 109, 111, 112, 113, 115, 116, 121, 122, 123, 125, 126, 127, 231, 232, 233, 235, 236
V_{TT}	PWR	DRAM Address/Command/Clcok Termination Power(V_{DD}/2)	15, 117, 135, 237
V_{DDSPD}	PWR	SPD Power	238
V_{SS}	GND	Ground	4, 8, 11, 14, 18, 21, 24, 27, 30, 33, 36, 39, 42, 43, 46, 47, 50, 53, 56, 59, 62, 65, 68, 69, 72, 75, 78, 81, 84, 85, 88, 89, 92, 95, 98, 101, 104, 107, 110, 114, 124, 128, 131, 134, 138, 141, 144, 147, 150, 153, 156, 159, 162, 163, 166, 167, 170, 173, 176, 179, 182, 185, 188, 189, 192, 195, 198, 201, 204, 205, 208, 209, 212, 215, 218, 221, 224, 227, 230, 234
DNU/M_Test	DNU	The DNU/M_Test pin provides an external connection R/Cs A-D for testing the margin of Vref which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and if it does, will be included in this specification at that time.	137

FB-DIMM Operation Overview

FB-DIMM(Fully Buffered Dual in Line Memory Module) is a high-bandwidth, large capacity channel solution that utilizes a narrow host interface. Its serial link interface with packet data format and dedicated read/write paths are main element of the FBDIMM protocol, which is very much different than the registered DIMM and Unbuffered DIMM. The architecture includes the AMB (Advanced Memory Buffer) that isolates the DDR2 SDRAM device from the channel. This single-chip AMB component, located in the center of each FBDIMM, acts as a repeater and buffer for all signals and commands exchanged betwenn the host controller and DDR2 SDRAM devices. The AMB communicates with the host controller and adjacent FBDIMMs on a system that using high speed 1.5V industrial-standard differential Point-to-Point interface. The AMB interface is responsible for handling all transaction to and from the local FBDIMM and for forwarding requests to other FBDIMMs on the memory channel.

Advanced Memory Buffer (AMB)

The AMB is a memory interface that connects the DDR2 SDRAM devices to the FBDIMM channel. The AMB is a slave device on the channel responding to channel commands and forwarding channel commands to the other AMB devices.

The AMB is expected to perform the following functions:

_Support channel initialization procedures as defined in the initialization section of the FBDIMM chitecture and Protocol Specification to align the clokcs and the fame boundaries and verigy channel connectivity

_Support the forwarding of southbound and northbound frames, servicing requests directed to a specific FBDIMM's AMB, as defined in the protocol chapter of the specification, and merging the return data into the northbound frames

_If the AMB resides on the last DIMM in the channel, the AMB initializes northbound frames

_Detects errors on the channel and reports them to the host memory controller

_Supports the FBDIMM configuration register set as defined in the FBDIMM AMB specification register chapter of the specification

_Acts as DRAM memory buffer for all read, write and configuration accesses addressed to the DIMM

_Provide a read and write buffer FIFO

_Support an SMBus protocol interface for access to the AMB configuration registers

_Provide features to support MEMBIST and IBISt test functions

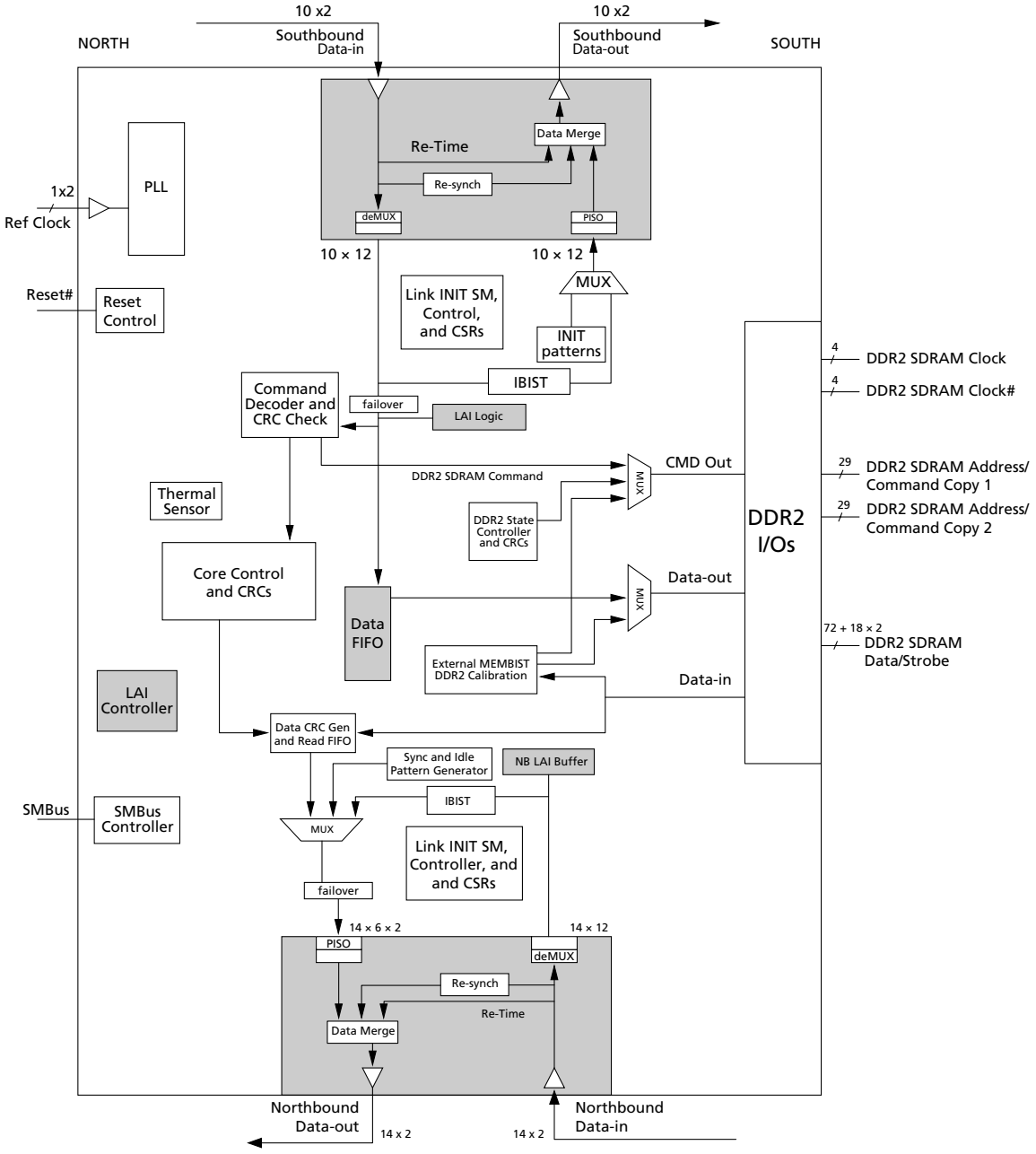
_Provide a register interface for the thermal sensor and status indicator

_Function as a repeater to extend the maximum length of the FBDIMM Links

_Reconfigures FBDIMM inputs from differential high speed link receivers to two single ended lower speed receivers (~200 MHz). These inputs directly control DDR2 command/address and input data that replicated to all DRAMs

_Uses low speed direct drive FBDINMM outputs to bypass high speed Parallel/Serial circuitry and provide test results back to tester

AMB Block Diagram



High-Speed Differential Point-to-Pint Link (at 1.5V) interfaces

The Advanced Memory Buffer supports one FBDIMM Channel consisting of two bidirectional link interfaces using highs peed differential point-to-point electrical signaling. The southbound input link is 10 lanes wide and carries commands and write data from the host memory controller or the adjacent DIMM in the host direction. The southbound output link forwards this same data to the next FBDIMM. The north-bound input link is 14 lanes wide and carries read return data or status information from the next FBDIMM in the chain back towards the host. The northbound output link forwards this information back towards the host and multiplexers in any read return data or status information that is generated internally. Data and commands sent to the DRAMs travel southbound on 10 primary differential signal line pairs. Data received from the DRAMs and status information travel northbound on 14 primary differential pairs. Data and commands sent to the adjacent DIMM upstream are repeated and travel further southbound on 10 secondary differential pairs. Data and status information received from the adjacent DIMM upstream travel further northbound on 14 secondary differential pairs.

DDR2 Channel

The DDR2 channel on the Advanced Memory Buffer supports direct connection to DDR2 SDRAMs. The DDR2 channel supports two ranks of eight banks with 16 row/column request, 64 data, and eight check-bit signals. There are two copies of address and command signals to support DIMM routing and electrical requirements. Four transfer bursts are driven on the data and check-bit lines at 800MHz. Propagation delays between read data/check-bit strobe lanes on a given channel can differ. Each strobe can be calibrated by hardware state machine using write/read trial and error. Hardware aligns the read data and check-bits to a single core clock. The Advanced Memory Buffer provides four copies of the command clock phase references(CLK[3:0]) and write data/check-bit strobes (DQSs) for each DRAM nibble.

SMBus Slave Interface

The Advanced Memory Buffer supports an SMBus interface to allow system access to configuration registers independent of the FBDIMM link. The Advanced Memory Buffer will never be a master on the SMBus, only a slave. Serial SMBus data transfer is supported at 100kHz. SMBus data transfer is supported at 100kHz. SMBus access to the Advanced Memory Buffer maybe a requirement to boot and to set link strength, frequency and other parameters needed to insure robust configurations. It is also required for diagnostic support when the link is down. The SMBus address straps located on the DIMM connector are used by the unique ID.

Channel Latency

FBDIMM channel latency is measured from the time a read request is driven on the FBDIMM channel pins to the time when the first 16 bytes (2nd chunk) of read completion data is sampled by the memory controller. When not using the variable read latency capability, the latency for a specific DIMM on a channel is always equal to the latency for any other DIMM on that channel. However, the latency for each DIMM in a specific configuration with some number of DIMMs installed may not be equal

Peak Theoretical Throughput

An FBDIMM channel transfers read completion data on the FBDIMM Northbound data connection. 144 bits of data are transferred for every FBDIMM Northbound data frame. This matches the 18 byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 from a single channel or a DRAM burst of four from to lock-stepped channels provides a total of 72 bytes of data (64 bytes plus 8 bytes ECC).

The FBDIMM frame rate matches the DRAM command clock because of the fixed 6:1 ratio of the channel clock to the DRAM command clock. Therefore, the Northbound data connection will exhibit the same peak theoretical throughput as a single DRAM channel. For example, when using the DDR2 533 DRAMs, the peak theoretical bandwidth of the Northbound data connection is 4.267 GB/sec. Write data is transferred on the Southbound command and data connection, via Command+Wdata frames. 72 bits of data are transferred for every Command+Wdata frame. Two Command+Wdata frames match the 18-byte data transfer of an ECC DDR DRAM in a single DRAM command clock. A DRAM burst of 8 transfers from a single channel,

one half the peak theoretical throughput of a single DRAM channel. For example, when using DDR2 533 DRAMs, the peak theoretical bandwidth of the Southbound command and data connection is 2.133GB/sec. The total peak theoretical throughput of a single FBDIMM channel is defined as the sum of peak theoretical throughput of the Northbound data connection and the South command and data connection. When the frame rate matches the DRAM command clock, this is equal to 1.5 times the peak theoretical throughput of a single DRAM channel. Foe example, when using DDR2 533 DRAMs, the peak theoretical throughput of a single DDR2-533 channel would be 4.267 GB/sec., while the peak theoretical throughput of the entire FB-DIMM 533 channel would be 6.4GB/sec.

Hot-add

The FBDIMM channel does not provide a mechanism to automatically detect and report the addition of a new FBDIMM south of the currently active last FBDIMM. It is assumed the system will be notified through some means of the addition of one or more new FBDIMMs so that specific commands can be sent to the host controller to initialize the newly added FBDIMM and perform a hot-add reset to bring them into the channel timing domain. It should be noted that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-remove

In order to accomplish the removal of the FBDIMM, the host must preform a fast reset sequence targeted at the last FBDIMM that will be retained on the channel. The fast reset re-establishes the appropriate last FB-DIMM so that the southbound transmission outputs of the last active FBDIMM and the southbound and northbound outputs of the FBDIMMs beyond the last active FBDIMM are disabled. Once the appropriate outputs are disbaled, the system can coordinate the procedure to remove power in preparation for physical removal of the FBDIMM if needed. Note that the power to the FBDIMM socket must be removed before a hot-add FBDIMM is inserted or removed. Applying or removing the power to a FBDIMM socket is a system platform function.

Hot-replace

Hot replace of FBDIMM is accomplished through combining the hot-remove and hotadd processes.

Serial Presence Detect Information

Bin Sort:

E4 (PC2-4200 @ CL4) F5 (PC2-5300 @ CL5)

Byte #	Function described	Function Supported		Hex value	
		E4	F5	E4	F5
0	CRC Coverage/Number of Serial PD Bytes Written /bytes used	CRC=116 Size=256 Used Bytes=176		92h	
1	SPD Revision	Rev 1.1		11h	
2	Key Byte / DRAM Device Type	DDR2 FBDIMM		09h	
3	Voltage Levels of this Assembly	DRAM=1.8V Channel=1.5V		12h	
4	SDRAM Addressing	512Mb		44h	
5	Module Physical Attributes	30 ~ 35mm height 8~ 9 mm thick		24h	
6	Module Type / Thickness	FBDIMM 133.35mm		07h	
7	Module Organization	2 rank/ x8 device		11h	
8	Fine Timebase Dividend and Divisor	2.5ps		52h	
9	Medium Timebase Dividend	1/4(0.25ns)		01h	
10	Medium Timebase Divisor	1/4(0.25ns)		04h	
11	SDRAM Minimum Cycle Time (tCKmin)	3.75ns	3ns	0Fh	0Ch
12	SDRAM Maximum Cycle Time (tCKmax)	8ns	8ns	20h	20h
13	SDRAM $\overline{CAS}$ Latencies Supported	CL3,4,5		33h	
14	SDRAM Minimum $\overline{CAS}$ Latency Time (tCAS)	15ns		3Ch	
15	SDRAM Write Recovery Time Supported	2,3,4 clk	2,3,4,5 clk	32h	42h
16	SDRAM Write Recovery Time (tWR)	15ns		3Ch	
17	SDRAM Write Latencies Supported	2,3,4 clk		32h	
18	SDRAM Additive Latencies Supported	0,1,2,3 clk		40h	
19	SDRAM Minimum $\overline{RAS}$ to $\overline{CAS}$ Delay (tRCD)	15ns		3Ch	
20	SDRAM Minimum Row Active to Row Active Delay (tRRD)	7.5ns		1Eh	
21	SDRAM Minimum Row Precharge Time (tRP)	15ns		3Ch	
22	SDRAM Upper Nibbles for tRAS and tRC	0		00h	
23	SDRAM Minimum Active to Precharge Time (tRAS)	45ns		B4h	
24	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Time (tRC)	60ns		F0h	
25	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC - MSB)	105ns		A4h	
26	SDRAM Minimum Auto-Refresh to Active/Auto-Refresh Command Period (tRFC - LSB)	105ns		01h	
27	SDRAM Internal Write to Read Command Delay (tWTR)	7.5ns		1Eh	
28	SDRAM Internal Read to Precharge Command Delay (tRTP)	7.5ns		1Eh	

Byte #	Function described	Function Supported		Hex value	
		E4	F5	E4	F5
29	SDRAM Burst Lengths Supported	BL 4,8		03h	
30	SDRAM Terminations Supported	50, 75, 150 ohm		07h	
31	SDRAM Drivers Supported	Weak Driver Supported		01h	
32	SDRAM Average Refresh Interval (tREFI)/Double Refresh mode bit/High Temperature self-refresh rate support indication	7.8us		02h	
33	Bit 7:4; Tcasemax Delta 3:0; DT4R4W Delta	_		02h	
34	Thermal resistance of SDRAM device package from top (case0 to ambient (Psi T-A SDRAM)	_		32h	
35	DT0/Tcase mode bits: Bits 7:2: Case temperature rise from ambient due to IDD0/activate precharge operation minus 2.8^{o}C offset temperature. Bit 1: Double refresh mode bit. Bit 0: High temperature self-refresh rate support indication	_		04h	
36	DT2N/DT2Q: Case temperature rise from ambient due to IDD2N/precharge standby operation for UDIMM and due to IDD2Q/precharge quiet standby operation for RDIMM	_		0Eh	
37	DT2P: Case temperature rise from ambient due to IDD2P/precharge power-down operation	_		0Ah	
38	DT3N: Case temperature rise from ambient due to IDD3N/active standby operation	_		0Dh	
39	DT4R/mode bit: Bits 7:1: Case temperature rise from ambient due to IDD4R/page open burst read operation. Bit 0: Mode bit to specify if DT4W is greater or less than DT4R	_		18h	
40	DT5B: Case temperature rise from ambient due to IDD5B/burst refresh operation	_		0Fh	
41	DT7: Case temperature rise from ambient due to IDD7/bank interleave read mode operation	_		12h	
42-78	FBDIMM reserved bytes	_		00h	
79	FBDIMM ODT definition	Rank 0(75 ohm)		01h	
80	FBDIMM reserved byte	_		00h	
81	Chanel protocol supported (lower byte)	_		02h	
82	Chanel protocol supported (upper byte)	_		00h	
83	Back-to-back turnaround clock cycles	_		10h	
84	Buffer read access at tCK for max CL	_		36h	
85	Buffer read access at tCK for max CL - 1	_		34h	
86	Buffer read access at tCK for max LC - 2	_		32h	
87	PSI T-A AMB	_		2Ah	
88	DT AMB idle_0	_		4Ch	56h
89	DT AMB idle_1	_		61h	6Bh
90	DT AMB idle_2	_		50h	5Ch
91	DT AMB active_1	_		82h	91h

Byte #	Function described	Function Supported		Hex value	
		E4	F5	E4	F5
92	DT AMB active_2	-		69h	76h
93	DT AMB LOS	-		00h	
94	PSI T-A DRAM-AF	-		00h	
95	PSI T-A AMB-AF	-		00h	
96	PSI D-A	-		00h	
97	PSI A-D	-		00h	
98	AMB TJMAX	-		1Fh	
99	Airflow imp/DRAM/heat spreader types	Type3, Planar, FMHS		CAh	
100	Reserved	-		00h	
101	AMB Pre-initialization bytes	-		40h	
102	AMB Pre-initialization bytes	-		C0h	
103	AMB Pre-initialization bytes	-		02h	
104	AMB Pre-initialization bytes	-		44h	
105	AMB Pre-initialization bytes	-		9Ch	
106	AMB Pre-initialization bytes	-		30h	
107	AMB Post-initialization bytes	-		60h	
108	AMB Post-initialization bytes	-		33h	
109	AMB Post-initialization bytes	-		60h	
110	AMB Post-initialization bytes	-		1Bh	
111	AMB Post-initialization bytes	-		60h	
112	AMB Post-initialization bytes	-		1Bh	
113	AMB Post-initialization bytes	-		60h	
114	AMB Post-initialization bytes	-		1Bh	
115	AMB manufacturer's ID code (lower byte)	IDT		80h	
116	AMB manufacturer's ID code (upper byte)	IDT		B3h	
117-118	Module ID: Module manufacturer's JEDEC ID code	ProMOS		40h	
119	Module ID: Module manufacturing location	02=Taiwan 05=China 0a=S-CH 04=Malaysia			
120-121	Module ID: Module manufacturing date	-			
122-125	Module ID: Module serial number	-			
126-127	Checksum for bytes 0-116	-			
128-145	Module part number	V91F565U24QB			
146-147	Module revision code	-		00h	
148-149	DRAM manufacturer's JEDEC ID code	ProMOS		40h	
150-175	Manufacturer-specific data (RSVD)	-		00h	
176-255	Open for customer use	-		00h	

Reference Clock Input Specifications

Parameter	Symbol	Values		Units	Note
		MIN	MAX		
Reference clock frequency	fsck	133	200	MHz	1.2
Rise time, fall time	$T_{SCK-RISE}$, $T_{SCK-FALL}$	175	700	ps	3
Voltage high	$V_{SCK-HIGH}$	660	850	mV	
Voltage low	$V_{SCK-LOW}$	-150		mV	
Absolute crossing point	$V_{CROSS-ABS}$	250	550	mV	4
Relative crossing	$V_{CROSS-REL}$	calculated	calculated		4,5
Percent mismatch between rise and fall times	$T_{SCK-RISE-FALL-MATCH}$	-	10	%	
Duty cycle of reference clock	$T_{SCK-DUTYCYCLE}$	40	60	%	
Clock leakage current	I_{I-CK}	-10	10	uA	6,7
Clock input capacitance	C_{I-CK}	0.5	2	pF	7
Clock input capacitance delta	$C_{I\_CK(D)}$	-0.25	0.25	pF	8
Transport delay	T1		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10^{16}		Periods	11
Reference clock jitter, filtered	$T_{REF-JITTER}$		40	ps	12,13
Reference clock deterministic jitter	T_{REF-DJ}		TBD	ps	

Notes :

1.133MHz for PC2-4200 and 166MHz for PC2-5300.

2. Measured with SSC disabled.

3. Measured differentially through the range of 0.175V to 0.525V.

4. The crossing point must meet the absolute and relative crossing point specification simultaneously.

5. $V_{CROSS\_REL\_(MIN)}$ and $V_{CROSS\_REL(MAX)}$ are derived using the following calculation : Min = $0.5(V_{havg}-0.710)+0.250$;and Max=$0.5(V_{havg}-0.710)+0.550$, where Vhavg is the average of $V_{SCK-HIGHM.}$

6. Measured with a single-ended input voltage of 1V.

7. Applies to reference clocks SCK and $\overline{SCK}$.

8. Difference between SCK and $\overline{SCK}$ input.

9. T1 = [Tdatapath-Tclockpath](excluding PLL loop delays). This parameter is not a direct clock output parameter but in indirectly determines the clock output parameter $T_{REF-JITTER.}$

10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data dampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. The path delays are caused by copper trace routes. on-chip routing, on-chip buffering, etc. They include the time-of flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.

11. Direct measurement of phase jitter records over 1016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10^{16} samples extrapolated from an estimate of the sigma of the random jitter components.

12. Measured with SSC enabled on reference clock generator.

13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal - MIN parameters

Differential Receiver Input Specifications

Parameter	Symbol	Values		Units	Comments
		MIN	MAX		
Differential peak-to-peak input voltage for large voltage swing	$V_{RX-DIFFp-p}$	170	TBD	mV	EQ 5, Note1
Maximum single-ended voltage in El condition	$V_{RX-IDLE-SE}$		75	mV	2,3
Maximum single-ended voltage in Ei condition (DC only)	$V_{RX-IDLE-SE-DC}$		50	mV	2,3
Maximum peak-to-peak differential voltage in El condition	$V_{RX-IDLE-DIFFp-p}$		65	mV	3
Single-ended voltage (w.r.t. V_{SS}) on D+/D-	V_{RX-SE}	-300	900	mV	4
Single-pulse peak differential input voltage	$V_{RX-DIFF-PULSE}$	85		mV	4,5
Amplitude ratio between adjacent symbols	$V_{RX-DIFF-ADJ-RATIO}$		TBD		4,6
Maximum RX inherent timing error, 3.2 and 4.0 Gb/x	$T_{RX-TJ-MAX}$		0.4	UI	4,7,8
Maximum RX inherent deterministic timing error, 3.2 and 4.8 Gb/s	$T_{RX-TJ-MAX4.8}$		TBD	UI	4,7,8
Single-pulse width as zero-voltage crossing	$V_{RX-DJ-DD}$		0.3	UI	4,7,8,9
Skingle-pulse width at minimum-level crossing	$V_{RX-DJ-DD-4.8}$		TBD	UI	4,7,8,9
Differential RX input rise/fall time	$T_{RX-PW-ZC}$	0.55		UI	4,5
common mode fo the input voltage	$T_{RX-PW-ML}$	0.2		UI	4.5
Differential RX output rise/fall time	$T_{RX-RISE}$ $T_{RX-FALL}$	50		ps	20~80% voltage
Common mode of input voltage	V_{RX-CM}	120	400	mV	EQ 6, Note1, 10
AC peak-to-peak common mode of input voltage	$V_{RX-CM-ACp-p}$		270	mV	EQ 7, Note 1
Ratio of $V_{RX-CM-ACp-p}$ to minimum $V_{RX-DIFFp-p}$	$V_{RX-CM-EH-RATOP}$		45	%	11
Differential return loss	$RL_{RX-DIFF}$	9		dB	1GHz-2.4 GHz, Note 12
Common mode return loss	RL_{RX-CM}	6		dB	1GHz-2.4 GHz, Note 12
RX termination impedance	R_{RX}	41	55		13
D+/D- RX Impedance difference	$R_{RX-MATCH-DC}$		4	%	EQ 8
Lane-to lane PCB skew at RX	$L_{RX-PCB-SKEW}$		6	UI	Lane-to-lane skew at the receiver that must be tolerated. Note 14
Minimum RX drift tolerance	$T_{RX-DRIFT}$	400		ps	15
Minim data tracking 3dB bandwidth	F_{TRK}	0.2		MHz	16
Electrical idle entry detect time	$T_{EI-ENTRY-DETECT}$		60	ns	17
Electrical idle exit detect time	$T_{EI-EXIT-DETECT}$		30	ns	
Bit Error Ratio	BER		10^{-12}		18

Notes :

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D-are interpreted as the Electrical Idle condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the El condition before the device can act upon the El detection.
4. Specified at the package pins into a timing and voltage compliance test setup.
5. The single-pulse mask provides suffcient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. The relative amplitude ratio limit between adjacent symbols prevents excessive intersymbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of SSC or reference clock jitter.
8. This number includes setup and hold of the RX sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15 mV DC offset between transmit and receive devices.

11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peaktopeak common mode specification. For example, if VRX-DIFFp-p is 200 mV, the maximum AC peak-to peak common mode is the lesser of (200 mV*0.45=90 mV)and VRX-CM-AC-p-p.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance; tolerance across voltage from 100 mV to 400 mV shall not exceed +/-5 W with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assume the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI,
17. The specified time includes the time required to forward the El entry condition.
18. BER per differential lane.

$V_{RX\text{-}DIFFp\text{-}p} = 2x[V_{RX\text{-}D}+\text{-}V_{RX\text{-}D\text{-}}]$ (EQ5)

($V_{RX\text{-}CM}$ = DC(avg) of $[V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}}] /2$) (EQ 6)

$V_{RX\text{-}CM\text{-}AC}=((Max[V_{RX\text{-}D+} + V_{RX\text{-}D})/2)((Min\ [V_{RX\text{-}D+} + V_{RX\text{-}D\text{-}})/2)$ (EQ 7)

$R_{RX\text{-}MATCH\text{-}DC} = 2x((R_{RX\text{-}D+}\text{-}R_{RX\text{-}D\text{-}})/(R_{RX\text{-}D+} + R_{RX\text{-}D\text{-}})$ (EQ 8)

Absolute Maximum DC Ratings

Symbol	Min	Typical	Max	Units	Notes
DRAM V_{DD} / V_{DDQ}, AMB V_{DDQ}	1.7	1.8	1.9	V	
AMB V_{CC} / V_{CCFBD}	1.46	1.5	1.54	V	1
DRAM Interface V_{TT}	0.48 x V_{DD}	0.5 x V_{DD}	0.52 x V_{DD}	V	
V_{DDSPD}	3.0	3.3	3.6	V	
Note 1: Estimate					

DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 85° C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter	Min	Max	Units	Notes
VDD	Supply Voltage	1.7	1.9	V	1
VDDQ	I/O Supply Voltage	1.7	1.9	V	1
VSS, VSSQ	Supply Voltage, I/O Supply Voltage	0	0	V	
VREF	I/O Reference Voltage	0.49 x VDDQ	0.51 x VDDQ	V	1, 2
VTT	I/O Termination Voltage (System)	VREF - 0.04	VREF + 0.04	V	1, 3
VIH (DC)	Input High (Logic1) Voltage	VREF + 0.125	VDDQ + 0.3	V	1
VIL (DC)	Input Low (Logic0) Voltage	-0.3	VREF - 0.125	V	1
VIN (DC)	Input Voltage Level, CK and Inputs	-0.3	VDDQ + 0.3	V	1
VID (DC)	Input Differential Voltage, CK and Inputs	0.30	V DDQ + 0.6	V	1, 4
IIL	Input Leakage Current Any input 0V ≤ VIN ≤ VDD; (All other pins not under test = 0V)	-5	5	uA	1
IOZ	Output Leakage Current (DQs are disabled; 0V ≤ Vout ≤ VDDQ	-5	5	uA	1

Note:
1. Inputs are not recognized as valid until VREF stabilizes.
2. VREF is expected to be equal to 0.5 V DDQ of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed 2% of the DC value.
3. VTT is not applied directly to the DIMM. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
4. VID is the magnitude of the difference between the input level on CK and the input level on .

AC Operating Conditions

(T_{CASE} = 0 °C ~ 85° C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter/Condition	Min	Max	Unit	Notes
VIH (AC)	Input High (Logic 1) Voltage	V REF + 0.31	-	V	1, 2
VIL (AC)	Input Low (Logic 0) Voltage	-	V REF - 0.31	V	1, 2
VID (AC)	Input Differential Voltage, CK and Inputs	0.7	V DDQ + 0.6	V	1, 2, 3
VIX (AC)	Input Differential Pair Cross Point Voltage, CK and Inputs	0.5 x VDDQ - 0.2	0.5 x VDDQ + 0.2	V	1, 2, 4

1. Input slew rate = 1V/ ns.
2. Inputs are not recognized as valid until VREF stabilizes.
3. VID is the magnitude of the difference between the input level on CK and the input level on .
4. The value of VIX is expected to equal 0.5 x VDDQ of the transmitting device and must track variations in the DC level of the same.

Operating, Standby, and Refresh Currents

(T_{CASE} = 0 °C ~ 85° C; V_{DDQ} = 1.8V ± 0.1V; V_{DD} = 1.8V ± 0.1V, See AC Characteristics)

Symbol	Parameter/Condition	DDR2-533 (-E4) Max.	DDR2-667 (-F5) Max.	Unit	Notes
Idd_Idle_0	Idle Current, single or last DIMM. L0 state, idle (0BW). Primary channel enabled; Secondary Channel disabled. CKE high. Command and address line stable. DRAM clock active.	TBD	TBD	mA	
Idd_Idle_1	Idle Current, first DIMM. L0 stage, idle (0BW). Primary and Secondary channels enabled. CKE high. Command and address line stable. DRAM clock active.	TBD	TBD	mA	
Idd_Idle_2	Idle Current, DRAM power down. L0stage, idle (0BW). Primary and Secondary channels enabled CKE low. Command and address lines floated. DRAM clock active, ODT and CKE driven low.	TBD	TBD	mA	
Idd_Active_1	Active Power. L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. DRAM clock active, CKE high.	TBD	TBD	mA	
Idd_Active_2	Active Power, data pass through. L0 state. 50% DRAM BW to downstream DIMM, 67% read, 33% write. Primary and Secondary channels enabled. CKE high. Command and address lines stable. DRAM clock active.	TBD	TBD	mA	
Idd_L0s	Channel Standby. Average power over 42 frames where the channel enters and exits L0s. DRAMs Idle (0BW). CKE low. Command and address lines floated. DRAM clock active, ODE and CKE driven low.	TBD	TBD	mA	
Idd_Training	Primary and Secondary channels enabled. 100% toggle on all channel lanes. DRAMs idle. 0BW. CKE high, Command and address line stable. DRAM clock active.	TBD	TBD	mA	
Note:					

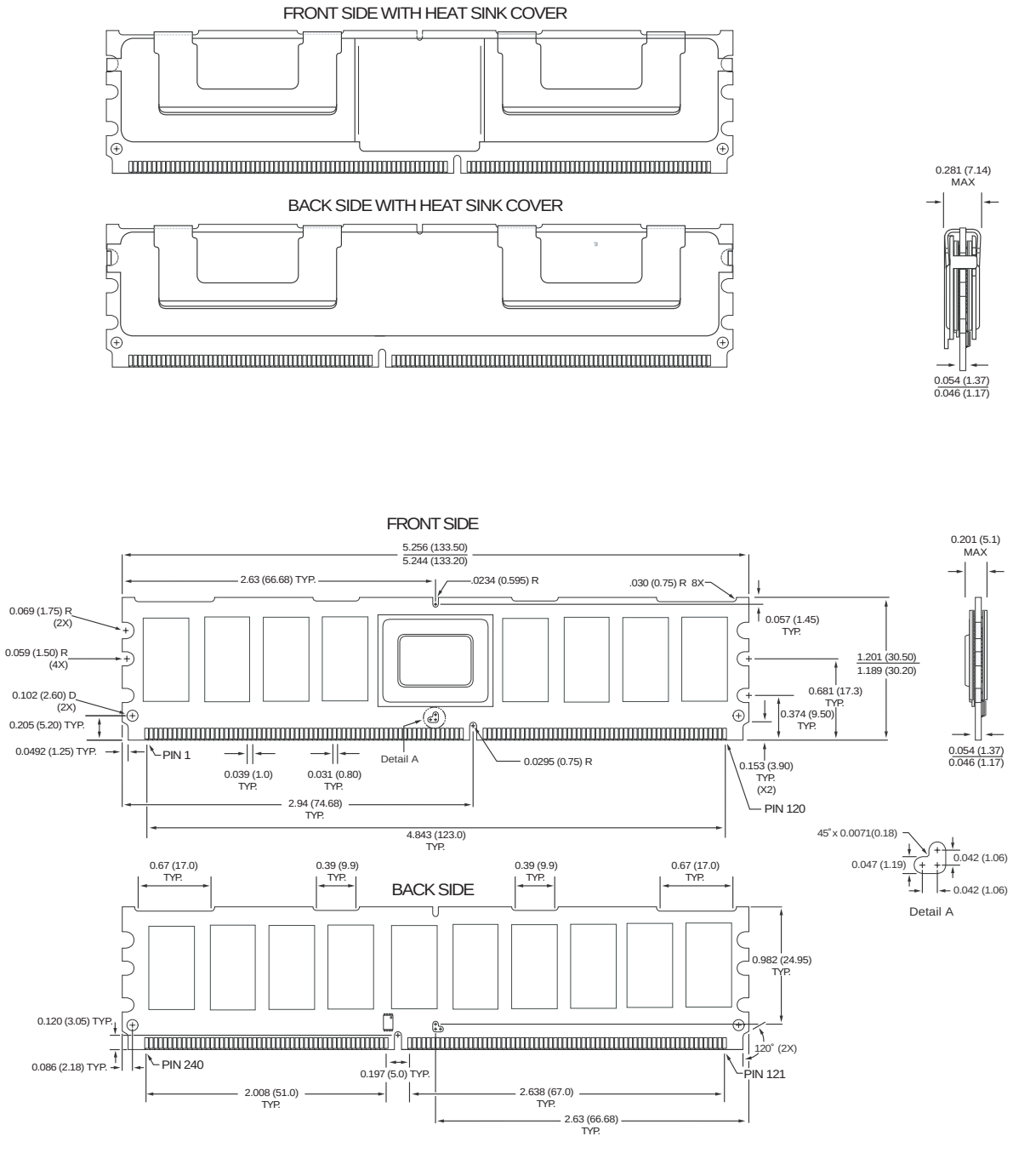
AC Characteristics (AC operating conditions unless otherwise noted)

Parameter		Symbol	(DDR2-533) -E4		(DDR2-667) -F5		Unit
			Min	Max	Min	Max	
Row Cycle Time		t_{RC}	60	-	60	-	ns
Auto Refresh Row Cycle Time		t_{RFC}	105	-	105	-	ns
Row Active Time		t_{RAS}	45	70K	45	70K	ns
Row Address to Column Address Delay		t_{RCD}	15	-	15	-	ns
Row Active to Row Active Delay (x4 & x8)		t_{RRD}	7.5	-	7.5	-	ns
Row Active to Row Active Delay (x16)		t_{RRD}	10	-	10	-	ns
Column Address to Column Address Delay		t_{CCD}	2	-	2	-	CLK
Row Precharge Time		t_{RP}	15	-	15	-	ns
Write Recovery Time		t_{WR}	15	-	15	-	ns
Last Data-In to Read Command		t_{DRL}	1	-	1	-	CLK
Auto Precharge Write Recovery + Precharge Time		t_{DAL}	t_{WR} +t_{RP}	-	t_{WR} +t_{RP}	-	ns
System Clock Cycle Time	$\overline{CAS}$ Latency = 3	t_{CK}	5	8	5	8	ns
	$\overline{CAS}$ Latency = 4		3.75	8	3.75	8	ns
	$\overline{CAS}$ Latency = 5		3.75	8	3	8	ns
Clock High Level Width		t_{CH}	0.45	0.55	0.45	0.55	CLK
Clock Low Level Width		t_{CL}	0.45	0.55	0.45	0.55	CLK
Data-Out edge to Clock edge Skew		t_{AC}	-0.50	0.50	-0.45	0.45	ns
DQS-Out edge to Clock edge Skew		t_{DQSCK}	-0.45	0.45	-0.40	0.40	ns
DQS-Out edge to Data-Out edge Skew		t_{DQSQ}	-	0.30	-	0.25	ns
Data-Out hold time from DQS		t_{QH}	t_{HPmin} -t_{QHS}	-	t_{HPmin} -t_{QHS}	-	ns
Data hold skew factor		t_{QHS}	-	400	-	350	ps
Clock Half Period		t_{HP}	$t_{CH/L}$ min	-	$t_{CH/L}$ min	-	ns
Input Setup Time (fast slew rate)		t_{IS}	250	-	200	-	ps
Input Hold Time (fast slew rate)		t_{IH}	375	-	325	-	ps
Input Pulse Width		t_{IPW}	0.35	-	0.35	-	CLK
Write DQS High Level Width		t_{DQSH}	0.35		0.35		CLK
Write DQS Low Level Width		t_{DQSL}	0.35		0.35		CLK
CLK to First Rising edge of DQS-In		t_{DQSS}	WL-0.25t_{CK}	WL+ 0.25t_{CK}	WL-0.25t_{CK}	WL+ 0.25t_{CK}	CLK
Data-In Setup Time to DQS-In (DQ & DM)		t_{DS}	100	-	50	-	ps
Data-in Hold Time to DQS-In (DQ & DM)		t_{DH}	225	-	175	-	ps
DQS falling edge to CLK rising Setup Time		t_{DSS}	0.2	-	0.2	-	CLK
DQS falling edge from CLK rising Hold Time		t_{DSH}	0.2	-	0.2	-	CLK

Parameter	Symbol	(DDR2-533) -E4		(DDR2-667) -F5		Unit
		Min	Max	Min	Max	
DQ & DM Input Pulse Width	t_{DIPW}	0.35	-	0.35	-	CLK
Read DQS Preamble Time	t_{RPRE}	0.9	1.1	0.9	1.1	CLK
Read DQS Postamble Time	t_{RPST}	0.4	0.6	0.4	0.6	CLK
Write DQS Preamble Setup Time	t_{WPRES}	0	-	0	-	CLK
Write DQS Preamble Hold Time	t_{WPREH}	0.25	-	0.25	-	CLK
Write DQS Postamble Time	t_{WPST}	0.4	0.6	0.4	0.6	CLK
Internal read to precharge command delay	t_{RTP}	7.5	-	7.5	-	ns
Internal write to read command delay	t_{WTR}	7.5	-	7.5	-	ns
Data out high impedance time from CLK/$\overline{CLK}$	t_{HZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Data out low impedance time from CLK/$\overline{CLK}$	t_{LZ}	$t_{AC(min)}$	$t_{AC(max)}$	$t_{AC(min)}$	$t_{AC(max)}$	ns
Mode Register Set Delay	t_{MRD}	2	-	2	-	CLK
Exit Self Refresh to Non-Read Command	t_{XSNR}	t_{RFC}+10	-	t_{RFC}+10	-	ns
Exit Self Refresh to Read Command	t_{XSRD}	200	-	200	-	CLK
Exit Precharge Power Down to any non-Read Command	t_{XP}	2	-	2	-	CLK
Exit Active Power Down to Read Command	t_{XARD}	2	-	2	-	CLK
Exit Active Power Down to Read Command (Slow exit, Lower Power)	t_{XARDS}	6-AL	-	6-AL	-	CLK
ODT drive mode output delay	t_{OIT}	0	12	0	12	ns
Minimum time clocks remains ON after CKE asynchronously drops LOW	t_{Delay}	tIS+tCK +tIH		tIS+tCK +tIH		ns
CKE minimum high and low pulse width	t_{CKE}	3	-	3	-	CLK
Average Periodic Refresh Interval 0C ≤ T ≤ 85C	t_{REFI}	-	7.8	-	7.8	us

Package Dimension

Units inches(milimeter), $\frac{\text{MIN}}{\text{MAX}}$ or Typical



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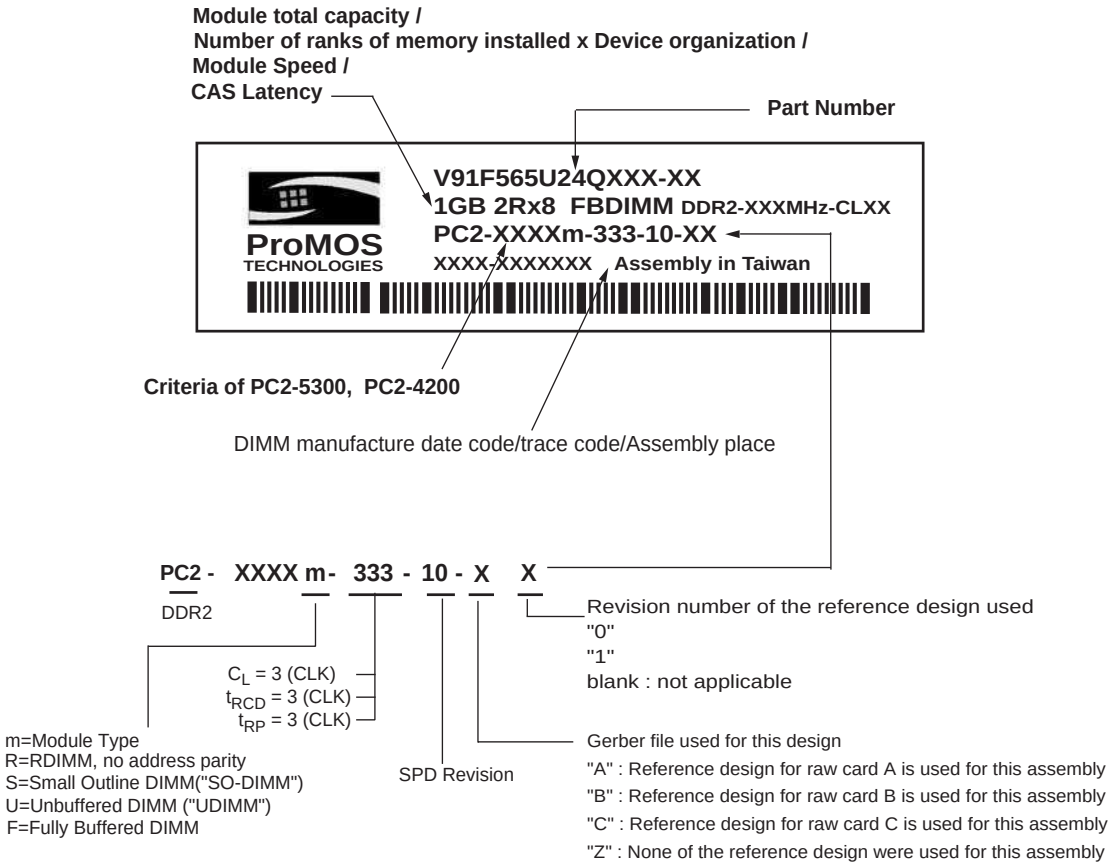

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