PIC24FJ64GA004 Family Silicon Errata and Data Sheet Clarification

The PIC24FJ64GA004 family devices that you have received conform functionally to the current Device Data Sheet (DS39881**D**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24FJ64GA004 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B8**).

Data Sheet clarifications and corrections start on page 17, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/ debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device*, and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24FJ64GA004 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A3/A4	B4	B5	B8
PIC24FJ64GA004	044Fh	3003h	3042h	3043h	3046h
PIC24FJ48GA004	044Eh				
PIC24FJ32GA004	044Dh				
PIC24FJ16GA004	044Ch				
PIC24FJ64GA002	0447h				
PIC24FJ48GA002	0446h				
PIC24FJ32GA002	0445h				
PIC24FJ16GA002	0444h				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC24FJXXXGA0XX Flash Programming Specification"* (DS39768) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3/A4	B4	B5	B8
JTAG	—	1.	Persistent pull-up (RA3) when JTAG disabled.	X			
LVD	—	2.	No LVD interrupt with low-voltage condition at Reset.	X			
Core	Idle mode	3.	Clock failure trap fails in Idle mode.	X			
Core	Doze mode	4.	RAM read repeat on entering Doze mode.	X			
Core	BOR	5.	POR and BOR flags both set on BOR.	X			
Core	RAM	6.	RAM size implementation on some devices.	X			
A/D	—	7.	Unimplemented channels may be selected.	X			
A/D	—	8.	Missing midscale conversion code.	X			
A/D	—	9.	Device may not wake when convert on INT0 trigger is selected.	X			
I^2C	SDA Line State (I2C1)	10.	Line state may not be detected correctly.	X			
UART	—	11.	Reception failures in High-Speed mode.	X			
UART	—	12.	Erroneous baud rate calculations in High-Speed mode.	X			
UART	Auto-Baud	13.	Double receive interrupt with auto-baud reception.	X			
UART	Auto-Baud	14.	Insertion of spurious data with auto-baud reception.	X			
UART	Auto-Baud	15.	Auto-baud calculation errors causing transmit or receive failures.	X			
UART	Break Character Generation	16.	The UART module will not generate back-to-back Break characters.	X	X	X	X
Output Compare	—	17.	Single missed compare events under certain conditions.	X			
SPI	Enhanced Buffer mode	18.	Some flag bits are set at incorrect times in Enhanced Buffer mode.	X			
SPI	—	19.	Module in Slave mode may ignore $\overline{SS}$ pin and receive data anyway.	X			
SPI	Enhanced Buffer mode	20.	No SPI interrupt in Enhanced Buffer mode under certain conditions.	X			
I/O	—	21.	Spec change for V_{OL} and V_{OH}.	X			
I/O	—	22.	OSCO/RA3 driven immediately following POR.	X			
JTAG	—	23.	Sync loss in ICSP™ mode.	X			
RTCC	—	24.	Write errors to ALCFGRPT register.	X			
I^2C	Slave mode	25.	In Slave mode, ACKSTAT bit state change.	X			
I^2C	—	26.	Issues with write operations on I2CxSTAT.	X			
UART	IrDA®	27.	IR baud clock only available during transmit.	X			
I/O	PPS	28.	Issues with digital signal priorities with RP12 and RP18.	X			
UART	UERIF Interrupt	29.	No UERIF flag with multiple errors.	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

TABLE 2: SILICON ISSUE SUMMARY (CONTINUED)

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A3/A4	B4	B5	B8
UART	FIFO Error Flags	30.	PERR and FERR not correctly set for all bytes in receive FIFO.	X	X	X	X
Core	BOR	31.	Spontaneous BOR events with low-range VDD.	X	X	X	X
Core	Instruction Set	32.	Loop count errors with REPEAT instruction and R-A-W stalls.	X			
Memory	PSV	33.	False address error traps at lower boundary of PSV space.	X	X	X	
RTCC	—	34.	Decrement of alarm repeat counter under certain conditions.	X	X	X	
SPI	Master mode	35.	SPIIF and SPIBEN may become set early under certain conditions.	X			
I^2C™	Master mode	36.	Module may respond to its own master transmission as a slave under certain conditions.	X	X	X	X
I^2C	Slave mode	37.	Failure to respond correctly to some reserved addresses in 10-bit mode.	X	X	X	X
I^2C	—	38.	TBF flag not cleared under certain conditions.	X			
UART	—	39.	Erroneous sampling and framing errors when using two Stop bits.	X	X	X	X
Oscillator	SOSC	40.	Low-power SOSC unimplemented.	X			
Voltage Regulator	—	41.	Standby mode not available.	X			
Core	Code-Protect	42.	General code protection disables bootloader functionality.		X		
SPI	—	43.	Interrupts when SPI is operating in Enhanced Buffer mode.	X	X	X	X
UART	IrDA®	44.	RXINV bit operation is inverted in IrDA® mode	X			
Core	Doze Mode	45.	Instruction execution glitches following DOZE bit changes.	X	X	X	X
SPI	Master mode	46.	Spurious transmission and reception of null data on wake-up from Sleep (Master mode).	X	X	X	X
SPI	Master mode	47.	Inaccurate SPITBF flag with high clock divider.		X	X	X
SPI	Framed modes	48.	Framed SPI modes not supported.	X	X	X	X
Core	Data SRAM	49.	Higher current consumption during SRAM operations.		X	X	
I/O Ports	PORTA and PORTB	50.	Some I/O pin functions do not work correctly under certain conditions	X	X	X	X
A/D Converter	—	51.	Once the A/D module is enabled, it may continue to draw extra current	X	X	X	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B8**).

1. Module: JTAG

When the JTAG is disabled, the pull-up resistor on the TDI pin (pin 35/RA9) will stay enabled on the 44-pin variants of the device. This can cause the device to draw extra current when asleep if the pin is used as an input and held low.

Work around:

The pin will not draw extra current if any of the following work around techniques are used:

- The pin is used as an output.
- The pin is driven high as an input.
- JTAG is enabled.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

2. Module: Low-Voltage Detect

The Low-Voltage Detect interrupt will not occur if the device comes out of Reset in a low-voltage state. To trigger an interrupt, the voltage must decrease to a low-voltage range while the device is running.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

3. Module: Core

If a clock failure occurs when the device is in Idle mode, the oscillator failure trap does not vector to the Trap Service Routine. Instead, the device will simply wake-up from Idle mode and continue code execution if the Fail-Safe Clock Monitor (FSCM) is enabled.

Work around

Whenever the device wakes up from Idle (assuming the FSCM is enabled), the user software should check the status of the OSCFAIL bit (INTCON1<1>) to determine whether a clock failure occurred, and then perform an appropriate clock switch operation.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

4. Module: Core

If a RAM read is performed on the instruction immediately prior to enabling Doze mode, then an extra read event will occur when Doze mode is enabled. On most SFRs and on user RAM space, this will have no visible effect. However, this can cause registers which perform actions on reads, such as auto-incrementing or decrementing a pointer or removing data from a FIFO buffer, to repeat that action, possibly resulting in lost data.

Work around

On the instruction prior to entering Doze mode, be sure not to read a register which performs a secondary action. Examples of this would be UART and SPI FIFO buffers, and the RTCVAL registers. The easiest way to ensure this does not occur is to execute a `NOP` instruction before entering Doze mode.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

5. Module: Core

On a Brown-out Reset, both the BOR and POR bits may be set. This may cause the Brown-out Reset condition to be indistinguishable from the Power-on Reset.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

6. Module: Core

The PIC24FJ16GA002 and PIC24FJ16GA004 devices have 8K of data RAM implemented instead of 4K. This will cause the address error trap not to function for addresses between 2000h and 27FFh.

Work around

Do not access RAM beyond address 17FFh to maintain software compatibility with future device revisions.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

7. Module: A/D

The AD1PCFG and AD1CHS registers allow unimplemented channels to be selected. If these channels are selected, they will read as if tied to VSS. These channels should be disabled.

Work around

Disable channels, AN13 and AN14, in the AD1PCFG register by ensuring that bits 13 and 14 are cleared.

Ensure that bits 5 and 12 of AD1CHS are maintained cleared. If these bits are set, it will cause the ADC to reference channels AN16-31.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

8. Module: A/D

The A/D module will not generate code 511. Any conversion which should result in 511 normally, will instead generate 510 or 512.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

9. Module: A/D

With the External Interrupt 0 (INT0) selected to start an A/D conversion (SSRC<2:0> = 001), the device may not wake-up from Sleep or Idle mode if more than one conversion is selected per interrupt (SMPI<3:0> <> 0000). Interrupts are generated correctly if the device is not in a Sleep or Idle mode.

Work around

Configure the A/D to generate an interrupt after every conversion (SMPI<3:0> = 0000). Use another wake-up source, such as the WDT or another interrupt source, to exit the Sleep or Idle mode. Alternatively, perform A/D conversions in Run mode.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

10. Module: I²C™ (I2C1, SDA Line State)

When using I2C1, the SDA1 line state may not be detected properly unless it is first held low for 150 ns after enabling the I²C module.

In Master mode, this error may cause a bus collision to occur instead of a Start bit transmission. Transmissions after the SDA1 pin has been held low will occur correctly.

In Slave mode, the device may not Acknowledge the first packet sent after enabling the I²C module. In this case, it will return a NACK instead of an ACK. The device will correctly respond to packets after detecting a low level on the line for 150 ns.

The I2C2 module operates as expected and does not exhibit this issue.

Work around

Using an external device or another I/O pin from the microcontroller, drive the SDA1 pin low.

If no external devices or additional I/O pins are available, it is sometimes possible to perform the work around internally, using the following steps:

- With the module in Master mode, configure the RB9 pin as an output.
- Clear the LATB9 bit (for the default I2C1 assignment) or LATB5 (for the alternate I2C1 assignment) to drive the pin low.
- Enable I2C1 by setting the I2CEN bit (I2C1CON<15>).

Note that this action could appear to be a Start bit to an I²C slave device on the bus if the RB8/SCL1 pin is not driven low prior to driving RB9/SDA1 low. It may be necessary to add additional capacitance to the SDA1 bus in order to maintain the low logic level long enough for the module to detect the low logic level. Make sure that when adding capacitance, that the application does not violate the I²C timing specifications.

In Slave mode, the I²C master device on the bus must either pull the SDAx line low, then high again, prior to sending the first packet to the device, or must resend the first packet.

Note that 150 ns is the *absolute maximum* time required to avoid the issue. It is possible to work around the issue using a shorter delay in some devices.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

11. Module: UART

When the UART is in High-Speed mode, BRGH (UxMODE<3>) is set; some optimal UxBRG values can cause reception to fail.

Work around

Test UxBRG values in the application to find a UxBRG value that works consistently for more high-speed applications. The user should verify that the UxBRG baud rate error does not exceed the application limits. If possible, it is recommended to use a comparable baud rate in Low-Speed mode.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

12. Module: UART

When the UART is in High-Speed mode (BRGH = 1), the auto-baud sequence can calculate the baud rate as if it were in Low-Speed mode.

Work around

The calculated baud rate can be modified by the following equation:

New BRG Value = (Auto-Baud BRG + 1) * 4 – 1

The user should verify that the baud rate error does not exceed application limits.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

13. Module: UART

When an auto-baud is detected, the receive interrupt may occur twice. The first interrupt occurs at the beginning of the Start bit and the second after reception of the Sync field character.

Work around

If a receive interrupt occurs, check the URXDA bit (UxSTA<0>) to ensure that valid data is available. On the first interrupt, no data will be present. The second interrupt will have the Sync field character (55h) in the receive FIFO.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

14. Module: UART

With the auto-baud feature selected, the Sync field character (0x55) may be loaded into the FIFO as data.

Work around

To prevent the Sync field character from being loaded into the FIFO, load the UxBRG register with either 0x0000 or 0xFFFF prior to enabling the auto-baud feature (ABAUD = 1).

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

15. Module: UART

The auto-baud may miscalculate for certain baud rates and clock speed combinations, resulting in a BRG value that is 1 greater or less than the expected value. When UxBRG is less than 50, this can result in transmission and reception failures due to introducing error greater than 1%.

Work around

Test auto-baud calculations at various clock speed and baud rate combinations that would be used in applications. If an inaccurate UxBRG value is generated, manually correct the baud rate in user code.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

16. Module: UART

The UART module will not generate consecutive Break characters. Trying to perform a back-to-back Break character transmission will cause the UART module to transmit the dummy character used to generate the first Break character instead of transmitting the second Break character. Break characters are generated correctly if they are followed by non-Break character transmission.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

17. Module: Output Compare

In PWM mode, the output compare module may miss a compare event when the current duty cycle register (OCxRS) value is 0x0000 (0% duty cycle) and the OCxRS register is updated with a value of 0x0001. The compare event is only missed the first time a value of 0x0001 is written to OCxRS and the PWM output remains low for one PWM period. Subsequent PWM high and low times occur as expected.

Work around

If the current OCxRS register value is 0x0000, avoid writing a value of 0x0001 to OCxRS. Instead, write a value of 0x0002. In this case, however, the duty cycle will be slightly different from the desired value.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

18. Module: SPI

When using Enhanced Buffer mode, some indicator bits may be set at incorrect times:

- For slave transfers, the SRMPT bit (SPIxSTAT<7>) is set early, after only 7 SCK periods.
- For Slave Interrupt modes (SISELx = 5), there is a one SCK period delay between the interrupt event and the SPIxIF bit being set.
- There may be several instruction cycle delays between the FIFO full or FIFO empty events and the interrupt flags or indicator bits being set.

Work around

None at this time.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

19. Module: SPI

In SPI Slave mode (MSTEN = 0), with the slave select option enabled (SSEN = 1), the peripheral may accept transfers regardless of the $\overline{SSx}$ pin state. The received data in SPIxBUF will be accurate but not intended for the device.

Work around

There is a work around using the Peripheral Pin Select (PPS) feature. One of the external interrupts (INT1 or INT2) can be mapped to the same pin as the $\overline{SSx}$ signal or the $\overline{SSx}$ signal can be mapped to a pin with interrupt-on-change (CNx) functionality. If the $\overline{SSx}$ signal changes to low (active), the interrupt flag will be set.

When an SPI data received interrupt occurs, the interrupt flag can be tested. If the interrupt mapped to $\overline{SSx}$ did not occur, discard the data.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

20. Module: SPI

When using Enhanced Buffer mode, an interrupt will not occur if the following conditions exist:

- SPI Buffer Interrupt mode, SISEL<2:0> (SPIxSTAT<4:2>), is set to interrupt when the Shift register is empty (SISEL<2:0> = 101).
- Slave Select mode is enabled (SSEN = 1).

This only occurs when Enhanced mode, Slave Select mode and interrupt on Shift register empty are all enabled. In other modes, the interrupt will work correctly.

Work around

When Slave Select mode is enabled, interrupting on SPIxSR empty and TX empty will occur at the same time. Therefore, interrupting on TX FIFO empty (SISEL<2:0> = 110) can be used as an alternative to interrupting when the Shift register is empty (SISEL<2:0> = 101).

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

21. Module: I/O Ports

The I/O pin outputs, VOL and VOH, meet the specifications in Table 3 below.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

TABLE 3: DC CHARACTERISTICS: I/O PIN OUTPUT SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	**Sym**	**Characteristic**	**Min**	**Typ(1)**	**Max**	**Units**	**Conditions**
	VOL	**Output Low Voltage**					
DO10		All I/O Pins	—	—	.55	V	IOL = 8.5 mA, VDD = 3.6V
			—	—	.4	V	IOL = 7.8 mA, VDD = 3.6V
			—	—	.55	V	IOL = 6.0 mA, VDD = 2.0V
			—	—	.4	V	IOL = 5.0 mA, VDD = 2.0V
	VOH	**Output High Voltage**					
DO20		All I/O Pins	3.0	—	—	V	IOH = -3.0 mA, VDD = 3.6V
			2.4	—	—	V	IOH = -6.0 mA, VDD = 3.6V
			1.65	—	—	V	IOH = -1.0 mA, VDD = 2.0V
			1.4	—	—	V	IOH = -3.0 mA, VDD = 2.0V

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

22. Module: I/O Ports

During Power-on Reset (POR), the device may drive the OSCO/RA3 pin as a clock out output for approximately 20 μS. During this time, the pin will be driven high and low rather than being set to high-impedance. This may cause issues on designs that use the pin as a general purpose I/O.

Designs should be reviewed to ensure that their intended operation will not be disrupted if the pin is driven during POR.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

23. Module: JTAG

When entering the SHIFT_DR state while in ICSP™ Communications mode, an extra clock edge may be generated, causing JTAG and ICSP communications to lose synchronization. This prevents device programming using ICSP over JTAG. JTAG boundary scan is not affected and operates as expected.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

24. Module: RTCC

When performing writes to the ALCFGRPT register, some bits may become corrupted. The error occurs because of desynchronization between the CPU clock domain and the RTCC clock domain.

The error causes data, from the instruction *following* the ALCFGRPT instruction, to overwrite the data in ALCFGRPT.

Work around

Always follow writes to the ALCFGRPT register with an additional write of the same data to a dummy location. These writes can be performed to RAM locations, W registers or unimplemented SFR space.

The optimal way to perform the work around:

1. Read ALCFGRPT into a RAM location.
2. Modify the ALCFGRPT data, as required, in RAM.
3. Move the RAM value into ALCFGRPT, and a dummy location, in back-to-back instructions.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

25. Module: I^2C

When the I^2C module is operating in Slave mode, after the ACKSTAT bit is set when receiving a NACK from the master, it may be cleared by the reception of a Start or Stop bit.

Due to this issue, the state of ACKSTAT after a transmission finishes will vary depending on device revision. On revisions with this issue, ACKSTAT will be clear at the end of the transmission, and will remain clear until the next NACK is received from the Master. On revisions without the issue, ACKSTAT will be set at the end of a transmission and will remain set until receiving an ACK from the Master.

Work around

Store the value of the ACKSTAT bit immediately after receiving a NACK from the master.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

26. Module: I²C

Bit and byte-based operations may not have the intended affect on the I2CxSTAT register. It is possible for bit and byte operations performed on the lower byte of I2CxSTAT to clear the BCL bit (I2CxSTAT<10>). Bit and byte operation performed on the upper byte of I2CxSTAT, or on the BCL bit directly, may not be able to clear the BCL bit.

Work around

Modifications to the I2CxSTAT register should be done using word writes only. This can be done in 'C' by always writing to the register itself and not the individual bits. For example, the code, `I2C1STAT &= 0xFBFF`, will force the compiler to use a word-based operation to clear the BCL bit. In assembly, it is done by not using `BSET` or `BCLR` instructions, or instructions with the `.b` modifier.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

27. Module: UART

When the UART is configured for IR interface operations (UxMODE<9:8> = 11), the 16x baud clock signal on the BCLK pin will only be present when the module is transmitting. The pin will be Idle at all other times.

Work around

Configure one of the output compare modules to generate the required baud clock signal when the UART is receiving data or in an Idle state.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

28. Module: I/O (Peripheral Pin Select)

The remappable pin functions multiplexed to some pins do not have a higher priority than fixed digital signals assigned to those pins. By design, a remapped digital function should always have priority over any other fixed digital function on the same pin.

Using these remappable and specific fixed digital functions at the same time may cause conflicts and unexpected results on:

- RP12 and PMD0
- RP18 and PMA2 (40-pin and 44-pin devices only)

No other fixed digital functions are affected.

Work around

On the affected pins, enable either the remappable peripherals, or the specific fixed digital peripherals, but not both at the same time.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

29. Module: UART (UERIF Interrupt)

The UART error interrupt may not occur, or occur at an incorrect time, if multiple errors occur during a short period of time.

Work around

Read the error flags in the UxSTA register whenever a byte is received to verify the error status. In most cases, these bits will be correct, even if the UART error interrupt fails to occur. For possible exceptions, refer to Errata # 30.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

30. Module: UART (FIFO Error Flags)

Under certain circumstances, the PERR and FERR error bits may not be correct for all bytes in the receive FIFO. This has only been observed when both of the following conditions are met:

- the UART receive interrupt is set to occur when the FIFO is full or 3/4 full (UxSTA<7:6> = 1x), and
- more than 2 bytes with an error are received.

In these cases, only the first two bytes, with a parity or framing error, will have the corresponding bits indicate correctly. The error bits will not be set after this.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

31. Module: Core (BOR)

When the on-chip regulator is enabled (DISVREG tied to VSS), a BOR event may spontaneously occur under the following circumstances:

- VDD is less than 2.5V, and
- the internal band gap reference is being used as a reference with the A/D converter (AD1PCFG<15> = 0)

Work around

Do not select the internal band gap as a reference for the A/D converter when the on-chip regulator is in Tracking mode (LVDIF (IFS4<8>) = 1).

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

32. Module: Core (Instruction Set)

If an instruction producing a read-after-write stall condition is executed inside a REPEAT loop, the instruction will be executed fewer times than was intended. For example, this loop:

```
repeat #0xf
inc [w1],[++w1]
```

will execute less than 16 times.

Work around

Avoid using REPEAT to repetitively execute instructions that create a stall condition. Instead, use a software loop using conditional branches.

The MPLAB® C Compiler will not generate REPEAT loops that cause this erratum.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

33. Module: Memory (Program Space Visibility)

When accessing data in the PSV area of data RAM, it is possible to generate a false address error trap condition by reading data located precisely at the lower address boundary (8000h). If data is read using an instruction with an auto-decrement, the resulting RAM address will be below the PSV boundary (i.e., at 7FFEh); this will result in an address error trap.

This false address error can also occur if a 32-bit MOV instruction is used to read the data at location, 8000h.

Work around

Do not use the first location of the a PSV page (address 8000h).

The MPLAB C Compiler (v3.11 or later) supports the option, `-merrata=psv_trap`, to prevent it from generating code that would cause this erratum.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X					

34. Module: RTCC

Under certain circumstances, the value of the Alarm Repeat Counter (ALCFGRPT<7:0>) may be unexpectedly decremented. This happens only when a byte write to the upper byte of ALCFGRPT is performed in the interval between a device POR/BOR and the first edge from the RTCC clock source.

Work around

Do not perform byte writes on ALCFGRPT, particularly the upper byte.

Alternatively, wait until one period of the SOSC has completed before performing byte writes to ALCFGRPT.

Affected Silicon Revisions

A3/A4	B4	B5	B8				
X	X	X					

35. Module: SPI (Master Mode)

In Master mode, the SPI Interrupt Flag (SPIxIF) and the SPIRBF bit (SPIxSTAT<0>) may both become set one-half clock cycle early, instead of on the clock edge. This occurs only under the following circumstances:

- Enhanced Buffer mode is disabled (SPIBEN = 0); and
- the module is configured for serial data output changes on transition from clock active to clock Idle state (CKE = 1).

If the application is using the interrupt flag to determine when data to be transmitted is written to the transmit buffer, the data currently in the buffer may be overwritten.

Work around

Before writing to the SPI buffer, check the SCK pin to determine if the last clock edge has passed. Example 1 (below) demonstrates a method for doing this. In this example, the RD1 pin functions as the SPI clock, SCK, which is configured as Idle low.

Affected Silicon Revisions

A3/A4	B4	B5	B8				
X							

36. Module: I²C (Master Mode)

Under certain circumstances, a module operating in Master mode may Acknowledge its own command addressed to a slave device. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- the I²C master has the same two upper address bits (I2CADD<9:8>) as the addressed slave module.

In these cases, the master also Acknowledges the address command and generates an erroneous I²C slave interrupt, as well as the I²C master interrupt.

Work around

Several options are available:

- When using 10-Bit Addressing mode, make certain that the master and slave devices do not share the same 2 MSbs of their addresses.

If this cannot be avoided:

- Clear the A10M bit (I2CxCON<10> = 0) prior to performing a Master mode transmit.
- Read the ADD10 bit (I2CxSTAT<8>) to check for a full 10-bit match whenever a slave I²C interrupt occurs on the master module.

Affected Silicon Revisions

A3/A4	B4	B5	B8				
X	X	X	X				

EXAMPLE 1: CHECKING THE STATE OF SPIxIF AGAINST THE SPI CLOCK

```
while(IFS0bits.SPI1IF == 0){}     //wait for the transmission to complete
while(PORTDbits.RD1 == 1){}       //wait for the last clock to finish
SPI1BUF = 0xFF;                   //write new data to the buffer
```

37. Module: I²C (Slave Mode)

Under certain circumstances, a module operating in Slave mode may not respond correctly to some of the special addresses reserved by the I²C protocol. This happens when the following occurs:

- 10-Bit Addressing mode is used (A10M = 1); and
- bits, A<7:1>, of the slave address (I2CADD<7:1>) fall into the range of the reserved 7-bit address ranges: '1111xxx' or '0000xxx'.

In these cases, the Slave module Acknowledges the command and triggers an I²C slave interrupt; it does *not* copy the data into the I2CxRCV register or set the RBF bit.

Work around

Do not set bits, A<7:1>, of the module's slave address equal to '1111xxx' or '0000xxx'.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

38. Module: I²C

The Transmit Buffer Full flag, TBF (I2CxSTAT<0>), may not be cleared by hardware if a collision on the I²C bus occurs before the first falling clock edge during a transmission.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

39. Module: UART

When the UART is operating using two Stop bits (STSEL = 1), it may sample the first Stop bit instead of the second one. If the device being communicated with is one using one Stop bit in its communications, this may lead to framing errors.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

40. Module: Oscillator (SOSC)

The low-power secondary oscillator option, selected by the SOSCSEL Configuration bits (CW2<12:11>), is not available in this silicon revision. The oscillator in all devices functions in the Default (High-Gain) mode only.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

41. Module: Voltage Regulator

The Standby mode wake-up option, selected by the WUTSEL Configuration bits (CW2<14:13>), is not available in this silicon revision. All devices use the default regulator wake-up time of 190 μs.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

42. Module: Core (Code Protection)

When General Segment Code Protection has been enabled (GCP Configuration bit is programmed), applications are unable to write to the first 512 bytes of the program memory space (0000h through 0200h). In applications that may require the interrupt vectors to be changed during run time, such as bootloaders, modifications to the Interrupt Vector Tables (IVTs) will not be possible.

Work around

Create two new Interrupt Vector Tables, one each for the IVT and AIVT, in an area of program space beyond the affected region. Map the addresses in the old vector tables to the new tables. These new tables can then be modified as needed to the actual addresses of the ISRs.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
	X						

43. Module: SPI

SPI operating in Enhanced Buffer mode (SPIBEN = 1) may set the interrupt flag, SPIxIF, before the last bit has been transmitted from the shift register. This issue only affects one of the eight Interrupt modes, SISEL<2:0> = 101, which generates an interrupt when the last bit has shifted out of the shift register, indicating the transfer is complete. All other Interrupt modes in Enhanced Buffer mode work as described in the product data sheet.

Work around

Multiple work arounds are available. Select another Buffer Interrupt mode using the SISEL<2:0> bits in the SPIxSTAT register. A comparable mode is to generate an interrupt when the FIFO is empty, SISEL<2:0> = 110. Another option is to monitor the SRMPT bit (SPIxSTAT<7>) to determine when the shift register is empty.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

44. Module: UART (IrDA®)

When IrDA reception is enabled (UxMODE<12> = 1), the operation of the RXINV bit (UxMODE<4>) is the opposite of its description in the device data sheet (DS39881); that is, setting the bit configures the module for a logic high Idle state, and clearing the bit configures the module for a logic low Idle state. Using the bit as described in the data sheet may result in reception errors.

Work around

Invert the state of the RXINV bit. If the Idle state of the received signal is logic high, set RXINV = 1. If the Idle state of the received signal is logic low, clear RXINV.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X							

45. Module: Core

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLKDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- Enabling or disabling Doze mode by setting or clearing the DOZEN bit.
- Before or after changing the DOZE<2:0> bits.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

46. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the module may transmit two bytes or two words of data with a value of 0h, immediately upon the microcontroller waking up from Sleep mode. At the same time, the module “receives” two words or two bytes of data, also with the value of 0h.

The transmission of null data occurs even if the Transmit Buffer registers are empty prior to the microcontroller entering Sleep mode. The received null data requires that the receive buffer be read twice to clear the “received” data.

This behavior has not been observed when the module is operating in any other mode.

Work around

When operating in Enhanced Buffer Master mode, disable the module (SPIEN = 0) before entering Sleep mode.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

47. Module: SPI (Master Mode)

When operating in Enhanced Buffer Master mode, the Transmit Buffer Full flag, SPITBF, may be cleared before all data in the FIFO buffer has actually been sent. This may result in data being overwritten before it can be sent.

This has only been observed when the SPI clock prescalers are configured for a divider of greater than 1:4.

This behavior has not been observed when the module is operating in any other mode.

Work around

Several options are available:

- If possible, use a total clock prescale factor of 1:4 or less.
- Do not use SPITBF to indicate when new data can be written to the buffer. Instead, use the SPIRBF or SPIBEC flags to track the number of bytes actually transmitted.
- If the SPITBF flag must be used, always wait at least one-half SPI clock cycle before writing to the transmit buffer.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
	X	X	X				

48. Module: SPI (Framed SPI Modes)

Framed SPI modes as described in the device data sheet are not supported. When using the module, verify the FRMEN bit (SPIxCON2<15>) is cleared.

All other SPI modes function as described.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

49. Module: Core (Data SRAM)

During any operations to data SRAM (addresses above the SFR space, starting at 0800h), the device's baseline current consumption (I_{DD}) may periodically be higher than previously specified in the data sheet. This occurs only with oscillator speeds of 1 MHz or slower, regardless of the clock mode.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
	X	X					

50. Module: I/O (PORTA and PORTB)

PORTA pin, RA0, may not operate correctly as an input when the open-drain output is enabled for PORTB pin, RB0 (ODCB<0>). RA0 will operate correctly as an output.

Work around

None.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

51. Module: A/D Converter

Once the A/D module is enabled (AD1CON1<15> = 1), it may continue to draw extra current even if the module is later disabled (AD1CON1<15> = 0).

Work around

In addition to disabling the module through the ADON bit, set the corresponding PMD bit (ADC1MD, PMD1<0>) to power it down completely.

Disabling the A/D module through the PMD register also disables the AD1PCFG registers, which in turn, affects the state of any port pins with analog inputs. Users should consider the effect on I/O ports and other digital peripherals on those ports when ADC1MD is used for power conservation.

Affected Silicon Revisions

A3/ A4	B4	B5	B8				
X	X	X	X				

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS39881**D**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Guidelines for Getting Started with 16-Bit Microcontrollers

Section 2.4 Voltage Regulator Pins (ENVREG/ DISVREG and VCAP/VDDCORE) has been replaced with a new and more detailed section. The entire text follows:

2.4 Voltage Regulator Pins (ENVREG/ DISVREG and VCAP/VDDCORE)

Note:	This section applies only to PIC24FJ devices with an on-chip voltage regulator.

The on-chip voltage regulator enable/disable pin (ENVREG or DISVREG, depending on the device family) must always be connected directly to either a supply voltage or to ground. The particular connection is determined by whether or not the regulator is to be used:

- For ENVREG, tie to VDD to enable the regulator, or to ground to disable the regulator
- For DISVREG, tie to ground to enable the regulator or to VDD to disable the regulator

Refer to **Section 24.2 “On-Chip Voltage Regulator”** for details on connecting and using the on-chip regulator.

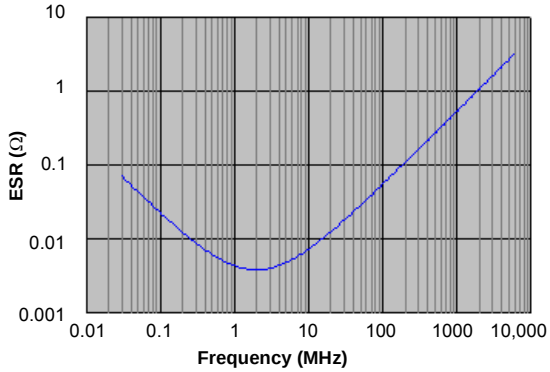
When the regulator is enabled, a low-ESR (< 5Ω) capacitor is required on the VCAP/VDDCORE pin to stabilize the voltage regulator output voltage. The VCAP/ VDDCORE pin must not be connected to VDD and must use a capacitor of 10 µF connected to ground. The type can be ceramic or tantalum. Suitable examples of capacitors are shown in Table 2-1. Capacitors with equivalent specifications can be used.

Designers may use Figure 2-3 to evaluate ESR equivalence of candidate devices.

The placement of this capacitor should be close to VCAP/VDDCORE. It is recommended that the trace length not exceed 0.25 inch (6 mm). Refer to **Section 27.0 “Electrical Characteristics”** for additional information.

When the regulator is disabled, the VCAP/VDDCORE pin must be tied to a voltage supply at the VDDCORE level. Refer to **Section 27.0 “Electrical Characteristics”** for information on VDD and VDDCORE.

FIGURE 2-3 FREQUENCY vs. ESR PERFORMANCE FOR SUGGESTED VCAP



Note: Typical data measurement at 25°C, 0V DC bias.

TABLE 2-1 SUITABLE CAPACITOR EQUIVALENTS

Make	Part #	Nominal Capacitance	Base Tolerance	Rated Voltage	Temp. Range
TDK	C3216X7R1C106K	10 µF	±10%	16V	-55 to 125ºC
TDK	C3216X5R1C106K	10 µF	±10%	16V	-55 to 85ºC
Panasonic	ECJ-3YX1C106K	10 µF	±10%	16V	-55 to 125ºC
Panasonic	ECJ-4YB1C106K	10 µF	±10%	16V	-55 to 85ºC
Murata	GRM32DR71C106KA01L	10 µF	±10%	16V	-55 to 125ºC
Murata	GRM31CR61C106KC31L	10 µF	±10%	16V	-55 to 85ºC

2.4.1 CONSIDERATIONS FOR CERAMIC CAPACITORS

In recent years, large value, low-voltage, surface mount ceramic capacitors have become very cost effective in sizes up to a few tens of microfarad. The low-ESR, small physical size and other properties make ceramic capacitors very attractive in many types of applications.

Ceramic capacitors are suitable for use with the internal voltage regulator of this microcontroller. However, some care is needed in selecting the capacitor to ensure that it maintains sufficient capacitance over the intended operating range of the application.

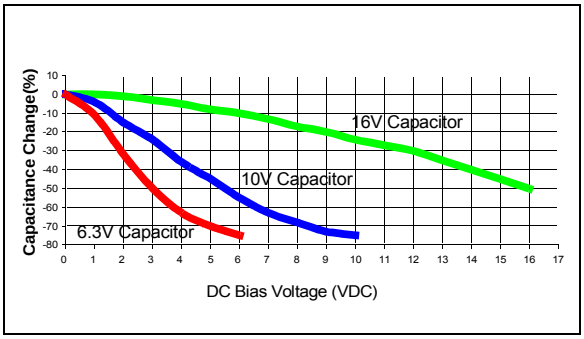
Typical low-cost 10 µF ceramic capacitors are available in X5R, X7R and Y5V dielectric ratings (other types are also available, but are less common). The initial tolerance specifications for these types of capacitors are often specified as ±10% to ±20% (X5R and X7R), or -20%/+80% (Y5V). However, the effective capacitance that these capacitors provide in an application circuit will also vary based on additional factors, such as the applied DC bias voltage and the temperature. The total in-circuit tolerance is, therefore, much wider than the initial tolerance specification.

The X5R and X7R capacitors typically exhibit satisfactory temperature stability (ex: ±15% over a wide temperature range, but consult the manufacturer's data sheets for exact specifications). However, Y5V capacitors typically have extreme temperature tolerance specifications of +22%/-82%. Due to the extreme temperature tolerance, a 10 µF nominal rated Y5V type capacitor may not deliver enough total capacitance to meet minimum internal voltage regulator stability and transient response requirements. Therefore, Y5V capacitors are not recommended for use with the internal voltage regulator if the application must operate over a wide temperature range.

In addition to temperature tolerance, the effective capacitance of large value ceramic capacitors can vary substantially, based on the amount of DC voltage applied to the capacitor. This effect can be very significant, but is often overlooked or is not always documented.

A typical DC bias voltage vs. capacitance graph for 16V, 10V and 6.3V rated capacitors is shown in Figure 2-4.

FIGURE 2-4 DC BIAS VOLTAGE vs. CAPACITANCE CHARACTERISTICS



When selecting a ceramic capacitor to be used with the internal voltage regulator, it is suggested to select a high-voltage rating, so that the operating voltage is a small percentage of the maximum rated capacitor voltage. For example, choose a ceramic capacitor rated at 16V for the 2.5V core voltage. Suggested capacitors are shown in Table 2-1.

2. Module: Electrical Characteristics

Changes, shown in bold, have been made to the DC10 and DC18 rows in Table 27-3. The updated table is shown below:

TABLE 27-3 DC CHARACTERISTICS: TEMPERATURE AND VOLTAGE SPECIFICATIONS

DC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C < TA < +85°C for Industrial -40°C < TA £ +125°C for Extended				
Param No.	Symbol	Characteristic	Min	Typ(1)	Max	Units	Conditions
Operating Voltage							
DC10	Supply Voltage						
	VDD		**VBORMIN**	—	3.6	V	Regulator enabled
	VDD		VDDCORE	—	3.6	V	Regulator disabled
	VDDCORE		**2.0**	—	2.75	V	Regulator disabled
DC12	VDR	RAM Data Retention Voltage(2)	1.5	—	—	V	
DC16	VPOR	VDD Start Voltage to Ensure Internal Power-on Reset Signal	VSS	—	—	V	
DC17	SVDD	VDD Rise Rate to Ensure Internal Power-on Reset Signal	0.05	—	—	V/ms	0-3.3V in 0.1s 0-2.5V in 60 ms
DC18	VBOR	Brown-out Reset Voltage	**1.96**	**2.10**	**2.2**	V	16 MHz (8 MIPS) operation is supported until BOR is active

Note 1: Data in “Typ” column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: This is the limit to which VDD can be lowered without losing RAM data.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (5/2009)

Initial release of this document; issued for silicon revision

B5. Incorporates the following current and historical silicon issues from revision A3 and B4:

- 1 (JTAG)
- 2 (Low-Voltage Detect)
- 3-6 (Core)
- 7-9 (A/D)
- 10 (I^2C – I2C1 and SDA Line State)
- 11-16 (UART)
- 17 (Output Compare)
- 18-20 (SPI)
- 21-22 (I/O Ports)
- 23 (JTAG)
- 24 (RTCC)
- 25-26 (I^2C)
- 27 (UART)
- 28 (I/O – Peripheral Pin Select)
- 29 (UART – UERIF Interrupt)
- 30 (UART – FIFO Error Flags)
- 31 (Core – BOR)
- 32 (Core – Instruction Set)
- 33 (Memory – Program Space Visibility)
- 34 (RTCC)
- 35 (SPI – Master Mode)
- 36 (I^2C – Master Mode)
- 37 (I^2C – Slave Mode)
- 38 (I^2C)
- 39 (UART)
- 40 (Oscillator – SOSC)
- 41 (Voltage Regulator)
- 42 (Core – Code Protection)
- 43 (SPI)
- 44 (Core)

For data sheet clarifications:

Includes Data Sheet Clarifications 1 (Electrical Characteristics), 2 (10-Bit High-Speed A/D Converter), 3 (I/O Ports), 4 (Oscillator Configuration), 5-6 (Special Features) and 7-9 (Electrical Characteristics).

This document replaces these errata documents:

- *"PIC24FJ64GA004 Family Revision A3 Silicon Errata"* (DS80316)
- *"PIC24FJ64GA004 Family Revision B4 Silicon Errata"* (DS80384)
- *"PIC24FJ64GA004 Family Data Sheet Errata"* (DS80333)

Rev B Document (7/2009)

Amended existing silicon revision A3 as joint revision A3/A4.

Added silicon issue 45 (UART) to silicon revision A3/A4.

Added silicon revision B5; includes existing issues 16 (UART), 29 (UART – UERIF Interrupt), 30 (UART – FIFO Error Flags), 30 (Core), 33 (Memory – Program Space Visibility), 34 (RTCC), 36 (I^2C – Master Mode), 37 (I^2C – Slave Mode), 39 (UART), 43 (SPI) and 44 (Core). No new silicon issues added for this revision.

Revised issue 25 (I^2C) with additional information, differentiating erroneous bit behavior from misinterpretation of the bit state.

Added data sheet clarification 10 (I^2C).

Rev C Document (2/2010)

Removed existing issue 44 (Core) entirely; issue 45 (UART – IrDA) now renumbered as issue 44.

Added new issues 45 (Core), 46 and 47 (SPI – Master Mode), 48 (SPI – Framed SPI Modes), 49 (Core – Data SRAM) and 50 (I/O – PORTA and PORTB) to various existing silicon revisions.

Added silicon revision B8; includes newly added and existing issues 16 (UART), 29 (UART – UERIF Interrupt), 30 (UART – FIFO Error Flags), 31 (Core – BOR), 33 (Memory – Program Space Visibility), 34 (RTCC), 36 (I^2C – Master Mode), 37 (I^2C – Slave Mode), 39 (UART), 43 (SPI), 45 (Core), 46 through 47 (SPI – Master Mode), 48 (SPI – Framed SPI Modes) and 50 (I/O – PORTA and PORTB).

Removed all data sheet clarifications as they are addressed in the new revision of the data sheet.

Amended revision history to include the addition of silicon revision B5 to this document.

Rev D Document (3/2010)

Updated silicon issue 50 (I/O – PORTA and PORTB) by removing PORTB issues not relevant to this device family.

Added data sheet clarification 1 (Electrical Specifications – DC Characteristics) to revision D of the data sheet.

Rev E Document (9/2010)

Added silicon issue 51 (A/D Converter), added data sheet clarification issues 1 (Guidelines For Getting Started with 16-Bit Microcontrollers) and 2 (Electrical Characteristics). Removed Table 27-10 because Table 27-3, a newer version, has been added.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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Printed on recycled paper.

ISBN: 978-1-60932-561-9

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08/04/10