PIC24F16KA102 Family Silicon Errata and Data Sheet Clarification

The PIC24F16KA102 family devices that you have received conform functionally to the current Device Data Sheet (DS39927**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC24F16KA102 family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**B0**).

Data Sheet clarifications and corrections start on page 7, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with MPLAB ICD 2 or PICkit™ 3:

1. Using the appropriate interface, connect the device to the MPLAB ICD 2 programmer/debugger or PICkit™ 3.
2. From the main menu in MPLAB IDE, select *Configure>Select Device* and then select the target part number in the dialog box.
3. Select the MPLAB hardware tool (*Debugger>Select Tool*).
4. Perform a "Connect" operation to the device (*Debugger>Connect*). Depending on the development tool used, the part number *and* Device Revision ID value appear in the Output window.

Note: If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC24F16KA102 family silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)			
		A5	A6	A7	B0
PIC24F08KA101	0B08h	05h	06h	07h	08h
PIC24F08KA102	0B0Ah				
PIC24F16KA101	0B01h				
PIC24F16KA102	0B03h				

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses in program memory. They are shown in hexadecimal in the format, "DEVID DEVREV".

2: Refer to the *"PIC24FXXKAXXX Flash Programming Specification"* (DS39919) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)			
				A5	A6	A7	B0
CTMU	—	1.	Module operates in Sleep mode.	X	X	X	
Resets	BOR	2.	Inadvertent Reset when disabling/enabling BOR.	X	X	X	X
Core	ICSP™	3.	Unable to use PGC/PGD pair under certain conditions.	X			
Core	Deep Sleep	4.	Failure to avoid Deep Sleep entry.	X	X	X	
Memory	Code Protection	5.	No direct jump to Boot Sector from Reset Vector.	X			
Comparator	—	6.	Change in maximum VIOFF.	X	X	X	X
SPI	Enhanced Buffer mode	7.	Errors when polling SPITBF flag.	X	X	X	
I/O Ports	PORTA and PORTB	8.	Under certain conditions, functionality for RB0 and RA0 pins do not work correctly.	X	X	X	
I/O Ports	PORTA and PORTB	9.	Under certain conditions, functionality for RB2 does not work correctly.	X	X	X	
Core	Low-Voltage BOR	10.	LPBOR configuration results in ambiguous Resets.	X	X	X	
Comparator	I/O Pins	11.	Enabling comparator outputs disables some digital I/O ports.	X	X	X	X
Comparator	—	12.	Output polarity inversion also inverts edge-detect sensing.	X	X	X	X
Core	Doze mode	13.	Instruction execution glitches following DOZE bit changes.	X	X	X	

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the following tables apply to the current silicon revision (**B0**).

1. Module: CTMU

The CTMU and its current source may continue to operate in Sleep mode. This results in current consumption in excess of the specifications for Sleep.

Work around

Clear the CTMU Enable bit (CTMUCON<15>) prior to entering Sleep mode.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

2. Module: Resets (BOR)

A device Reset may occur if the BOR is disabled and immediately re-enabled in software (RCON<14> is cleared and then immediately set).

Work around

It is recommended that several NOP instructions be added to a BOR disable/enable sequence. Alternatively, place several instructions or a short routine between the instructions to disable and enable the BOR.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X	X				

3. Module: Core (ICSP™)

Under certain circumstances, a PGC/PGD pin pair may not function to enter ICSP Programming mode. This has been observed only when both the following conditions are met:

a) Pin, RA5, is configured as $\overline{\text{MCLR}}$ (FPOR<5> = 1), and

b) The pins of the PGEC/PGED pair were configured as digital outputs (corresponding TRIS bit cleared) in software.

In these circumstances, the pins do not switch to a high-impedance state upon entry into Programming mode, but remain configured as outputs.

Work around

Choose a PGC/PGD pair with pins that are always configured as inputs (TRIS bits are set).

Affected Silicon Revisions

A5	A6	A7	B0				
X							

4. Module: Core (Deep Sleep)

Deep Sleep wake-up sources may be ignored if they occur just prior to entry into Deep Sleep mode. As a result, the device may enter Deep Sleep mode when it should not.

Work around

If possible, configure external Deep Sleep wake-up sources to repeat themselves once. If the device does enter Deep Sleep, the second occurrence of the wake-up source will wake the device.

Alternatively, synchronize the entry into Deep Sleep with external wake-up sources, where possible.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

5. Module: Memory (Code Protection)

When any boot segment is enabled in program memory (FBS<3:1> ≠ 111), it is not possible to jump directly from the Reset vector to any address in the boot segment.

Work around

Point the Reset vector to an address in the general segment. From there, it is possible to jump into the boot segment.

Affected Silicon Revisions

A5	A6	A7	B0				
X							

6. Module: Comparator

The maximum value for the input offset voltage (specification D300, VIOFF), shown in Table 29-13 of the Device Data Sheet, has changed for this silicon revision. The new value is shown in Table 3 (changes in **bold**).

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X	X				

7. Module: SPI (Enhanced Buffer Mode)

In Enhanced Buffer mode (SPI1CON2<0> = 1), polling the SPI Transmit Buffer Full bit, SPITBF (SPI1STAT<1>), may produce erroneous results. This occurs only under two circumstances:

a) In Master mode, when the SPI divide clock is 4 or greater.

b) In Slave mode, when the SPI sample clock is slower than 1/4 of the CPU instruction time (TCY).

For Master mode, this includes all combinations of the primary prescale bits (SPI11CON1<1:0>) and secondary prescale bits (SPI1CON1<4:2>) that, when combined, create an SPI sample clock divisor with a value of four or greater.

Work around

Instead of polling the SPITBF bit to test for an empty buffer (SPI1STAT<1> = 0), implement a SPI receive interrupt handler in software and add to the SPI transmit buffer in this routine.

Alternatively, poll the SPI Receive Full bit, SPIRBF (SPI1STAT<0>), or the Shift Register Empty bit, SRMPT (SPI1STAT<7>), to determine when to service the SPI transmit and transmit buffers.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

TABLE 3: COMPARATOR DC SPECIFICATIONS (PARTIAL)

Param No.	Symbol	Characteristics	Min	Typ	Max	Units	Comments
	VIOFF	Input Offset Voltage	—	20	**60**	mV	

8. Module: I/O Ports (PORTA and PORTB)

The functions associated with port pins, RB0 and RA0, may be interconnected in unexpected ways.

PORTB pin, RB0, may not operate correctly as an input if the SPI module is enabled (SPI1CON<15> = 1). Additionally, the pull-up, pull-down and the Change Notification (CN4) functionality are disabled. RB0 does operate correctly with the SPI enabled if it is configured as an output.

PORTA pin, RA0, may not operate correctly as an input when the open-drain output is enabled for RB0 (ODCB<0>). RA0 will operate correctly as an output.

However, when the analog input on RB0 (AN2) is enabled (AD1PCFG<2> = 0) and the SPI module is enabled, RB0 will be driven as a digital output, not as a analog input.

Work around

To enable RB0 as a digital input, enable the open-drain output for RB0 (ODCB<0>) and set the latch bit (LATB<0> = 1). The Change Notification (CN4), pull-up and pull-down for this pin will function correctly as well.

This work around may cause RA0 to function incorrectly. There is no known work around for RA0 as an input and RB0 with the open-drain output enabled.

To enable RB0 as an analog input when SPI is enabled:

1. Enable the open-drain output for RB0 (ODCB<0>).
2. Set the latch bit (LATB<0> = 1).
3. Clear TRISB<0>.
4. Clear AD1PCFG<2>.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

9. Module: I/O Ports (PORTA and PORTB)

Note: This issue occurs in PIC24FXXKA101 (20-pin) devices only.

On 20-pin devices of the PIC24F16KA102 family, the functions associated with port pins, RB2 and RA2, may be interconnected in unexpected ways.

PORTB pin, RB2, may not operate correctly as a digital I/O if the analog input on PORTA pin, RA2 (AN4), is enabled (AD1PCFG<4> = 0). Both the digital port, and the U1RX functionality multiplexed to RB2, are disabled.

Although this issue is similar in form to silicon issue 8, it appears to be independent in its root cause.

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

10. Module: Core (Low-Power BOR)

When the Low-Power BOR is enabled (FPOR<6:5> = 00), BOR events may result in a device Reset in which both the BOR and POR bits are set.

This differs from the expected behavior of simply re-arming the POR circuit to ensure that a POR occurs when V_{DD} drops below the POR threshold.

Work around

None.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

11. Module: Comparator (I/O Pins)

Certain I/O pins may not function correctly as digital inputs or outputs after specific comparator outputs have been enabled with the COE bit (CMxCON<14> = 1). These are:

- RB14 (with Comparator 1)
- RA6 (with Comparator 2)

This condition may continue even after the comparator in question has been disabled, using the corresponding CON bit (CMxCON<15> = 0).

Work around

In addition to clearing the CON bit, also clear the COE bit.

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X	X				

12. Module: Comparator

When a comparator is programmed to trigger on certain edge-detect events (CMxCON<7:6> = 10 or 01), setting the CPOL bit (CMxCON<13> = 1) may cause the comparator to flag the opposite edge-detect event (e.g., a high-to-low edge instead of the programmed low-to-high).

Work around

Leave CPOL = 0. In addition, use the opposite setting of CMxCON<7:6> to achieve the correct response (e.g., use '10' for '01').

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X	X				

13. Module: Core (Doze Mode)

Operations that immediately follow any manipulations of the DOZE<2:0> or DOZEN bits (CLDIV<14:11>) may not execute properly. In particular, for instructions that operate on an SFR, data may not be read properly. Also, bits automatically cleared in hardware may not be cleared if the operation occurs during this interval.

Work around

Always insert a NOP instruction before and after either of the following:

- Enabling or disabling Doze mode by setting or clearing the DOZEN bit
- Before or after changing the DOZE<2:0> bits

Affected Silicon Revisions

A5	A6	A7	B0				
X	X	X					

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the Device Data Sheet (DS39927**B**):

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

1. Module: Memory

In Table 4-4, the CN9IE, CN9PUE and CN9PDE bits (CNEN1<9>, CNPU1<9> and CNPD1<9>, respectively) are not implemented on 20-pin devices. These bits are to be marked with the existing footnote 1 (“These bits are not implemented in 20-pin devices”).

2. Module: Electrical Specifications (AC Specifications)

In Table 29-25, the maximum Differential Nonlinearity specification for the A/D module (parameter AD22b) has changed. The new value is shown below (changes in bold).

TABLE 29-25: ADC MODULE SPECIFICATIONS

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
ADC Accuracy							
AD22b	DNL	Differential Nonlinearity	—	±1	**-1** **+1.5**	LSb	VINL = AVSS = VREFL = 0V, AVDD = VREFH = 3V

Note 1: The ADC conversion result never decreases with an increase in the input voltage and has no missing codes.

2: Measurements taken with external VREF+ and VREF- used as the ADC voltage reference.

3. Module: Electrical Specifications (DC Specifications)

In Table 29-6, the values for parameters, DC20d and DC20e (IDD for Deep Sleep), have changed. The corrected values are shown below (changes in bold).

TABLE 29-6: DC CHARACTERISTICS: OPERATING CURRENT (IDD)

DC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial			
Parameter No.	Typical(1)	Max	Units	Conditions		
IDD Current						
DC20	195	330	µA	-40°C	1.8V	0.5 MIPS, FOSC = 1 MHz
DS20a		330		+25°C		
DC20b		330		+60°C		
DC20c		330		+85°C		
DC20d	365	**590**	µA	-40°C	3.3V	
DC20e		**590**		+25°C		
DC20f		645		+60°C		
DC20g		720		+85°C		

Note 1: Data in "Typical" column is at 3.3V, 25°C unless otherwise stated. Parameters are for design guidance only and are not tested.

2: Operating Parameters:
- EC mode with clock input driven with a square wave rail-to-rail
- I/O configured as outputs driven low
- $\overline{MCLR}$ – VDD
- WDT FSCM disabled
- SRAM, program and data memory active
- All PMD bits set except for modules being measured

4. Module: Electrical Specifications (DC Specifications)

In Table 29-8, the typical values for the Watch-dog Timer Current at 1.8V and all temperatures (parameters D61 through D61C) are changed to 0.55 µA.

5. Module: Electrical Specifications (DC Specifications)

In Table 29-8, footnote 2 includes the text: "All I/Os are configured as inputs and pulled high….". This is changed to read as, "All I/Os are configured as outputs and set low….".

6. Module: A/D

In Register 22-3, the values shown for AD1CON3<5:0> (ADCS<5:0>) are incorrect. The corrected values are shown below (changes in bold).

REGISTER 22-3: AD1CON3: A/D CONTROL REGISTER 3

R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADRC	—	—	SAMC4	SAMC3	SAMC2	SAMC1	SAMC0
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	ADCS5	ADCS4	ADCS3	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 5-0 ADCS<5:0>: A/D Conversion Clock Select bits

111111 = 64 • TCY
111110 = 63 • TCY
.
.
.
000001 = 2 • TCY
000000 = TCY

7. Module: Comparators

The descriptions given for the CMIDL bit (CMSTAT<15>) are incorrect. The correct descriptions are shown below (changes in bold).

REGISTER 23-2: CMSTAT: COMPARATOR MODULE STATUS REGISTER

R/W-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
CMIDL	—	—	—	—	—	C2EVT	C1EVT
bit 15							bit 8

U-0	U-0	U-0	U-0	U-0	U-0	R-0, HSC	R-0, HSC
—	—	—	—	—	—	C2OUT	C1OUT
bit 7							bit 0

Legend:	HSC = Hardware Settable/Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **CMIDL: Stop in Idle Mode bit**

1 = Disable comparator interrupts when the device enters Idle mode; the module is still enabled
0 = Continue normal module operation in Idle mode

8. Module: Pin Diagrams

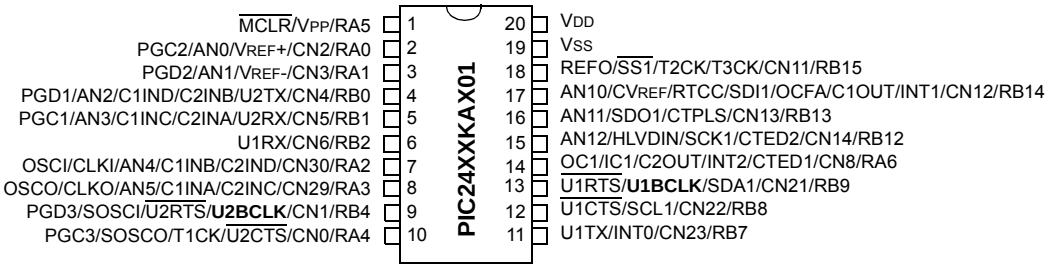
In many places in the data sheet, the UART Baud Clock output functions, U1BCLK and U2BCLK, are shown as being multiplexed on the same pins as the UART Receive input functions (U1RX and U2RX). The Baud Clock is actually multiplexed with the UART Ready-to-Send output function ($\overline{U1RTS}$ and $\overline{U2RTS}$) on completely different pins. This mapping is correctly described in the UART chapter, but incorrectly shown on pin diagrams and pin function listings.

The pin diagrams from the data sheet are replaced by the pin diagrams shown in Figure 1, Figure 2 and Figure 3. Changes are noted in bold. Footnotes present in the original diagrams have been omitted here for clarity.

In addition, Table 1-2 of the device data sheet is amended as shown. Footnotes in the original table have been omitted for clarity. Changes are indicated in bold.

FIGURE 1: PIN DIAGRAMS

20-Pin PDIP, SSOP, SOIC



28-Pin SPDIP, SSOP, SOIC

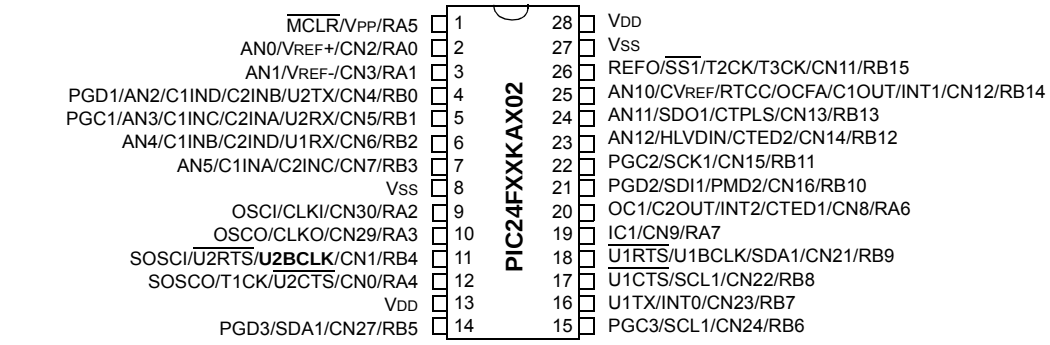


FIGURE 2: PIN DIAGRAMS (CONTINUED)

20-Pin QFN

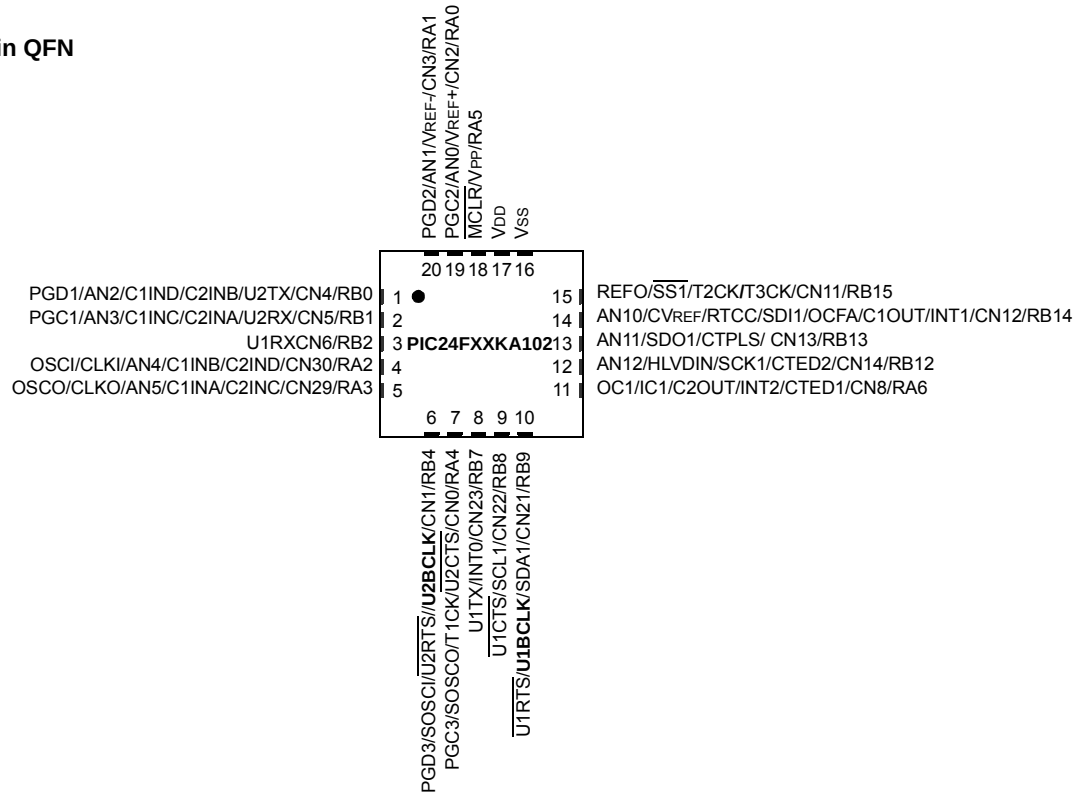


FIGURE 3: PIN DIAGRAMS (CONTINUED)

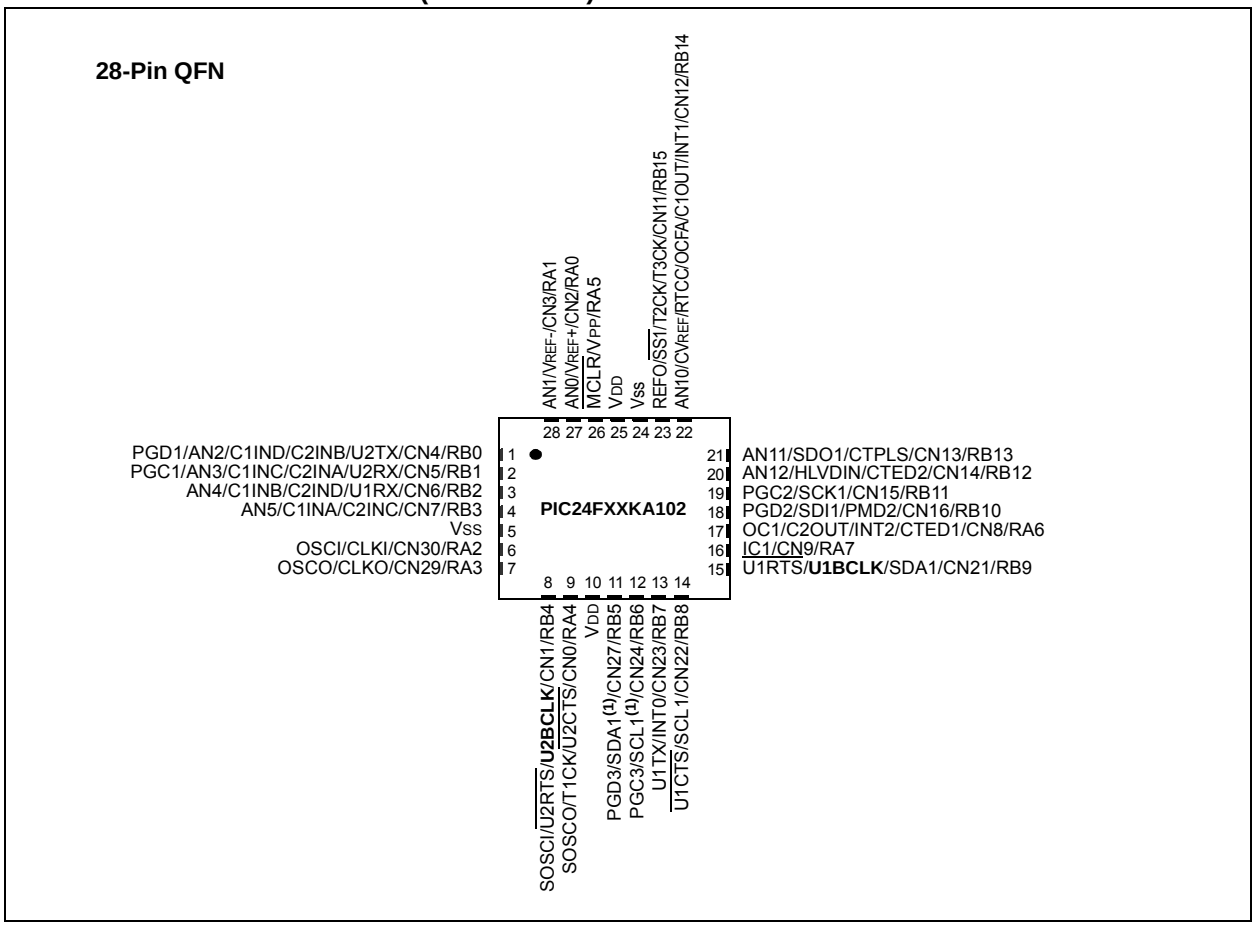


TABLE 1-2: PIC24F16KA102 FAMILY PINOUT DESCRIPTIONS (PARTIAL REPRESENTATION)

Function	Pin Number				I/O	Input Buffer	Description
	20-Pin PDIP/SSOP/ SOIC	20-Pin QFN	28-Pin SPDIP/ SSOP/SOIC	28-Pin QFN			
AN0	2	19	2	27	I	ANA	A/D Analog Inputs
AN1	3	20	3	28	I	ANA	
AN2	4	1	4	1	I	ANA	
AN3	5	2	5	2	I	ANA	
AN4	7	4	6	3	I	ANA	
AN5	8	5	7	4	I	ANA	
AN10	17	14	25	22	I	ANA	
AN11	16	13	24	21	I	ANA	
AN12	15	12	23	20	I	ANA	
U1BCLK	**13**	**10**	**18**	**15**	O	—	UART1 IrDA® Baud Clock
U2BCLK	**9**	**6**	**11**	**8**	O	—	UART2 IrDA Baud Clock

9. Module: A/D Converter (AD1CHS Register)

In Register 22-4, the bit fields, CHOSB<3:0> and CHOSA<3:0>, both assign the value '0110' to both AVDD and AVSS inputs. For both bit fields, '0111' corresponds to AVDD and '0110' corresponds to AVSS.

Also, the bit fields, CHOSB<3:0> and CHOSA<3:0>, both assign the value, '0010', to both AN2 and AN3 inputs. For both bit fields, '0011' corresponds to AN3 and '0110' corresponds to AN2.

In addition, the CH0SA bit field is only four bits wide, comprising AD1CHS<3:0>; CH0SA4 is not implemented. This deletion applies to all occurrences of CH0SA4, including the device memory map.

All changes to AD1CHS are shown in Register 22-4 below; changes are in bold.

-

REGISTER 22-4: AD1CHS: A/D INPUT SELECT REGISTER (PARTIAL REPRESENTATION)

R/W-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
CH0NB	—	—	—	CH0SB3	CH0SB2	CH0SB1	CH0SB0
bit 15							bit 8

R/W-0	U-0	U-0	**U-0**	R/W-0	R/W-0	R/W-0	R/W-0
CH0NA	—	—	**—**	CH0SA3	CH0SA2	CH0SA1	CH0SA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 11-8 CH0SB<3:0>: Channel 0 Positive Input Select for MUX B Multiplexer Setting bits

1111 = Channel 0 positive input is band gap reference (VBG)
.
.
1000 = Reserved
0111 = AVDD
0110 = AVSS
.
.
0100 = Channel 0 positive input is AN4
0011 = Channel 0 positive input is AN3
0010 = Channel 0 positive input is AN2

bit 4-0 CH0SA<4:0>: Channel 0 Positive Input Select for Sample A bits

1111 = Channel 0 positive input is band gap reference (VBG)
.
.
1000 = Reserved
0111 = AVDD
0110 = AVSS
.
.
0100 = Channel 0 positive input is AN4
0011 = Channel 0 positive input is AN3
0010 = Channel 0 positive input is AN2

10. Module: A/D Converter

In Figure 22-2, the interconnect resistance, RIC, is shown as having a value of no more than 250W. The proper value for RIC is no more than 250 **ohms**.

11. Module: Special Features (Configuration Bits)

In the FDS Configuration register, the Configuration bits, DSLPBOR and DSWCKSEL (FDS<6,4>), have been renamed: DSBOREN and DSWDTOSC. This has been done to unify the naming conventions for all nanoWatt XLP devices. The changes apply to all occurrences throughout the device data sheet.

It is anticipated that the former names of these bits will be supported through the next release of all Microchip development tools.

12. Module: Power-Saving Features

The Deep Sleep Wake-up Source register, DSWSRC (Register 10-2), has been renamed DSWAKE. This has been done to unify the naming conventions for all nanoWatt XLP devices. This change applies to all occurrences throughout the device data sheet, including the device memory map.

It is anticipated that the register name, DSWSRC, will be supported through the next release of all Microchip development tools.

13. Module: Electrical Specifications (AC Specifications)

Parameter, AD08 (current specification for the external ADC voltage reference), has been added to the specifications for the A/D module. Table 29-25 is amended as shown (additions in **bold**).

14. Module: Electrical Specifications (DC Specifications)

In Table 29-9 (“DC Characteristics: I/O Pin Input Specifications”), the maximum value of Parameter D151, the input leakage current (IIL) on the VREF+ and VREF- pins has been changed to +1.00 µA. The rest of the parameter is unchanged.

TABLE 29-25: ADC MODULE SPECIFICATIONS (PARTIAL REPRESENTATION)

AC CHARACTERISTICS			Standard Operating Conditions: 1.8V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial				
Param No.	Symbol	Characteristic	Min.	Typ	Max.	Units	Conditions
Reference Inputs							
AD05	VREFH	Reference Voltage High	AVSS + 1.7	—	AVDD	V	
AD06	VREFL	Reference Voltage Low	AVSS	—	AVDD – 1.7	V	
AD07	VREF	Absolute Reference Voltage	AVSS – 0.3	—	AVDD + 0.3	V	
AD08	**IVREF+**	**External VREF+ Current**	**—**	**200**	**—**	**µA**	**VREF+ = 3.3V; sampling**
			—	**1.0**	**—**	**mA**	**VREF+ = 3.3V; converting**

15. Module: Electrical Specifications (DC Specification)

Table 29-5 (“BOR Trip Points”) has changed to reflect the functionality of the LPBOR trip point (BORV<1:0> = 00), and to make other typographic corrections. The minimum and maximum values for the BOR trip points in Table 29-5 have changed. The new version of the table is shown below (changes in **bold**).

TABLE 29-5: BOR TRIP POINTS

Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for industrial								
Param No.	Sym	Characteristic		Min	Typ	Max	Units	Conditions
DC19		BOR Voltage on VDD Transition	BOR**V** = 00	—	—	—	—	**Note (1)**
			BOR**V** = 01	2.92	3	3.25	V	
			BOR**V** = 10	2.63	2.7	2.92	V	
			BOR**V** = 11	1.75	1.82	2.01	V	

Note 1: LPBOR re-arms the POR circuit, but does not cause a BOR.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (6/2009)

Initial release of this document; issued for revision A5. Includes silicon issues 1 (CTMU), 2 (Resets – BOR), 3 (Core – ICSP), 4 (Core – Deep Sleep), 5 (Memory – Code Protection), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode). Includes data sheet clarifications 1 (Memory), 2 (Electrical Specifications – AC Specifications), 3-6 (Electrical Specifications – DC Specifications), 7 (A/D) and 8 (Comparators).

Rev B Document (6/2009)

Revision issued for silicon revision A6. Existing silicon issues 1 (CTMU), 2 (Resets – BOR), 4 (Core – Deep Sleep), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode) added to revision A6. No new issues added.

Rev C Document (10/2009)

Revision issued for silicon revision A7. Existing silicon issues 1 (CTMU), 2 (Resets – BOR), 4 (Core – Deep Sleep), 6 (Comparator) and 7 (SPI – Enhanced Buffer Mode) added to revision A7. Added new silicon issue 8 (I/O Ports – PORTA and PORTB).

To revision B of the data sheet, adds data sheet clarifications 9 (Pin Diagrams), 10 (A/D Converter – AD1CHS Register), 11 (A/D Converter – AD1CHS Register), 12 (Special Features – Configuration Bits), 13 (Power-Saving Features) and 14 (Electrical Specifications – AC Specifications).

Rev D Document (10/2009)

Typographic correction: updated Table 2 with the correct associations between silicon issues and silicon revisions.

Rev E Document (4/2010)

Added new silicon issue 9 (I/O Ports – PORTA and PORTB) to all silicon revisions.

Updated existing silicon issue 8 to include additional interactions and work arounds between RA0 and RB0.

Added data sheet clarification 15 (Electrical Specifications – DC Specifications) to revision B of the data sheet.

Updated revision history to include entry for revision D.

Rev F Document (11/2010)

Revision issued for silicon revision B0. Existing silicon issues 2 (Resets – BOR) and 6 (Comparator) added to revision B0.

Amended existing silicon issue 8 (I/O Ports – PORTA and PORTB), to change “digital input” to analog input” at the end of the fourth paragraph.

Added new silicon issue 10 (Core – Low Power BOR) to silicon revisions A5, A6 and A7.

Added new silicon issues 11, 12 (Comparator) and 13 (Core – Doze Mode) to silicon revisions A5, A6 and A7.

Removed data sheet clarification 16 (Electrical Specifications – DC Specifications) to revision B of the data sheet.

Removed data sheet clarification 6 (Electrical Specifications – DC Specifications) and combined it with data sheet clarification 16 which is now data sheet clarification 15.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

Printed on recycled paper.

ISBN: 978-1-60932-646-3

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

Worldwide Sales and Service

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Cleveland
Independence, OH
Tel: 216-447-0464
Fax: 216-447-0643

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Harbour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Chongqing
Tel: 86-23-8980-9588
Fax: 86-23-8980-9500

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Nanjing
Tel: 86-25-8473-2460
Fax: 86-25-8473-2470

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7252
Fax: 86-29-8833-7256

China - Xiamen
Tel: 86-592-2388138
Fax: 86-592-2388130

China - Zhuhai
Tel: 86-756-3210040
Fax: 86-756-3210049

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-3090-4444
Fax: 91-80-3090-4123

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Daegu
Tel: 82-53-744-4301
Fax: 82-53-744-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Kuala Lumpur
Tel: 60-3-6201-9857
Fax: 60-3-6201-9859

Malaysia - Penang
Tel: 60-4-227-8870
Fax: 60-4-227-4068

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-6578-300
Fax: 886-3-6578-370

Taiwan - Kaohsiung
Tel: 886-7-213-7830
Fax: 886-7-330-9305

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

08/04/10