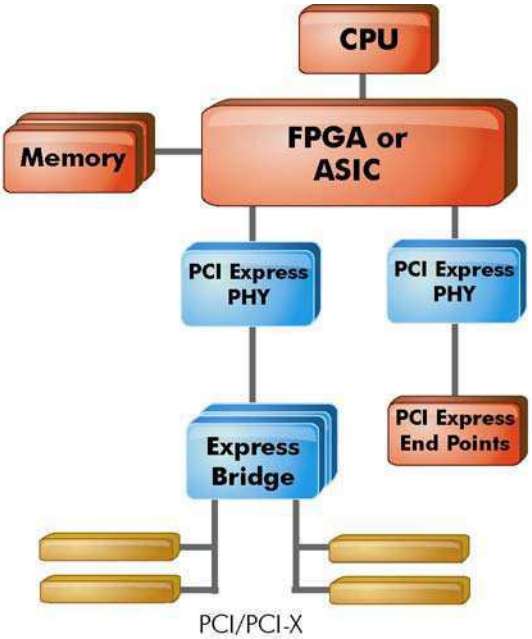
Product: PCI Express Single PHY
Part Number: PI7C9X1011

Product Description

The PI7C9X1011 is a single-lane PCI Express electrical PHYsical (PHY) layer chip, which operates at a high speed of 2.5 Gbps for serial link transmissions and operates at 250MHz or 125MHz for parallel interfaces. This low-power consuming single PHY device integrates all the circuitry required to implement the physical portion of a PCI Express link, including the PLL, Serializer/Deserializer (SerDes), receiver detection, beacon transmitter/detector, 8b/10b encoding/decoding, framer, elastic buffer and parallel data/control interface. To facilitate the access to the PHY by the Media Access Control (MAC) layer devices, an Intel-based PHY interface for PCI Express architecture v1.0 (PIPE) is employed for parallel data/control signals at the boundary of PHY/MAC. The parallel interface is an 8-bit or 16-bit PIPE bus operating at 250MHz or 125MHz through a strapped pin selection. Two additional clock signals for transmit and receive respectively are added to synchronize with the PIPE data and control signals in order to increase the timing margin of setup and hold times. To achieve the purpose of low voltage swing, low power, and low noise, the PIPE signals adopt the SSTL2 (8-bit or 16-bit PIPE) I/O standard, which is available among most high-speed devices including FPGA products.

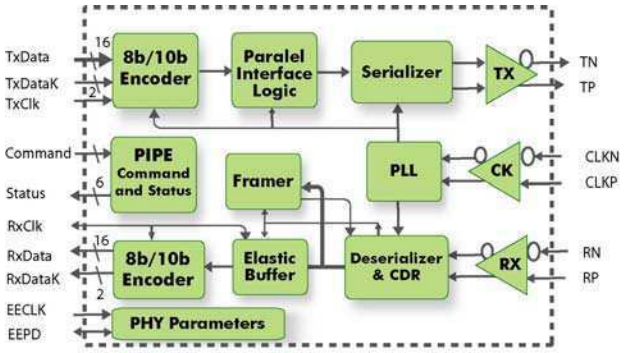
Application Example



Product Features

- Operates at full-duplex 2.5Gbps data rate for single PCI Express lane
- Fully compliant with *PCI Express Base 1.0a* Specification
- TX Electrical Idle and RX Electrical Idle Detect
- Complete support for L0, L0s, L1, L2 power management
- Receiver Detect, integrated Beacon transmitter and detector
- Programmable serial transmit current and transmit de-emphasis
- Selectable serial receiver equalizer
- On-chip selectable low impedance/high impedance terminations
- Latency introduced by elastic buffer is programmable
- Intel PHY Interface for PCI Express architecture v1.0 (PIPE) at PHY/MAC boundary
- 8-bit/16-bit PIPE data interface for transmit and receive running at 250MHz/125 MHz
- Provides source-synchronous method for both transmit and receive direction
- Uses SSTL signaling for PIPE data and control to retain signal integrity at high-speed
- Provides I^2C interface for PHY parameters tuning
- Consumes only auxiliary power at L2 power state for saving power
- Supports JTAG (IEEE 1149.1) boundary scan interface
- Package: 100-pin LFBGA 9 x 9 mm

Functional Block Diagram



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