DATA SHEET

TDA8003TS
I²C-bus SIM card interface

Product specification
Supersedes data of 2000 Feb 29
File under Integrated Circuits, IC02

2000 Apr 20

Philips
Semiconductors

PHILIPS

I²C-bus SIM card interface TDA8003TS

FEATURES

- Subscriber Identification Module (SIM) card interface in accordance with GSM11.11, GSM11.12 (Global System for Mobile communication) and ISO 7816 requirements
- V_{CC} regulation (3 or 5 V ±8%) with controlled rise and fall times
- Card take-off protection
- One protected and buffered pseudo-bidirectional I/O line (I/O referenced to V_{CC} and SIMI/O referenced to V_{DDI})
- Clock generation (up to 10 MHz) with synchronous start and frequency doubling
- Clock stop LOW, clock stop HIGH or 1.25 MHz (from internal oscillator) for cards Power-down mode
- Automatic activation and deactivation sequences of an independent sequencer
- Automatic processing of pin RST with count of the CLK cycles for start of the Answer To Reset (ATR)
- Warm reset command
- Supply voltage supervisor for Power-on reset, spike killing and emergency deactivation in case of supply drop-out
- DC-to-DC converter (doubler, tripler or follower) allowing operation in a 3 or 5 V environment ($2.5 \leq V_{DD} \leq 6$ V)
- Enhanced Electrostatic Discharge (ESD) protections on card side (6 kV minimum)
- Power-down mode with several active features and current reduction
- Off mode with 2 μA current
- Control from a microcontroller via a 400 kHz slave I²C-bus (4 possible addresses: 48H, 4AH, 4CH and 4EH)
- Four parallel devices possible due to 2 sub-address wires
- Interface signals supplied by an independent voltage ($1.5 \leq V_{DDI} \leq 6$ V).

APPLICATIONS

- GSM mobile phones
- SAM interfaces in banking terminals
- Portable card readers, etc.

GENERAL DESCRIPTION

The TDA8003TS is a low cost one chip SIM interface, in accordance with GSM11.11, GSM11.12 and EMV96 (Europay, Mastercard, Visa) with card current limitation. Controlled by I²C-bus, it is optimized in terms of board space, external components count and connection count (see Chapter “Application information”).

The integrated DC-to-DC converter ensures full cross-compatibility between 3 or 5 V cards and 3 or 5 V environments. The very low-power consumption in Power-down mode and Off mode saves battery power.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8003TS/C1	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
TDA8003TS/C2	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode; V_{DD} = 3 V	–	–	2	µA
		Power-down mode; V_{DD} = 3 V; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to PGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{DD} = 3 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	18	mA
		active mode; V_{DD} = 3 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA; f_{CLK} = 3.25 MHz	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA; f_{CLK} = 3.25 MHz	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
V_{CC}	card supply voltage	5 V card; active mode; 0 < I_{CC} < 15 mA; 40 nAs dynamic load on 200 nF capacitor	4.6	5	5.4	V
		3 V card; active mode; 0 < I_{CC} < 10 mA; 24 nAs dynamic load on 200 nF capacitor	2.75	3	3.25	V
		5 V card; bit PDOWN = 1; I_{CC} < 5 mA	4.6	–	5.4	V
		3 V card; bit PDOWN = 1; I_{CC} < 5 mA	2.75	–	3.25	V
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 200 nF	0.05	–	0.25	V/µs
t_{de}	deactivation time		–	–	120	µs
t_{act}	activation time		–	–	150	µs
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
T_{amb}	operating ambient temperature		–40	–	+85	°C

BLOCK DIAGRAM

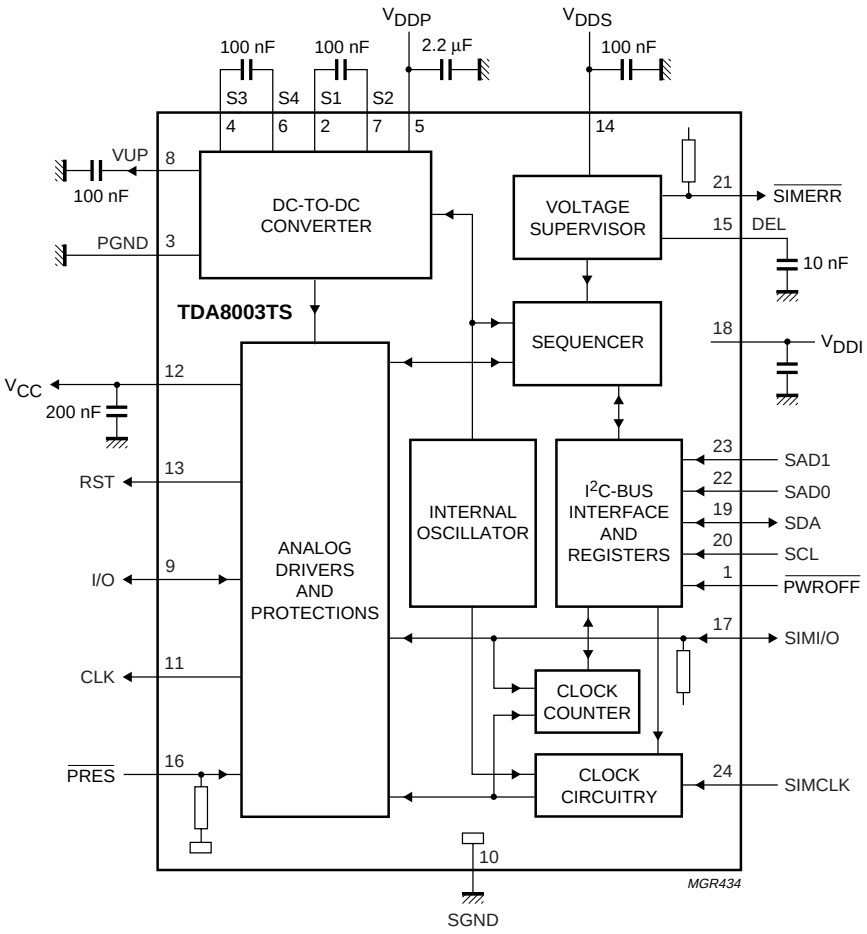


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{PWROFF}$	1	control input for entering the Off mode (active LOW)
S1	2	capacitor connection for the DC-to-DC converter (between S1 and S2)
PGND	3	power ground
S3	4	capacitor connection for the DC-to-DC converter (between S3 and S4)
V_{DDP}	5	power supply voltage
S4	6	capacitor connection for the DC-to-DC converter (between S3 and S4)
S2	7	capacitor connection for the DC-to-DC converter (between S1 and S2)
VUP	8	DC-to-DC converter output (must be decoupled with 100 nF to ground)
I/O	9	input/output to and from the card reader (C7I); see Fig.7
SGND	10	signal ground
CLK	11	clock output to the card reader (C3I)
V_{CC}	12	supply voltage to the card reader (C1I)
RST	13	reset output to the card reader (C2I)
V_{DDS}	14	signal supply voltage
DEL	15	external capacitor connection for the delay on voltage supervisor
$\overline{PRES}$	16	card presence indication input (active LOW); note 1
SIMI/O	17	input/output to and from the microcontroller (internal 20 kΩ pull-up resistor connected to V_{DDI})
V_{DDI}	18	supply voltage for the interface signals with the system
SDA	19	I²C-bus serial data input/output
SCL	20	I²C-bus serial clock input
$\overline{SIMERR}$	21	interrupt output (active LOW; internal 100 kΩ pull-up resistor connected to V_{DDI})
SAD0	22	I²C-bus slave address selection input
SAD1	23	I²C-bus slave address selection input
SIMCLK	24	external clock input

Note

1. Card presence input with negative current source. To be used with the card reader switch connected to V_{DDS} or V_{DDP}. The switch is normally closed when the card is not present. If the switch connection is open-circuit or pin 16 is not connected, then the interface will always detect a present card (see Fig.7).

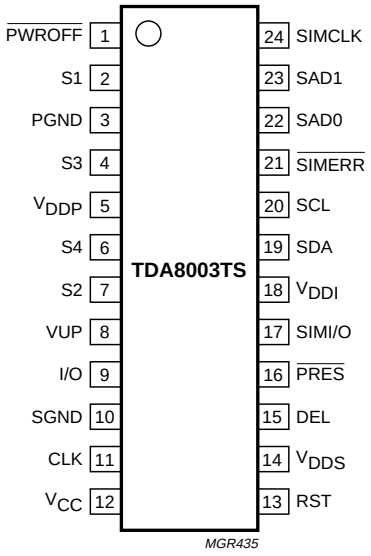


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Figure 1 shows the block diagram of the TDA8003TS. The functional blocks are described in the following sections. It is assumed that the reader of this specification is aware of GSM11.11 and ISO 7816 terminology.

I²C-bus control

The I²C-bus interface is used:

- To configure the clock to the card in active mode ($\frac{1}{2}f_{SIMCLK}$ and $\frac{1}{4}f_{SIMCLK}$)
- To configure the clock to the card in power reduction mode (stop LOW, stop HIGH or ±1.25 MHz derived from the internal oscillator)
- To select operation with a 3 or 5 V card
- To start or stop sessions (cold reset)
- To initiate a warm reset
- To enter or leave the Power-down mode
- To request the status (card present or not, hardware problem occurred, unresponsive card after activation, supply drop-out detected by the voltage supervisor, card powered or not)
- To configure SIMI/O and I/O in high-impedance (for use of several TDA8003TS in parallel).

The structure of the I²C-bus data frames is as follows:

- Commands to the TDA8003TS:
  - START/ADDRESS/WRITE
  - COMMAND BYTE
  - STOP.

  The fixed address is 01001XY. X and Y are defined by the logic levels on pins SAD1 and SAD0 as shown in Table 1 (connect to ground for logic 0; connect to V_{DDI} for logic 1). The command bits are described in Table 2. The commands are executed on the rising edge of the 9th SCL pulse.
- Status from the TDA8003TS (see Table 4). The fixed address is 01001XY. X and Y are defined by the logic levels on pins SAD1 and SAD0 as shown in Table 1.

Table 1 Address selections

ADDRESS	SAD1	SAD0
48H	0	0
4AH	0	1
4CH	1	0
4EH	1	1

Table 2 Description of the command bits; (all bits are cleared at reset)

SYMBOL	BIT	DESCRIPTION
START/STOP	0	Logic 1 initiates an activation sequence and a cold reset procedure. Logic 0 initiates a deactivation sequence.
WARM	1	Logic 1 initiates a warm reset procedure. TDA8003TS/C1: warm reset performed only when the 2 times 45000 CLK pulses have expired without answer from the card.
		TDA8003TS/C2: warm reset performed whatever the card has answered or not at the cold reset procedure but the count is 2 times 44745 CLK pulses.
3 V/5 VN	2	Logic 1 sets the card supply voltage V_{CC} to 3 V. Logic 0 sets V_{CC} to 5 V.
PDOWN	3	Logic 1 applies on CLK the frequency defined by bits CLKPD1 and CLKPD2, and enters a reduced consumption mode. Logic 0 sets the circuit back to normal mode.
CLKPD1	4	Bits 4 and 5 determine the clock to the card at power-down as shown in Table 3.
CLKPD2	5	
DT/DFN	6	Logic 1 sets f_{CLK} to $\frac{1}{2}f_{SIMCLK}$ (in active mode). Logic 0 sets f_{CLK} to $\frac{1}{4}f_{SIMCLK}$.
I/OEN	7	Logic 1 will transfer I/O to SIMI/O. Logic 0 sets I/O and SIMI/O to high-impedance.

Table 3 Clock to the card at power-down

BIT 4	BIT 5	FUNCTION
0	0	clock stop LOW
0	1	clock stop HIGH
1	0	clock is $\frac{1}{2}f_{osc}$
1	1	no change

Table 4 Description of the status bits; note 1

SYMBOL	BIT	DESCRIPTION
PRES	0	Logic 1 when the card is present. Logic 0 when the card is not present.
PRESL	1	Logic 1 when the card has been extracted or inserted. Logic 0 when the status is read-out.
–	2	Bit 2 is not used and is fixed to logic 0.
SUPL	3	Logic 1 when the voltage supervisor has signalled a fault. Logic 0 when the status is read-out.
PROT	4	Logic 1 when an overload has occurred during a session. Logic 0 when the status is read-out.
MUTE	5	TDA8003TS/C1: Logic 1 when a card has not answered after 2 times 45000 CLK pulses. Logic 0 when the status is read-out.
		TDA8003TS/C2: Same as for C1, but the count is 2 times 44745 CLK pulses.
EARLY	6	Logic 1 when a card has answered between 200 and 352 CLK cycles. Logic 0 when the status is read-out.
ACTIVE	7	Logic 1 when the card is power-on. Logic 0 when the card is power-off.

Note

1. In case of card extraction, supply drop-out or overload detection within a session, the card will be automatically deactivated, $\overline{\text{SIMERR}}$ pulled LOW, bit START = 0 and the corresponding status bit = 1. The status bit will be logic 0 and $\overline{\text{SIMERR}}$ will be released when the microcontroller reads out the status register, on the 7th SCL pulse. After a supply drop-out, $\overline{\text{SIMERR}}$ will be released at the end of the alarm pulse and bit SUPL = 1.

Power supply

The circuit operates within a supply voltage range of 2.5 to 6 V. The supply pins are V_{DDS} and SGND. Pins V_{DDP} and PGND only supply the DC-to-DC converter for the analog drivers to the card and must be decoupled externally because of the large current spikes that the card and the DC-to-DC converter can create. An integrated spike killer ensures the card contacts to remain inactive during power-up or power-down. An internal voltage reference is generated for the DC-to-DC converter, the voltage supervisor and the V_{CC} generator.

All interface signals with the microcontroller ($\overline{PWROFF}$, SIMCLK, SAD1, SAD0, $\overline{SIMERR}$, SCL, SDA and SIMI/O) are referenced to a separate supply pin V_{DDI}, which may be different from V_{DD} ($1.5 \leq V_{DDI} \leq 6$ V).

The pull-up resistors on bus lines SDA and SCL may be referenced to a voltage higher than V_{DDI}. This allows the use of peripherals which do not operate at V_{DDI}.

The voltage supervisor (see Fig.3) senses V_{DDS}. It generates an alarm pulse, whose length t_W is defined by an external capacitor connected to pin DEL, when V_{DD} is too low to ensure proper operation (1 ms per 1 nF typical).

During this alarm pulse, $\overline{SIMERR}$ is LOW and the I²C-bus is unresponsive. $\overline{SIMERR}$ goes back to HIGH, and the I²C-bus becomes operational at the end of this alarm pulse. Bit SUPL is set as long as the status has not been read.

It is also used to either block any spurious signals on card contacts during microcontroller reset, or to force an automatic deactivation of the contacts in the event of supply drop-out.

Outside a card session, $\overline{SIMERR}$ is LOW as long as the voltage supervisor is active. If a supply drop-out occurs during a session, $\overline{SIMERR}$ falls to LOW, bit START is cleared and an automatic deactivation is initiated.

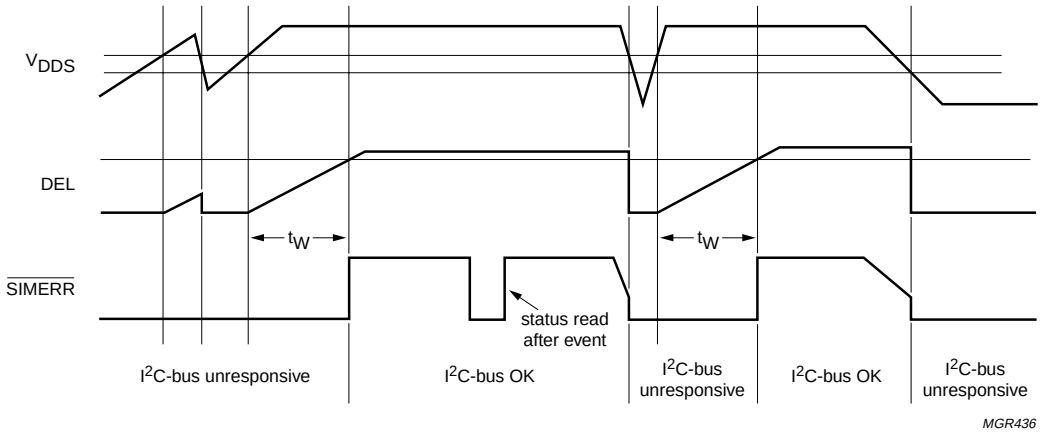


Fig.3 Voltage supervisor.

DC-to-DC converter

The whole circuit is powered by V_{DDS}, except for the V_{CC} generator, the other card contact buffers and the interface signals.

The DC-to-DC converter acts as a doubler or a tripler, depending on the supply voltage V_{DD} and the card supply voltage V_{CC}. There are basically four possible situations:

- V_{DD} = 3 V and V_{CC} = 3 V. The DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 4.5 V
- V_{DD} = 3 V and V_{CC} = 5 V. The DC-to-DC converter acts as a tripler with a regulation of V_{VUP} at approximately 6.5 V
- V_{DD} = 5 V and V_{CC} = 3 V. The DC-to-DC converter is disabled and V_{DD} is applied to pin VUP
- V_{DD} = 5 V and V_{CC} = 5 V. The DC-to-DC converter acts as a doubler with a regulation of V_{VUP} at approximately 6.5 V.

The supply voltage is recognized by the TDA8003TS at approximately 3.75 V for the C1 and 3.3 V for the C2.

When a card session is requested by the microcontroller, the sequencer will first start the DC-to-DC converter, which is a switched capacitor type, clocked by an internal oscillator at a frequency f_{osc} of approximately 2.5 MHz. The output voltage V_{VUP} is regulated at approximately 4.5 or 6.5 V and subsequently fed to the V_{CC} generator. V_{CC} and PGND are used as a reference for all other card contacts.

Power-down mode

The Power-down mode is used for current consumption reduction when the card is in Sleep mode.

To enter Power-down mode, the microcontroller must first select CLK in this mode (stop LOW, stop HIGH or 1.25 MHz from the internal oscillator) with bits CLKPD1 and CLKPD2. Subsequently, the microcontroller sends the command PDOWN, CLK is switched to the value predefined by bits CLKPD1 and CLKPD2, and SIMCLK may be stopped (HIGH or LOW).

If the selected CLK is stopped, the biasing currents in the buffers to the card will be reduced. The voltage supervisor and all control functions also remain active. The maximum current taken by the card in this mode when CLK is stopped is assumed to be less than 5 mA.

Before leaving the Power-down mode, the clock signal must first be applied to SIMCLK, and then bit PDOWN must be set to logic 0.

Off mode

The Off mode is entered when the $\overline{\text{PWROFF}}$ signal is LOW. In this mode, no function is valid. This mode avoids switching off the power supply of the device, and gives a current consumption less than 2 μA. Before entering the Off mode, the card must be deactivated.

The Off mode is resumed when the $\overline{\text{PWROFF}}$ signal returns to HIGH. This re-initializes the voltage supervisor, and has the same effect as a reset of the device. As long as the device is not ready to operate, the $\overline{\text{SIMERR}}$ signal will remain LOW.

Sequencer and clock counter

The sequencer handles the ensuring activation and deactivation sequences in accordance with GSM11.11 and ISO 7816, even in case of emergency (card take-off, short circuit and supply drop-out). The sequencer is clocked with the internal oscillator frequency f_{osc}.

The activation is initiated with the START command (only if the card is present, and if the voltage supervisor does not detect a fault on the supply). During activation, V_{CC} goes HIGH and subsequently I/O is enabled and CLK is started with RST = LOW. The clock counter counts the CLK pulses till a start bit is detected on I/O.

After 45000 CLK pulses for the C1 (44745 for the C2), if no start bit on I/O has been detected, the sequencer toggles RST to HIGH, and counts again 45000 CLK pulses (44745 for the C2). If, again, no start bit has been detected, $\overline{\text{SIMERR}}$ will be pulled LOW and the information of bit MUTE is set in the status register.

If a start bit has been detected during the two 45000 CLK pulse slots (44745 for the C2), the clock counter is stopped, RST is kept at the same level and the session can go on between the card and the system.

The clock counter does not take care of any start bit during the 200 first CLK pulses of both slots; if a start bit is detected between 200 and 352 CLK pulses of both slots, then $\overline{\text{SIMERR}}$ will be pulled LOW and the information of bit EARLY is set in the status register.

The deactivation is initiated either by the microcontroller (STOP command), or automatically by the TDA8003TS in case of card take-off, short circuit or supply voltage drop-out detected by the voltage supervisor. During deactivation, RST will go LOW, CLK is stopped, I/O is disabled and V_{CC} goes LOW.

Clock circuit

The clock to the card is either derived from pin SIMCLK (2 to 20 MHz) or from the internal oscillator.

During a card session, f_{CLK} may be chosen to be $\frac{1}{2}f_{SIMCLK}$ or $\frac{1}{4}f_{SIMCLK}$ depending on bit DT/DFN.

For the card Sleep mode, CLK may be chosen stop LOW, stop HIGH or $\frac{1}{2}f_{osc}$ (1.25 MHz) with bits CLKPD1 and CLKPD2. This predefined value will be applied to CLK when bit PDOWN is set to logic 1.

The first CLK pulse has the correct width, and all frequency changes are synchronous, ensuring that no pulse is smaller than 45% of the shortest period.

The duty cycle is within 45 and 55% in stable state, the rise and fall times are less than 8% of the period and precaution has been taken so that there is no overshoot or undershoot.

Activation sequence

Figure 4 shows the activation sequence. When the card is inactive, V_{CC}, CLK, RST and I/O are LOW, with low-impedance with respect to ground. The DC-to-DC converter is stopped. SIMI/O is pulled HIGH at V_{DDI} via the 20 kΩ pull-up resistor. When all conditions are met (supply voltage, card present, no hardware problems), the microcontroller may initiate an activation sequence by setting bit START to logic 1 (t_0) via the I²C-bus:

1. The DC-to-DC converter is started (t_1).
2. V_{CC} starts rising from 0 to 3 or to 5 V according to 3 V/5 VN control bit with a controlled rise time of 0.17 V/µs typically (t_2).
3. I/O buffer is enabled in reception mode (t_3).
4. CLK is sent to the card reader with RST = LOW, and the count of 45000 (44745 for C2) CLK pulses is started ($t_4 = t_{act}$).
5. If a start bit is detected on I/O, the clock counter is stopped with RST = LOW. If not, RST = HIGH, and a new count of 45000 (44745 for C2) CLK pulses is started (t_5).

If a start bit is detected on I/O and the clock counter is stopped with RST = HIGH, the card session may continue. If not, bit MUTE is set in the status register and $\overline{\text{SIMERR}}$ is pulled LOW. The microcontroller may initiate a deactivation sequence by setting bit START to logic 0.

If a start bit is detected during the 200 first CLK pulses of each count slot, then it will not be taken into account. If a start bit is detected during 200 and 352 CLK pulses of each slot, then bit EARLY is set in the status register and $\overline{\text{SIMERR}}$ is pulled LOW. The microcontroller may initiate a deactivation sequence by setting bit START to logic 0.

The sequencer is clocked by $\frac{1}{64}f_{osc}$ which leads to a time interval T of 25 µs typically. Thus t_1 = 0 to $\frac{1}{64}T$; $t_2 = t_1 + \frac{3}{2}T$; $t_3 = t_1 + \frac{7}{2}T$; $t_4 = t_1 + 4T$ and t_5 depends on the SIMCLK frequency.

Deactivation sequence

Figure 5 shows the deactivation sequence. When the session is completed, the microcontroller sets bit START to logic 0. The circuit will execute an automatic deactivation sequence:

1. Card reset, RST falls to LOW (t_{10}).
2. CLK is stopped (t_{11}).
3. I/O falls to LOW (t_{12}).
4. V_{CC} falls to 0 V with typically 0.17 V/µs slew rate (t_{13}). The deactivation is completed when V_{CC} reaches 0.4 V (t_{de}).
5. The DC-to-DC converter is stopped and CLK, RST, V_{CC} and I/O become low-impedance with respect to PGND (t_{14}).

Where $t_{10} < \frac{1}{64}T$; $t_{11} = t_{10} + \frac{1}{2}T$; $t_{12} = t_{10} + T$; $t_{13} = t_{12}$ + 5 µs and $t_{14} = t_{10} + 4T$.

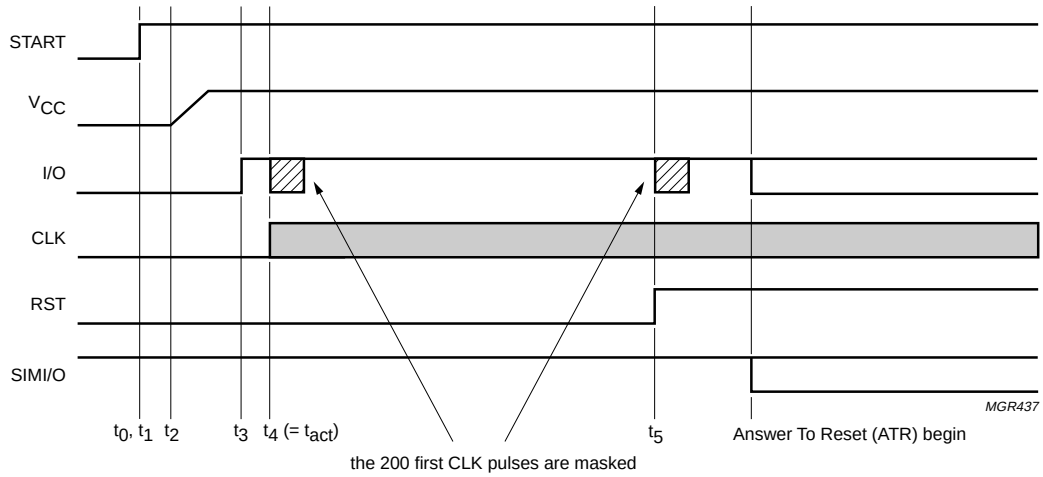


Fig.4 Activation sequence.

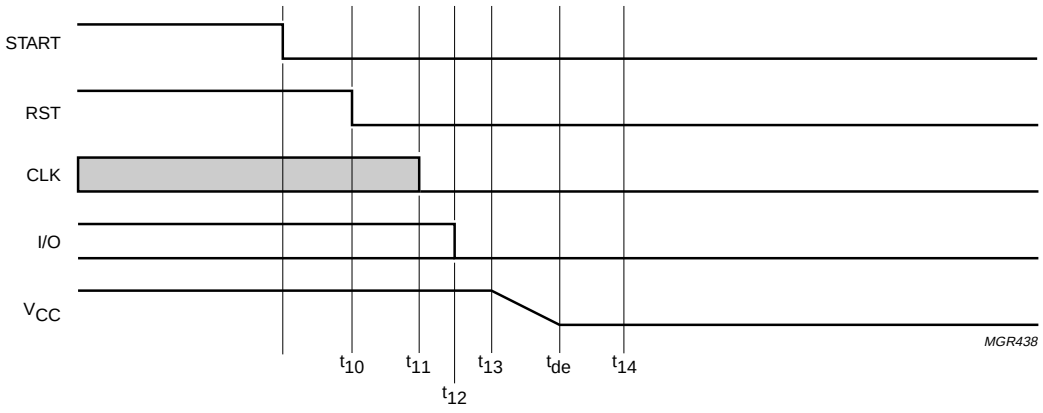


Fig.5 Deactivation sequence.

Protections

The following main hardware fault conditions are monitored by the circuit:

- Short circuits between V_{CC} and other contacts
- Card take-off during transaction
- Supply drop-out.

When one of these problems is detected during a card session, the security logic block pulls $\overline{SIMERR}$ to LOW, to warn the microcontroller and initiates an automatic deactivation of the contacts (see Fig.6).

I/O circuit

The Idle state is realized by both I/O and SIMI/O being pulled HIGH (via a 10 kΩ pull-up resistor from I/O to V_{CC} and via a 20 kΩ pull-up resistor from SIMI/O to V_{DDI}).

I/O is referenced to V_{CC} and SIMI/O to V_{DDI}, thus allowing operation with $V_{CC} \neq V_{DD} \neq V_{DDI}$.

When configuration bit I/OEN is logic 0, then I/O and SIMI/O are independent, which allows parallelization of several TDA8003TS with only one I/O line on the microcontroller side (up to 4 different I²C-bus addresses).

When bit I/OEN is logic 1, then the data transmission between I/O and SIMI/O is enabled.

The first side on which a falling edge occurs becomes the master. An anti-latch circuit disables the detection of falling edges on the other side, which becomes a slave.

After a delay time t_d (<500 ns) on the falling edge, the N transistor on the slave side is turned on, thus transmitting the logic 0 present on the master side.

When the master goes back to logic 1, the P transistor on the slave side is turned on during t_d, and then both sides return to their Idle states.

The maximum frequency on these lines is 1 MHz.

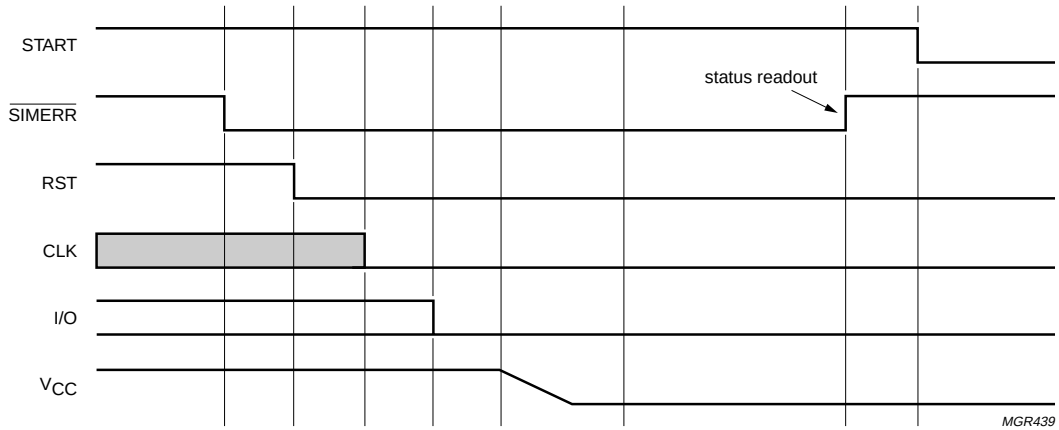


Fig.6 Emergency deactivation.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DDP}	power supply voltage		–0.5	+6.5	V
V_{DDS}	signal supply voltage		–0.5	+6.5	V
V_{DDI}	interface signal supply voltage		–0.5	+6.5	V
$V_{i(n)}$	input voltage				
	on pins 1, 17, 21 and 24		–0.5	+6.5	V
	on pins 15, 16, 22 and 23		–0.5	V_{DDS} + 0.5	V
	on pins 19 and 20		–0.5	+6.5	V
	on pins 9, 11 and 13		–0.5	V_{CC} + 0.5	V
	on pin 12		–0.5	+6.5	V
	on pin 8		–0.5	+7.5	V
	on pins 2, 4, 6 and 7		–0.5	V_{VUP} + 0.5	V
$I_{i(n)}$	DC input current				
	on pins 1, 17, 19, 20, 21, 22, 23 and 24		–5	+5	mA
	on pin 15		–5	+10	mA
$I_{i/o(n)}$	DC input/output current				
	on pins 2, 4, 6, 7 and 8		–40	+40	mA
	on pin 16		–5	+5	mA
$I_{i/o(17)}$	transient input/output current on pin 17	duration 1 ms	–40	+40	mA
P_{tot}	continuous total power dissipation	T_{amb} = –40 to +85 °C	–	230	mW
T_j	operating junction temperature		–	125	°C
T_{stg}	IC storage temperature		–55	+150	°C
$V_{esd(n)}$	electrostatic discharge voltage				
	on pins 9, 11, 12, 13 and 16		–6	+6	kV
	on any other pin		–2	+2	kV

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handle Metal Oxide Semiconductor (MOS) devices.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	102	K/W

CHARACTERISTICS

V_{DD} = 3 V; V_{DDI} = 1.5 V; f_{SIMCLK} = 13 MHz; f_{CLK} = 3.25 MHz; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage on pins V_{DDS} and V_{DDP}		2.5	–	6.0	V
I_{DD}	supply current on pins V_{DDS} and V_{DDP}	Off mode	–	–	2	µA
		inactive mode	–	–	50	µA
		Power-down mode; V_{CC} = 5 V; I_{CC} = 100 µA; SIMCLK connected to SGND or V_{DDI}; CLK is stopped	–	–	500	µA
		active mode; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	18	mA
		active mode; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	50	mA
		active mode; V_{DD} = 5 V; V_{CC} = 3 V; I_{CC} = 6 mA	–	–	10	mA
		active mode; V_{DD} = 5 V; V_{CC} = 5 V; I_{CC} = 10 mA	–	–	30	mA
V_{DDI}	interface signal supply voltage		1.5	–	6	V
I_{DDI}	interface signals supply current	SIMCLK connected to PGND or V_{DDI}	–	–	2	µA
		f_{SIMCLK} = 13 MHz; V_{DDI} = 1.5 V	–	–	120	µA
$V_{th(VDD)}$	threshold voltage on V_{DD}	falling edge	2	–	2.3	V
V_{hys}	hysteresis voltage on $V_{th(VDD)}$		40	–	200	mV
$V_{th(DEL)}$	threshold voltage on pin DEL		–	1.38	–	V
V_{DEL}	voltage on pin DEL		–	–	V_{DD}	V
$I_{ch(DEL)}$	charge current on pin DEL		–0.5	–1	–2.5	µA
$I_{dch(DEL)}$	discharge current on pin DEL	V_{DEL} = V_{DD}	0.5	–	–	mA
t_W	alarm pulse width	C_{DEL} = 10 nF	15	–	25	ms
Pin SIMCLK						
$f_{i(SIMCLK)}$	clock input frequency		0	–	20	MHz
t_f	fall time		–	–	1	µs
t_r	rise time		–	–	1	µs
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_L	leakage current		–	–	±3	µA
DC-to-DC converter						
$\frac{1}{2}f_{osc}$	oscillator frequency		1	–	1.6	MHz
V_{VUP}	voltage on pin VUP	5 V card	–	6.0	–	V
		3 V card	–	4.5	–	V

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin SDA (open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LH}	HIGH-level leakage current		–	–	1	µA
I_{IL}	LOW-level input current	depends on the pull-up resistor	–	–	–	µA
V_{OL}	LOW-level output voltage	I_{OL} = 3 mA	–	–	0.3	V
Pin SCL (open-drain)						
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	6	V
I_{LI}	input leakage current		–	–	1	µA
Pin $\overline{\text{SIMERR}}$ (100 kΩ pull-up resistor to V_{DDI})						
V_{OL}	LOW-level output voltage	I_{OL} < 1 mA	–	–	$0.3V_{DDI}$	V
V_{OH}	HIGH-level output voltage	I_{OH} < –1 µA	$0.7V_{DDI}$	–	–	V
Pins SAD0, SAD1 and $\overline{\text{PWROFF}}$						
V_{IL}	LOW-level input voltage		0	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LI}	input leakage current		–	–	±1	µA
Pin RST						
V_O	output voltage	inactive mode; I_O = 1 mA	–0.3	–	+0.4	V
I_O	output current	inactive mode; pin RST short circuit to ground	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} < –200 µA	V_{CC} – 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	0.5	µs
t_r	rise time	C_L = 30 pF	–	–	0.5	µs
Pin CLK						
V_O	output voltage	inactive mode; I_O = 1 mA	–0.3	–	+0.4	V
I_O	output current	inactive mode; pin CLK short circuit to ground	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 200 µA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –200 µA	V_{CC} – 0.5	–	V_{CC} + 0.2	V
t_f	fall time	C_L = 30 pF	–	–	8	ns
t_r	rise time	C_L = 30 pF	–	–	8	ns
f_{clk}	clock frequency	1 MHz power-down configuration	1	–	1.5	MHz
		regular activity	0	–	10	MHz
δ	duty factor	C_L = 30 pF	45	–	55	%

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pin V_{CC}						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.4	V
		active mode; 5 V card; no load	4.85	5.10	5.40	V
		active mode; 3 V card; no load	2.8	3.05	3.22	V
		active mode; with 200 nF capacitor; including static load (up to 20 mA) and dynamic current pulses; I_{max} = 200 mA, f_{max} = 5 MHz; duration <400 ns				
		5 V card; 40 nAs pulses	4.60	–	5.40	V
		3 V card; 24 nAs pulses	2.75	–	3.22	V
I_O	output current	inactive mode; pin V_{CC} short circuit to ground	–	–	–1	mA
		V_{CC} = 5 or 3 V; V_{DD} = 2.5 V	–	–	15	mA
		V_{CC} = 5 or 3 V; V_{DD} = 5.5 V	–	–	40	mA
$\lvert I_{CC} \rvert$	output current	V_{CC} short circuit to ground	–	–	120	mA
SR	slew rate on V_{CC} (rise and fall)	$C_{L(max)}$ = 300 nF	0.05	0.17	0.25	V/µs
Pin I/O						
V_O	output voltage	inactive mode; I_O = 1 mA	–	–	0.4	V
I_O	output current	inactive mode; pin I/O short circuit to ground	–	–	–1	mA
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.4	V
V_{OH}	HIGH-level output voltage	+25 < I_{OH} < –25 µA	$0.8V_{CC}$	–	V_{CC} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	+0.8	V
V_{IH}	HIGH-level input voltage		1.5	–	V_{CC} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA
I_{IL}	LOW-level input current		–	–	–600	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1	µs
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns
$R_{pu(int)}$	internal pull-up resistance between pins I/O and V_{CC}	C1 version	8	–	13	kΩ
		C2 version	13	–	18	kΩ
Pin SIMI/O						
V_{OL}	LOW-level output voltage	I_{OL} = 1 mA	–0.2	–	+0.3	V
V_{OH}	HIGH-level output voltage	with internal 20 kΩ pull-up resistor to V_{DDI}; I_O = 10 µA	V_{DDI} – 0.3	–	V_{DDI} + 0.2	V
V_{IL}	LOW-level input voltage		–0.3	–	$+0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI} + 0.3	V
I_{LIH}	HIGH-level input leakage current		–	–	10	µA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{IL}	LOW-level input current	with internal 20 kΩ pull-up resistor to V_{DDI}; V_I = 0 V	–	–	–100	µA
$t_{t(DI)}$	data input transition time	C_L = 30 pF	–	–	1	µs
$t_{t(DO)}$	data output transition time	C_L = 30 pF	–	–	0.5	µs
t_d	delay time on falling edge		–	–	500	ns
$R_{pu(int)}$	internal pull-up resistance between pins SIMI/O and V_{DDI}		16	–	26	kΩ
Pin $\overline{PRES}$						
V_{IL}	LOW-level input voltage		–0.3	–	+0.3V_{DD}	V
V_{IH}	HIGH-level input voltage		0.7V_{DD}	–	V_{DD} + 0.3	V
I_{IL}	LOW-level input current		–	–	5	µA
I_{IH}	HIGH-level input current		–	–	–5	µA
Timing						
t_{act}	activation time		–	–	150	µs
t_{de}	deactivation time		–	–	120	µs

APPLICATION INFORMATION

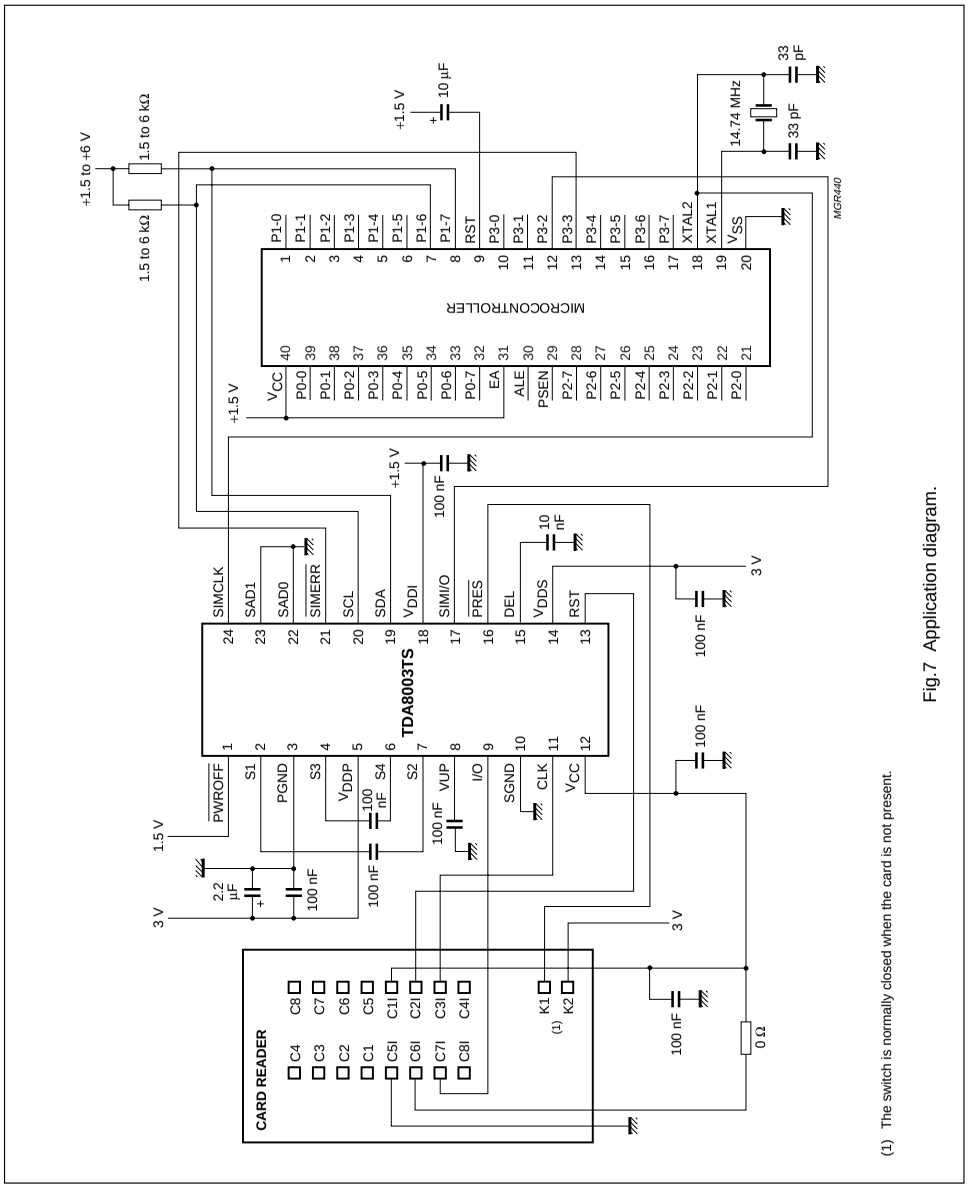
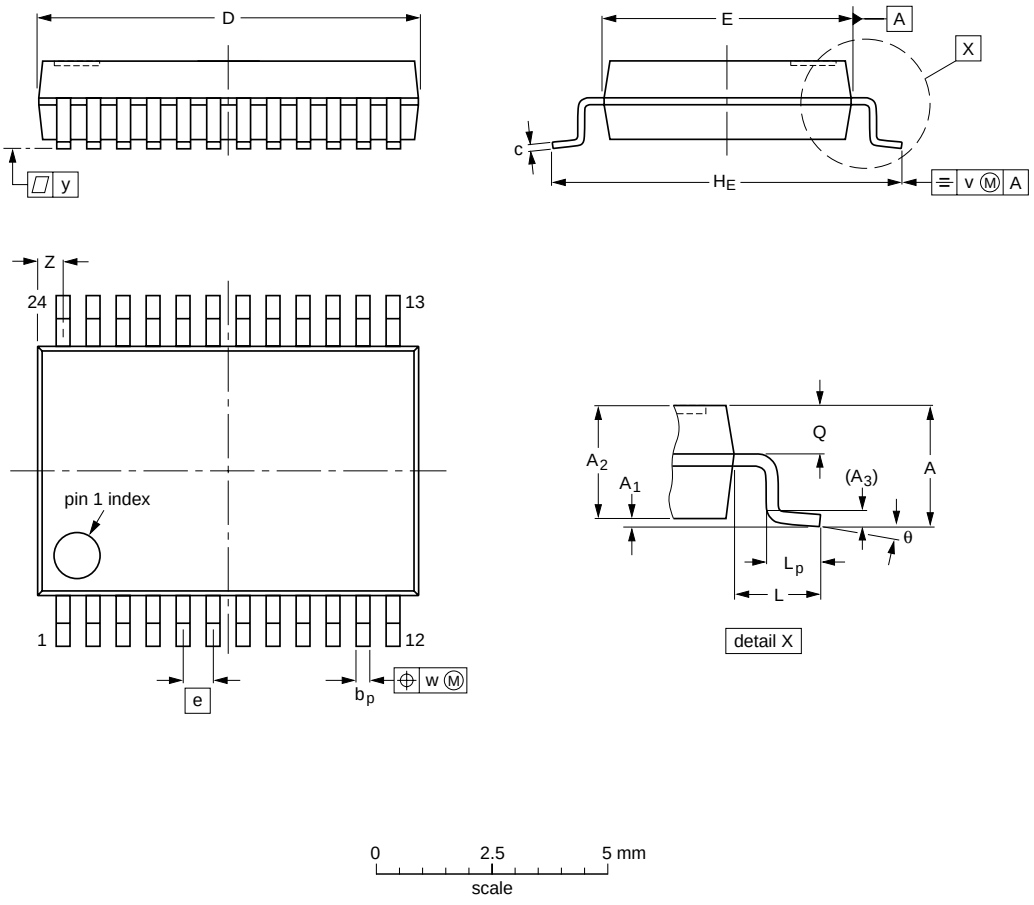


Fig.7 Application diagram.

(1) The switch is normally closed when the card is not present.

PACKAGE OUTLINE

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8^o 0^o

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150				~~95-02-04~~ 99-12-27

SOLDERING

Introduction to soldering surface mount packages

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed-circuit boards with high population densities. In these situations reflow soldering is often used.

Reflow soldering

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method.

Typical reflow peak temperatures range from 215 to 250 °C. The top-surface temperature of the packages should preferable be kept below 230 °C.

Wave soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed-circuit boards with a high component density, as solder bridging and non-wetting can present major problems.

To overcome these problems the double-wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double-wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - larger than or equal to 1.27 mm, the footprint longitudinal axis is **preferred** to be parallel to the transport direction of the printed-circuit board;
  - smaller than 1.27 mm, the footprint longitudinal axis **must** be parallel to the transport direction of the printed-circuit board.

  The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed-circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Typical dwell time is 4 seconds at 250 °C.
A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Manual soldering

Fix the component by first soldering two diagonally-opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C.

When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

Suitability of surface mount IC packages for wave and reflow soldering methods

PACKAGE	SOLDERING METHOD	
	WAVE	REFLOW(1)
BGA, LFBGA, SQFP, TFBGA	not suitable	suitable
HBCC, HLQFP, HSQFP, HSOP, HTQFP, HTSSOP, SMS	not suitable(2)	suitable
PLCC(3), SO, SOJ	suitable	suitable
LQFP, QFP, TQFP	not recommended(3)(4)	suitable
SSOP, TSSOP, VSO	not recommended(5)	suitable

Notes

1. All surface mount (SMD) packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the Drypack information in the *"Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods"*.
2. These packages are not suitable for wave soldering as a solder joint between the printed-circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
3. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
4. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.65 mm.
5. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

DISCLAIMERS

Life support applications — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

PURCHASE OF PHILIPS I²C COMPONENTS

Purchase of Philips I²C components conveys a license under the Philips' I²C patent to use the components in the I²C system provided the system conforms to the I²C specification defined by Philips. This specification can be ordered using the code 9398 393 40011.

NOTES

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 3 Figtree Drive, HOMEBUSH, NSW 2140,
Tel. +61 2 9704 8141, Fax. +61 2 9704 8139

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101 1248, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Via Casati, 23 - 20052 MONZA (MI),
Tel. +39 039 203 6838, Fax +39 039 203 6800

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku,
TOKYO 108-8507, Tel. +81 3 3740 5130, Fax. +81 3 3740 5057

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381, Fax +9-5 800 943 0087

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Al.Jerozolimskie 195 B, 02-222 WARSAW,
Tel. +48 22 5710 000, Fax. +48 22 5710 001

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 58088 Newville 2114,
Tel. +27 11 471 5401, Fax. +27 11 471 5398

South America: Al. Vicente Pinzon, 173, 6th floor,
04547-130 SÃO PAULO, SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Yukari Dudullu, Org. San. Blg., 2.Cad. Nr. 28 81260 Umraniye,
ISTANBUL, Tel. +90 216 522 1500, Fax. +90 216 522 1813

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 208 730 5000, Fax. +44 208 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 3341 299, Fax.+381 11 3342 553

For all other countries apply to: Philips Semiconductors,
International Marketing & Sales Communications, Building BE-p, P.O. Box 218,
5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in The Netherlands 753504/03/pp24 Date of release: 2000 Apr 20 Document order number: 9397 750 07034

Let's make things better.

Philips Semiconductors

PHILIPS