TV AND VTR STEREO/DUAL SOUND PROCESSOR WITH I²C BUS CONTROL

GENERAL DATA

The TDA8405 integrated circuit is a processor for stereo/dual-language signals for stereo-sound television receivers and VTR. The modulated signals at the TDA8405 inputs need to be "(L+R)/2" or "language A" on one channel and "R" or "language B" on the second channel (where L = left and R = right). The second channel is also modulated with the pilot carrier. The IC is controlled via the two-line, bidirectional I²C bus.

Features

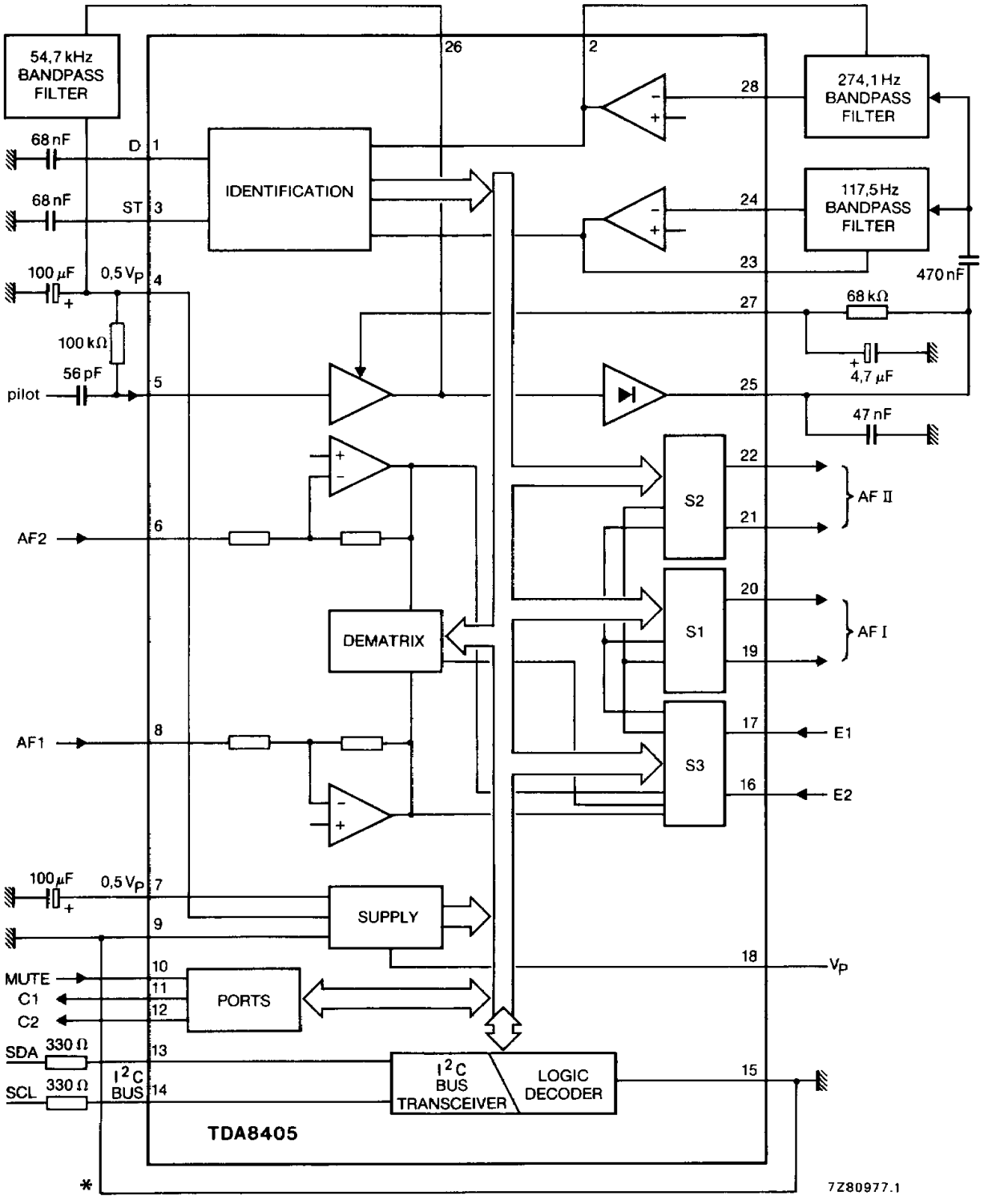
- Amplification of the two a.f. input signals by integrated operational amplifiers.
- Low distortion stereo dematrix
- All operational amplifiers are offset compensated
- I²C bus transceiver for system control (port control, mute, mode select, identification, etc.)
- Input port for fast muting
- Two general purpose output ports (three-state, bus-controlled)

QUICK REFERENCE DATA

Supply voltage	$V_P = V_{18\text{-}9\text{-}15}$	typ.	12 V
Supply current	$I_P = I_{18}$	typ.	25 mA
A.F. input signal	$V_{i(rms)} = V_{6\text{-}9}, V_{8\text{-}9}$	typ.	1 V
Weighted signal-to-noise ratio of the a.f. output-signals (CCIR 468/2)	(S+N)/N	⩾	70 dB
Crosstalk attenuation: stereo mode at f = 1 kHz	α_S	>	40 dB
dual sound mode at f = 40 to 12 500 Hz	α_{DS}	>	70 dB
Pilot signal input sensitivity	$V_i = V_{5\text{-}9(rms)}$	typ.	5 mV
Pilot signal amplifier gain control range	ΔG_V	>	40 dB

PACKAGE OUTLINE

28-lead DIL; plastic (SOT-117).



* Direct connection between pins 9 and 15 is needed.

Fig. 1 Block diagram.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage (pin 18)*	$V_P = V_{18-9, 15}$	max.	13,2 V
Output current (pins 19, 20, 21, 22)	I_n	max.	5 mA
Output current (pins 2, 23)	I_n	max.	1 mA
Output current (pins 11, 12)	I_n	max.	3 mA
Voltage range at any pin	V_n		0 to V_P V
Total power dissipation	P_{tot}	max.	1 W
Storage temperature range	T_{stg}		−40 to + 150 °C
Operating ambient temperature range	T_{amb}		0 to + 70 °C

DEVELOPMENT DATA

* Supply voltage may be applied only when pins 9 and 15 are connected to ground.

CHARACTERISTICS

T_{amb} = 25 °C; V_P = 12 V; $V_{i(af)rms}$ = 1 V; f = 1 kHz; dematrix aligned; $V_{i\,pilot(rms)}$ = 16 mV; test circuit Fig. 2; unless otherwise specified.

parameter	symbol	min.	typ.	max.	unit
Supply voltage	$V_P = V_{18\text{-}9,\,15}$	10,8	12	13,2	V
Supply current at V_P = 12 V	$I_P = I_{18}$	–	25	–	mA
Reference voltage	$V_{ref} = V_{4\text{-}9,\,15}$	–	$V_P/2$	–	V
DC levels (pins 5, 6, 7, 8, 16 17, 19, 20, 21, 22, 24, 28)	$V_{n\text{-}9,\,15}$	–	$V_P/2$	–	V
BUS TRANSCEIVER (pins 13, 14) (note 1)					
Clock SCL					
Voltage level LOW	$V_{14\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{14\text{-}15}$	3,0	–	–	V
Timing LOW period	t_{PL}	4,7	–	–	μs
Timing HIGH period	t_{PH}	4,0	–	–	μs
Rise time	t_r	–	–	1	μs
Fall time	t_f	–	–	0,3	μs
Input current HIGH	I_{IH}	–	–	10	μA
Input current LOW	$-I_{IL}$	–	–	10	μA
Data					
Voltage level LOW	$V_{13\text{-}15}$	−0,3	–	1,5	V
Voltage level HIGH	$V_{13\text{-}15}$	3,0	–	–	V
Rise time	t_r	–	–	1,0	μs
Fall time	t_f	–	–	0,3	μs
Set-up time data	t_{SU}	0,25	–	–	μs
Input current HIGH	I_{13}	–	–	10	μA
Input current LOW	$-I_{13}$	–	–	10	μA
Output current LOW	$+I_{13}$	3,0	–	–	mA
MUTE PORT (pin 10) note 2					
Input voltage LOW	$V_{10\text{-}15}$	–	–	1,5	V
Input voltage HIGH	$V_{10\text{-}15}$	8	–	–	V

DEVELOPMENT DATA

parameter	symbol	min.	typ.	max.	unit
CONTROL PORTS (pins 11, 12)					
3-state HIGH, LOW, high ohmic					
Output resistance in open state	$R_{11, 12\text{-}15}$	50	–	–	kΩ
Output voltage LOW	$V_{11, 12\text{-}15}$	–	–	0,8	V
Output voltage HIGH	$V_{11, 12\text{-}15}$	$V_{P\text{-}1}$	–	–	V
Output current LOW	$I_{11, 12}$	500	–	–	μA
Output current HIGH	$-I_{11, 12}$	80	–	–	μA
IDENTIFICATION (See Fig. 3)					
Input amplifier and demodulator					
Input voltage	$V_{5\text{-}9(p\text{-}p)}$	–	–	2,0	V
Min. input voltage	$V_{5\text{-}9(rms)}$	5,0	–	–	mV
Input resistance	$R_{5\text{-}9}$	500	–	–	kΩ
Gain	$G_{25\text{-}9}$	–	42	–	dB
Gain control range	ΔG	40	–	–	dB
Output voltage (gain-controlled)	$V_{25\text{-}9(p\text{-}p)}$	–	1,5	–	V
Operational amplifiers					
Input current	$I_{24, 28}$	–	70	–	nA
Gain at f = 200 Hz	$G_{23\text{-}24}$, $G_{2\text{-}28}$	78	–	–	dB
Output current	$I_{2, 23}$	1,5	–	–	mA
Output resistance	$R_{2, 23\text{-}9}$	–	2	–	kΩ
Output load capacitance	$C_{2, 23\text{-}9}$	–	–	30	pF
Schmitt trigger					
A.C. input signal	$V_{2, 23\text{-}9(rms)}$	–	1	–	V
Internal discharge resistors	$R_{1, 3\text{-}9}$	–	3	–	kΩ
A.F. STAGES					
Input resistance (pins 6, 8, 16 and 17)	$R_{n\text{-}9}$	10	–	–	kΩ
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{6, 8\text{-}9}$)	G1	–	6	–	dB
Gain ($V_{19, 20, 21, 22\text{-}9}/V_{16, 17\text{-}9}$)	G2	–	0	–	dB
Input voltage	$V_{6, 8\text{-}9(rms)}$	–	1	–	V
Crosstalk attenuation (notes 3, 4 and 9)					
dual sound	α_{DS}	70	–	–	dB
stereo f = 250 Hz to 6,3 kHz	α_S	40	–	–	dB
stereo f = 40 Hz to 250 Hz; 6,3 kHz to 12,5 kHz	α_S	30	–	–	dB

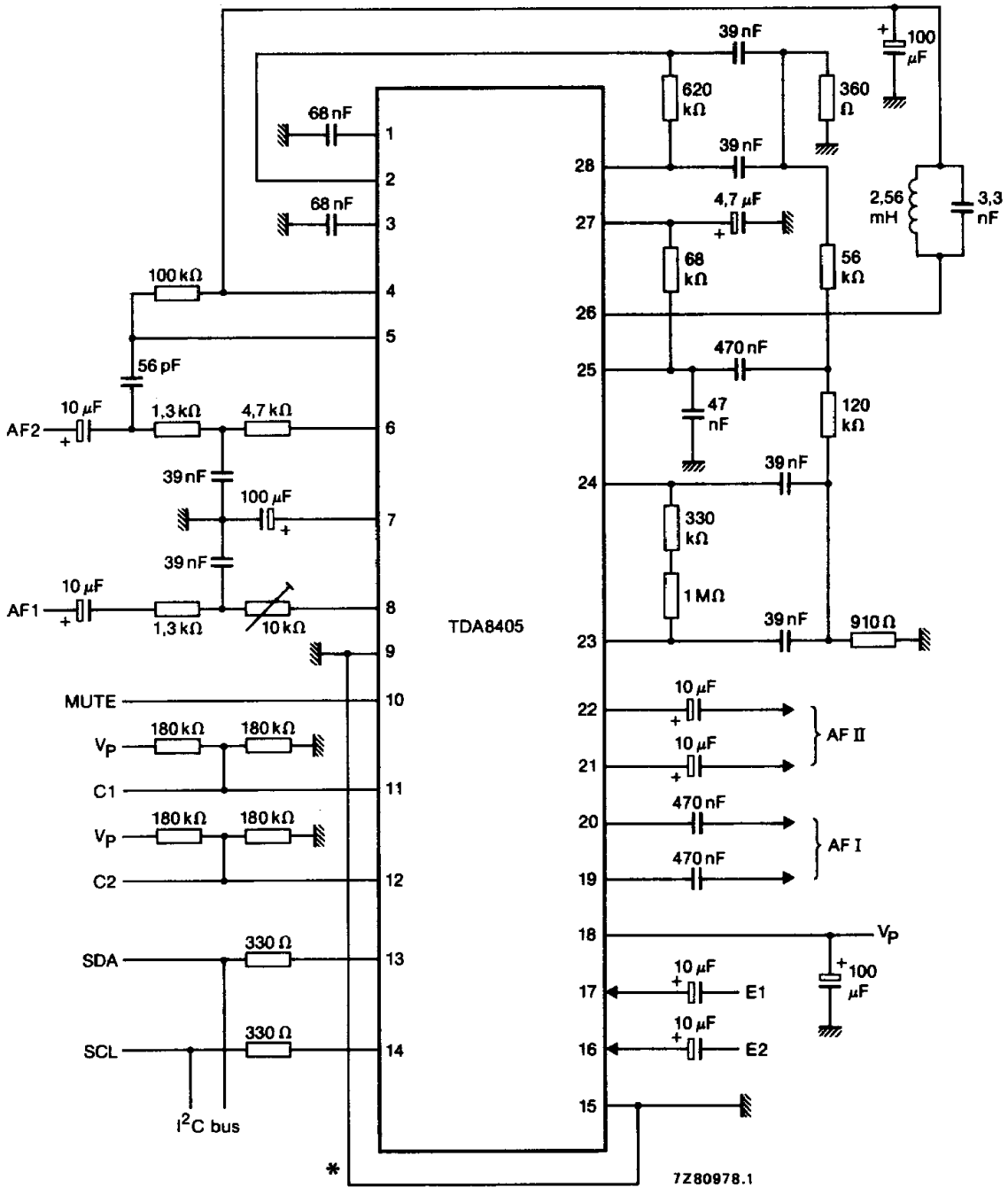
CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
A.F. STAGES (continued)					
Output resistance	$R_{19,20,21,22}$	–	200	300	Ω
Output load capacitance (pins 19, 20, 21 and 22)	$C_{n\text{-}9}$	–	–	1,5	nF
D.C. offsets (note 8) at pins 19,20,21 and 22	Δ_V	–	–	30	mV
Total harmonic distortion (notes 4 and 5)	THD	–	0,1	0,5	%
Output signal (r.m.s. value) (pins 19, 20, 21 and 22)	$V_{n\text{-}9(rms)}$	–	–	2,0	V
Ripple rejection (note 6)	RR	30	35	–	dB
Noise rejection (note 7) (noise from I^2C bus)	NR	80	–	–	dB
Signal-to-noise ratio (note 7)	(S+N)/N	70	–	–	dB
Ident signal suppression		70	–	–	dB
Signal suppression during mute (notes 4 and 7)		70	–	–	dB

Notes to the characteristics

1. Full specification of the I^2C bus will be supplied on request.
2. Programmable mute state. If the SC3 bit in the I^2C bus is LOW then the mute input is active LOW; if the mute bit is set to HIGH then the mute input is active HIGH.
3. Crosstalk attenuation definition: 20 log (unwanted output signal/input signal).
4. Frequency range: 40 Hz $<$ f $<$ 12,5 kHz.
5. In dual sound mode.
6. Test circuit as in Fig. 4: ripple rejection = output modulation due to hum on the supply line.
7. Related to 2 V (r.m.s.) output signal at pin 19, 20, 21 or 22; noise weighted according to CCIR 468/2.
8. Caused by any change of the switch position.
9. α_S measured without de-emphasis network.

DEVELOPMENT DATA



* Direct connection between pins 9 and 15 is needed.

Fig. 2 Test circuit.

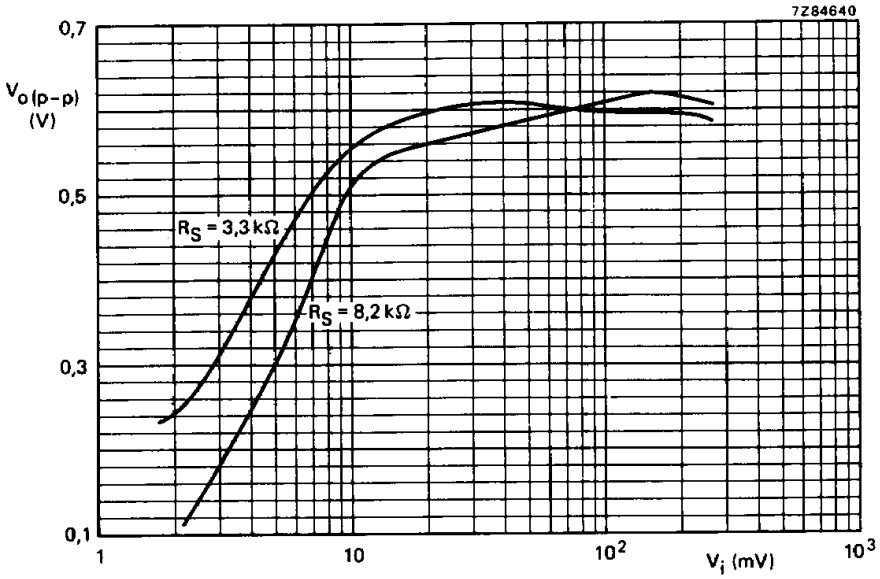


Fig. 3 Controlled output voltage as a function of the input signal (Q = 80); pilot frequency f_o = 54 kHz; R_S = source resistance.

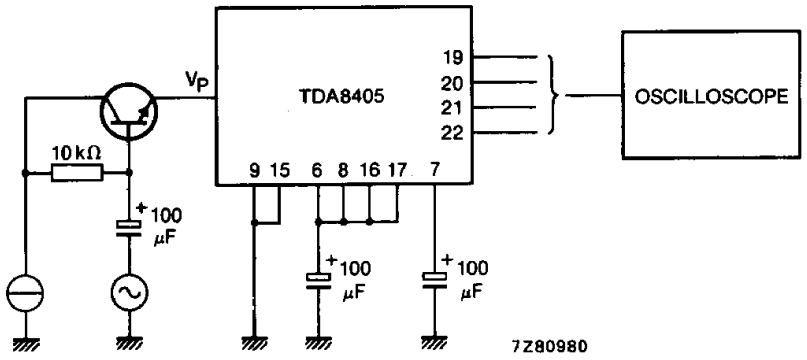
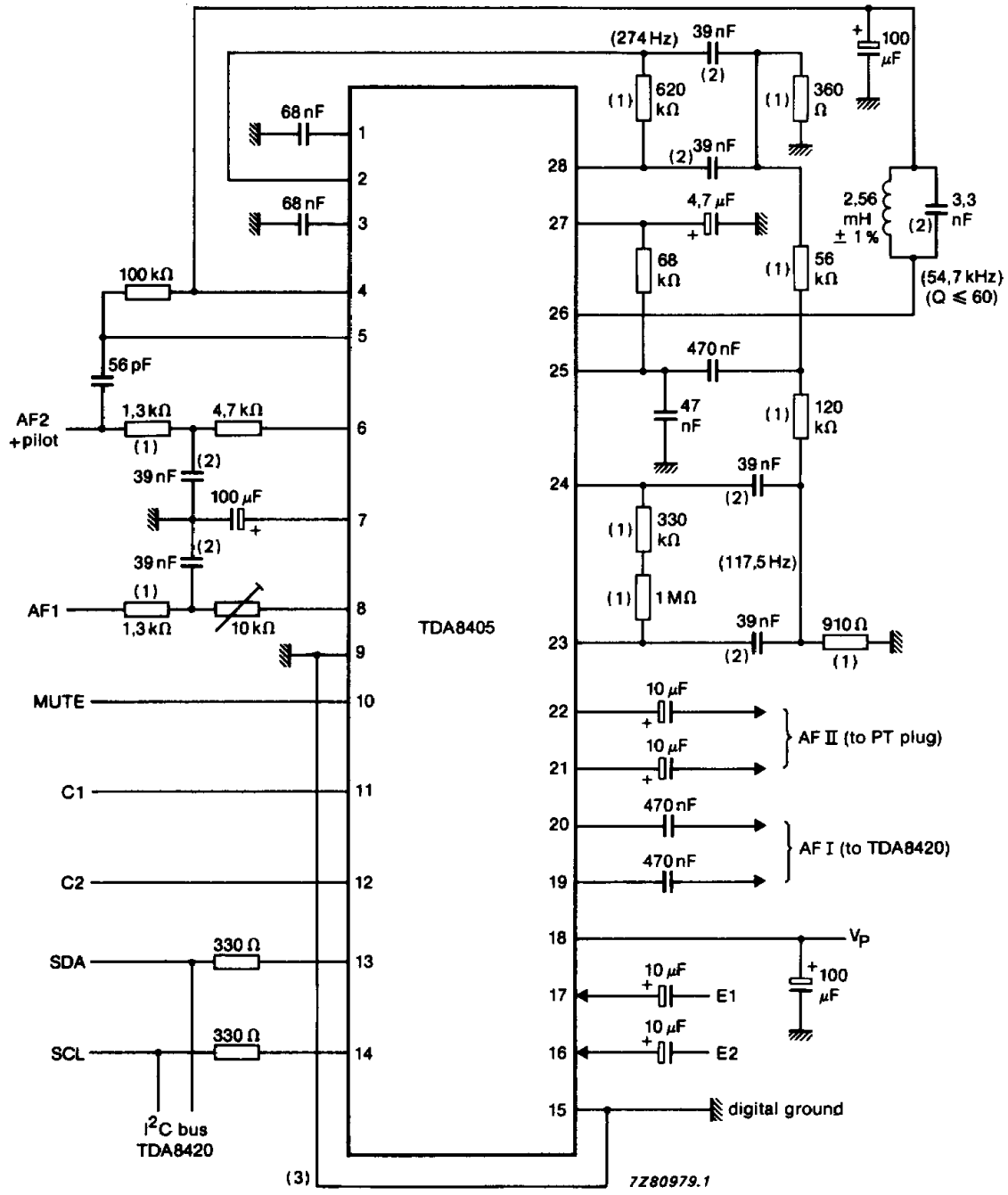


Fig. 4 Test circuit for ripple rejection: supply (d.c.) + pulse (r.m.s.) voltage at 100 Hz = 12 V + 50 mV.

DEVELOPMENT DATA



(1) ± 1 % tolerance

(2) polystyrene film/foil capacitors (KS) : ± 1 % tolerance

metallized polyethylenetherephthalate film capacitors (MKT) : ± 10 % tolerance

(3) Direct connection is needed between pins 9 and 15

Fig. 5 Application diagram.