



P89LPC9321

8-bit microcontroller with accelerated two-clock 80C51 core
8 kB 3 V byte-erasable flash with 512-byte data EEPROM

Rev. 01 — 9 December 2008

Product data sheet

1. General description

The P89LPC9321 is a single-chip microcontroller, available in low cost packages, based on a high performance processor architecture that executes instructions in two to four clocks, six times the rate of standard 80C51 devices. Many system-level functions have been incorporated into the P89LPC9321 in order to reduce component count, board space, and system cost.

2. Features

2.1 Principal features

- 8 kB byte-erasable flash code memory organized into 1 kB sectors and 64-byte pages. Single-byte erasing allows any byte(s) to be used as non-volatile data storage.
- 256-byte RAM data memory and a 512-byte auxiliary on-chip RAM.
- 512-byte customer data EEPROM on-chip allows serialization of devices, storage of setup parameters, etc.
- Two analog comparators with selectable inputs and reference source.
- Single Programmable Gain Amplifier (PGA) with selectable gains of 2x, 4x, 8x, or 16x can be applied to analog comparator inputs.
- Two 16-bit counter/timers (each may be configured to toggle a port output upon timer overflow or to become a PWM output).
- A 23-bit system timer that can also be used as real-time clock consisting of a 7-bit prescaler and a programmable and readable 16-bit timer.
- Enhanced UART with a fractional baud rate generator, break detect, framing error detection, and automatic address detection; 400 kHz byte-wide I²C-bus communication port and SPI communication port.
- Capture/Compare Unit (CCU) provides PWM, input capture, and output compare functions.
- 2.4 V to 3.6 V V_{DD} operating range. I/O pins are 5 V tolerant (may be pulled up or driven to 5.5 V).
- 4-level low voltage (brownout) detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- 28-pin TSSOP, PLCC and DIP packages with 23 I/O pins minimum and up to 26 I/O pins while using on-chip oscillator and reset options.

2.2 Additional features

- A high performance 80C51 CPU provides instruction cycle times of 111 ns to 222 ns for all instructions except multiply and divide when executing at 18 MHz. This is six times the performance of the standard 80C51 running at the same clock frequency. A lower clock frequency for the same performance results in power savings and reduced EMI.
- Serial flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Serial flash In-System Programming (ISP) allows coding while the device is mounted in the end application.
- In-Application Programming (IAP) of the flash code memory. This allows changing the code in a running application.
- Watchdog timer with separate on-chip oscillator, nominal 400 kHz, calibrated to $\pm 5\%$, requiring no external components. The watchdog prescaler is selectable from eight values.
- High-accuracy internal RC oscillator option, with clock doubler option, allows operation without external oscillator components. The RC oscillator option is selectable and fine tunable.
- Switching on the fly among internal RC oscillator, watchdog oscillator, external clock source provides optimal support of minimal power active mode with fast switching to maximum performance.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A software reset function is also available.
- Configurable on-chip oscillator with frequency range options selected by user programmed flash configuration bits. Oscillator options support frequencies from 20 kHz to the maximum operating frequency of 18 MHz.
- Oscillator fail detect. The watchdog timer has a separate fully on-chip oscillator allowing it to perform an oscillator fail detect function.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- High current sourcing/sinking (20 mA) on eight I/O pins (P0.3 to P0.7, P1.4, P1.6, P1.7). All other port pins have high sinking capability (20 mA). A maximum limit is specified for the entire chip.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC9321 when internal reset option is selected.
- Four interrupt priority levels.
- Eight keypad interrupt inputs, plus two additional external interrupt inputs.
- Schmitt trigger port inputs.
- Second data pointer.
- Emulation support.

3. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|---------------|---------|--|----------|
| | Name | Description | |
| P89LPC9321FA | PLCC28 | plastic leaded chip carrier; 28 leads | SOT261-2 |
| P89LPC9321FDH | TSSOP28 | plastic thin shrink small outline package; 28 leads; body width 4.4 mm | SOT361-1 |
| P89LPC9321FN | DIP28 | plastic dual in-line package; 28 leads; (600 mil) | SOT117-1 |

3.1 Ordering options

Table 2. Ordering options

| Type number | Flash memory | Temperature range | Frequency |
|---------------|--------------|-------------------|-----------------|
| P89LPC9321FA | 8 kB | -40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC9321FDH | 8 kB | -40 °C to +85 °C | 0 MHz to 18 MHz |
| P89LPC9321FN | 8 kB | -40 °C to +85 °C | 0 MHz to 18 MHz |

4. Block diagram

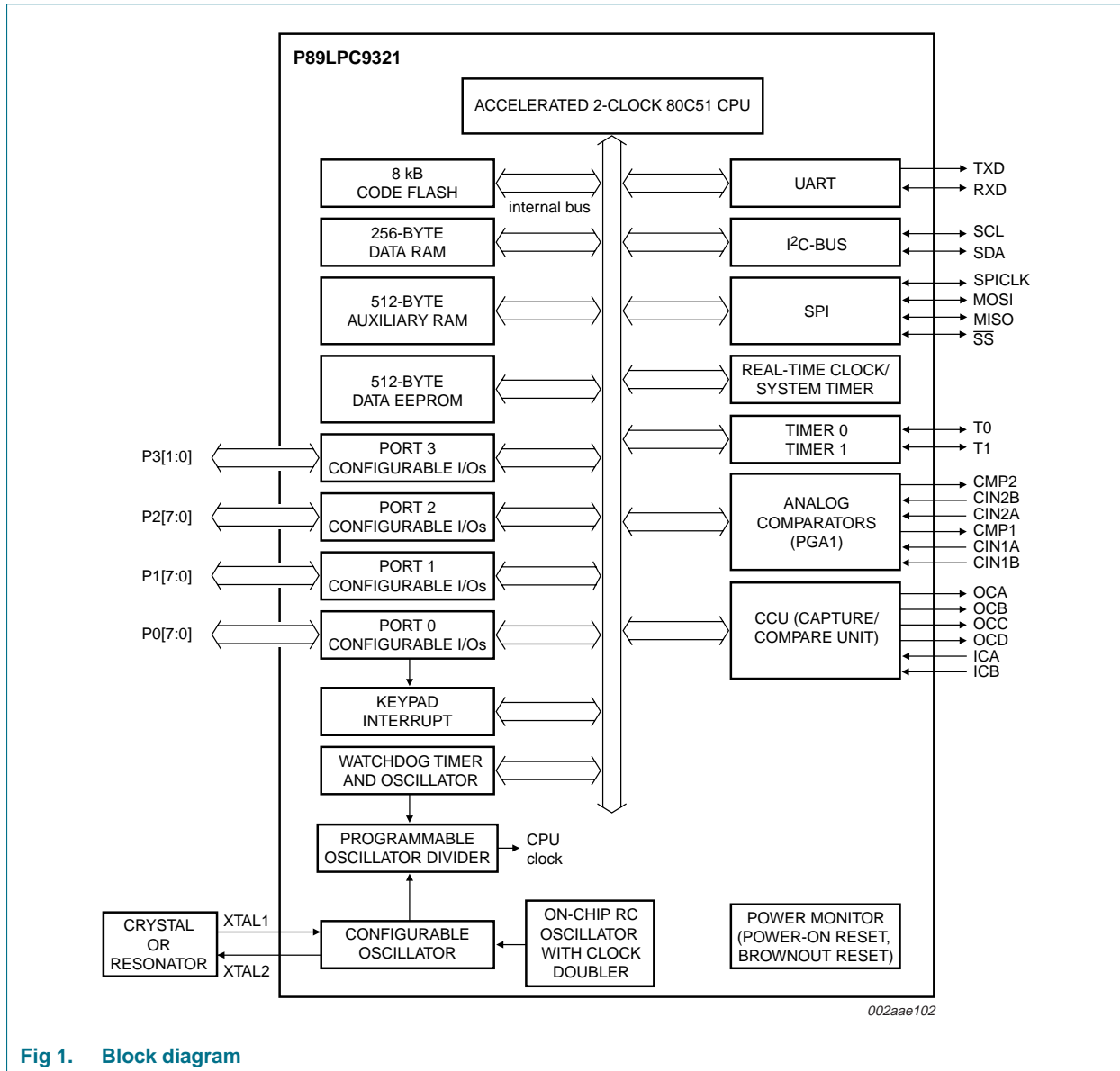


Fig 1. Block diagram

5. Functional diagram

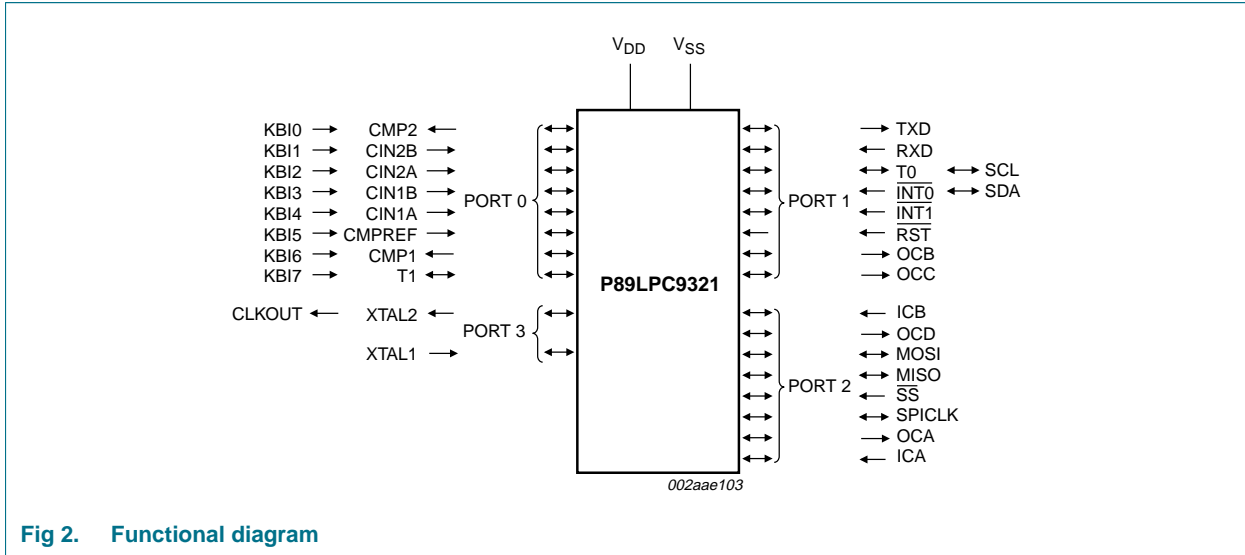
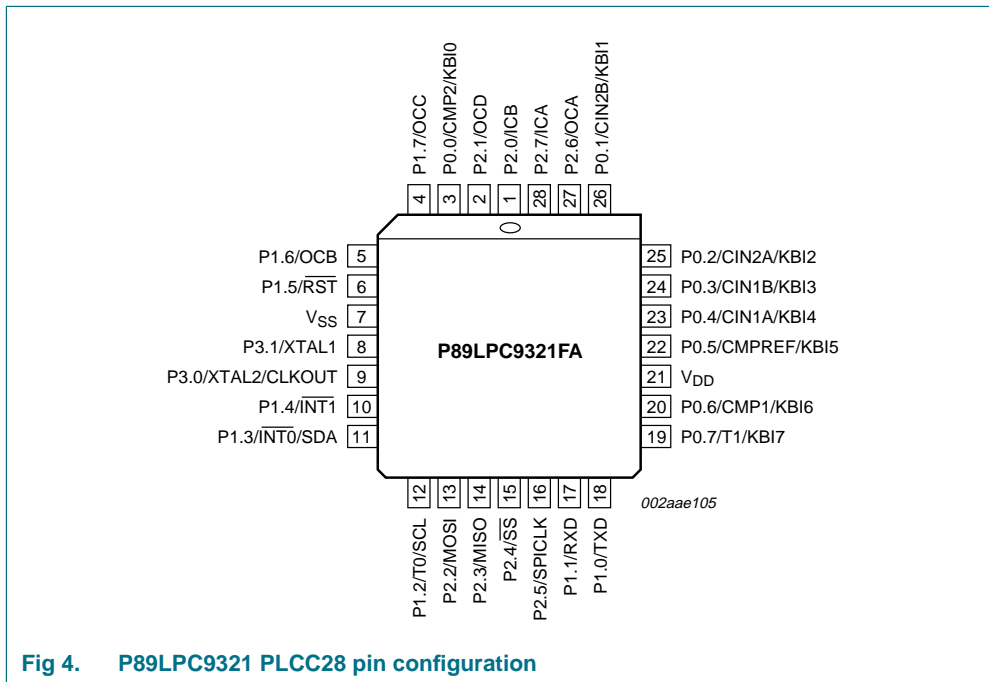
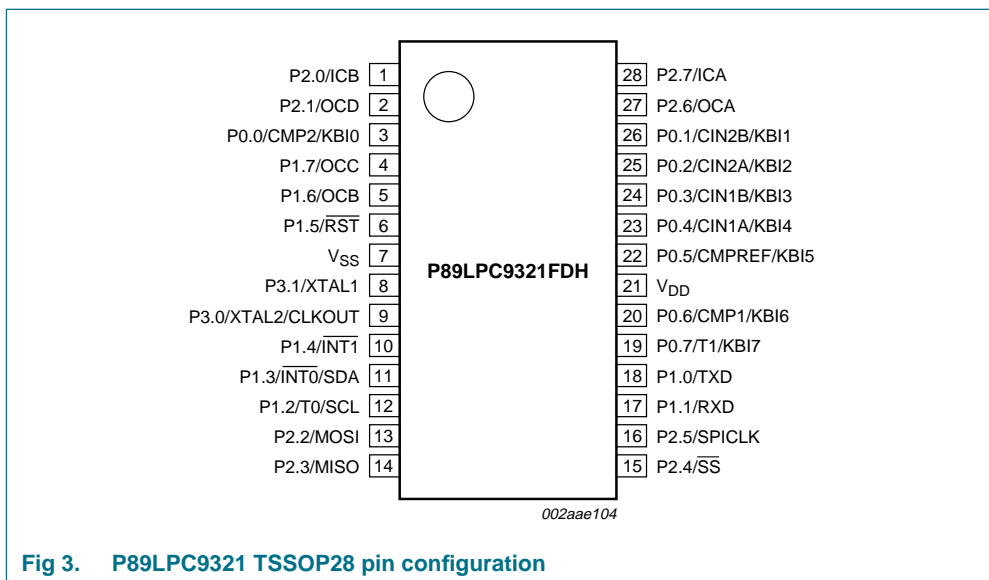
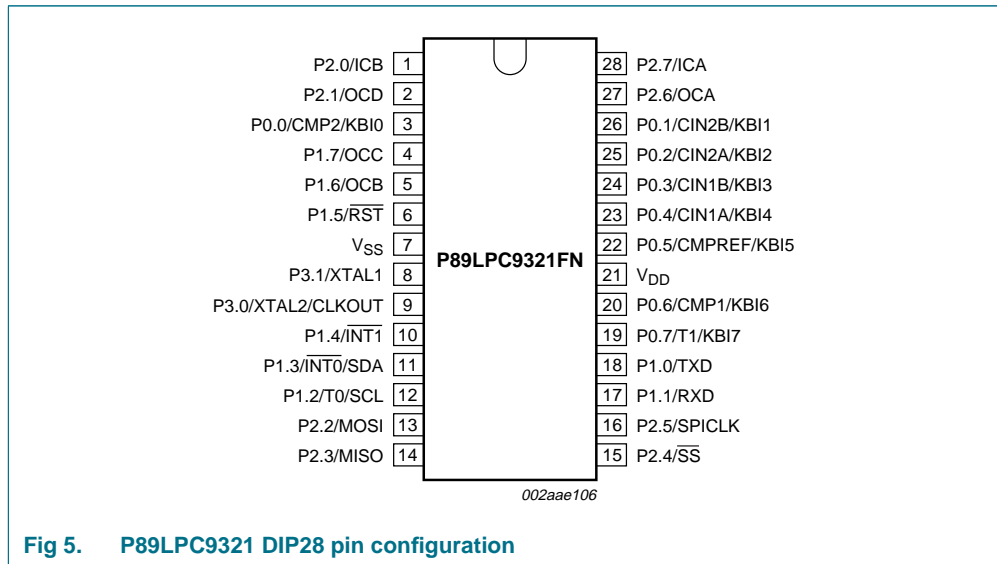


Fig 2. Functional diagram

6. Pinning information

6.1 Pinning





6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Type | Description |
|----------------------|-----|------|--|
| P0.0 to P0.7 | | I/O | <p>Port 0: Port 0 is an 8-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 10 "Static characteristics" for details.</p> <p>The Keypad Interrupt feature operates with Port 0 pins.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 0 also provides various special functions as described below:</p> |
| P0.0/CMP2/ KBI0 | 3 | I/O | P0.0 — Port 0 bit 0. |
| | | O | CMP2 — Comparator 2 output |
| | | I | KBI0 — Keyboard input 0. |
| P0.1/CIN2B/ KBI1 | 26 | I/O | P0.1 — Port 0 bit 1. |
| | | I | CIN2B — Comparator 2 positive input B. |
| | | I | KBI1 — Keyboard input 1. |
| P0.2/CIN2A/ KBI2 | 25 | I/O | P0.2 — Port 0 bit 2. |
| | | I | CIN2A — Comparator 2 positive input A. |
| | | I | KBI2 — Keyboard input 2. |
| P0.3/CIN1B/ KBI3 | 24 | I/O | P0.3 — Port 0 bit 3. High current source. |
| | | I | CIN1B — Comparator 1 positive input B. |
| | | I | KBI3 — Keyboard input 3. |
| P0.4/CIN1A/ KBI4 | 23 | I/O | P0.4 — Port 0 bit 4. High current source. |
| | | I | CIN1A — Comparator 1 positive input A. |
| | | I | KBI4 — Keyboard input 4. |
| P0.5/CMPREF/ KBI5 | 22 | I/O | P0.5 — Port 0 bit 5. High current source. |
| | | I | CMPREF — Comparator reference (negative) input. |
| | | I | KBI5 — Keyboard input 5. |

Table 3. Pin description ...continued

| Symbol | Pin | Type | Description |
|----------------|-----|-------------------------------|--|
| P0.6/CMP1/KBI6 | 20 | I/O | P0.6 — Port 0 bit 6. High current source. |
| | | O | CMP1 — Comparator 1 output. |
| | | I | KBI6 — Keyboard input 6. |
| P0.7/T1/KBI7 | 19 | I/O | P0.7 — Port 0 bit 7. High current source. |
| | | I/O | T1 — Timer/counter 1 external count input or overflow output. |
| | | I | KBI7 — Keyboard input 7. |
| P1.0 to P1.7 | | I/O, I [1] | <p>Port 1: Port 1 is an 8-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 7.16.1 "Port configurations" and Table 10 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 1 also provides various special functions as described below:</p> |
| P1.0/TXD | 18 | I/O | P1.0 — Port 1 bit 0. |
| | | O | TXD — Transmitter output for serial port. |
| P1.1/RXD | 17 | I/O | P1.1 — Port 1 bit 1. |
| | | I | RXD — Receiver input for serial port. |
| P1.2/T0/SCL | 12 | I/O | P1.2 — Port 1 bit 2 (open-drain when used as output). |
| | | I/O | T0 — Timer/counter 0 external count input or overflow output (open-drain when used as output). |
| | | I/O | SCL — I ² C-bus serial clock input/output. |
| P1.3/INT0/SDA | 11 | I/O | P1.3 — Port 1 bit 3 (open-drain when used as output). |
| | | I | INT0 — External interrupt 0 input. |
| | | I/O | SDA — I ² C-bus serial data input/output. |
| P1.4/INT1 | 10 | I/O | P1.4 — Port 1 bit 4. High current source. |
| | | I | INT1 — External interrupt 1 input. |
| P1.5/RST | 6 | I | P1.5 — Port 1 bit 5 (input only). |
| | | I | RST — External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. |
| P1.6/OCB | 5 | I/O | <p>P1.6 — Port 1 bit 6. High current source.</p> <p>OCB — Output Compare B</p> |
| P1.7/OCC | 4 | I/O | P1.7 — Port 1 bit 7. High current source. |
| | | O | OCC — Output Compare C. |
| P2.0 to P2.7 | | I/O | <p>Port 2: Port 2 is an 8-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 10 "Static characteristics" for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 2 also provides various special functions as described below:</p> |

Table 3. Pin description ...continued

| Symbol | Pin | Type | Description |
|-----------------------|-----|------|--|
| P2.0/ICB | 1 | I/O | P2.0 — Port 2 bit 0. |
| | | I | ICB — Input Capture B. |
| P2.1/OCD | 2 | I/O | P2.1 — Port 2 bit 1. |
| | | O | OCD — Output Compare D. |
| P2.2/MOSI | 13 | I/O | P2.2 — Port 2 bit 2. |
| | | I/O | MOSI — SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input. |
| P2.3/MISO | 14 | I/O | P2.3 — Port 2 bit 3. |
| | | I/O | MISO — When configured as master, this pin is input, when configured as slave, this pin is output. |
| P2.4/SS | 15 | I/O | P2.4 — Port 2 bit 4. |
| | | I/O | SS — SPI Slave select. |
| P2.5/SPICLK | 16 | I/O | P2.5 — Port 2 bit 5. |
| | | I/O | SPICLK — SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input. |
| P2.6/OCA | 27 | I/O | P2.6 — Port 2 bit 6. |
| | | O | OCA — Output Compare A. |
| P2.7/ICA | 28 | I/O | P2.7 — Port 2 bit 7. |
| | | I | ICA — Input Capture A. |
| P3.0 to P3.1 | | I/O | <p>Port 3: Port 3 is a 2-bit I/O port with a user-configurable output type. During reset Port 3 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 3 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 7.16.1 "Port configurations" and Table 10 "Static characteristics" for details.</p> <p>All pins have Schmitt trigger inputs.</p> <p>Port 3 also provides various special functions as described below:</p> |
| P3.0/XTAL2/ CLKOUT | 9 | I/O | P3.0 — Port 3 bit 0. |
| | | O | XTAL2 — Output from the oscillator amplifier (when a crystal oscillator option is selected via the flash configuration). |
| | | O | CLKOUT — CPU clock divided by 2 when enabled via SFR bit (ENCLK -TRIM.6). It can be used if the CPU clock is the internal RC oscillator, watchdog oscillator or external clock input, except when XTAL1/XTAL2 are used to generate clock source for the RTC/system timer. |
| P3.1/XTAL1 | 8 | I/O | P3.1 — Port 3 bit 1. |
| | | I | XTAL1 — Input to the oscillator circuit and internal clock generator circuits (when selected via the flash configuration). It can be a port pin if internal RC oscillator or watchdog oscillator is used as the CPU clock source, and if XTAL1/XTAL2 are not used to generate the clock for the RTC/system timer. |
| V _{SS} | 7 | I | Ground: 0 V reference. |
| V _{DD} | 21 | I | Power supply: This is the power supply voltage for normal operation as well as Idle and Power-down modes. |

[1] Input/output for P1.0 to P1.4, P1.6, P1.7. Input for P1.5.

7. Functional description

Remark: Please refer to the P89LPC9321 *User manual* for a more detailed functional description.

7.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
 - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
 - '0' **must** be written with '0', and will return a '0' when read.
 - '1' **must** be written with '1', and will return a '1' when read.

Table 4. Special function registers
** indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|----------------------|------------------------------------|-----------|-----------------------------|--------|--------|-------|-------|--------|--------|-------|-------------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| Bit address | | | E7 | E6 | E5 | E4 | E3 | E2 | E1 | E0 | | |
| ACC* | Accumulator | EOH | | | | | | | | | 00 | 0000 0000 |
| AUXR1 | Auxiliary function register | A2H | CLKLP | EBRR | ENT1 | ENT0 | SRST | 0 | - | DPS | 00 | 0000 00x0 |
| Bit address | | | F7 | F6 | F5 | F4 | F3 | F2 | F1 | F0 | | |
| B* | B register | FOH | | | | | | | | | 00 | 0000 0000 |
| BRGR0 ^[2] | Baud rate generator 0 rate low | BEH | | | | | | | | | 00 | 0000 0000 |
| BRGR1 ^[2] | Baud rate generator 0 rate high | BFH | | | | | | | | | 00 | 0000 0000 |
| BRGCON | Baud rate generator 0 control | BDH | - | - | - | - | - | - | SBRGS | BRGEN | 00 ^[2] | xxxx xx00 |
| CCCR A | Capture compare A control register | EAH | ICECA2 | ICECA1 | ICECA0 | ICESA | ICNFA | FCOA | OCMA1 | OCMA0 | 00 | 0000 0000 |
| CCCR B | Capture compare B control register | EBH | ICECB2 | ICECB1 | ICECB0 | ICESB | ICNFB | FCOB | OCMB1 | OCMB0 | 00 | 0000 0000 |
| CCCR C | Capture compare C control register | ECH | - | - | - | - | - | FCOC | OCMC1 | OCMC0 | 00 | xxxx x000 |
| CCCR D | Capture compare D control register | EDH | - | - | - | - | - | FCOD | OCMD1 | OCMD0 | 00 | xxxx x000 |
| CMP1 | Comparator 1 control register | ACH | - | - | CE1 | CP1 | CN1 | OE1 | CO1 | CMF1 | 00 ^[1] | xx00 0000 |
| CMP2 | Comparator 2 control register | ADH | - | - | CE2 | CP2 | CN2 | OE2 | CO2 | CMF2 | 00 ^[1] | xx00 0000 |
| DEECON | Data EEPROM control register | F1H | EEIF | HVERR | ECTL1 | ECTL0 | - | EWERR1 | EWERR0 | EADR8 | 08 | 00001000 |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | | |
|--------|---|--------------------|-----------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|--------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary | |
| DEEDAT | Data EEPROM data register | F2H | | | | | | | | | | 00 | 0000 0000 |
| DEEADR | Data EEPROM address register | F3H | | | | | | | | | | 00 | 0000 0000 |
| DIVM | CPU clock divide-by-M control | 95H | | | | | | | | | | 00 | 0000 0000 |
| DPTR | Data pointer (2 bytes) | | | | | | | | | | | | |
| DPH | Data pointer high | 83H | | | | | | | | | | 00 | 0000 0000 |
| DPL | Data pointer low | 82H | | | | | | | | | | 00 | 0000 0000 |
| FMADRH | Program flash address high | E7H | | | | | | | | | | 00 | 0000 0000 |
| FMADRL | Program flash address low | E6H | | | | | | | | | | 00 | 0000 0000 |
| FMCON | Program flash control (Read) | E4H | BUSY | - | - | - | HVA | HVE | SV | OI | | 70 | 0111 0000 |
| | Program flash control (Write) | E4H | FMCMD.7 | FMCMD.6 | FMCMD.5 | FMCMD.4 | FMCMD.3 | FMCMD.2 | FMCMD.1 | FMCMD.0 | | | |
| FMDATA | Program flash data | E5H | | | | | | | | | | 00 | 0000 0000 |
| I2ADR | I ² C-bus slave address register | DBH | I2ADR.6 | I2ADR.5 | I2ADR.4 | I2ADR.3 | I2ADR.2 | I2ADR.1 | I2ADR.0 | GC | | 00 | 0000 0000 |
| | | Bit address | DF | DE | DD | DC | DB | DA | D9 | D8 | | | |
| I2CON* | I ² C-bus control register | D8H | - | I2EN | STA | STO | SI | AA | - | CRSEL | | 00 | x000 00x0 |
| I2DAT | I ² C-bus data register | DAH | | | | | | | | | | | |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|--------|---|-----------|-----------------------------|--------------------|------------------|----------------------|-------------------|------------------|-------------------|------------------|-------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| I2SCLH | Serial clock generator/SCL duty cycle register high | DDH | | | | | | | | | 00 | 0000 0000 |
| I2SCLL | Serial clock generator/SCL duty cycle register low | DCH | | | | | | | | | 00 | 0000 0000 |
| I2STAT | I ² C-bus status register | D9H | STA.4 | STA.3 | STA.2 | STA.1 | STA.0 | 0 | 0 | 0 | F8 | 1111 1000 |
| ICRAH | Input capture A register high | ABH | | | | | | | | | 00 | 0000 0000 |
| ICRAL | Input capture A register low | AAH | | | | | | | | | 00 | 0000 0000 |
| ICRBH | Input capture B register high | AFH | | | | | | | | | 00 | 0000 0000 |
| ICRBL | Input capture B register low | AEH | | | | | | | | | 00 | 0000 0000 |
| | Bit address | | AF | AE | AD | AC | AB | AA | A9 | A8 | | |
| IEN0* | Interrupt enable 0 | A8H | EA | EWDRT | EBO | ES/ESR | ET1 | EX1 | ET0 | EX0 | 00 | 0000 0000 |
| | Bit address | | EF | EE | ED | EC | EB | EA | E9 | E8 | | |
| IEN1* | Interrupt enable 1 | E8H | EIEE | EST | - | ECCU | ESPI | EC | EKBI | EI2C | 00 | 00x0 0000 |
| | Bit address | | BF | BE | BD | BC | BB | BA | B9 | B8 | | |
| IP0* | Interrupt priority 0 | B8H | - | PWDRT | PBO | PS/PSR | PT1 | PX1 | PT0 | PX0 | 00 | x000 0000 |
| IP0H | Interrupt priority 0 high | B7H | - | PWDRT ^H | PBO ^H | PSH/PSR ^H | PT1 ^H | PX1 ^H | PT0 ^H | PX0 ^H | 00 | x000 0000 |
| | Bit address | | FF | FE | FD | FC | FB | FA | F9 | F8 | | |
| IP1* | Interrupt priority 1 | F8H | PIEE | PST | - | PCCU | PSPI | PC | PKBI | PI2C | 00 | 00x0 0000 |
| IP1H | Interrupt priority 1 high | F7H | PIEE ^H | PST ^H | - | PCCU ^H | PSPI ^H | PCH | PKBI ^H | PI2CH | 00 | 00x0 0000 |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|--------|--------------------------------|--------------------|-----------------------------|-----------|------------|-----------|-----------|-----------|-----------|-----------|-------------------|-----------|
| | | | MSB | | | | | | LSB | Hex | Binary | |
| KBCON | Keypad control register | 94H | - | - | - | - | - | - | PATN_SEL | KBIF | 00 ^[1] | xxxx xx00 |
| KBMASK | Keypad interrupt mask register | 86H | | | | | | | | | 00 | 0000 0000 |
| KBPATN | Keypad pattern register | 93H | | | | | | | | | FF | 1111 1111 |
| OCRAH | Output compare A register high | EFH | | | | | | | | | 00 | 0000 0000 |
| OCRAL | Output compare A register low | EEH | | | | | | | | | 00 | 0000 0000 |
| OCRBH | Output compare B register high | FBH | | | | | | | | | 00 | 0000 0000 |
| OCRBL | Output compare B register low | FAH | | | | | | | | | 00 | 0000 0000 |
| OCRCH | Output compare C register high | FDH | | | | | | | | | 00 | 0000 0000 |
| OCRCL | Output compare C register low | FCH | | | | | | | | | 00 | 0000 0000 |
| OCRDH | Output compare D register high | FFH | | | | | | | | | 00 | 0000 0000 |
| OCRDL | Output compare D register low | FEH | | | | | | | | | 00 | 0000 0000 |
| | | Bit address | 87 | 86 | 85 | 84 | 83 | 82 | 81 | 80 | | |
| P0* | Port 0 | 80H | T1/KB7 | CMP1/KB6 | CMPREF/KB5 | CIN1A/KB4 | CIN1B/KB3 | CIN2A/KB2 | CIN2B/KB1 | CMP2/KB0 | ^[1] | |
| | | Bit address | 97 | 96 | 95 | 94 | 93 | 92 | 91 | 90 | | |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|--------|------------------------------|--------------------|-----------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| P1* | Port 1 | 90H | OCC | OCB | RST | INT1 | INT0/SDA | T0/SCL | RXD | TXD | [1] | |
| | | Bit address | A7 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | | |
| P2* | Port 2 | A0H | ICA | OCA | SPICK | SS | MISO | MOSI | OCD | ICB | [1] | |
| | | Bit address | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 | | |
| P3* | Port 3 | B0H | - | - | - | - | - | - | XTAL1 | XTAL2 | [1] | |
| P0M1 | Port 0 output mode 1 | 84H | (P0M1.7) | (P0M1.6) | (P0M1.5) | (P0M1.4) | (P0M1.3) | (P0M1.2) | (P0M1.1) | (P0M1.0) | FF[1] | 1111 1111 |
| P0M2 | Port 0 output mode 2 | 85H | (P0M2.7) | (P0M2.6) | (P0M2.5) | (P0M2.4) | (P0M2.3) | (P0M2.2) | (P0M2.1) | (P0M2.0) | 00[1] | 0000 0000 |
| P1M1 | Port 1 output mode 1 | 91H | (P1M1.7) | (P1M1.6) | - | (P1M1.4) | (P1M1.3) | (P1M1.2) | (P1M1.1) | (P1M1.0) | D3[1] | 11x1 xx11 |
| P1M2 | Port 1 output mode 2 | 92H | (P1M2.7) | (P1M2.6) | - | (P1M2.4) | (P1M2.3) | (P1M2.2) | (P1M2.1) | (P1M2.0) | 00[1] | 00x0 xx00 |
| P2M1 | Port 2 output mode 1 | A4H | (P2M1.7) | (P2M1.6) | (P2M1.5) | (P2M1.4) | (P2M1.3) | (P2M1.2) | (P2M1.1) | (P2M1.0) | FF[1] | 1111 1111 |
| P2M2 | Port 2 output mode 2 | A5H | (P2M2.7) | (P2M2.6) | (P2M2.5) | (P2M2.4) | (P2M2.3) | (P2M2.2) | (P2M2.1) | (P2M2.0) | 00[1] | 0000 0000 |
| P3M1 | Port 3 output mode 1 | B1H | - | - | - | - | - | - | (P3M1.1) | (P3M1.0) | 03[1] | xxxx xx11 |
| P3M2 | Port 3 output mode 2 | B2H | - | - | - | - | - | - | (P3M2.1) | (P3M2.0) | 00[1] | xxxx xx00 |
| PCON | Power control register | 87H | SMOD1 | SMOD0 | - | BOI | GF1 | GF0 | PMOD1 | PMOD0 | 00 | 0000 0000 |
| PCONA | Power control register A | B5H | RTCPD | DEEPPD | VCPD | - | I2PD | SPPD | SPD | CCUPD | 00[1] | 0000 0000 |
| | | Bit address | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| PSW* | Program status word | D0H | CY | AC | F0 | RS1 | RS0 | OV | F1 | P | 00 | 0000 0000 |
| PT0AD | Port 0 digital input disable | F6H | - | - | PT0AD.5 | PT0AD.4 | PT0AD.3 | PT0AD.2 | PT0AD.1 | - | 00 | xx00 000x |
| RSTSRC | Reset source register | DFH | - | BOIF | BOF | POF | R_BK | R_WD | R_SF | R_EX | [3] | |
| RTCCON | RTC control | D1H | RTCF | RTCS1 | RTCS0 | - | - | - | ERTC | RTCEN | 60[1][6] | 011x xx00 |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|--------|--------------------------------------|--------------------|-----------------------------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-------------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| RTCH | RTC register high | D2H | | | | | | | | | 00 ^[6] | 0000 0000 |
| RTCL | RTC register low | D3H | | | | | | | | | 00 ^[6] | 0000 0000 |
| SADDR | Serial port address register | A9H | | | | | | | | | 00 | 0000 0000 |
| SADEN | Serial port address enable | B9H | | | | | | | | | 00 | 0000 0000 |
| SBUF | Serial Port data buffer register | 99H | | | | | | | | | xx | xxxx xxxx |
| | | Bit address | 9F | 9E | 9D | 9C | 9B | 9A | 99 | 98 | | |
| SCON* | Serial port control | 98H | SM0/FE | SM1 | SM2 | REN | TB8 | RB8 | TI | RI | 00 | 0000 0000 |
| SSTAT | Serial port extended status register | BAH | DBMOD | INTLO | CIDIS | DBISEL | FE | BR | OE | STINT | 00 | 0000 0000 |
| SP | Stack pointer | 81H | | | | | | | | | 07 | 0000 0111 |
| SPCTL | SPI control register | E2H | SSIG | SPEN | DORD | MSTR | CPOL | CPHA | SPR1 | SPR0 | 04 | 0000 0100 |
| SPSTAT | SPI status register | E1H | SPIF | WCOL | - | - | - | - | - | - | 00 | 00xx xxxx |
| SPDAT | SPI data register | E3H | | | | | | | | | 00 | 0000 0000 |
| TAMOD | Timer 0 and 1 auxiliary mode | 8FH | - | - | - | T1M2 | - | - | - | T0M2 | 00 | xxx0 xxx0 |
| | | Bit address | 8F | 8E | 8D | 8C | 8B | 8A | 89 | 88 | | |
| TCON* | Timer 0 and 1 control | 88H | TF1 | TR1 | TF0 | TR0 | IE1 | IT1 | IE0 | IT0 | 00 | 0000 0000 |
| TCR20* | CCU control register 0 | C8H | PLEEN | HLTRN | HLTEN | ALTCO | ALTAB | TDIR2 | TMOD21 | TMOD20 | 00 | 0000 0000 |
| TCR21 | CCU control register 1 | F9H | TCOU2 | - | - | - | PLLDV.3 | PLLDV.2 | PLLDV.1 | PLLDV.0 | 00 | 0xxx 0000 |

Table 4. Special function registers ...continued
 * indicates SFRs that are bit addressable.

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|--------|--------------------------------------|-----------|-----------------------------|----------|----------|----------|----------|----------|----------|----------|-------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| TH0 | Timer 0 high | 8CH | | | | | | | | | 00 | 0000 0000 |
| TH1 | Timer 1 high | 8DH | | | | | | | | | 00 | 0000 0000 |
| TH2 | CCU timer high | CDH | | | | | | | | | 00 | 0000 0000 |
| TICR2 | CCU interrupt control register | C9H | TOIE2 | TOCIE2D | TOCIE2C | TOCIE2B | TOCIE2A | - | TICIE2B | TICIE2A | 00 | 0000 0x00 |
| TIFR2 | CCU interrupt flag register | E9H | TOIF2 | TOCF2D | TOCF2C | TOCF2B | TOCF2A | - | TICF2B | TICF2A | 00 | 0000 0x00 |
| TISE2 | CCU interrupt status encode register | DEH | - | - | - | - | - | ENCINT.2 | ENCINT.1 | ENCINT.0 | 00 | xxxx x000 |
| TL0 | Timer 0 low | 8AH | | | | | | | | | 00 | 0000 0000 |
| TL1 | Timer 1 low | 8BH | | | | | | | | | 00 | 0000 0000 |
| TL2 | CCU timer low | CCH | | | | | | | | | 00 | 0000 0000 |
| TMOD | Timer 0 and 1 mode | 89H | T1GATE | T1C/T | T1M1 | T1M0 | T0GATE | T0C/T | T0M1 | T0M0 | 00 | 0000 0000 |
| TOR2H | CCU reload register high | CFH | | | | | | | | | 00 | 0000 0000 |
| TOR2L | CCU reload register low | CEH | | | | | | | | | 00 | 0000 0000 |
| TPCR2H | Prescaler control register high | CBH | - | - | - | - | - | - | TPCR2H.1 | TPCR2H.0 | 00 | xxxx xx00 |
| TPCR2L | Prescaler control register low | CAH | TPCR2L.7 | TPCR2L.6 | TPCR2L.5 | TPCR2L.4 | TPCR2L.3 | TPCR2L.2 | TPCR2L.1 | TPCR2L.0 | 00 | 0000 0000 |
| TRIM | Internal oscillator trim register | 96H | RCCLK | ENCLK | TRIM.5 | TRIM.4 | TRIM.3 | TRIM.2 | TRIM.1 | TRIM.0 | [5][6] | |
| WDCON | Watchdog control register | A7H | PRE2 | PRE1 | PRE0 | - | - | WDRUN | WDTOF | WDCLK | [4][6] | |

Table 4. Special function registers ...continued
** indicates SFRs that are bit addressable.*

| Name | Description | SFR addr. | Bit functions and addresses | | Reset value | |
|--------|-----------------|-----------|-----------------------------|-----|-------------|-----------|
| | | | MSB | LSB | Hex | Binary |
| WDL | Watchdog load | C1H | | | FF | 1111 1111 |
| WFEED1 | Watchdog feed 1 | C2H | | | | |
| WFEED2 | Watchdog feed 2 | C3H | | | | |

- [1] All ports are in input only (high-impedance) state after power-up.
- [2] BRGR1 and BRGR0 must only be written if BRGEN in BRGCON SFR is logic 0. If any are written while BRGEN = 1, the result is unpredictable.
- [3] The RSTSRC register reflects the cause of the P89LPC9321 reset except BOIF bit. Upon a power-up reset, all reset source flags are cleared except POF and BOF; the power-on reset value is x011 0000.
- [4] After reset, the value is 1110 01x1, i.e., PRE2 to PRE0 are all logic 1, WDRUN = 1 and WDCLK = 1. WDTDF bit is logic 1 after watchdog reset and is logic 0 after power-on reset. Other resets will not affect WDTDF.
- [5] On power-on reset and watchdog reset, the TRIM SFR is initialized with a factory preprogrammed value. Other resets will not cause initialization of the TRIM register.
- [6] The only reset sources that affect these SFRs are power-on reset and watchdog reset.

Table 5. Extended special function registers^[1]

| Name | Description | SFR addr. | Bit functions and addresses | | | | | | | | Reset value | |
|---------------|------------------------------------|-----------|-----------------------------|----------|----------|----------|---------|---------|---------|---------|-------------|-----------|
| | | | MSB | | | | LSB | | | | Hex | Binary |
| BODCFG | BOD configuration register | FFC8H | - | - | - | - | - | - | BOICFG1 | BOICFG0 | [2] | |
| CLKCON | CLOCK Control register | FFDEH | CLKOK | - | - | XTALWD | CLKDBL | FOSC2 | FOSC1 | FOSC0 | [3] | 1000 0100 |
| PGACON1 | PGA1 control register | FFE1H | ENPGA1 | PGASEL1 | PGASEL1 | PGATRIM | - | - | PGAG11 | PGAG10 | 00 | 0000 0000 |
| PGACON1B | PGA1 control register B | FFE4H | - | - | - | - | - | - | PGAENO | FF1 | 00 | 0000 0000 |
| PGA1TRIM8X16X | PGA1 trim register | FFE3H | 16XTRIM3 | 16XTRIM2 | 16XTRIM1 | 16XTRIM0 | 8XTRIM3 | 8XTRIM2 | 8XTRIM1 | 8XTRIM0 | [4] | |
| PGA1TRIM2X4X | PGA1 trim register | FFE2H | 4XTRIM3 | 4XTRIM2 | 4XTRIM1 | 4XTRIM0 | 2XTRIM3 | 2XTRIM2 | 2XTRIM1 | 2XTRIM0 | [4] | |
| RTCDATH | Real-time clock data register high | FFBFH | | | | | | | | | 00 | 0000 0000 |
| RTCDATL | Real-time clock data register low | FFBEH | | | | | | | | | 00 | 0000 0000 |

- [1] Extended SFRs are physically located on-chip but logically located in external data memory address space (XDATA). The MOVX A, @DPTR and MOVX @DPTR, A instructions are used to access these extended SFRs.
- [2] The BOICFG1/0 will be copied from UCFG1.5 and UCFG1.3 when power-on reset.
- [3] CLKCON register reset value comes from UCFG1 and UCFG2. The reset value of CLKCON.2 to CLKCON.0 come from UCFG1.2 to UCFG1.0 and reset value of CLKDBL bit comes from UCFG2.7.
- [4] On power-on reset and watchdog reset, the PGAxTRIM8X16X and PGAxTRIM2X4X registers are initialized with a factory preprogrammed value. Other resets will not cause initialization.

7.2 Enhanced CPU

The P89LPC9321 uses an enhanced 80C51 CPU which runs at six times the speed of standard 80C51 devices. A machine cycle consists of two CPU clock cycles, and most instructions execute in one or two machine cycles.

7.3 Clocks

7.3.1 Clock definitions

The P89LPC9321 device has several internal clocks as defined below:

OSCCLK — Input to the DIVM clock divider. OSCCLK is selected from one of four clock sources (see [Figure 6](#)) and can also be optionally divided to a slower frequency (see [Section 7.11 “CCLK modification: DIVM register”](#)).

Remark: f_{osc} is defined as the OSCCLK frequency.

CCLK — CPU clock; output of the clock divider. There are two CCLK cycles per machine cycle, and most instructions are executed in one to two machine cycles (two or four CCLK cycles).

RCCLK — The internal 7.373 MHz RC oscillator output. The clock doubler option, when enabled, provides an output frequency of 14.746 MHz.

PCLK — Clock for the various peripheral devices and is $CCLK/2$.

7.3.2 CPU clock (OSCCLK)

The P89LPC9321 provides several user-selectable oscillator options in generating the CPU clock. This allows optimization for a range of needs from high precision to lowest possible cost. These options are configured when the flash is programmed and include an on-chip watchdog oscillator, an on-chip RC oscillator, an oscillator using an external crystal, or an external clock source.

7.4 External crystal oscillator option

The external crystal oscillator can be optimized for low, medium, or high frequency crystals covering a range from 20 kHz to 18 MHz. It can be the clock source of OSCCLK, RTC and WDT.

7.4.1 Low speed oscillator option

This option supports an external crystal in the range of 20 kHz to 100 kHz. Ceramic resonators are also supported in this configuration.

7.4.2 Medium speed oscillator option

This option supports an external crystal in the range of 100 kHz to 4 MHz. Ceramic resonators are also supported in this configuration.

7.4.3 High speed oscillator option

This option supports an external crystal in the range of 4 MHz to 18 MHz. Ceramic resonators are also supported in this configuration.

7.5 Clock output

The P89LPC9321 supports a user-selectable clock output function on the XTAL2/CLKOUT pin when crystal oscillator is not being used. This condition occurs if another clock source has been selected (on-chip RC oscillator, watchdog oscillator, external clock input on XTAL1) and if the RTC and WDT are not using the crystal oscillator as their clock source. This allows external devices to synchronize to the P89LPC9321. This output is enabled by the ENCLK bit in the TRIM register.

The frequency of this clock output is $\frac{1}{2}$ that of the CCLK. If the clock output is not needed in Idle mode, it may be turned off prior to entering Idle, saving additional power.

7.6 On-chip RC oscillator option

The P89LPC9321 has a 6-bit TRIM register that can be used to tune the frequency of the RC oscillator. During reset, the TRIM value is initialized to a factory preprogrammed value to adjust the oscillator frequency to $7.373 \text{ MHz} \pm 1\%$ at room temperature. End-user applications can write to the TRIM register to adjust the on-chip RC oscillator to other frequencies. When the clock doubler option is enabled ($\text{UCFG2.7} = 1$), the output frequency is 14.746 MHz . If CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to reduce power consumption. On reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower. When clock doubler option is enabled, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.7 Watchdog oscillator option

The watchdog has a separate oscillator which has a frequency of 400 kHz, calibrated to $\pm 5\%$ at room temperature. This oscillator can be used to save power when a high clock frequency is not needed.

7.8 External clock input option

In this configuration, the processor clock is derived from an external source driving the P3.1/XTAL1 pin. The rate may be from 0 Hz up to 18 MHz. The P3.0/XTAL2 pin may be used as a standard port pin or a clock output. When using an oscillator frequency above 12 MHz, BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are required to hold the device in reset at power-up until V_{DD} has reached its specified level.

7.9 Clock sources switch on the fly

P89LPC9321 can implement clock source switch in any sources of watchdog oscillator, 7 MHz/14 MHz IRC oscillator, external clock source (external crystal or external clock input) during code is running. CLKOK bit in CLKCON register is used to indicate the clock switch status. CLKOK is cleared when starting clock source switch and set when completed. Notice that when CLKOK is '0', writing to CLKCON register is not allowed.

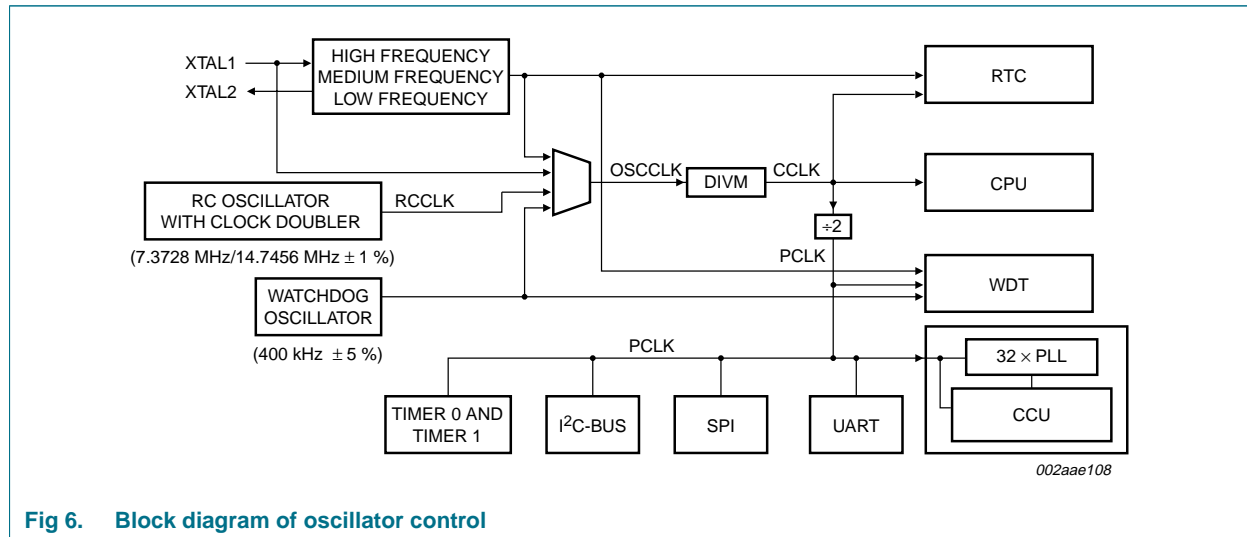


Fig 6. Block diagram of oscillator control

7.10 CCLK wake-up delay

The P89LPC9321 has an internal wake-up timer that delays the clock until it stabilizes depending on the clock source used. If the clock source is any of the three crystal selections (low, medium and high frequencies) the delay is 1024 OSCCLK cycles plus 60 μ s to 100 μ s. If the clock source is the internal RC oscillator, the delay is 200 μ s to 300 μ s. If the clock source is watchdog oscillator or external clock, the delay is 32 OSCCLK cycles.

7.11 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

7.12 Low power select

The P89LPC9321 is designed to run at 18 MHz (CCLK) maximum. However, if CCLK is 8 MHz or slower, the CLKLP SFR bit (AUXR1.7) can be set to logic 1 to lower the power consumption further. On any reset, CLKLP is logic 0 allowing highest performance access. This bit can then be set in software if CCLK is running at 8 MHz or slower.

7.13 Memory organization

The various P89LPC9321 memory spaces are as follows:

- DATA
128 bytes of internal data memory space (00H:7FH) accessed via direct or indirect addressing, using instructions other than MOVX and MOVC. All or part of the Stack may be in this area.
- IDATA
Indirect Data. 256 bytes of internal data memory space (00H:FFH) accessed via indirect addressing using instructions other than MOVX and MOVC. All or part of the Stack may be in this area. This area includes the DATA area and the 128 bytes immediately above it.
- SFR
Special Function Registers. Selected CPU registers and peripheral control and status registers, accessible only via direct addressing.
- XDATA
'External' Data or Auxiliary RAM. Duplicates the classic 80C51 64 kB memory space addressed via the MOVX instruction using the DPTR, R0, or R1. All or part of this space could be implemented on-chip. The P89LPC9321 has 512 bytes of on-chip XDATA memory, plus extended SFRs located in XDATA.
- CODE
64 kB of Code memory space, accessed as part of program execution and via the MOVC instruction. The P89LPC9321 has 8 kB of on-chip Code memory.

The P89LPC9321 also has 512 bytes of on-chip data EEPROM that is accessed via SFRs (see [Section 7.14](#)).

7.14 Data RAM arrangement

The 768 bytes of on-chip RAM are organized as shown in [Table 6](#).

Table 6. On-chip data memory usages

| Type | Data RAM | Size (bytes) |
|-------|---|--------------|
| DATA | Memory that can be addressed directly and indirectly | 128 |
| IDATA | Memory that can be addressed indirectly | 256 |
| XDATA | Auxiliary ('External Data') on-chip memory that is accessed using the MOVX instructions | 512 |

7.15 Interrupts

The P89LPC9321 uses a four priority level interrupt structure. This allows great flexibility in controlling the handling of the many interrupt sources. The P89LPC9321 supports 15 interrupt sources: external interrupts 0 and 1, timers 0 and 1, serial port TX, serial port RX, combined serial port RX/TX, brownout detect, watchdog/RTC, I²C-bus, keyboard, comparators 1 and 2, SPI, CCU, data EEPROM write completion.

Each interrupt source can be individually enabled or disabled by setting or clearing a bit in the interrupt enable registers IEN0 or IEN1. The IEN0 register also contains a global disable bit, EA, which disables all interrupts.

Each interrupt source can be individually programmed to one of four priority levels by setting or clearing bits in the interrupt priority registers IP0, IP0H, IP1 and IP1H. An interrupt service routine in progress can be interrupted by a higher priority interrupt, but not by another interrupt of the same or lower priority. The highest priority interrupt service cannot be interrupted by any other interrupt source. If two requests of different priority levels are pending at the start of an instruction, the request of higher priority level is serviced.

If requests of the same priority level are pending at the start of an instruction, an internal polling sequence determines which request is serviced. This is called the arbitration ranking. Note that the arbitration ranking is only used to resolve pending requests of the same priority level.

7.15.1 External interrupt inputs

The P89LPC9321 has two external interrupt inputs as well as the Keypad Interrupt function. The two interrupt inputs are identical to those present on the standard 80C51 microcontrollers.

These external interrupts can be programmed to be level-triggered or edge-triggered by setting or clearing bit IT1 or IT0 in Register TCON.

In edge-triggered mode, if successive samples of the $\overline{\text{INTn}}$ pin show a HIGH in one cycle and a LOW in the next cycle, the interrupt request flag IEn in TCON is set, causing an interrupt request.

If an external interrupt is enabled when the P89LPC9321 is put into Power-down or Idle mode, the interrupt will cause the processor to wake-up and resume operation. Refer to [Section 7.18 "Power reduction modes"](#) for details.

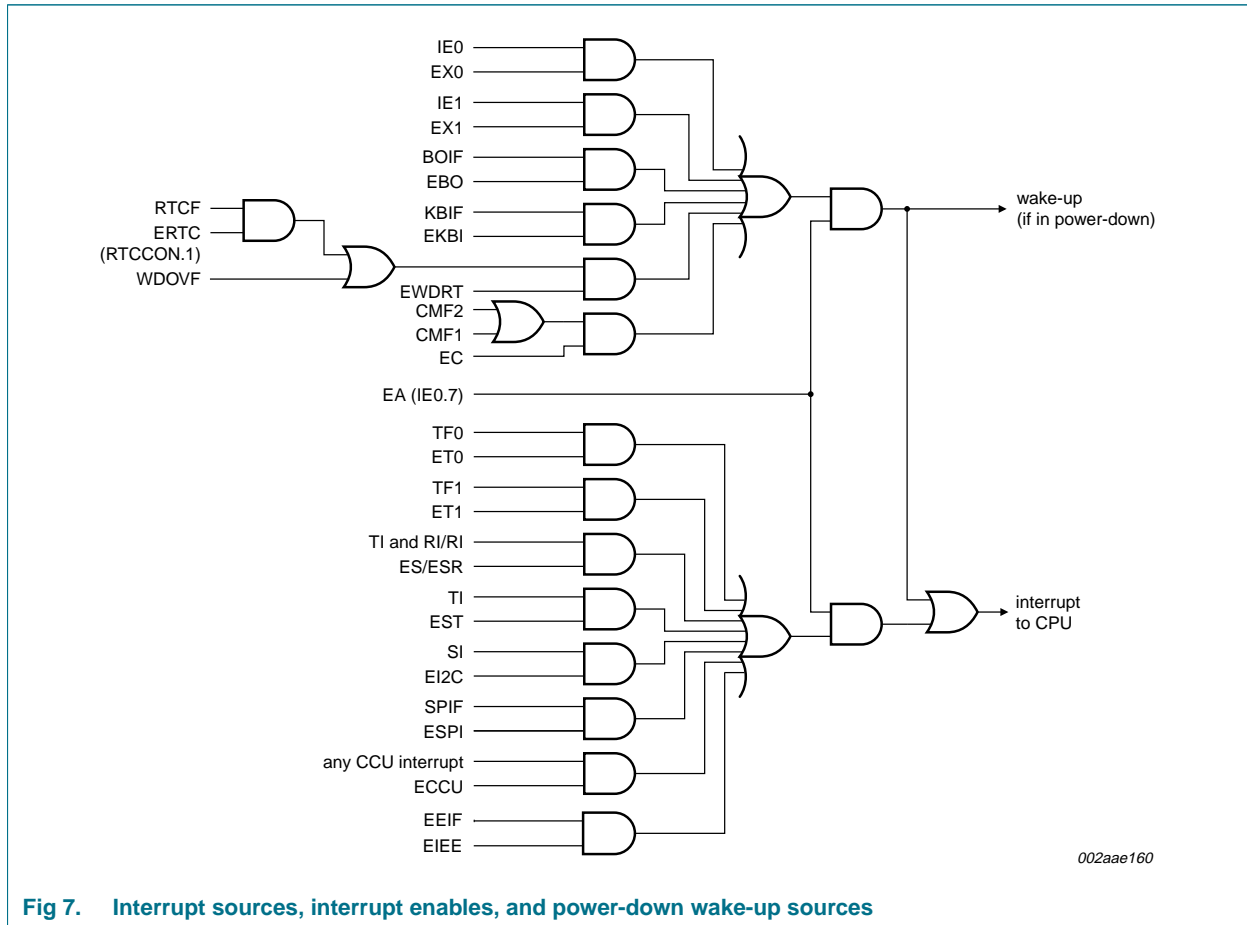


Fig 7. Interrupt sources, interrupt enables, and power-down wake-up sources

7.16 I/O ports

The P89LPC9321 has four I/O ports: Port 0, Port 1, Port 2 and Port 3. Ports 0, 1, and 2 are 8-bit ports, and Port 3 is a 2-bit port. The exact number of I/O pins available depends upon the clock and reset options chosen, as shown in [Table 7](#).

Table 7. Number of I/O pins available

| Clock source | Reset option | Number of I/O pins (28-pin package) |
|--|--|-------------------------------------|
| On-chip oscillator or watchdog oscillator | No external reset (except during power-up) | 26 |
| | External $\overline{\text{RST}}$ pin supported | 25 |
| External clock input | No external reset (except during power-up) | 25 |
| | External $\overline{\text{RST}}$ pin supported | 24 |
| Low/medium/high speed oscillator (external crystal or resonator) | No external reset (except during power-up) | 24 |
| | External $\overline{\text{RST}}$ pin supported | 23 |

7.16.1 Port configurations

All but three I/O port pins on the P89LPC9321 may be configured by software to one of four types on a bit-by-bit basis. These are: quasi-bidirectional (standard 80C51 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output type for each port pin.

1. P1.5 ($\overline{\text{RST}}$) can only be an input and cannot be configured.
2. P1.2 (SCL/T0) and P1.3 (SDA/ $\overline{\text{INT0}}$) may only be configured to be either input-only or open-drain.

7.16.1.1 Quasi-bidirectional output configuration

Quasi-bidirectional output type can be used as both an input and output without the need to reconfigure the port. This is possible because when the port outputs a logic HIGH, it is weakly driven, allowing an external device to pull the pin LOW. When the pin is driven LOW, it is driven strongly and able to sink a fairly large current. These features are somewhat similar to an open-drain output except that there are three pull-up transistors in the quasi-bidirectional output that serve different purposes.

The P89LPC9321 is a 3 V device, but the pins are 5 V-tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD} , causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD} .

An open-drain port pin has a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt trigger input that also has a glitch suppression circuit.

7.16.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit. The P89LPC9321 device has high current source on eight pins in push-pull mode. See [Table 9 “Limiting values”](#).

7.16.2 Port 0 analog functions

The P89LPC9321 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register, bits 1:5. On any reset, PT0AD[1:5] defaults to logic 0s to enable digital functions.

7.16.3 Additional port features

After power-up, all pins are in Input-Only mode. **Please note that this is different from the LPC76x series of devices.**

- After power-up, all I/O pins except P1.5, may be configured by software.
- Pin P1.5 is input only. Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC9321 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to [Table 10 “Static characteristics”](#) for detailed specifications.

All ports pins that can function as an output have slew rate controlled outputs to limit noise generated by quickly switching output signals. The slew rate is factory-set to approximately 10 ns rise and fall times.

7.17 Power monitoring functions

The P89LPC9321 incorporates power monitoring functions designed to prevent incorrect operation during initial power-up and power loss or reduction during operation. This is accomplished with two hardware functions: Power-on detect and brownout detect.

7.17.1 Brownout detection

The brownout detect function determines if the power supply voltage drops below a certain level. Enhanced brownout detection has 3 independent functions: BOD reset, BOD interrupt and BOD EEPROM/FLASH.

BOD reset is always on except in total power-down mode. It could not be disabled in software. BOD interrupt may be enabled or disabled in software. BOD EEPROM/FLASH is always on, except in power-down modes and could not be disabled in software.

BOD reset and BOD interrupt, each has four trip voltage levels. BOE1 bit (UCFG1.5) and BOE0 bit (UCFG1.3) are used as trip point configuration bits of BOD reset. BOICFG1 bit and BOICFG0 bit in register BODCFG are used as trip point configuration bits of BOD interrupt. BOD reset voltage should be lower than BOD interrupt trip point. BOD EEPROM/FLASH is used for flash/Data EEPROM programming/erase protection and has only 1 trip voltage of 2.4 V. Please refer to P89LPC9321 *User manual* for detail configurations.

If brownout detection is enabled the brownout condition occurs when V_{DD} falls below the brownout trip voltage and is negated when V_{DD} rises above the brownout trip voltage.

For correct activation of brownout detect, the V_{DD} rise and fall times must be observed. Please see [Table 10 "Static characteristics"](#) for specifications.

7.17.2 Power-on detection

The Power-on detect has a function similar to the brownout detect, but is designed to work as power comes up initially, before the power supply voltage reaches a level where brownout detect can work. The POF flag in the RSTSRC register is set to indicate an initial power-up condition. The POF flag will remain set until cleared by software.

7.18 Power reduction modes

The P89LPC9321 supports three different power reduction modes. These modes are Idle mode, Power-down mode, and total Power-down mode.

7.18.1 Idle mode

Idle mode leaves peripherals running in order to allow them to activate the processor when an interrupt is generated. Any enabled interrupt source or reset may terminate Idle mode.

7.18.2 Power-down mode

The Power-down mode stops the oscillator in order to minimize power consumption. The P89LPC9321 exits Power-down mode via any reset, or certain interrupts. In Power-down mode, the power supply voltage may be reduced to the data retention supply voltage V_{DDR} . This retains the RAM contents at the point where Power-down mode was entered. SFR contents are not guaranteed after V_{DD} has been lowered to V_{DDR} , therefore it is highly recommended to wake-up the processor via reset in this case. V_{DD} must be raised to within the operating range before the Power-down mode is exited.

Some chip functions continue to operate and draw power during Power-down mode, increasing the total power used during power-down. These include: Brownout detect, watchdog timer, comparators (note that comparators can be powered down separately), and RTC/system timer. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock and the RTC is enabled.

7.18.3 Total Power-down mode

This is the same as Power-down mode except that the brownout detection circuitry and the voltage comparators are also disabled to conserve additional power. The internal RC oscillator is disabled unless both the RC oscillator has been selected as the system clock **and** the RTC is enabled. If the internal RC oscillator is used to clock the RTC during power-down, there will be high power consumption. Please use an external low frequency clock to achieve low power with the RTC running during power-down.

7.19 Reset

The P1.5/ $\overline{\text{RST}}$ pin can function as either a LOW-active reset input or as a digital input, P1.5. The Reset Pin Enable (RPE) bit in UCFG1, when set to logic 1, enables the external reset input function on P1.5. When cleared, P1.5 may be used as an input pin.

Remark: During a power-up sequence, the RPE selection is overridden and this pin always functions as a reset input. **An external circuit connected to this pin should not hold this pin LOW during a power-on sequence as this will keep the device in reset.** After power-up this pin will function as defined by the RPE bit. Only a power-up reset will temporarily override the selection defined by RPE bit. Other sources of reset will not override the RPE bit.

Note: During a power cycle, V_{DD} must fall below V_{POR} before power is reapplied, in order to ensure a power-on reset (see [Table 10 "Static characteristics"](#)).

Reset can be triggered from the following sources:

- External reset pin (during power-up or if user configured via UCFG1)
- Power-on detect
- Brownout detect
- Watchdog timer
- Software reset
- UART break character detect reset

For every reset source, there is a flag in the Reset Register, RSTSRC. The user can read this register to determine the most recent reset source. These flag bits can be cleared in software by writing a logic 0 to the corresponding bit. More than one flag bit may be set:

- During a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- A Watchdog reset is similar to a power-on reset, both POF and BOF are set but the other flag bits are cleared.
- For any other reset, previously set flag bits that have not been cleared will remain set.

7.19.1 Reset vector

Following reset, the P89LPC9321 will fetch instructions from either address 0000H or the Boot address. The Boot address is formed by using the boot vector as the high byte of the address and the low byte of the address = 00H.

The boot address will be used if a UART break reset occurs, or the non-volatile boot status bit (BOOTSTAT.0) = 1, or the device is forced into ISP mode during power-on (see P89LPC9321 *User manual*). Otherwise, instructions will be fetched from address 0000H.

7.20 Timers/counters 0 and 1

The P89LPC9321 has two general purpose counter/timers which are upward compatible with the standard 80C51 Timer 0 and Timer 1. Both can be configured to operate either as timers or event counters. An option to automatically toggle the T0 and/or T1 pins upon timer overflow has been added.

In the 'Timer' function, the register is incremented every machine cycle.

In the 'Counter' function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 and Timer 1 have five operating modes (Modes 0, 1, 2, 3 and 6). Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

7.20.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

7.20.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

7.20.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

7.20.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

7.20.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

7.20.6 Timer overflow toggle output

Timers 0 and 1 can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

7.21 RTC/system timer

The P89LPC9321 has a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down counter comprised of a 7-bit prescaler and a 16-bit loadable down counter. When it reaches all logic 0s, the counter will be reloaded again and the RTCF flag will be set. The clock source for this counter can be either the CPU clock (CCLK) or the XTAL oscillator. Only power-on reset and watchdog reset will reset the RTC and its associated SFRs to the default state.

The 16-bit loadable counter portion of the RTC is readable by reading the RTCDATL and RTCDATH registers.

7.22 CCU

This unit features:

- A 16-bit timer with 16-bit reload on overflow.
- Selectable clock, with prescaler to divide clock source by any integral number between 1 and 1024.
- Four compare/PWM outputs with selectable polarity
- Symmetrical/asymmetrical PWM selection
- Two capture inputs with event counter and digital noise rejection filter
- Seven interrupts with common interrupt vector (one overflow, two capture, four compare)
- Safe 16-bit read/write via shadow registers.

7.22.1 CCU clock

The CCU runs on the CCUCLK, which is either PCLK in basic timer mode, or the output of a PLL. The PLL is designed to use a clock source between 0.5 MHz to 1 MHz that is multiplied by 32 to produce a CCUCLK between 16 MHz and 32 MHz in PWM mode (asymmetrical or symmetrical). The PLL contains a 4-bit divider to help divide PCLK into a frequency between 0.5 MHz and 1 MHz.

7.22.2 CCUCLK prescaling

This CCUCLK can further be divided down by a prescaler. The prescaler is implemented as a 10-bit free-running counter with programmable reload at overflow.

7.22.3 Basic timer operation

The timer is a free-running up/down counter with a direction control bit. If the timer counting direction is changed while the counter is running, the count sequence will be reversed. The timer can be written or read at any time.

When a reload occurs, the CCU Timer Overflow Interrupt Flag will be set, and an interrupt generated if enabled. The 16-bit CCU timer may also be used as an 8-bit up/down timer.

7.22.4 Output compare

There are four output compare channels: A, B, C and D. Each output compare channel needs to be enabled in order to operate and the user will have to set the associated I/O pin to the desired output mode to connect the pin. When the contents of the timer matches that of a capture compare control register, the Timer Output Compare Interrupt Flag (TOCFx) becomes set. An interrupt will occur if enabled.

7.22.5 Input capture

Input capture is always enabled. Each time a capture event occurs on one of the two input capture pins, the contents of the timer is transferred to the corresponding 16-bit input capture register. The capture event can be programmed to be either rising or falling edge triggered. A simple noise filter can be enabled on the input capture by enabling the Input Capture Noise Filter bit. If set, the capture logic needs to see four consecutive samples of the same value in order to recognize an edge as a capture event. An event counter can be set to delay a capture by a number of capture events.

7.22.6 PWM operation

PWM operation has two main modes, symmetrical and asymmetrical.

In asymmetrical PWM operation the CCU timer operates in down-counting mode regardless of the direction control bit.

In symmetrical mode, the timer counts up/down alternately. The main difference from basic timer operation is the operation of the compare module, which in PWM mode is used for PWM waveform generation.

As with basic timer operation, when the PWM (compare) pins are connected to the compare logic, their logic state remains unchanged. However, since bit FCO is used to hold the halt value, only a compare event can change the state of the pin.

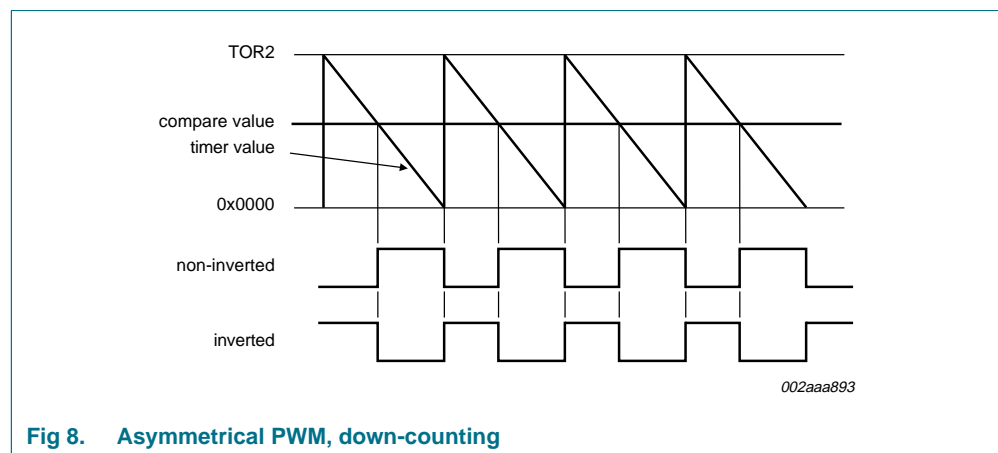


Fig 8. Asymmetrical PWM, down-counting

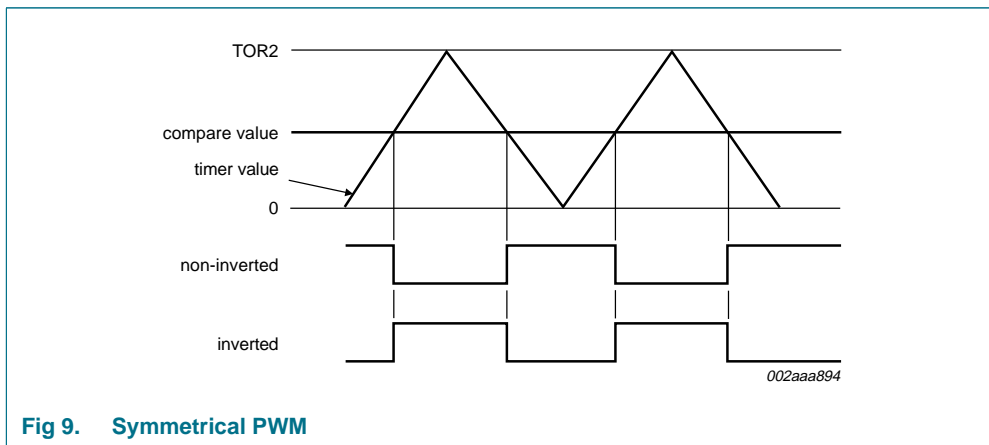


Fig 9. Symmetrical PWM

7.22.7 Alternating output mode

In asymmetrical mode, the user can set up PWM channels A/B and C/D as alternating pairs for bridge drive control. In this mode the output of these PWM channels are alternately gated on every counter cycle.

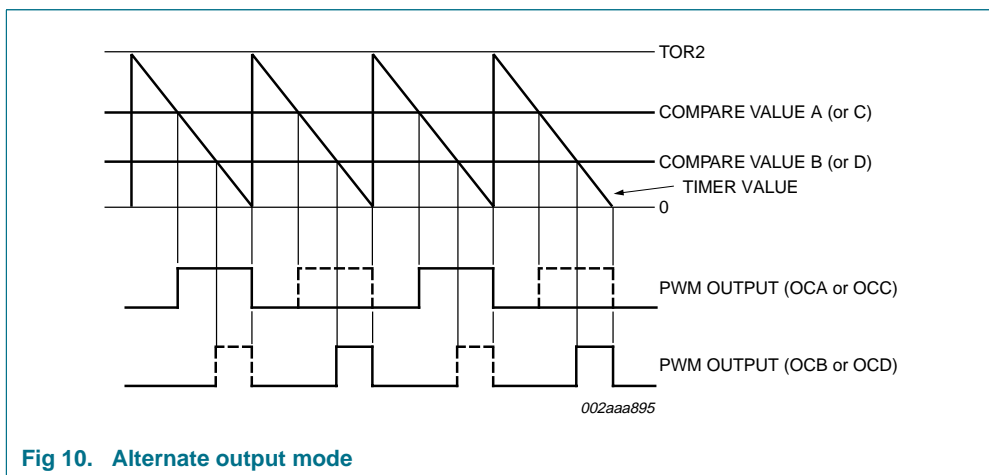


Fig 10. Alternate output mode

7.22.8 PLL operation

The PWM module features a Phase Locked Loop that can be used to generate a CCUCLK frequency between 16 MHz and 32 MHz. At this frequency the PWM module provides ultrasonic PWM frequency with 10-bit resolution provided that the crystal frequency is 1 MHz or higher. The PLL is fed an input signal from 0.5 MHz to 1 MHz and generates an output signal of 32 times the input frequency. This signal is used to clock the timer. The user will have to set a divider that scales PCLK by a factor from 1 to 16. This divider is found in the SFR register TCR21. The PLL frequency can be expressed as shown in [Equation 1](#):

$$\text{PLL frequency} = \frac{\text{PCLK}}{(N + 1)} \tag{1}$$

Where: N is the value of PLLDV3:0.

Since N ranges from 0 to 15, the CCLK frequency can be in the range of PCLK to PCLK16.

7.22.9 CCU interrupts

There are seven interrupt sources on the CCU which share a common interrupt vector.

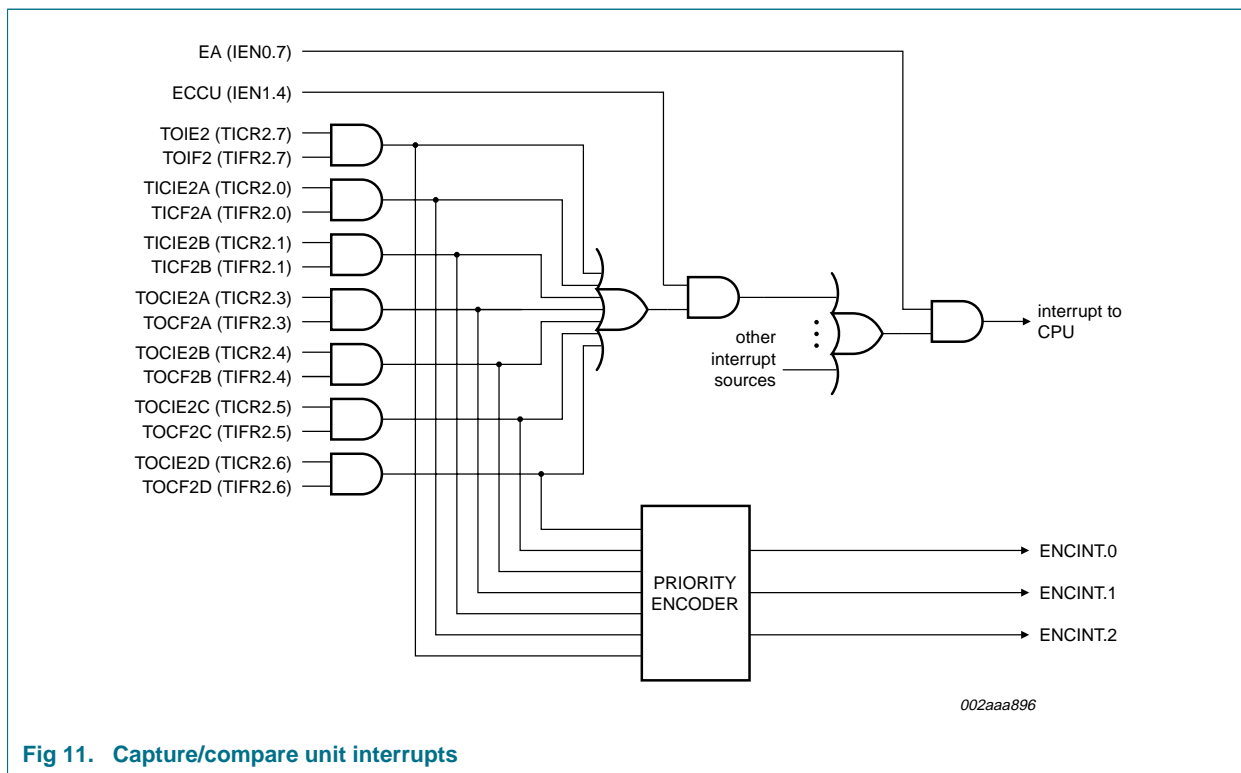


Fig 11. Capture/compare unit interrupts

7.23 UART

The P89LPC9321 has an enhanced UART that is compatible with the conventional 80C51 UART except that Timer 2 overflow cannot be used as a baud rate source. The P89LPC9321 does include an independent baud rate generator. The baud rate can be selected from the oscillator (divided by a constant), Timer 1 overflow, or the independent baud rate generator. In addition to the baud rate generation, enhancements over the standard 80C51 UART include Framing Error detection, automatic address recognition, selectable double buffering and several interrupt options. The UART can be operated in four modes: shift register, 8-bit UART, 9-bit UART, and CPU clock/32 or CPU clock/16.

7.23.1 Mode 0

Serial data enters and exits through RXD. TXD outputs the shift clock. 8 bits are transmitted or received, LSB first. The baud rate is fixed at $1/16$ of the CPU clock frequency.

7.23.2 Mode 1

10 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), and a stop bit (logic 1). When data is received, the stop bit is stored in RB8 in special function register SCON. The baud rate is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in [Section 7.23.5 “Baud rate generator and selection”](#)).

7.23.3 Mode 2

11 bits are transmitted (through TXD) or received (through RXD): start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). When data is transmitted, the 9th data bit (TB8 in SCON) can be assigned the value of logic 0 or logic 1. Or, for example, the parity bit (P, in the PSW) could be moved into TB8. When data is received, the 9th data bit goes into RB8 in special function register SCON, while the stop bit is not saved. The baud rate is programmable to either $\frac{1}{16}$ or $\frac{1}{32}$ of the CPU clock frequency, as determined by the SMOD1 bit in PCON.

7.23.4 Mode 3

11 bits are transmitted (through TXD) or received (through RXD): a start bit (logic 0), 8 data bits (LSB first), a programmable 9th data bit, and a stop bit (logic 1). In fact, Mode 3 is the same as Mode 2 in all respects except baud rate. The baud rate in Mode 3 is variable and is determined by the Timer 1 overflow rate or the baud rate generator (described in [Section 7.23.5 “Baud rate generator and selection”](#)).

7.23.5 Baud rate generator and selection

The P89LPC9321 enhanced UART has an independent baud rate generator. The baud rate is determined by a baud-rate preprogrammed into the BRGR1 and BRGR0 SFRs which together form a 16-bit baud rate divisor value that works in a similar manner as Timer 1 but is much more accurate. If the baud rate generator is used, Timer 1 can be used for other timing functions.

The UART can use either Timer 1 or the baud rate generator output (see [Figure 12](#)). Note that Timer T1 is further divided by 2 if the SMOD1 bit (PCON.7) is cleared. The independent baud rate generators use OSCCLK.

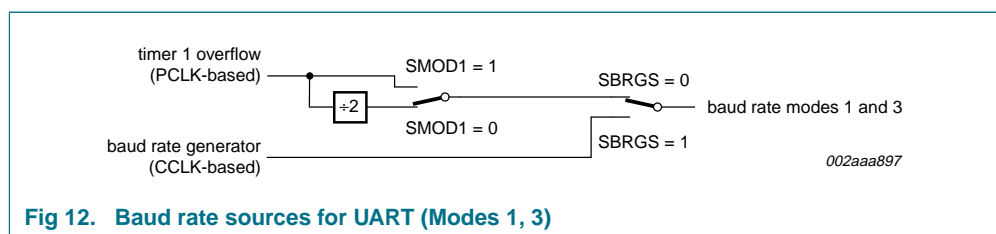


Fig 12. Baud rate sources for UART (Modes 1, 3)

7.23.6 Framing error

Framing error is reported in the status register (SSTAT). In addition, if SMOD0 (PCON.6) is logic 1, framing errors can be made available in SCON.7 respectively. If SMOD0 is logic 0, SCON.7 is SM0. It is recommended that SM0 and SM1 (SCON.7:6) are set up when SMOD0 is logic 0.

7.23.7 Break detect

Break detect is reported in the status register (SSTAT). A break is detected when 11 consecutive bits are sensed LOW. The break detect can be used to reset the device and force the device into ISP mode.

7.23.8 Double buffering

The UART has a transmit double buffer that allows buffering of the next character to be written to SnBUF while the first character is being transmitted. Double buffering allows transmission of a string of characters with only one stop bit between any two characters, as long as the next character is written between the start bit and the stop bit of the previous character.

Double buffering can be disabled. If disabled (DBMOD, i.e., SSTAT.7 = 0), the UART is compatible with the conventional 80C51 UART. If enabled, the UART allows writing to SBUF while the previous data is being shifted out. Double buffering is only allowed in Modes 1, 2 and 3. When operated in Mode 0, double buffering must be disabled (DBMOD = 0).

7.23.9 Transmit interrupts with double buffering enabled (modes 1, 2 and 3)

Unlike the conventional UART, in double buffering mode, the TI interrupt is generated when the double buffer is ready to receive new data.

7.23.10 The 9th bit (bit 8) in double buffering (modes 1, 2 and 3)

If double buffering is disabled TB8 can be written before or after SBUF is written, as long as TB8 is updated some time before that bit is shifted out. TB8 must not be changed until the bit is shifted out, as indicated by the TI interrupt.

If double buffering is enabled, TB **must** be updated before SBUF is written, as TB8 will be double-buffered together with SBUF data.

7.24 I²C-bus serial interface

The I²C-bus uses two wires (SDA and SCL) to transfer information between devices connected to the bus, and it has the following features:

- Bidirectional data transfer between masters and slaves
- Multi master bus (no central master)
- Arbitration between simultaneously transmitting masters without corruption of serial data on the bus
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer
- The I²C-bus may be used for test and diagnostic purposes.

A typical I²C-bus configuration is shown in [Figure 13](#). The P89LPC9321 device provides a byte-oriented I²C-bus interface that supports data transfers up to 400 kHz.

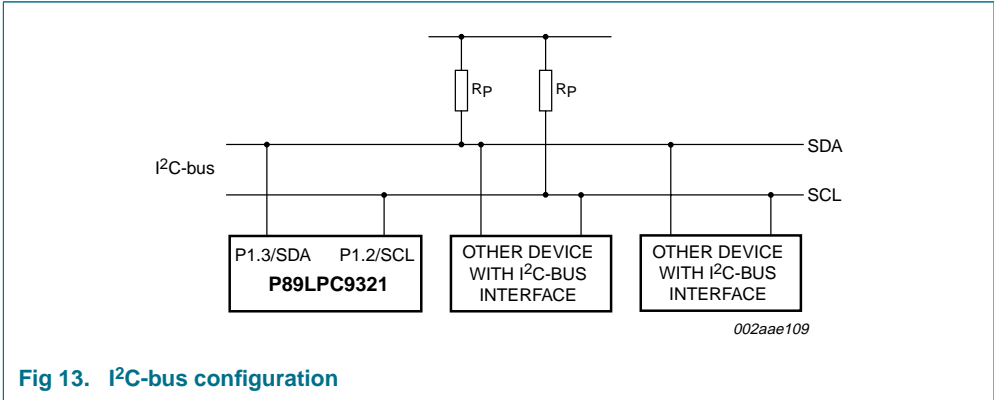


Fig 13. I2C-bus configuration

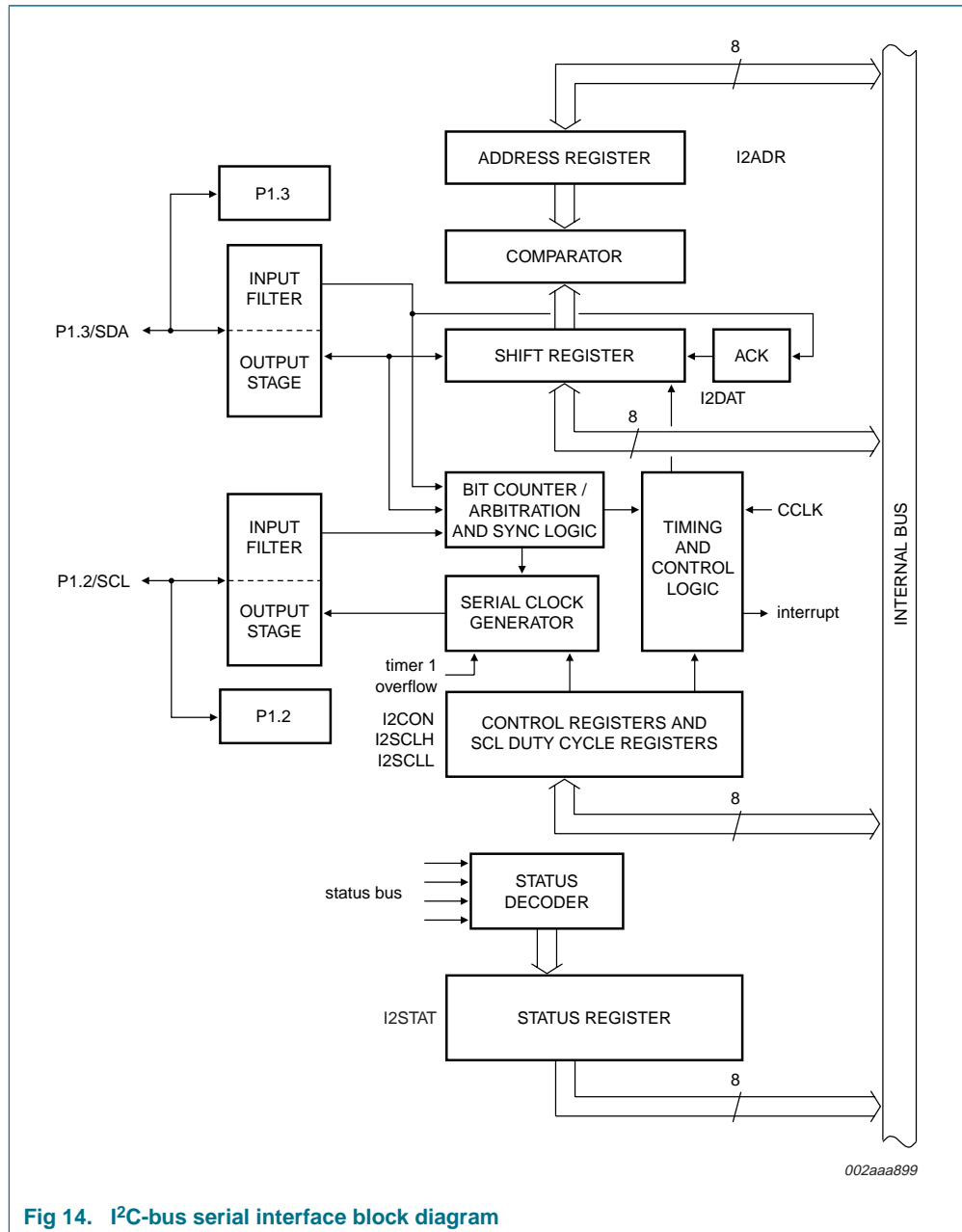


Fig 14. I²C-bus serial interface block diagram

7.25 SPI

The P89LPC9321 provides another high-speed serial communication interface: the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 3 Mbit/s can be supported in either Master mode or Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

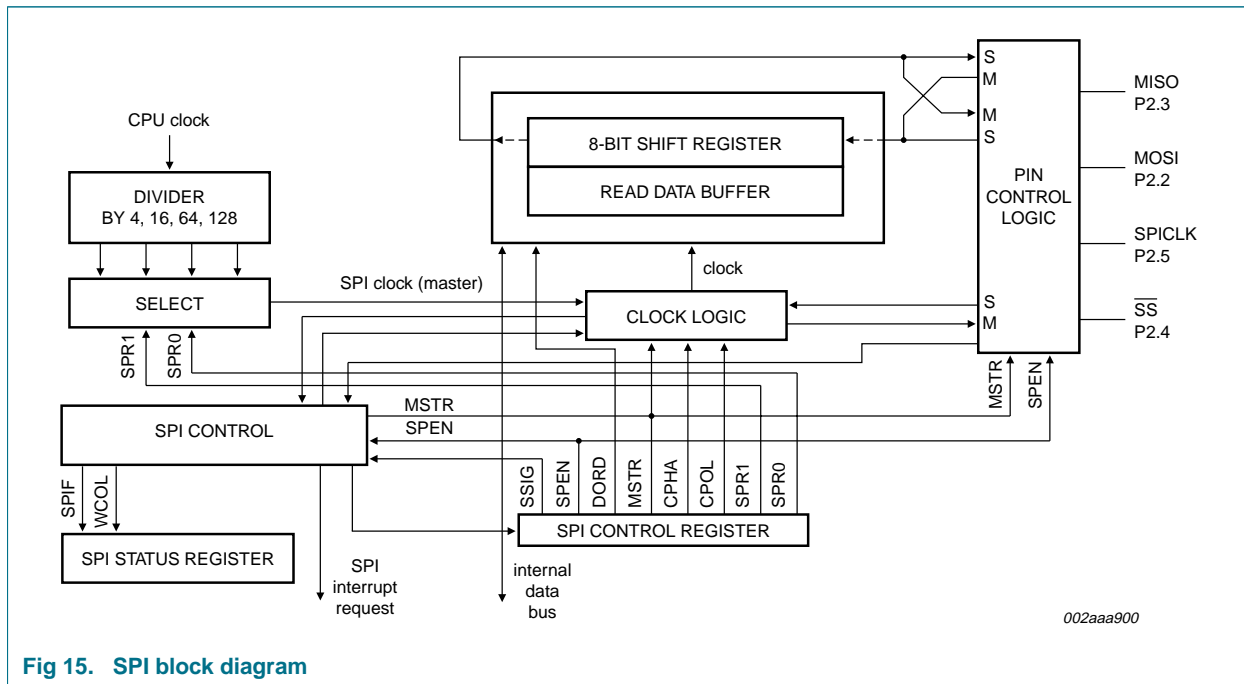


Fig 15. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and \overline{SS} :

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the Master mode and is input in the Slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- \overline{SS} is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its \overline{SS} pin to determine whether it is selected.

Typical connections are shown in [Figure 16](#) through [Figure 18](#).

7.25.1 Typical SPI configurations

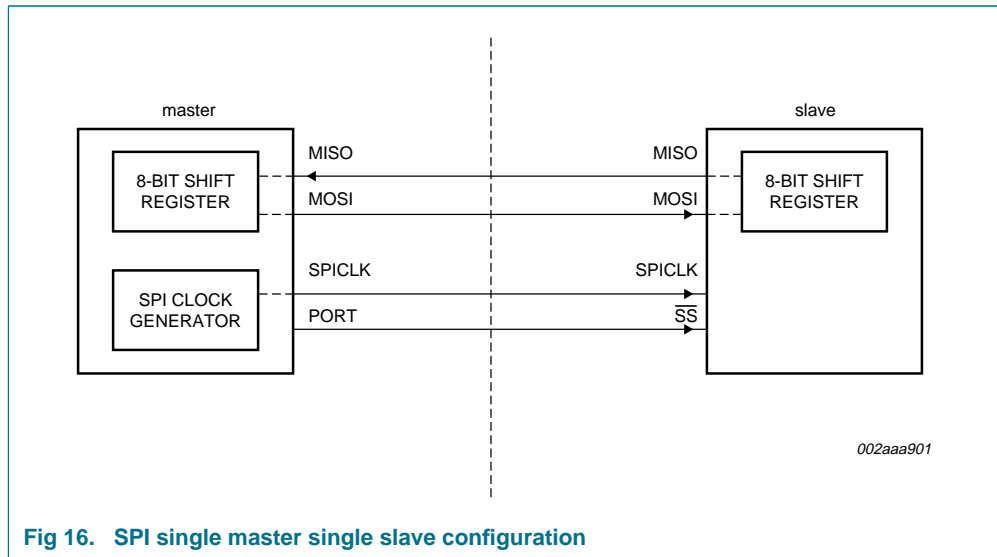


Fig 16. SPI single master single slave configuration

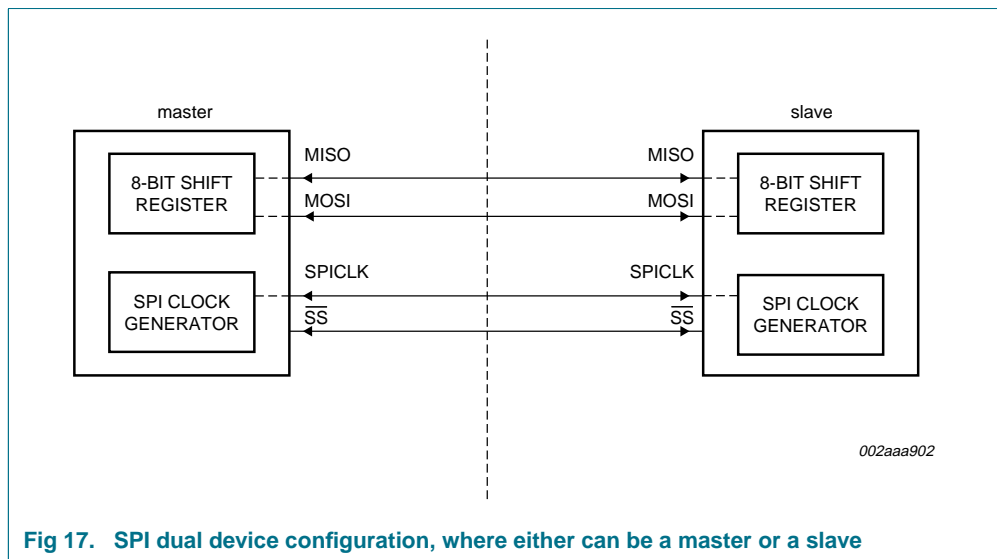


Fig 17. SPI dual device configuration, where either can be a master or a slave

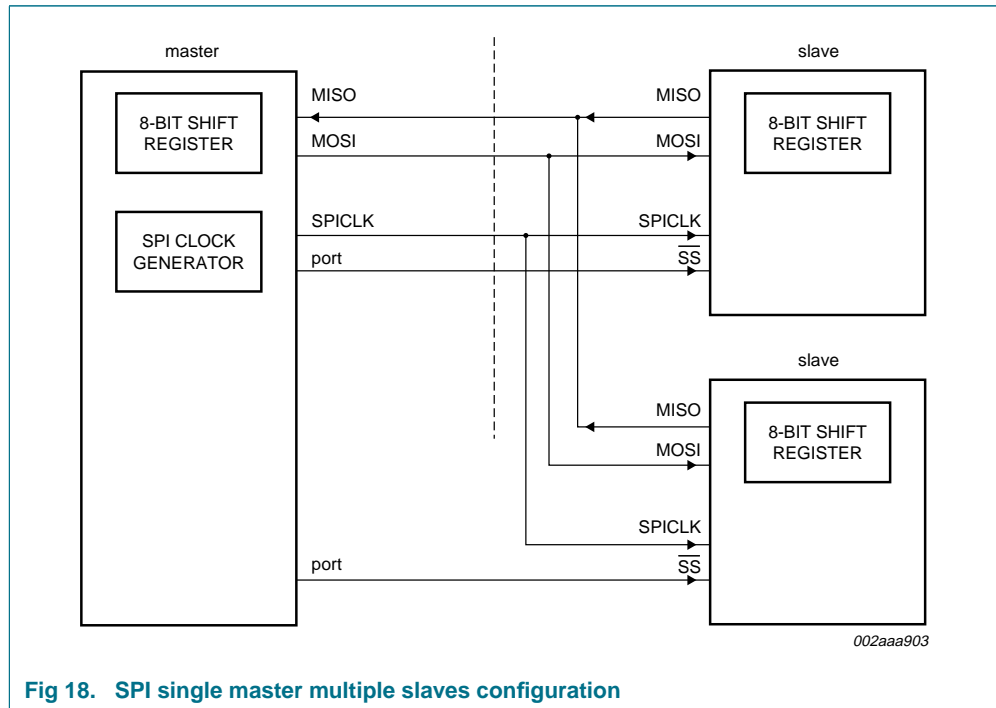


Fig 18. SPI single master multiple slaves configuration

7.26 Analog comparators

Two analog comparators are provided on the P89LPC9321. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one (which may be read in a register and/or routed to a pin) when the positive input (one of two selectable inputs) is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes.

The positive inputs of comparators could be amplified by Programmable Gain Amplifier 1 (PGA1) module. The PGA1 can supply gain factors of 2x, 4x, 8x, or 16x, eliminating the need for external op-amps in the end application.

The overall connections to both comparators are shown in [Figure 19](#). The comparators function to $V_{DD} = 2.4$ V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 μ s. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

When a comparator is disabled the comparator's output, CO_n , goes HIGH. If the comparator output was LOW and then is disabled, the resulting transition of the comparator output from a LOW to HIGH state will set the comparator flag, CMF_n . This will cause an interrupt if the comparator interrupt is enabled. The user should therefore disable the comparator interrupt prior to disabling the comparator. Additionally, the user should clear the comparator flag, CMF_n , after disabling the comparator.

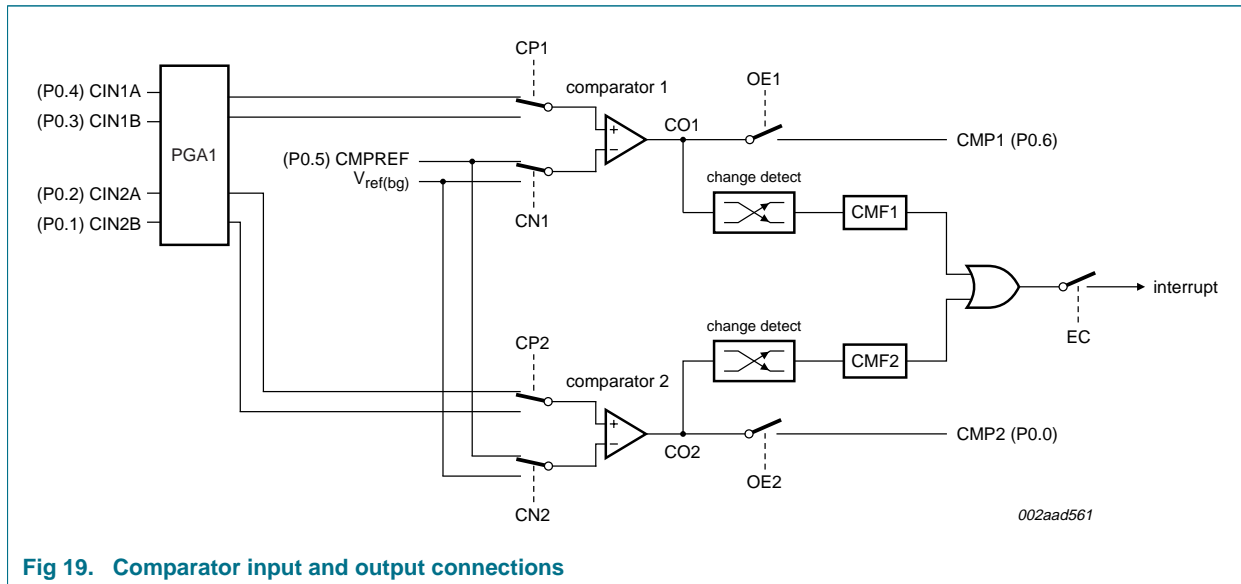


Fig 19. Comparator input and output connections

7.26.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is $1.23\text{ V} \pm 10\%$.

7.26.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

7.26.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

7.27 KBI

The Keypad Interrupt function (KBI) is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

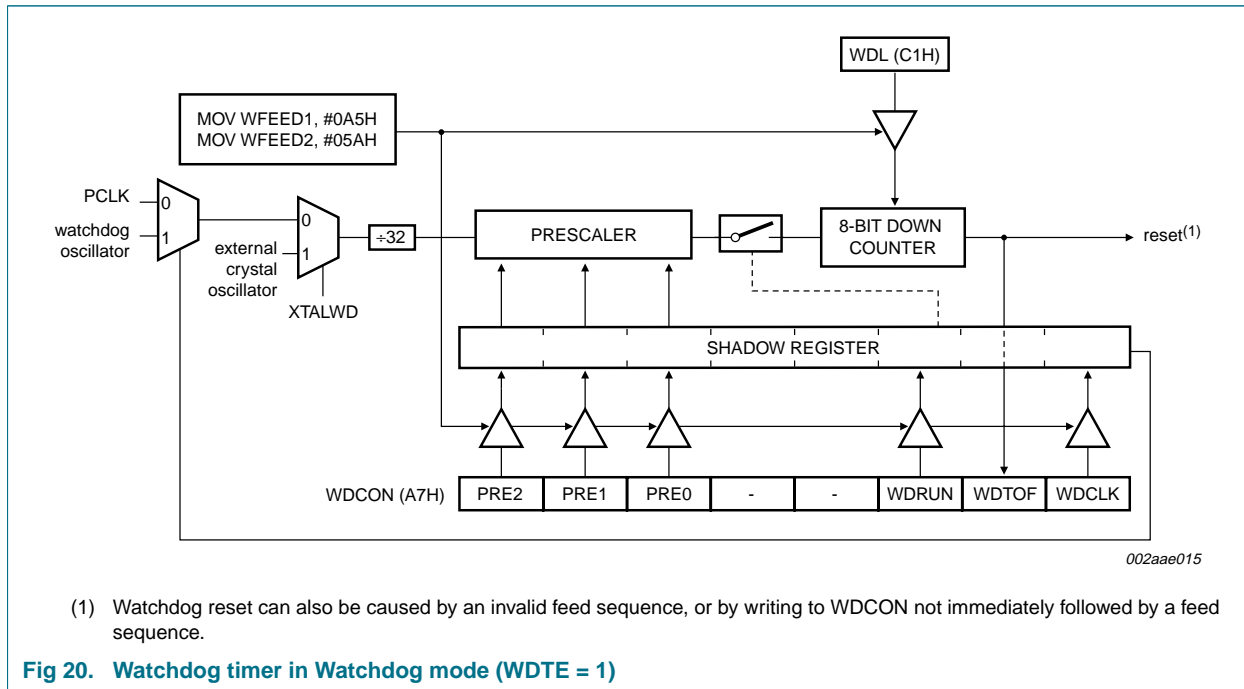
The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

7.28 Watchdog timer

The watchdog timer causes a system reset when it underflows as a result of a failure to feed the timer prior to the timer reaching its terminal count. It consists of a programmable 12-bit prescaler, and an 8-bit down counter. The down counter is decremented by a tap taken from the prescaler. The clock source for the prescaler can be the PCLK, the nominal 400 kHz watchdog oscillator or external crystal oscillator. The watchdog timer can only be reset by a power-on reset. When the watchdog feature is disabled, it can be used as an interval timer and may generate an interrupt. [Figure 20](#) shows the watchdog timer in Watchdog mode. Feeding the watchdog requires a two-byte sequence. If PCLK is selected as the watchdog clock and the CPU is powered down, the watchdog is disabled. The watchdog timer has a time-out period that ranges from a few μ s to a few seconds. Please refer to the P89LPC9321 *User manual* for more details.



7.29 Additional features

7.29.1 Software reset

The SRST bit in AUXR1 gives software the opportunity to reset the processor completely, as if an external reset or watchdog reset had occurred. Care should be taken when writing to AUXR1 to avoid accidental software resets.

7.29.2 Dual data pointers

The dual Data Pointers (DPTR) provides two different Data Pointers to specify the address used with certain instructions. The DPS bit in the AUXR1 register selects one of the two Data Pointers. Bit 2 of AUXR1 is permanently wired as a logic 0 so that the DPS bit may be toggled (thereby switching Data Pointers) simply by incrementing the AUXR1 register, without the possibility of inadvertently altering other bits in the register.

7.29.3 Data EEPROM

The P89LPC9321 has 512 bytes of on-chip Data EEPROM. The Data EEPROM is SFR based, byte readable, byte writable, and erasable (via row fill and sector fill). The user can read, write and fill the memory via SFRs and one interrupt. This Data EEPROM provides 100,000 minimum erase/program cycles for each byte.

- Byte mode: In this mode, data can be read and written one byte at a time.
- Row fill: In this mode, the addressed row (64 bytes) is filled with a single value. The entire row can be erased by writing 00H.
- Sector fill: In this mode, all 512 bytes are filled with a single value. The entire sector can be erased by writing 00H.

After the operation finishes, the hardware will set the EEIF bit, which if enabled will generate an interrupt. The flag is cleared by software.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and Data EEPROM program or erase is blocked. EWERR1 and EWERR0 bits are used to indicate the write error for BOD EEPROM. Both can be cleared by power on reset, watchdog reset or software write.

7.30 Flash program memory

7.30.1 General description

The P89LPC9321 flash memory provides in-circuit electrical erasure and programming. The flash can be erased, read, and written as bytes. The Sector and Page Erase functions can erase any flash sector (1 kB) or page (64 bytes). The Chip Erase operation will erase the entire program memory. ICP using standard commercial programmers is available. In addition, IAP and byte-erase allows code memory to be used for non-volatile data storage. On-chip erase and write timing generation contribute to a user-friendly programming interface. The P89LPC9321 flash reliably stores memory contents even after 100,000 erase and program cycles. The cell is designed to optimize the erase and programming mechanisms. The P89LPC9321 uses V_{DD} as the supply voltage to perform the Program/Erase algorithms. When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

7.30.2 Features

- Programming and erase over the full operating voltage range.
- Byte erase allows code memory to be used for data storage.
- Read/Programming/Erase using ISP/IAP/ICP.
- Internal fixed boot ROM, containing low-level IAP routines available to user code.
- Default loader providing ISP via the serial port, located in upper end of user program memory.
- Boot vector allows user-provided flash loader code to reside anywhere in the flash memory space, providing flexibility to the user.
- Any flash program/erase operation in 2 ms.
- Programming with industry-standard commercial programmers.
- Programmable security for the code in the flash for each sector.
- 100,000 typical erase/program cycles for each byte.
- 10 year minimum data retention.

7.30.3 Flash organization

The program memory consists of eight 1 kB sectors on the P89LPC9321 devices. Each sector can be further divided into 64-byte pages. In addition to sector erase, page erase, and byte erase, a 64-byte page register is included which allows from 1 to 64 bytes of a given page to be programmed at the same time, substantially reducing overall programming time.

7.30.4 Using flash as data storage

The flash code memory array of this device supports individual byte erasing and programming. Any byte in the code memory array may be read using the MOV_C instruction, provided that the sector containing the byte has not been secured (a MOV_C instruction is not allowed to read code memory contents of a secured sector). Thus any byte in a non-secured sector may be used for non-volatile data storage.

7.30.5 Flash programming and erasing

Four different methods of erasing or programming of the flash are available. The flash may be programmed or erased in the end-user application (IAP) under control of the application's firmware. Another option is to use the ICP mechanism. This ICP system provides for programming through a serial clock/serial data interface. As shipped from the factory, the upper 512 bytes of user code space contains a serial ISP routine allowing for the device to be programmed in circuit through the serial port. The flash may also be programmed or erased using a commercially available EPROM programmer which supports this device. This device does not provide for direct verification of code memory contents. Instead, this device provides a 32-bit Cyclic Redundancy Check (CRC) result on either a sector or the entire user code space.

Remark: When voltage supply is lower than 2.4 V, the BOD FLASH is tripped and flash erase/program is blocked.

7.30.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC9321 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application - using commercially available programmers - possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC9321 *User manual*.

7.30.7 IAP

IAP is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The NXP IAP has made in-application programming in an embedded application possible without additional components. Two methods are available to accomplish IAP. A set of predefined IAP functions are provided in a Boot ROM and can be called through a common interface, PGM_MTP. Several IAP calls are available for use by an application program to permit selective erasing and programming of flash sectors, pages, security bits, configuration bytes, and device ID. These functions are selected by setting up the microcontroller's registers before making a call to PGM_MTP at FF03H. The Boot ROM occupies the program memory space at the top of the address space from FF00H to FEFFH, thereby not conflicting with the user program memory space.

In addition, IAP operations can be accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC9321 *User manual*.

7.30.8 ISP

ISP is performed without removing the microcontroller from the system. The ISP facility consists of a series of internal hardware resources coupled with internal firmware to facilitate remote programming of the P89LPC9321 through the serial port. This firmware is provided by NXP and embedded within each P89LPC9321 device. The NXP ISP facility has made in-system programming in an embedded application possible with a minimum of additional expense in components and circuit board area. The ISP function uses five pins (V_{DD} , V_{SS} , TXD, RXD, and RST). Only a small connector needs to be available to interface your application to an external circuit in order to use this feature.

7.30.9 Power-on reset code execution

The P89LPC9321 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC9321 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

[Table 8](#) shows the factory default Boot Vector setting for these devices. A factory-provided boot loader is pre-programmed into the address space indicated and uses the indicated boot loader entry point to perform ISP functions. This code can be erased by the user.

Remark: Users who wish to use this loader should take precautions to avoid erasing the 1 kB sector that contains this boot loader. Instead, the page erase function can be used to erase the first eight 64-byte pages located in this sector.

A custom boot loader can be written with the Boot Vector set to the custom boot loader, if desired.

Table 8. Default boot vector values and ISP entry points

| Device | Default boot vector | Default boot loader entry point | Default boot loader code range | 1 kB sector range |
|------------|---------------------|---------------------------------|--------------------------------|-------------------|
| P89LPC9321 | 1FH | 1F00H | 1E00H to 1FFFH | 1C00H to 1FFFH |

7.30.10 Hardware activation of the boot loader

The boot loader can also be executed by forcing the device into ISP mode during a power-on sequence (see the P89LPC9321 *User manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code but can be manually forced into ISP operation. If the factory default setting for the boot vector (1FH) is changed, it will no longer point to the factory pre-programmed ISP boot loader code. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

7.31 User configuration bytes

Some user-configurable features of the P89LPC9321 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1 and UCFG2. Please see the P89LPC9321 *User's Manual* for additional details.

7.32 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC9321. Each byte corresponds to one sector. Please see the P89LPC9321 *User manual* for additional details.

7.33 PGA

Additional PGA module is integrated. The gain of PGA can be programmable to 2, 4, 8 and 16. Please refer to [Table 10 “Static characteristics”](#) for detailed specifications.

Register PGACON1 and PGACON1B are used to for PGA1 configuration. Register PGA1TRIM2X4X and PGA1TRIM8X16X provide trim value of PGA1 gain level. As power-on, default trim value for each gain setting is loaded into the PGA1 trim registers. For accurate measurements, offset calibration is required.

Please see the P89LPC9321 *User manual* for detail configuration, calibration, and usage information.

In Power-down mode or Total Power-down mode, the PGA1 does not function. If the PGAs, is enabled, it will consume power. Power can be reduced by disabling the PGA1.

8. Limiting values

Table 9. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).^[1]

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-------------------|--|--|-----|------|------|
| $T_{amb(bias)}$ | bias ambient temperature | | -55 | +125 | °C |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| $I_{OH(I/O)}$ | HIGH-level output current per input/output pin | | - | 20 | mA |
| $I_{OL(I/O)}$ | LOW-level output current per input/output pin | | - | 20 | mA |
| $I_{I/Otot(max)}$ | maximum total input/output current | | - | 100 | mA |
| V_n | voltage on any other pin | except V_{SS} , with respect to V_{DD} | - | 3.5 | V |
| $P_{tot(pack)}$ | total power dissipation (per package) | based on package heat transfer, not device power consumption | - | 1.5 | W |

[1] The following applies to [Table 9](#):

- This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.
- Parameters are valid over ambient temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

9. Static characteristics

Table 10. Static characteristics
 $V_{DD} = 2.4\text{ V to }3.6\text{ V unless otherwise specified.}$
 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial applications, unless otherwise specified.}$

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|----------------|--------------------------------------|--|----------------|--------------------|-------------|-------------------------|
| $I_{DD(oper)}$ | operating supply current | $V_{DD} = 3.6\text{ V};$ $f_{osc} = 12\text{ MHz}$ | [2] - | 10 | 15 | mA |
| | | $V_{DD} = 3.6\text{ V};$ $f_{osc} = 18\text{ MHz}$ | [2] - | 14 | 23 | mA |
| $I_{DD(idle)}$ | Idle mode supply current | $V_{DD} = 3.6\text{ V};$ $f_{osc} = 12\text{ MHz}$ | [2] - | 3.25 | 5 | mA |
| | | $V_{DD} = 3.6\text{ V};$ $f_{osc} = 18\text{ MHz}$ | [2] - | 5 | 7 | mA |
| $I_{DD(pd)}$ | Power-down mode supply current | $V_{DD} = 3.6\text{ V};$ voltage comparators powered down | [2] - | 20 | 40 | μA |
| $I_{DD(tpd)}$ | total Power-down mode supply current | $V_{DD} = 3.6\text{ V}$ | [3] - | 1 | 5 | μA |
| $(dV/dt)_r$ | rise rate | of V_{DD} | - | - | 2 | $\text{mV}/\mu\text{s}$ |
| $(dV/dt)_f$ | fall rate | of V_{DD} | - | - | 50 | $\text{mV}/\mu\text{s}$ |
| V_{DDR} | data retention supply voltage | | 1.5 | - | - | V |
| $V_{th(HL)}$ | HIGH-LOW threshold voltage | except SCL, SDA | $0.22V_{DD}$ | $0.4V_{DD}$ | - | V |
| V_{IL} | LOW-level input voltage | SCL, SDA only | -0.5 | - | $0.3V_{DD}$ | V |
| $V_{th(LH)}$ | LOW-HIGH threshold voltage | except SCL, SDA | - | $0.6V_{DD}$ | $0.7V_{DD}$ | V |
| V_{IH} | HIGH-level input voltage | SCL, SDA only | $0.7V_{DD}$ | - | 5.5 | V |
| V_{hys} | hysteresis voltage | port 1 | - | $0.2V_{DD}$ | - | V |
| V_{OL} | LOW-level output voltage | $I_{OL} = 20\text{ mA};$ $V_{DD} = 2.4\text{ V to }3.6\text{ V}$ all ports, all modes except high-Z | [4] - | 0.6 | 1.0 | V |
| | | $I_{OL} = 3.2\text{ mA}; V_{DD} = 2.4\text{ V to }3.6\text{ V}$ all ports, all modes except high-Z | [4] - | 0.2 | 0.3 | V |
| V_{OH} | HIGH-level output voltage | $I_{OH} = -20\text{ }\mu\text{A};$ $V_{DD} = 2.4\text{ V to }3.6\text{ V};$ all ports, quasi-bidirectional mode | $V_{DD} - 0.3$ | $V_{DD} - 0.2$ | - | V |
| | | $I_{OH} = -3.2\text{ mA};$ $V_{DD} = 2.4\text{ V to }3.6\text{ V};$ all ports, push-pull mode | $V_{DD} - 0.7$ | $V_{DD} - 0.4$ | - | V |
| | | $I_{OH} = -10\text{ mA};$ $V_{DD} = 2.4\text{ V to }3.6\text{ V};$ all ports, push-pull mode | - | 3.2 | - | V |
| V_{xtal} | crystal voltage | on XTAL1, XTAL2 pins; with respect to V_{SS} | -0.5 | - | +4.0 | V |
| V_n | voltage on any other pin | except XTAL1, XTAL2, $V_{DD};$ with respect to V_{SS} | [5] -0.5 | - | +5.5 | V |
| C_{iss} | input capacitance | | [6] - | - | 15 | pF |

Table 10. Static characteristics ...continued

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$ unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ ^[1] | Max | Unit |
|-------------------------|--|--|---------|--------------------|---------|-------------------------------|
| I_{IL} | LOW-level input current | $V_I = 0.4\text{ V}$ | [7] - | - | -80 | μA |
| I_{LI} | input leakage current | $V_I = V_{IL}, V_{IH}, \text{ or } V_{th(HL)}$ | [8] - | - | ± 1 | μA |
| I_{THL} | HIGH-LOW transition current | all ports; $V_I = 1.5\text{ V}$ at $V_{DD} = 3.6\text{ V}$ | [9] -30 | - | -450 | μA |
| $R_{RST_N(int)}$ | internal pull-up resistance on pin $\overline{\text{RST}}$ | pin $\overline{\text{RST}}$ | 10 | - | 30 | $\text{k}\Omega$ |
| BOD interrupt | | | | | | |
| V_{trip} | trip voltage | falling stage | | | | |
| | | BOICFG1, BOICFG0 = 01 | 2.25 | - | 2.55 | V |
| | | BOICFG1, BOICFG0 = 10 | 2.60 | - | 2.80 | V |
| | | BOICFG1, BOICFG0 = 11 | 3.10 | - | 3.40 | V |
| | | rising stage | | | | |
| | | BOICFG1, BOICFG0 = 01 | 2.30 | - | 2.60 | V |
| | | BOICFG1, BOICFG0 = 10 | 2.70 | - | 2.90 | V |
| BOICFG1, BOICFG0 = 11 | 3.15 | - | 3.45 | V | | |
| BOD reset | | | | | | |
| V_{trip} | trip voltage | falling stage | | | | |
| | | BOE1, BOE0 = 01 | 2.10 | - | 2.30 | V |
| | | BOE1, BOE0 = 10 | 2.25 | - | 2.55 | V |
| | | BOE1, BOE0 = 11 | 2.80 | - | 3.20 | V |
| | | rising stage | | | | |
| | | BOE1, BOE0 = 01 | 2.20 | - | 2.40 | V |
| | | BOE1, BOE0 = 10 | 2.30 | - | 2.60 | V |
| BOE1, BOE0 = 11 | 2.90 | - | 3.30 | V | | |
| BOD EEPROM/FLASH | | | | | | |
| V_{trip} | trip voltage | falling stage | 2.25 | - | 2.55 | V |
| | | rising stage | 2.30 | - | 2.60 | V |
| $V_{ref(bg)}$ | band gap reference voltage | | 1.11 | 1.23 | 1.34 | V |
| TC_{bg} | band gap temperature coefficient | | - | 10 | 20 | $\text{ppm}/^{\circ}\text{C}$ |

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 8 "Limiting values" for steady state (non-transient) limits on I_{OL} or I_{OH} . If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

- [5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS} .
- [6] Pin capacitance is characterized but not tested.
- [7] Measured with port in quasi-bidirectional mode.
- [8] Measured with port in high-impedance mode.
- [9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

10. Dynamic characteristics

Table 11. Dynamic characteristics (12 MHz)
 $V_{DD} = 2.4\text{ V to }3.6\text{ V}$ unless otherwise specified.

 $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified. [1][2]

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc} = 12\text{ MHz}$ | | Unit |
|-------------------------------------|---|---|-----------------|--------------------------|---------------------------|--------|------|
| | | | Min | Max | Min | Max | |
| $f_{osc(RC)}$ | internal RC oscillator frequency | nominal $f = 7.3728\text{ MHz}$ trimmed to $\pm 1\%$ at $T_{amb} = 25\text{ }^{\circ}\text{C}$; clock doubler option = OFF (default) | 7.189 | 7.557 | 7.189 | 7.557 | MHz |
| | | nominal $f = 14.7456\text{ MHz}$; clock doubler option = ON, $V_{DD} = 2.7\text{ V to }3.6\text{ V}$ | 14.378 | 15.114 | 14.378 | 15.114 | MHz |
| $f_{osc(WD)}$ | internal watchdog oscillator frequency | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | 380 | 420 | 380 | 420 | kHz |
| f_{osc} | oscillator frequency | | 0 | 12 | - | - | MHz |
| $T_{cy(clk)}$ | clock cycle time | see Figure 22 | 83 | - | - | - | ns |
| f_{CLKLP} | low-power select clock frequency | | 0 | 8 | - | - | MHz |
| Glitch filter | | | | | | | |
| t_{gr} | glitch rejection time | P1.5/ $\overline{\text{RST}}$ pin | - | 50 | - | 50 | ns |
| | | any pin except P1.5/ $\overline{\text{RST}}$ | - | 15 | - | 15 | ns |
| t_{sa} | signal acceptance time | P1.5/ $\overline{\text{RST}}$ pin | 125 | - | 125 | - | ns |
| | | any pin except P1.5/ $\overline{\text{RST}}$ | 50 | - | 50 | - | ns |
| External clock | | | | | | | |
| t_{CHCX} | clock HIGH time | see Figure 22 | 33 | $T_{cy(clk)} - t_{CLCX}$ | 33 | - | ns |
| t_{CLCX} | clock LOW time | see Figure 22 | 33 | $T_{cy(clk)} - t_{CHCX}$ | 33 | - | ns |
| t_{CLCH} | clock rise time | see Figure 22 | - | 8 | - | 8 | ns |
| t_{CHCL} | clock fall time | see Figure 22 | - | 8 | - | 8 | ns |
| Shift register (UART mode 0) | | | | | | | |
| T_{XLXL} | serial port clock cycle time | see Figure 21 | $16T_{cy(clk)}$ | - | 1333 | - | ns |
| t_{QVXH} | output data set-up to clock rising edge time | see Figure 21 | $13T_{cy(clk)}$ | - | 1083 | - | ns |
| t_{XHQX} | output data hold after clock rising edge time | see Figure 21 | - | $T_{cy(clk)} + 20$ | - | 103 | ns |
| t_{XHDX} | input data hold after clock rising edge time | see Figure 21 | - | 0 | - | 0 | ns |
| t_{XHDV} | input data valid to clock rising edge time | see Figure 21 | 150 | - | 150 | - | ns |
| SPI interface | | | | | | | |
| f_{SPI} | SPI operating frequency | | | | | | |
| | slave | | 0 | $CCLK/6$ | 0 | 2.0 | MHz |
| | master | | - | $CCLK/4$ | - | 3.0 | MHz |

Table 11. Dynamic characteristics (12 MHz) ...continued $V_{DD} = 2.4\text{ V to }3.6\text{ V unless otherwise specified.}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial applications, unless otherwise specified.}[1][2]$

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc} = 12\text{ MHz}$ | | Unit |
|---------------|---|---|----------------|------|---------------------------|------|------|
| | | | Min | Max | Min | Max | |
| T_{SPICYC} | SPI cycle time | see Figure 23, 24, 25, 26 | | | | | |
| | slave | | $6/CCLK$ | - | 500 | - | ns |
| | master | | $4/CCLK$ | - | 333 | - | ns |
| $t_{SPILEAD}$ | SPI enable lead time | see Figure 25, 26 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| t_{SPILAG} | SPI enable lag time | see Figure 25, 26 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| t_{SPICLK} | SPICLK HIGH time | see Figure 23, 24, 25, 26 | | | | | |
| | master | | $2/CCLK$ | - | 165 | - | ns |
| | slave | | $3/CCLK$ | - | 250 | - | ns |
| t_{SPICLK} | SPICLK LOW time | see Figure 23, 24, 25, 26 | | | | | |
| | master | | $2/CCLK$ | - | 165 | - | ns |
| | slave | | $3/CCLK$ | - | 250 | - | ns |
| t_{SPIDSU} | SPI data set-up time | see Figure 23, 24, 25, 26 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| t_{SPIDH} | SPI data hold time | see Figure 23, 24, 25, 26 | 100 | - | 100 | - | ns |
| | master or slave | | | | | | |
| t_{SPIA} | SPI access time | see Figure 25, 26 | | | | | |
| | slave | | 0 | 120 | 0 | 120 | ns |
| t_{SPIDIS} | SPI disable time | see Figure 25, 26 | | | | | |
| | slave | | 0 | 240 | - | 240 | ns |
| t_{SPIDV} | SPI enable to output data valid time | see Figure 23, 24, 25, 26 | | | | | |
| | slave | | - | 240 | - | 240 | ns |
| | master | | - | 167 | - | 167 | ns |
| t_{SPIOH} | SPI output data hold time | see Figure 23, 24, 25, 26 | 0 | - | 0 | - | ns |
| | | | | | | | |
| t_{SPIR} | SPI rise time | see Figure 23, 24, 25, 26 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, \overline{SS}) | | - | 2000 | - | 2000 | ns |
| t_{SPIF} | SPI fall time | see Figure 23, 24, 25, 26 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, \overline{SS}) | | - | 2000 | - | 2000 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

Table 12. Dynamic characteristics (18 MHz) $V_{DD} = 3.0\text{ V to }3.6\text{ V unless otherwise specified.}$ $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C for industrial applications, unless otherwise specified.}[1][2]$

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc} = 18\text{ MHz}$ | | Unit |
|-------------------------------------|---|---|---|--------------------------|---------------------------|--------|------|
| | | | Min | Max | Min | Max | |
| $f_{osc(RC)}$ | internal RC oscillator frequency | nominal $f = 7.3728\text{ MHz}$ trimmed to $\pm 1\%$ at $T_{amb} = 25\text{ }^{\circ}\text{C}$; clock doubler option = OFF (default) | 7.189 | 7.557 | 7.189 | 7.557 | MHz |
| | | nominal $f = 14.7456\text{ MHz}$; clock doubler option = ON | 14.378 | 15.114 | 14.378 | 15.114 | MHz |
| $f_{osc(WD)}$ | internal watchdog oscillator frequency | $T_{amb} = 25\text{ }^{\circ}\text{C}$ | 380 | 420 | 380 | 420 | kHz |
| f_{osc} | oscillator frequency | | 0 | 18 | - | - | MHz |
| $T_{cy(clk)}$ | clock cycle time | see Figure 22 | 55 | - | - | - | ns |
| f_{CLKLP} | low-power select clock frequency | | 0 | 8 | - | - | MHz |
| Glitch filter | | | | | | | |
| t_{gr} | glitch rejection time | P1.5/ $\overline{\text{RST}}$ pin | - | 50 | - | 50 | ns |
| | | any pin except P1.5/ $\overline{\text{RST}}$ | - | 15 | - | 15 | ns |
| t_{sa} | signal acceptance time | P1.5/ $\overline{\text{RST}}$ pin | 125 | - | 125 | - | ns |
| | | any pin except P1.5/ $\overline{\text{RST}}$ | 50 | - | 50 | - | ns |
| External clock | | | | | | | |
| t_{CHCX} | clock HIGH time | see Figure 22 | 22 | $T_{cy(clk)} - t_{CLCX}$ | 22 | - | ns |
| t_{CLCX} | clock LOW time | see Figure 22 | 22 | $T_{cy(clk)} - t_{CHCX}$ | 22 | - | ns |
| t_{CLCH} | clock rise time | see Figure 22 | - | 5 | - | 5 | ns |
| t_{CHCL} | clock fall time | see Figure 22 | - | 5 | - | 5 | ns |
| Shift register (UART mode 0) | | | | | | | |
| T_{XLXL} | serial port clock cycle time | see Figure 21 | $16T_{cy(clk)}$ | - | 888 | - | ns |
| t_{QVXH} | output data set-up to clock rising edge time | see Figure 21 | $13T_{cy(clk)}$ | - | 722 | - | ns |
| t_{XHQX} | output data hold after clock rising edge time | see Figure 21 | - | $T_{cy(clk)} + 20$ | - | 75 | ns |
| t_{XHDX} | input data hold after clock rising edge time | see Figure 21 | - | 0 | - | 0 | ns |
| t_{XHDV} | input data valid to clock rising edge time | see Figure 21 | 150 | - | 150 | - | ns |
| SPI interface | | | | | | | |
| f_{SPI} | SPI operating frequency | | | | | | |
| | slave | | 0 | $CCLK/6$ | 0 | 3.0 | MHz |
| | master | | - | $CCLK/4$ | - | 4.5 | MHz |
| T_{SPICYC} | SPI cycle time | | see Figure 23, 24, 25, 26 | | | | |
| | slave | | $6/CCLK$ | - | 333 | - | ns |
| | master | | $4/CCLK$ | - | 222 | - | ns |

Table 12. Dynamic characteristics (18 MHz) ...continued $V_{DD} = 3.0\text{ V to }3.6\text{ V}$ unless otherwise specified. $T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.^{[1][2]}

| Symbol | Parameter | Conditions | Variable clock | | $f_{osc} = 18\text{ MHz}$ | | Unit |
|---------------|---|---|-------------------|------|---------------------------|------|------|
| | | | Min | Max | Min | Max | |
| $t_{SPILEAD}$ | SPI enable lead time | see Figure 25, 26 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| t_{SPILAG} | SPI enable lag time | see Figure 25, 26 | | | | | |
| | slave | | 250 | - | 250 | - | ns |
| t_{SPICLK} | SPICLK HIGH time | see Figure 23, 24, 25, 26 | | | | | |
| | slave | | $\frac{3}{4}CCLK$ | - | 167 | - | ns |
| | master | | $\frac{2}{4}CCLK$ | - | 111 | - | ns |
| t_{SPICLK} | SPICLK LOW time | see Figure 23, 24, 25, 26 | | | | | |
| | slave | | $\frac{3}{4}CCLK$ | - | 167 | - | ns |
| | master | | $\frac{2}{4}CCLK$ | - | 111 | - | ns |
| t_{SPIDSU} | SPI data set-up time | see Figure 23, 24, 25, 26 | | | | | |
| | master or slave | | 100 | - | 100 | - | ns |
| t_{SPIDH} | SPI data hold time | see Figure 23, 24, 25, 26 | | | | | |
| | master or slave | | 100 | - | 100 | - | ns |
| t_{SPIA} | SPI access time | see Figure 25, 26 | | | | | |
| | slave | | 0 | 80 | 0 | 80 | ns |
| t_{SPIDIS} | SPI disable time | see Figure 25, 26 | | | | | |
| | slave | | 0 | 160 | - | 160 | ns |
| t_{SPIDV} | SPI enable to output data valid time | see Figure 23, 24, 25, 26 | | | | | |
| | slave | | - | 160 | - | 160 | ns |
| | master | | - | 111 | - | 111 | ns |
| t_{SPIOH} | SPI output data hold time | see Figure 23, 24, 25, 26 | 0 | - | 0 | - | ns |
| t_{SPIR} | SPI rise time | see Figure 23, 24, 25, 26 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, \overline{SS}) | | - | 2000 | - | 2000 | ns |
| t_{SPIF} | SPI fall time | see Figure 23, 24, 25, 26 | | | | | |
| | SPI outputs (SPICLK, MOSI, MISO) | | - | 100 | - | 100 | ns |
| | SPI inputs (SPICLK, MOSI, MISO, \overline{SS}) | | - | 2000 | - | 2000 | ns |

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

10.1 Waveforms

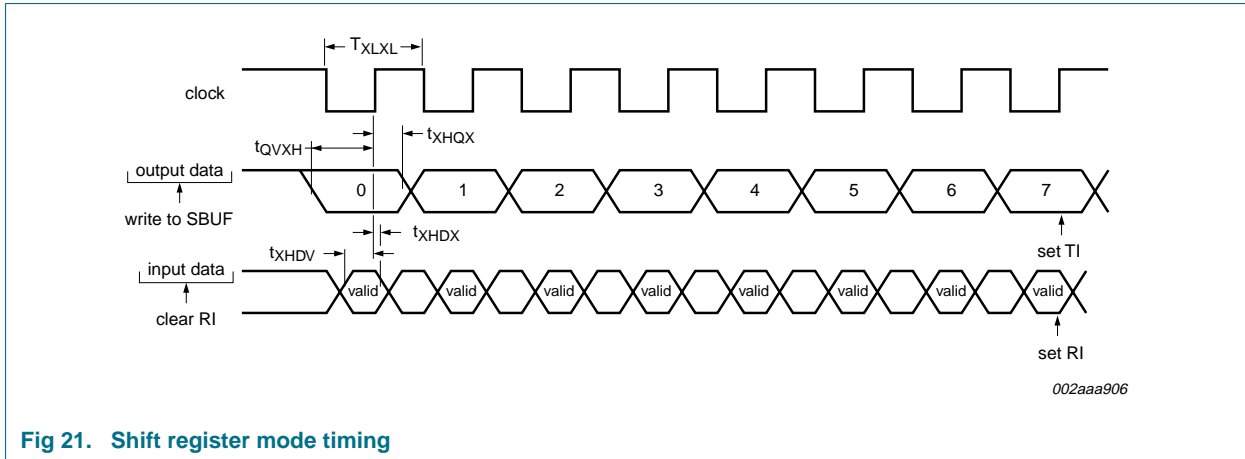


Fig 21. Shift register mode timing

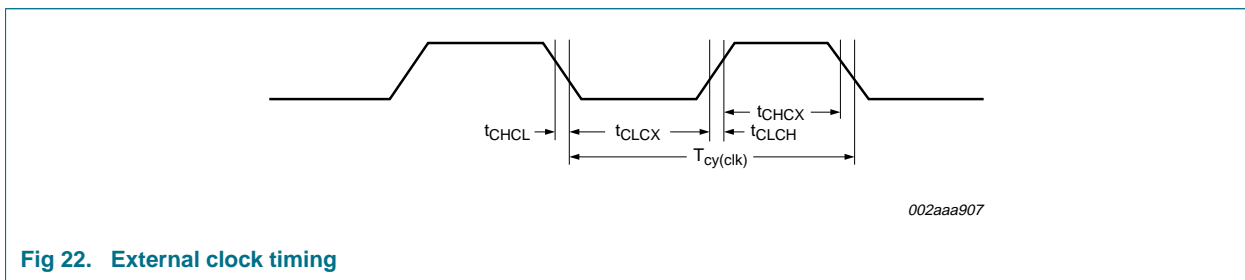


Fig 22. External clock timing

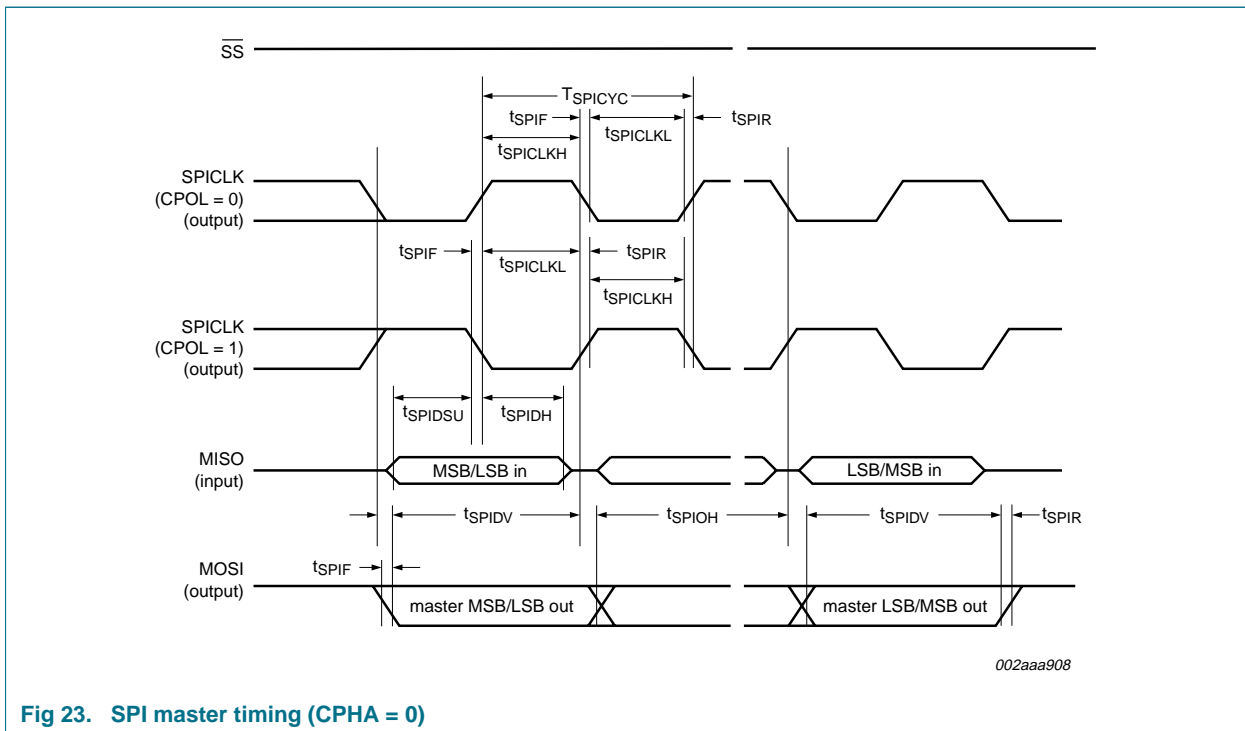


Fig 23. SPI master timing (CPHA = 0)

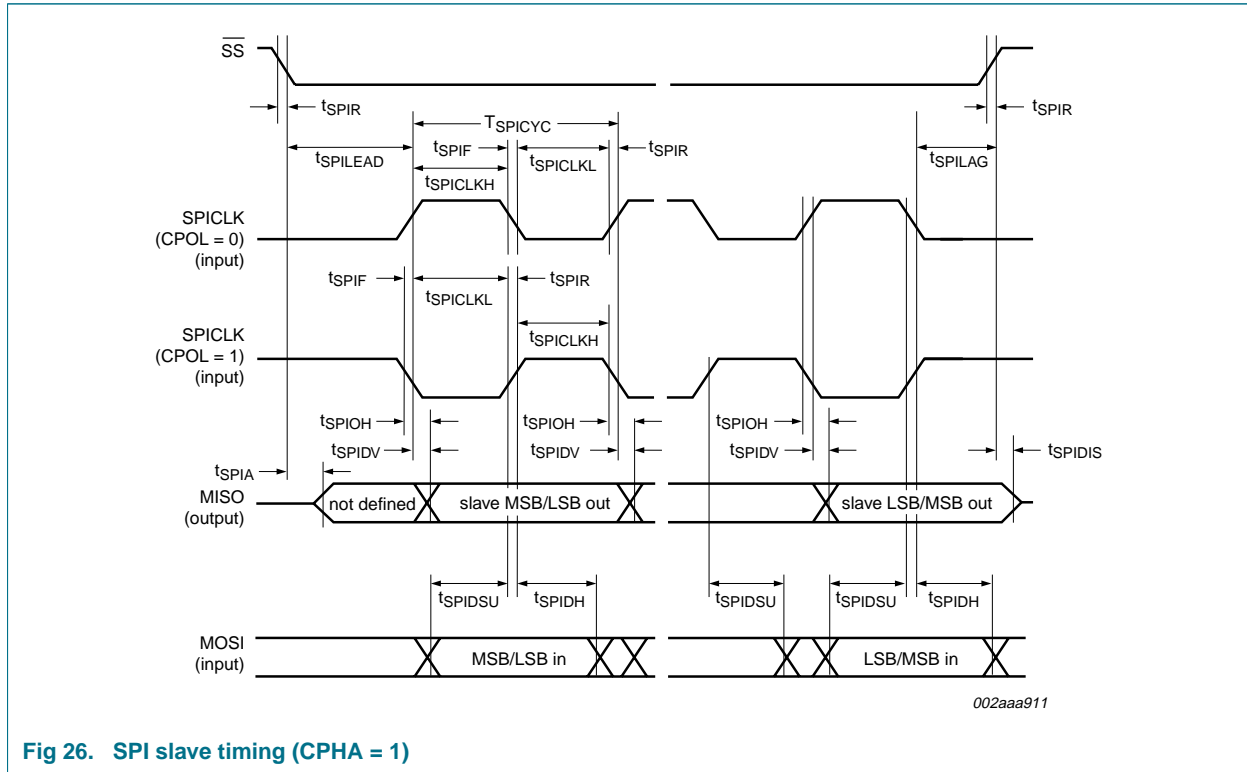


Fig 26. SPI slave timing (CPHA = 1)

10.2 ISP entry mode

Table 13. Dynamic characteristics, ISP entry mode

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------|--|-----------------------------|-----|-----|-----|---------------|
| t_{VR} | V_{DD} active to $\overline{\text{RST}}$ active delay time | pin $\overline{\text{RST}}$ | 50 | - | - | μs |
| t_{RH} | $\overline{\text{RST}}$ HIGH time | pin $\overline{\text{RST}}$ | 1 | - | 32 | μs |
| t_{RL} | $\overline{\text{RST}}$ LOW time | pin $\overline{\text{RST}}$ | 1 | - | - | μs |

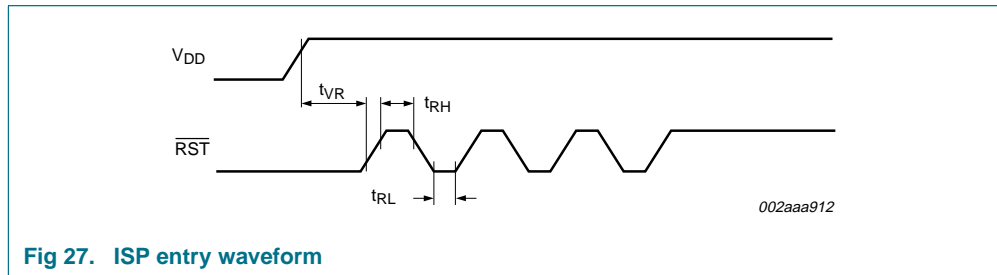


Fig 27. ISP entry waveform

11. Other characteristics

11.1 Comparator electrical characteristics

Table 14. Comparator electrical characteristics

$V_{DD} = 2.4\text{ V to }3.6\text{ V}$, unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C to }+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|----------------------------------|-----------------------------|-----|-----|----------------|---------------|
| V_{IO} | input offset voltage | | - | - | ± 20 | mV |
| V_{IC} | common-mode input voltage | | 0 | - | $V_{DD} - 0.3$ | V |
| CMRR | common-mode rejection ratio | | [1] | - | -50 | dB |
| $t_{res(tot)}$ | total response time | | - | 250 | 500 | ns |
| $t_{(CE-OV)}$ | chip enable to output valid time | | - | - | 10 | μs |
| I_{LI} | input leakage current | $0\text{ V} < V_I < V_{DD}$ | - | - | ± 10 | μA |

[1] This parameter is characterized, but not tested in production.

11.2 PGA electrical characteristics

Table 15. PGA electrical characteristics

$V_{DD} = 2.4\text{ V}$ to 3.6 V , unless otherwise specified.

$T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ for industrial applications, unless otherwise specified.

All limits valid for an external source impedance of less than $10\text{ k}\Omega$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------------------------|-------------------------------|------------------------|-------|-------|-------|---------------|
| $t_{s(\text{PGA})}$ | PGA settling time | within accuracy of ADC | - | - | 1 | μs |
| G_{PGA} | PGA gain | $G = 1$ | 0.95 | 1.00 | 1.05 | V/V |
| | | $G = 2$ | 1.87 | 1.97 | 2.07 | V/V |
| | | $G = 4$ | 3.70 | 3.89 | 4.08 | V/V |
| | | $G = 8$ | 7.22 | 7.60 | 7.98 | V/V |
| | | $G = 16$ | 14.38 | 15.14 | 15.90 | V/V |
| t_{startup} | start-up time | | - | - | 2 | μs |
| $V_{\text{offset(O)}(\text{nom})}$ | nominal output offset voltage | | - | 100 | - | mV |

12. Package outline

PLCC28: plastic leaded chip carrier; 28 leads

SOT261-2

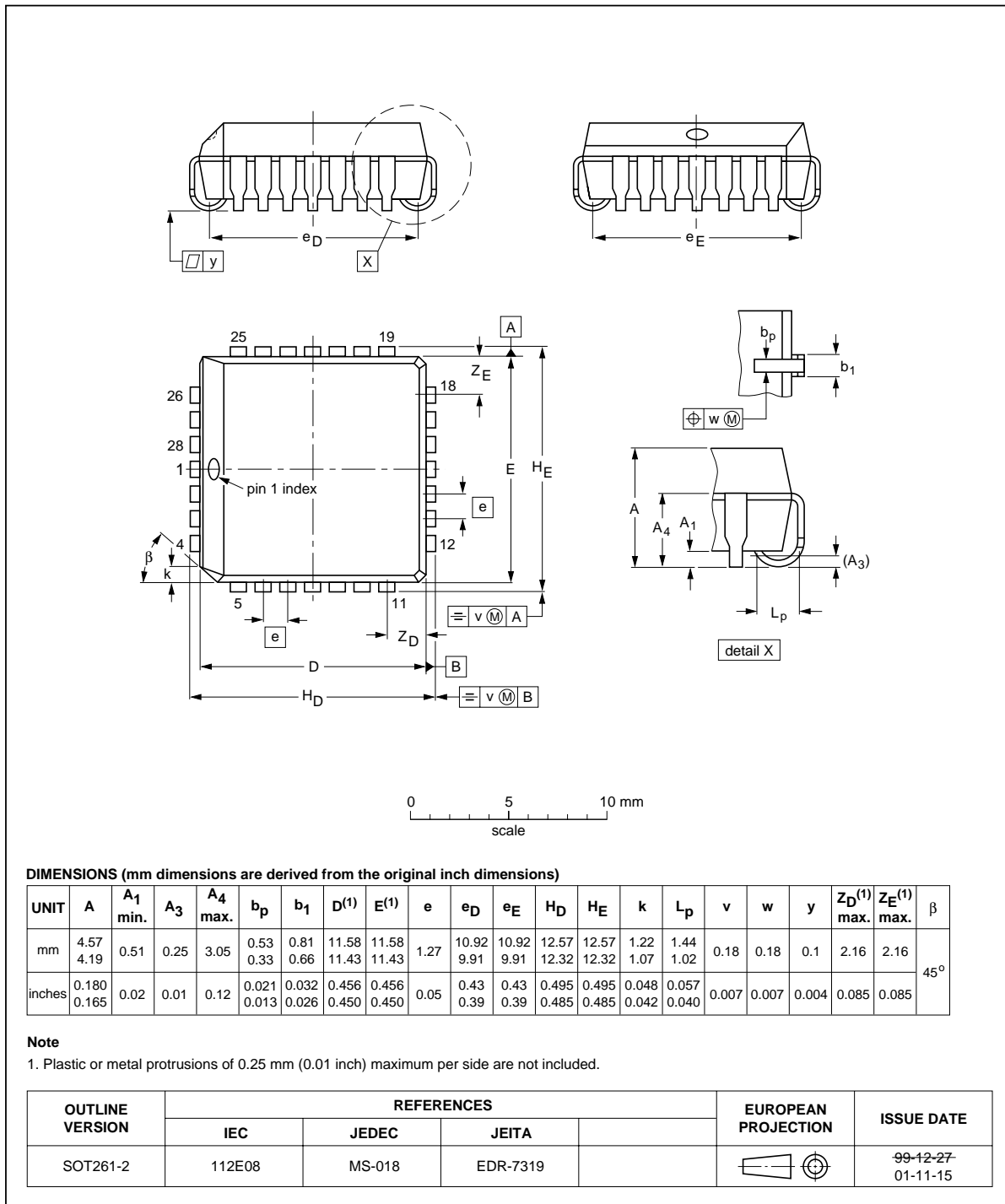


Fig 28. PLCC28 package outline (SOT261-2)

TSSOP28: plastic thin shrink small outline package; 28 leads; body width 4.4 mm

SOT361-1

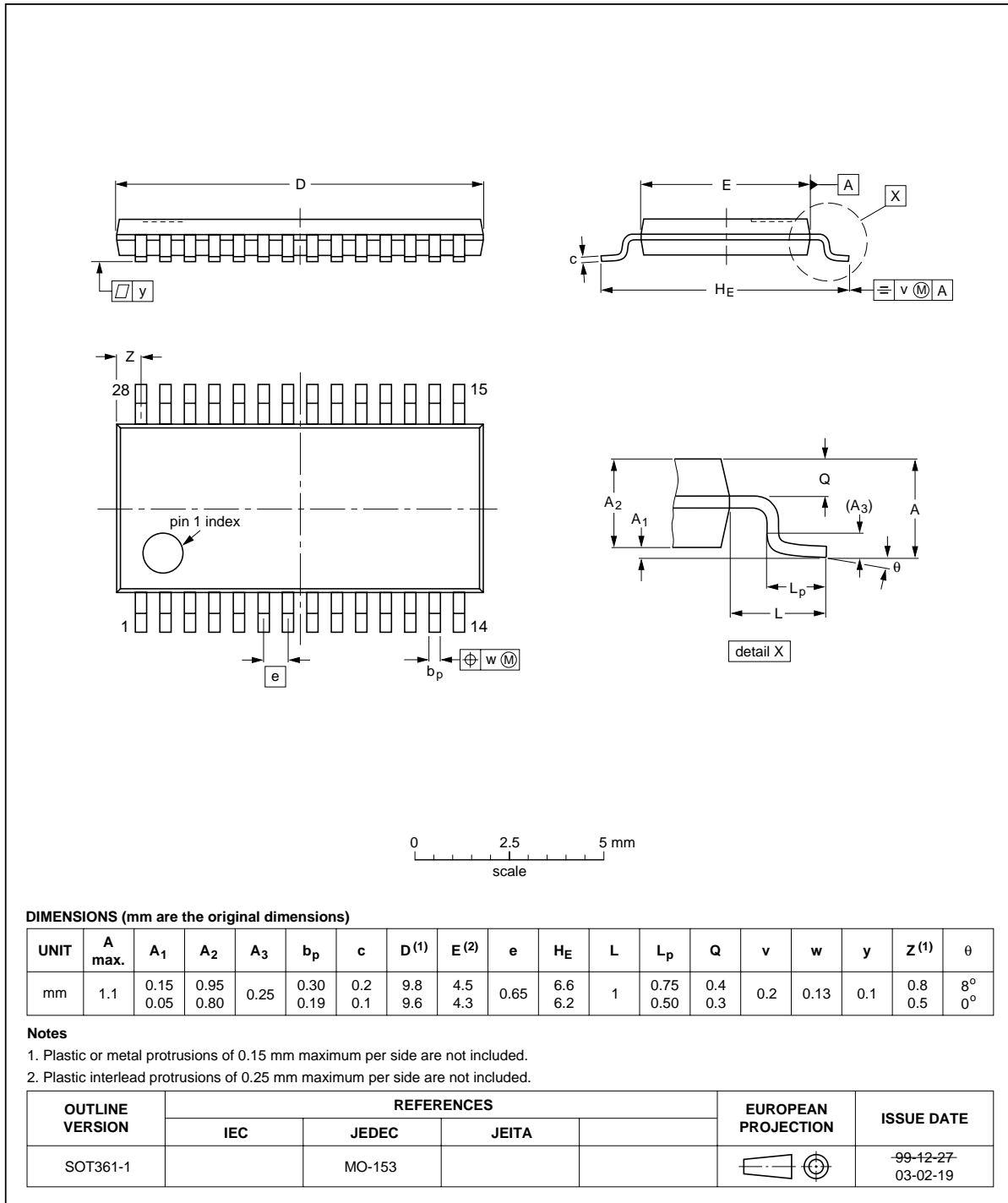


Fig 29. TSSOP28 package outline (SOT361-1)

DIP28: plastic dual in-line package; 28 leads (600 mil)

SOT117-1

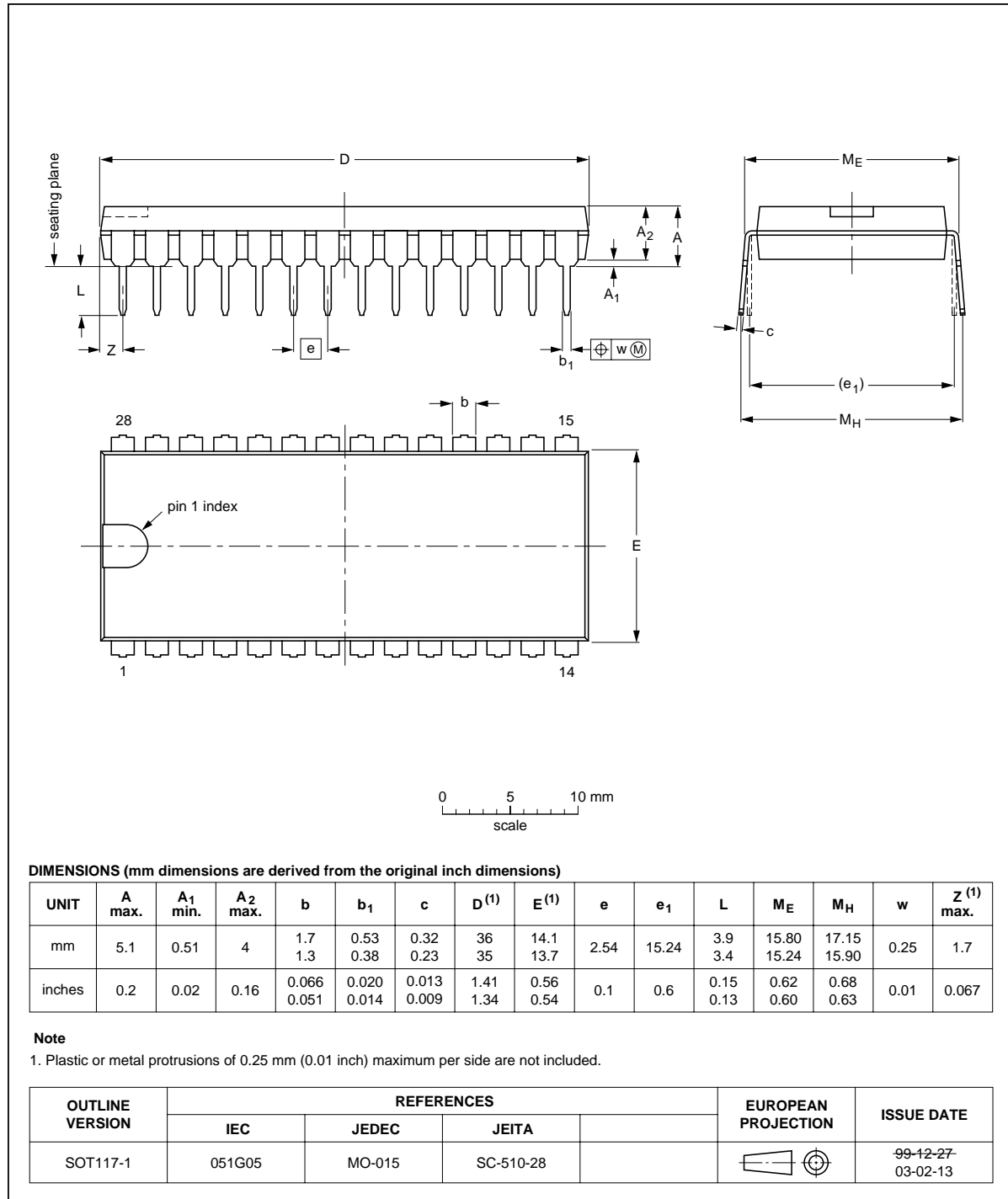


Fig 30. DIP28 package outline (SOT117-1)

13. Abbreviations

Table 16. Abbreviations

| Acronym | Description |
|---------|---|
| ADC | Analog to Digital Converter |
| BOD | Brownout Detection |
| CPU | Central Processing Unit |
| CCU | Capture/Compare Unit |
| DAC | Digital to Analog Converter |
| EPROM | Erasable Programmable Read-Only Memory |
| EEPROM | Electrically Erasable Programmable Read-Only Memory |
| EMI | Electro-Magnetic Interference |
| PGA | Programmable Gain Amplifier |
| PLL | Phase-Locked Loop |
| PWM | Pulse Width Modulator |
| RAM | Random Access Memory |
| RC | Resistance-Capacitance |
| RTC | Real-Time Clock |
| SAR | Successive Approximation Register |
| SFR | Special Function Register |
| SPI | Serial Peripheral Interface |
| UART | Universal Asynchronous Receiver/Transmitter |

14. Revision history

Table 17. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|--------------|--------------|--------------------|---------------|------------|
| P89LPC9321_1 | 20081209 | Product data sheet | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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