# Dual 9 MHz Precision Operational Amplifier

# OP285*

## FEATURES

**Low Offset Voltage: 250 μV**
**Low Noise: 6 nV/√Hz**
**Low Distortion: 0.0006%**
**High Slew Rate: 22 V/μs**
**Wide Bandwidth: 9 MHz**
**Low Supply Current: 5 mA**
**Low Offset Current: 2 nA**
**Unity-Gain Stable**
**SO-8 Package**

## APPLICATIONS

**High Performance Audio**
**Active Filters**
**Fast Amplifiers**
**Integrators**

## GENERAL DESCRIPTION

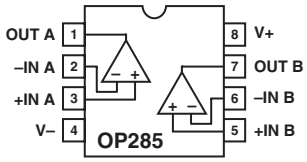
The OP285 is a precision high-speed amplifier featuring the Butler Amplifier front-end. This new front-end design combines the accuracy and low noise performance of bipolar transistors with the speed of JFETs. This yields an amplifier with high slew rates, low offset and good noise performance at low supply currents. Bias currents are also low compared to bipolar designs.

The OP285 offers the slew rate and low power of a JFET amplifier combined with the precision, low noise and low drift of a bipolar amplifier. Input offset voltage is laser-trimmed and guaranteed less than 250 μV. This makes the OP285 useful in dc-coupled or summing applications without the need for special selections or the added noise of additional offset adjustment circuitry. Slew rates of 22 V/μs and a bandwidth of 9 MHz make the OP285 one of the most accurate medium speed amplifiers available.

## PIN CONNECTIONS

**8-Lead Narrow-Body SO (S-Suffix)**


**8-Lead Epoxy DIP (P-Suffix)**




The combination of low noise, speed and accuracy can be used to build high speed instrumentation systems. Circuits such as instrumentation amplifiers, ramp generators, bi-quad filters and dc-coupled audio systems are all practical with the OP285. For applications that require long term stability, the OP285 has a guaranteed maximum long term drift specification.

The OP285 is specified over the XIND—extended industrial—(–40°C to +85°C) temperature range. OP285s are available in 8-pin plastic DIP and SOIC-8 surface mount packages.

*Patents pending

# OP285–SPECIFICATIONS (@ Vs = ±15.0 V, TA = 25°C, unless otherwise noted.)

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT CHARACTERISTICS | | | | | | |
| Offset Voltage | $V_{OS}$ | | | 35 | 250 | µV |
| | $V_{OS}$ | $-40°C \le T_A \le +85°C$ | | | 600 | µV |
| Input Bias Current | $I_B$ | $V_{CM}$ = 0 V | | 100 | 350 | nA |
| | $I_B$ | $V_{CM}$ = 0 V, $-40°C \le T_A \le +85°C$ | | | 400 | nA |
| Input Offset Current | $I_{OS}$ | $V_{CM}$ = 0 V | | 2 | ±50 | nA |
| | $I_{OS}$ | $V_{CM}$ = 0 V, $-40°C \le T_A \le +85°C$ | | 2 | ±100 | nA |
| Input Voltage Range | $V_{CM}$ | | –10.5 | | 10.5 | V |
| Common-Mode Rejection | CMRR | $V_{CM}$ = ±10.5 V, | | | | |
| | | $-40°C \le T_A \le +85°C$ | 80 | 106 | | dB |
| Large-Signal Voltage Gain | $A_{VO}$ | $R_L$ = 2 kΩ | 250 | | | V/mV |
| | $A_{VO}$ | $R_L$ = 2 kΩ, $-40°C \le T_A \le +85°C$ | 175 | | | V/mV |
| | $A_{VO}$ | $R_L$ = 600 Ω | | 200 | | V/mV |
| Common-Mode Input Capacitance | | | | 7.5 | | pF |
| Differential Input Capacitance | | | | 3.7 | | pF |
| Long-Term Offset Voltage | $\Delta V_{OS}$ | Note 1 | | | 300 | µV |
| Offset Voltage Drift | $\Delta V_{OS}/\Delta T$ | | | 1 | | µV/°C |
| OUTPUT CHARACTERISTICS | | | | | | |
| Output Voltage Swing | $V_O$ | RL = 2 kΩ | –13.5 | +13.9 | +13.5 | V |
| | $V_O$ | RL = 2 kΩ, $-40°C \le T_A \le +85°C$ | –13 | +13.9 | +13 | V |
| | | RL = 600 Ω, $V_S$ = ±18 V | | –16/+14 | | V |
| POWER SUPPLY | | | | | | |
| Power Supply Rejection Ratio | PSRR | $V_S$ = ±4.5 V to ±18 V | 85 | 111 | | dB |
| | PSRR | $V_S$ = ±4.5 V to ±18 V, | | | | |
| | | $-40°C \le T_A \le +85°C$ | 80 | | | dB |
| Supply Current | $I_{SY}$ | $V_S$ = ±4.5 V to ±18 V, $V_O$ = 0 V, | | | | |
| | | $R_L$ = x, $-40°C \le T_A \le +85°C$ | | 4 | 5 | mA |
| | $I_{SY}$ | $V_S$ = ±22 V, $V_O$, = 0 V, $R_L$ = x | | | | |
| | | $-40°C \le T_A \le +85°C$ | | | 5.5 | mA |
| Supply Voltage Range | VS | | ±4.5 | | ±22 | V |
| DYNAMIC PERFORMANCE | | | | | | |
| Slew Rate | SR | $R_L$ = 2 kΩ | 15 | 22 | | V/µs |
| Gain Bandwidth Product | GBP | | | 9 | | MHz |
| Phase Margin | θo | | | 62 | | Degrees |
| Settling Time | $t_s$ | To 0.1%, 10 V Step | | 625 | | ns |
| | $t_s$ | To 0.01%, 10 V Step | | 750 | | ns |
| Distortion | | $A_V$ = 1, $V_{OUT}$ = 8.5 V p-p, | | | | |
| | | f = 1 kHz, $R_L$ = 2 kΩ | | –104 | | dB |
| Voltage Noise Density | $e_n$ | f = 30 Hz | | 7 | | nV/√Hz |
| | $e_n$ | f = 1 kHz | | 6 | | nV/√Hz |
| Current Noise Density | $i_n$ | f = 1 kHz | | 0.9 | | pA/√Hz |
| Headroom | | THD + Noise ≤ 0.01%, | | | | |
| | | $R_L$ = 2 kΩ, $V_S$ = ±18 V | | >12.9 | | dBu |

NOTE

[1]Long-term offset voltage is guaranteed by a 1,000 hour life test performed on three independent wafer lots at 125 °C, with an LTPD of 1.3.

Specifications subject to change without notice.

**ABSOLUTE MAXIMUM RATINGS**[1]

Supply Voltage . . . . . ±22 V
Input Voltage[2] . . . . . ±18 V
Differential Input Voltage[2] . . . . . ±7.5 V
Output Short-Circuit Duration to Gnd[3] . . . . . Indefinite
Storage Temperature Range
P, S Package . . . . . –65°C to +150°C
Operating Temperature Range
OP285G . . . . . –40°C to +85°C
Junction Temperature Range
P, S Package . . . . . –65°C to +150°C
Lead Temperature Range (Soldering 60 Sec) . . . . . 300°C

| Package Type | $\theta_{JA}$[4] | $\theta_{JC}$ | Unit |
|---|---|---|---|
| 8-Pin Plastic DIP (P) | 103 | 43 | °C/W |
| 8-Pin SOIC (S) | 158 | 43 | °C/W |

NOTES
[1]Absolute Maximum Ratings apply to packaged parts, unless otherwise noted.
[2]For supply voltages less than ±7.5 V, the absolute maximum input voltage is equal to the supply voltage.
[3]Shorts to either supply may destroy the device. See data sheet for full details.
[4]$\theta_{JA}$ is specified for the worst case conditions, i.e., $\theta_{JA}$ is specified for device in socket for cerdip, P-DIP, and LCC packages; $\theta_{JA}$ is specified for device soldered in circuit board for SOIC package.

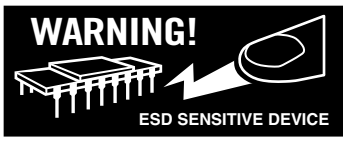
**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| OP285GP* | –40°C to +85°C | 8-Pin Plastic DIP | N-8 |
| OP285GS | –40°C to +85°C | 8-Pin SOIC | S0-8 |
| OP285GSR | –40°C to +85°C | S0-8 Reel, 2500 pcs. | |

*Not for new designs. Obsolete April 2002.

**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the OP285 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



# OP285

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OP285 SPICE Model
* Node assignments
*                          noninverting input
*                          |  inverting input
*                          |  |  positive supply
*                          |  |  |  negative supply
*                          |  |  |  |  output
*                          |  |  |  |  |
*                          |  |  |  |  |
.SUBCKT OP285              1  2  99 50 34
*
* INPUT STAGE & POLE AT 100 MHZ
*
R3          5 51           2.188
R4          6 51           2.188
CIN 1 2     1.5E-12
C2          5 6            364E-12
I1          97 4           100E-3
IOS 1 2     1E-9
EOS 9 3     POLY(1) 26 28 35E-6 1
Q1          5 2 7 QX
Q2          6 9 8 QX
R5          7 4            1.672
R6          8 4            1.672
D1          2 36           DZ
D2          1 36           DZ
EN          3 1            100 1
GN1 0 2     13 0 1
GN20 1      16 0 1
*
EREF 98 0   28 0 1
EP          97 0           99 0 1
EM          510            50 0 1
*
* VOLTAGE NOISE SOURCE
*
DN1 35 10   DEN
DN2 10 11   DEN
VN1 35 0    DC 2
VN2 0 11    DC 2
*
* CURRENT NOISE SOURCE
*
DN3 12 13   DIN
DN4 13 14   DIN
VN3 12 0    DC 2
VN4 0 14    DC 2
CN1 13 0    7.53E-3
*
* CURRENT NOISE SOURCE
*
DN5 15 16   DIN
DN6 16 17   DIN
VN5 15 0    DC 2
VN6 0 17    DC2
CN2 16 0    7.53E-3
*
* GAIN STAGE & DOMINANT POLE AT 32 HZ *
R7 18 98    1.09E6
C3 18 98    4.55E-9
G1 98 18    5 6 4.57E-1
V2 97 19    1.4
V3 20 51    1.4
D3 18 19    DX
D4 20 18    DX
*
* POLE/ZERO PAIR AT 1.5MHz/2.7MHz
*
R8 21 98    1E3
R9 21 22    1.25E3
C4 22 98    47.2E-12
G2 98 21    18 28 1E-3
*
* POLE AT 100 MHZ
*
R10 23 98   1
C5 23 98    1.59E-9
G3 98 23    21 28 1
*
* POLE AT 100 MHZ
*
R11 24 98   l
C6 24 98    1.59E-9
G4 98 24    23 28 1
*
* COMMON-MODE GAIN NETWORK WITH ZERO AT
  1 kHZ *
R12 25 26   1E6
C7 25 26    1.59E-12
R13 26 98   1
E2 25 98    POLY(2) 1 98 2 98 0 2.506 2.506
*
* POLE AT 100 MHZ
*
R14 27 98   1
C8 27 98    1.59E-9
G5 98 27    24 28 1
*
* OUTPUT STAGE
*
Rl5 28 99          100E3
R16 28 50          100E3
C9 28 50           1 E-6
ISY 99 50          1.85E-3
R17 29 99          100
R18 29 50          100
L2 29 34           1E-9
G6 32 50           27 29 10E-3
G7 33 50           29 27 10E-3
G8 29 99           99 27 10E-3
G9 50 29           27 50 10E-3
V4 30 29           1.3
V5 29 31           3.8
F1 29 0            V4 1
F2 0 29            V5 1
D5 27 30           DX
D6 31 27           DX
D7 99 32           DX
D8 99 33           DX
D9 50 32           DY
D10 50 33          DY
*
* MODELS USED
*
.MODEL QX PNP(BF = 5E5)
.MODEL DX          D(IS = lE-12)
.MODEL DY          D(IS = lE-15 BV = 50)
.MODEL DZ          D(IS = lE-15 BV = 7.0)
.MODEL DEN D(IS = lE-12 RS = 4.35K KF = 1.95E-15
AF = l) .MODEL DIN D(IS = lE-12 RS = 77.3E-6
KF = 3.38E-15 AF = 1) .ENDS OP-285
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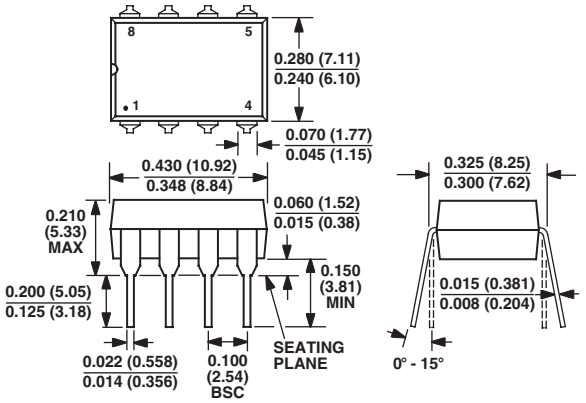
## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 8-Lead PDIP Package

### (N-8)




### 8-Lead SOIC Package

### (R-8)