# LV47022P

**Monolithic Linear IC**

# 4-Channel BTL Power Amplifier for Car Audio Systems

**ON Semiconductor®**

http://onsemi.com

## Overview

The LV47022P is the IC for 4-channel BTL power amplifier that is developed for car audio system.
Pch DMOS in the upper side of the output stage and Nch DMOS in the lower side of the output stage are complimentary. High power and high quality sound are realized by that.
This IC incorporate various functions (standby switch, muting function, and various protection circuit) necessary for car audio system. Also, it has a self-diagnosis function.

## Functions

- High output : $P_O$ max = 48W (typical) ($V_{CC}$ = 15.2V, f = 1kHz, $R_L$ = 4Ω, Max Power)
  : $P_O$ max = 28W (typical) ($V_{CC}$ = 14.4V, f = 1kHz, THD = 10%, $R_L$ = 4Ω)
  : $P_O$ max = 21W (typical) ($V_{CC}$ = 14.4V, f = 1kHz, THD = 1%, $R_L$ = 4Ω)
- Built-in muting function (pin 22)
- Built-in Standby switch (pin 4)
- Built-in Self-diagnosis function (pin 25) :
  Signal output in case of output offset detection, shorting to $V_{CC}$, shorting to ground, load shorting and over voltage.
- Circuit that decrease of Electric mirror noise and GSM noise.
- Built-in various protection circuit (shorting to ground, shorting to $V_{CC}$, load shorting, over voltage and thermal shut down)

Note 1 : Please do not mistake connection.
　　　　 A wrong connection may produce destruction, deterioration and damage for the IC or equipment.
Note 2 : The protective circuit function is provided to temporarily avoid abnormal state such as incorrect output connection. But, there is no guarantee that the IC is not destroyed by the accident.
　　　　 The protective function do not operate of the operation guarantee range. If the outputs are connected incorrectly, IC destruction may occur when used outside of the operation guarantee range.

# Specifications

## Absolute Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Maximum supply voltage | $V_{CC}$ max1 | No signal, t = 1 minute | 26 | V |
| | $V_{CC}$ max2 | During operations | 18 | V |
| Maximum output current | $I_O$ peak | Per channel | 4.5/ch | A |
| Allowable power dissipation | Pd max | With an infinity heat sink | 50 | W |
| Operating temperature | Topr | | -40 to +85 | °C |
| Storage temperature | Tstg | | -40 to +150 | °C |
| Junction temperature | Tj | | 150 | °C |
| Thermal resistance between the junction and case | θj-c | | 1 | °C/W |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

## Recommended Operating Ranges at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Recommended load resistance | $R_L$ op | | 4 | Ω |
| Operating supply voltage range | $V_{CC}$ op | A range not exceeding Pdmax | 8 to 16 | V |

## Electrical Characteristics at Ta = 25°C, $V_{CC}$ = 14.4V, $R_L$ = 4Ω, f = 1kHz, Rg = 600Ω

| Parameter | Symbol | Conditions | Ratings Min. | Ratings Typ. | Ratings Max. | Unit |
|---|---|---|---|---|---|---|
| Quiescent current | $I_{CCO}$ | $R_L$ = ∞, Rg = 0Ω | | 200 | 400 | mA |
| Standby current | Ist | Vst = 0V | | | 3 | μA |
| Voltage gain | VG | $V_O$ = 0dBm | 25 | 26 | 27 | dB |
| Voltage gain difference | ΔVG | | -1 | | +1 | dB |
| Output power | $P_O$ | THD = 10% | 23 | 28 | | W |
| | $P_O$ max1 | Max Power | | 43 | | W |
| | $P_O$ max2 | $V_{CC}$ = 15.2, Max Power | | 48 | | W |
| Output offset voltage | Vn offset | Rg = 0Ω | -100 | | +100 | mV |
| Total harmonic distortion | THD | $P_O$ = 4W | | 0.02 | 0.10 | % |
| Channel separation | CHsep | $V_O$ = 0dBm, Rg = 10kΩ | 55 | 65 | | dB |
| Ripple rejection ratio | SVRR | Rg = 0Ω, fr = 100Hz, $V_{CC}$R = 0dBm | 50 | 65 | | dB |
| Output noise voltage | $V_{NO}$ | Rg = 0Ω, B.P.F. = 20Hz to 20kHz | | 60 | 120 | μVrms |
| Input resistance | Ri | | 80 | 100 | 120 | kΩ |
| Mute attenuation | Matt | $V_O$ = 20dBm, mute : on | 80 | 90 | | dB |
| Standby pin control voltage | Vstby H | Amp : on | 2.5 | | $V_{CC}$ | V |
| | Vstby L | Amp : off | 0.0 | | 0.5 | V |
| Mute pin control voltage | Vmute H | Mute : off | 2.9 | | 6.0 | V |
| | Vmute L | Mute : on | 0.0 | | 1.0 | V |
| Output offset detection | | | | | | |
| Detection threshold voltage | Vosdet | | ±1.2 | ±1.8 | ±2.4 | V |

* 0dBm = 0.775Vrms

# LV47022P

## Block Diagram
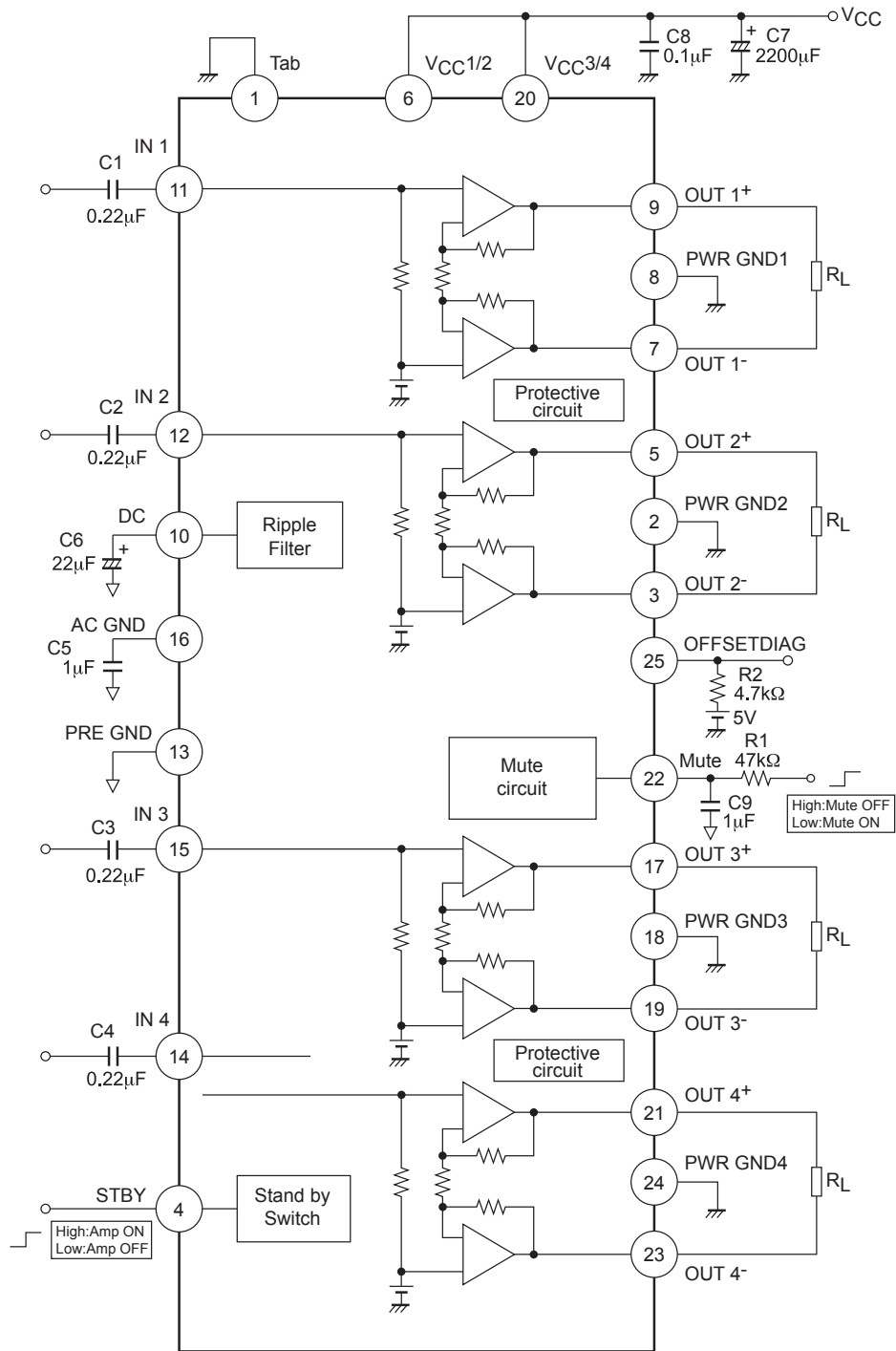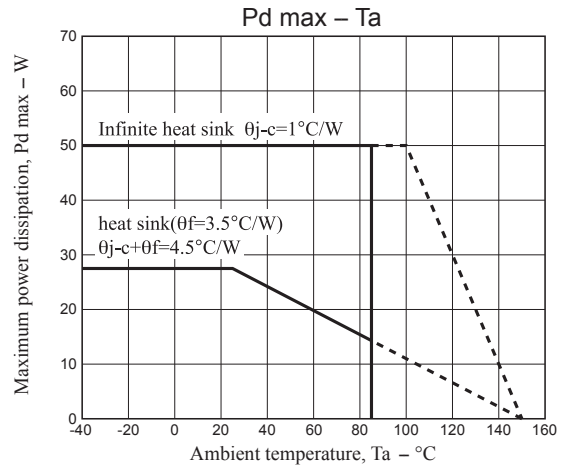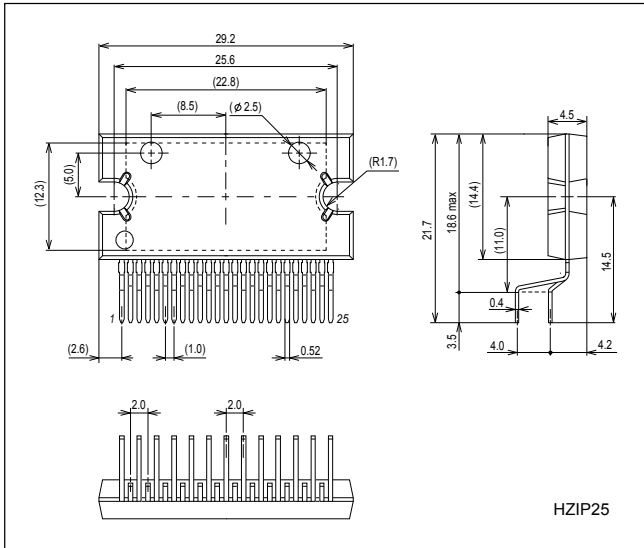


Important points
Please connect Pin1 line near C7 and C8. Because Pin1 is substrate of IC.

## Package Dimensions

unit : mm (typ)

3236A



Pd max – Ta

HZIP25

## External Components

| Part Name | Recommended Value | Purpose | Remarks |
|---|---|---|---|
| C1 to C4 | 0.22μF | Cuts DC voltage | The larger the constant value, the lower the cut-off frequency. When AMP ON, bigger value worse pop noise. The values of C1 to C4 must be the same. C1 to C4 must use capacitor of low leak current. |
| C5 | 1μF | Cuts DC voltage | The ratio of the input capacitance (C1 to C4) to the ACGND capacitance (C5) should be 1:4. If the ratio deviates, pop noise and SVRR are worse. Use capacitor same as C1 to C4. |
| C6 | 22μF | Reduces pop noise (AMP ON/OFF) Reduces ripples | The larger the constant value, the longer the amplifier ON/OFF time. The larger the constant value, SVRR is good. On the other hand, the smaller constant value. AMP ON/OFF will be shoeter. |
| C7 | 2200μF | Ripple filter | Eliminating power supply ripples. Please put near IC. |
| C8 | 0.1μF | Improves oscillation stability | Reducing high-frequency noise. Please put near IC. |
| C9 | 1μF | Reduces pop noise (Mute ON↔OFF) | The larger the constant value, pop noise is small. The large the constant value, the longer the mute ON/OFF time. On the other hand, the smaller constant value. Mute ON/OFF will be shorter. And, Mute ON↔OFF pop noise will be worse. |
| R1 | 47kΩ | | |
| R2 | 4.7kΩ | Pull-up resistor | Because of transistor ability in IC, Please use 2.2kΩ or more. |

* The components and constant values within the test circuit are used for confirmation of characteristics and are not guarantees that incorrect or trouble will not occur in application equipment.

## Explanation for the function

1. Standby switch function (pin 4)

   Threshold voltage of the Pin 4 is set by about 2VBE.

   The amplifier is turned on by the applied voltage of 2.5V or more. Also, the amplifier is turned off by the applied voltage of 0.5V or less.
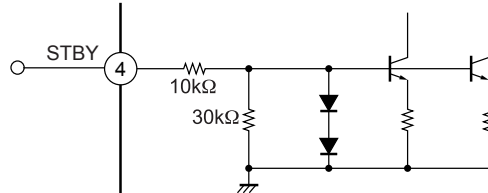


Fig1 Standby equivalent circuit

2. Muting function (Pin 22)

   The muting function is turned on by the applied voltage of 1.0V or less to 22pin. And the muting function is turn off by the applied voltage 2.9V or more.

   Also, the time constant of the muting function is determined by external capacitor and resistor constants.

   It is concerned with mute ON/OFF. After enough examination, please set it.

   Switching time

   Mute ON: $C9 \times R1$

   Mute OFF: $(C9 \times V) / I$ (V= When Mute ON Pin 22 voltage, I=about 5μA)
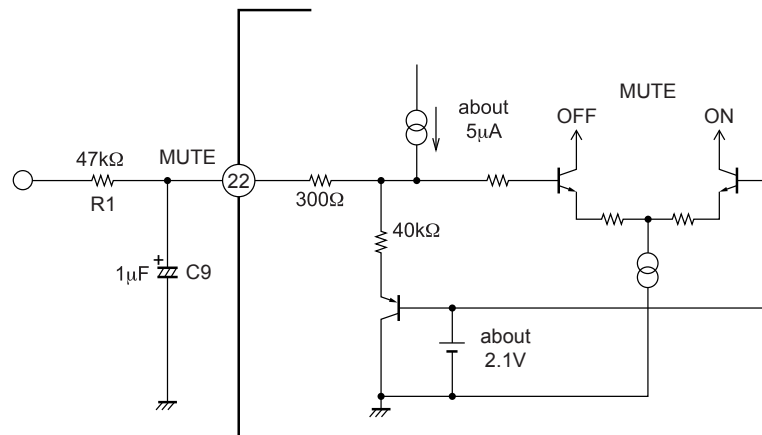


Fig2 Mute equivalent circuit

3. Input pin (Pin 11/ Pin 12/ Pin 14/ Pin 15), ACGND pin (Pin 16)

   The ratio of the input capacitance (C1 to C4) to the ACGND capacitance (C5) should be 1:4.

   Please use same kind of capacitor.

   Please connect the ACGND capacitor to PREGND.

   It is all five pin 100kΩ of input resistance.

   Do not input below 0V to Pin-IN (Pin 11/ Pin12/ Pin 14/ Pin15).

   If you input below 0V to Pin-IN, LV47022P can not function well.

4. Self-diagnostics function (Pin 25)
   In four modes to write below, the signal is output to the Pin 25.
   Also, by controlling the standby switch after the signal of the Pin 25 is detected by the microcomputer, the burnout of the speaker can be prevented.

   (1) Shorting to $V_{CC}$/Shorting to ground : The Pin 25 becomes the low level.
   (2) Load shorting                          : The Pin 25 is alternated between the low level and the high level according to the output signal.
   (3) Over voltage                           : When the voltage of $V_{CC}$ exceeds voltage 21V (typical), the Pin 25 becomes the low level.
   (4) Output offset detection                : When the output offset voltage exceeds the detection threshold voltage, the Pin 25 becomes the low level.

   In addition, the Pin 25 has become the NPN open collector output (active low).
   The Pin 25 must be left open when this function is not used.
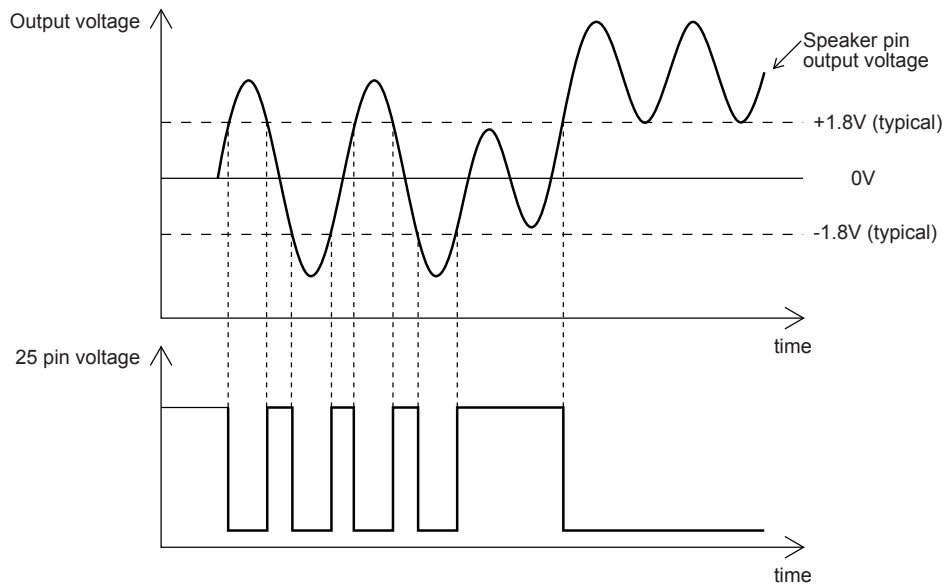
Fig3 Offset detection
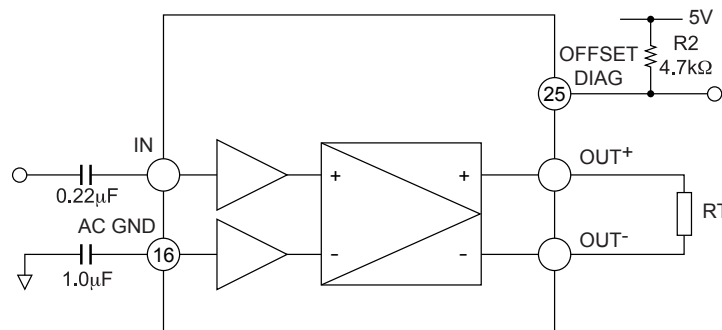
Fig4 Operating Pin 25

5. Sound quality (low frequencies)

By varying the value of input capacitor, low-frequency characteristic can be improved.

However, it is concerned the pop noise. Please confirm in each set when the capacitance value varies.

6. Pop noise

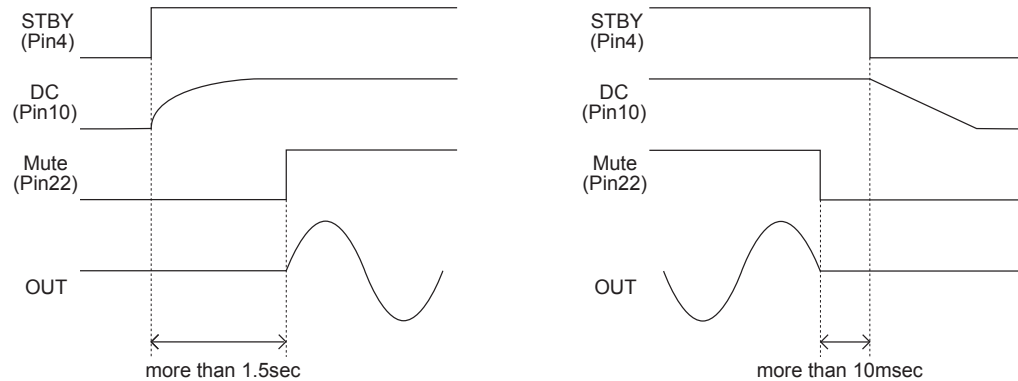For pop noise prevention, it is recommended to use the muting function at the same time.

  At AMP ON

    Set MUTE ON first, then set STBY pin High ( AMP ON).

    About 1.5sec later, set to be MUTE OFF.

  At AMP OFF

    After 10msec later MUTE ON, please do STBY pin Low ( AMP OFF).



7. Oscillation stability

Pay due attention on the following points because parasitic oscillation may occur due to effects of the board layout, etc.

Board layout

  • Provide the $V_{CC}$ capacitor of 0.1μF in the position nearest to IC.
  • PREGND must be independently wired and connected to the GND point that is as stable as possible, such as the minus pin of the 2200μF $V_{CC}$ capacitor.

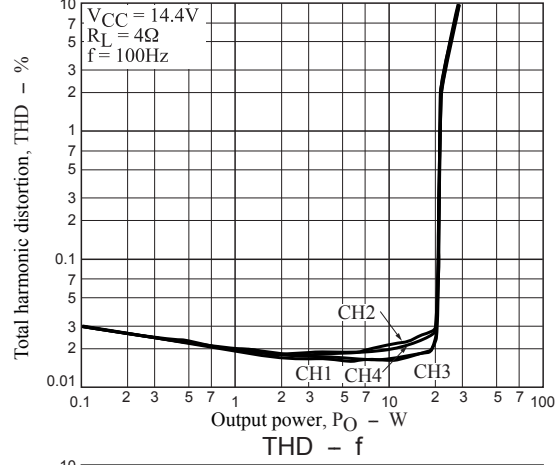In case of occurrence of parasitic oscillation, any one of following parts may be added as a countermeasure.
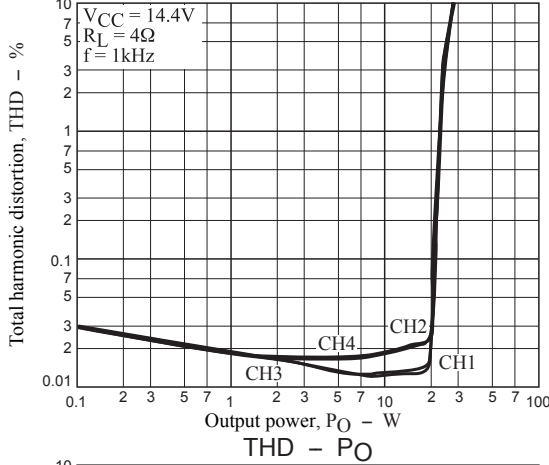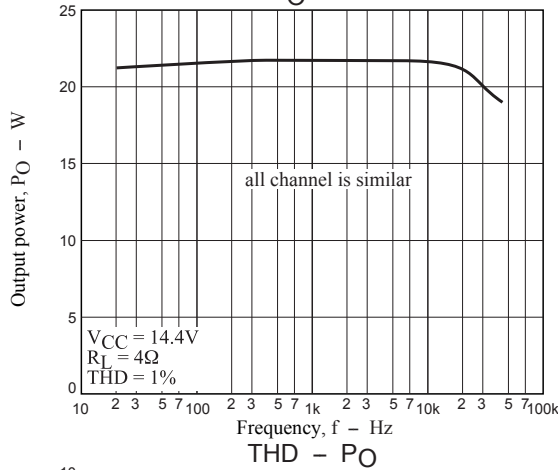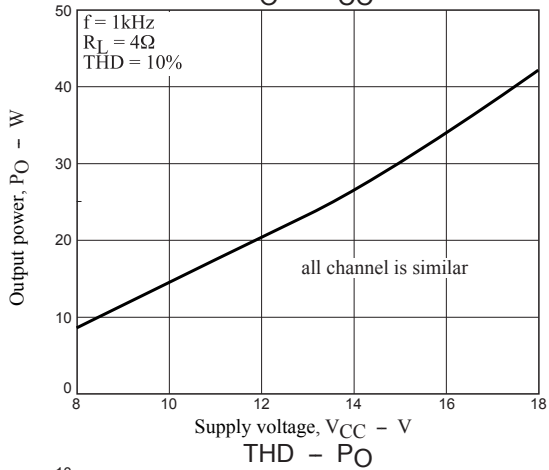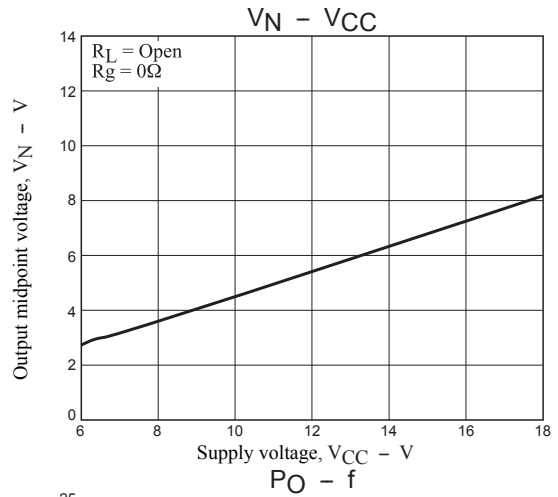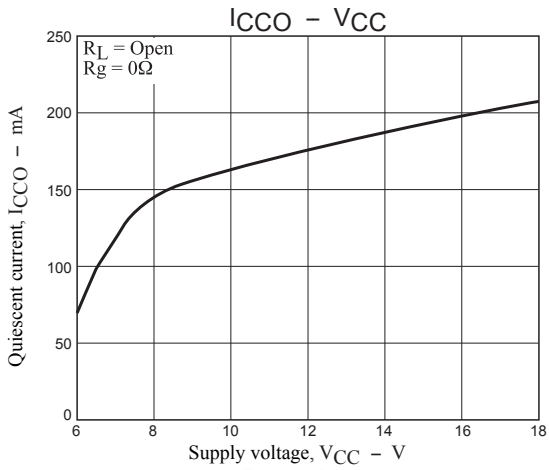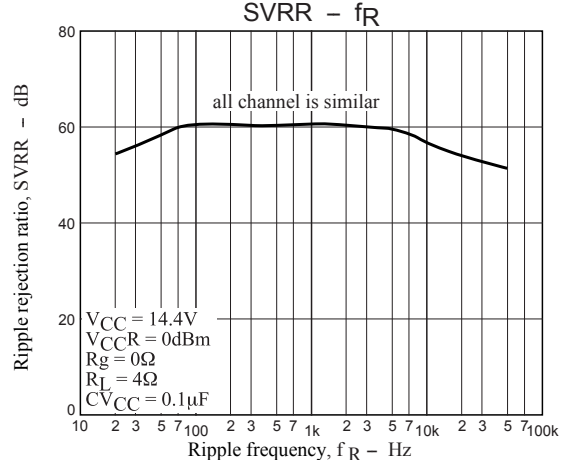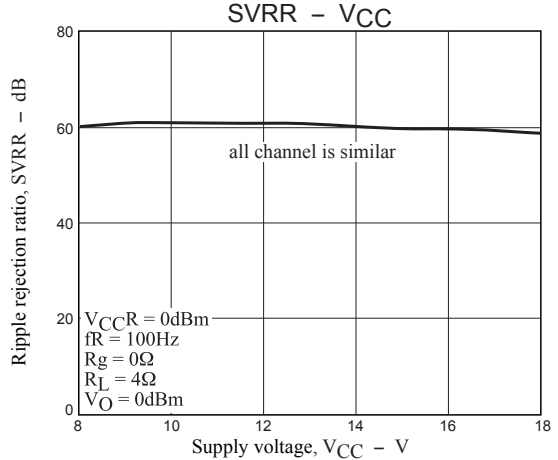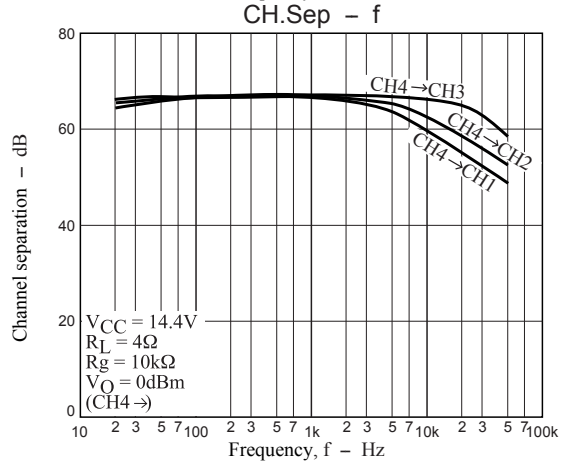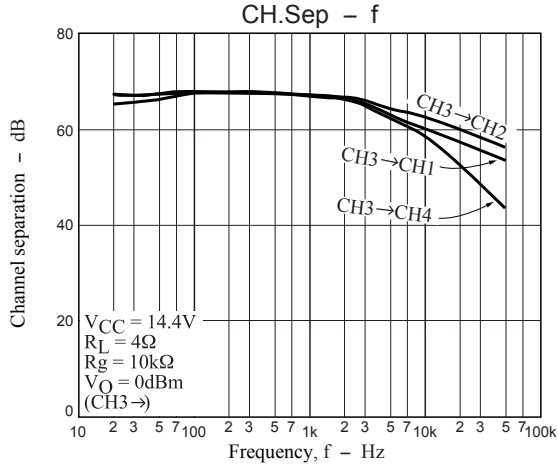
Please check your capacitor of optimal value at set
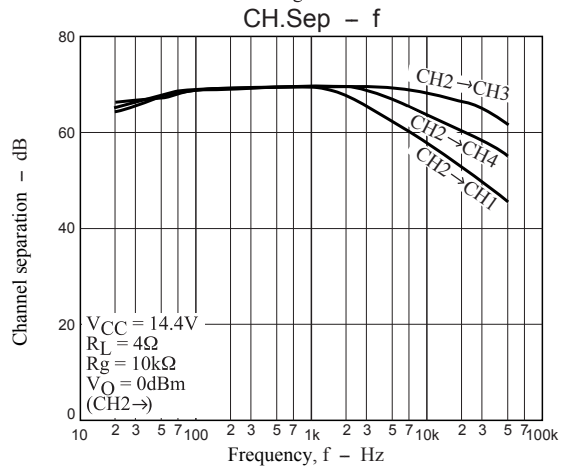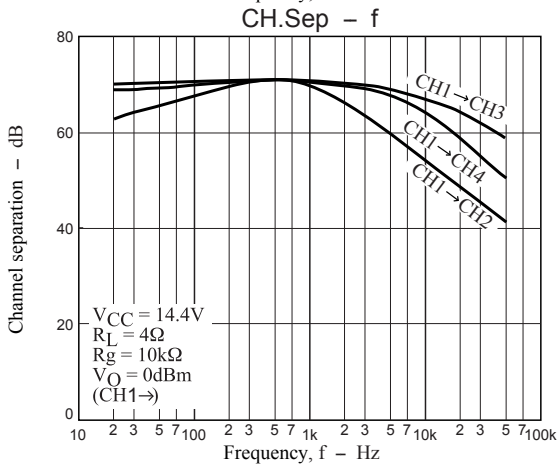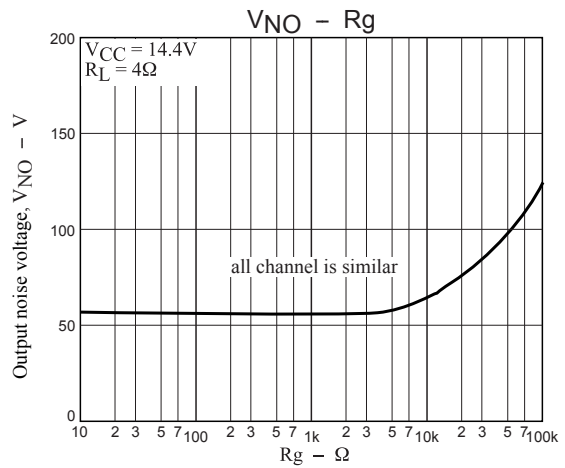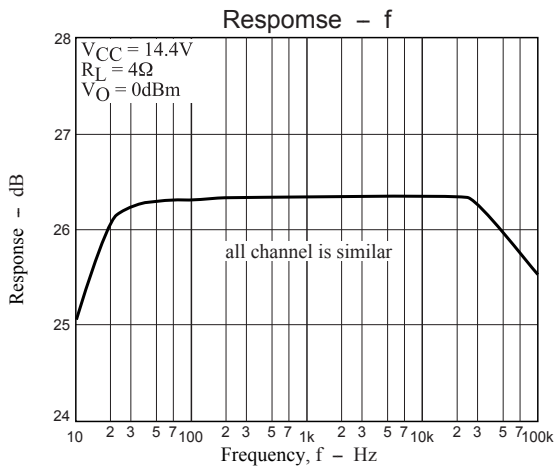
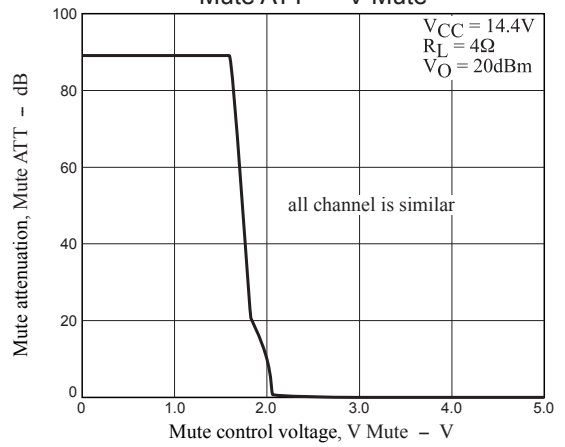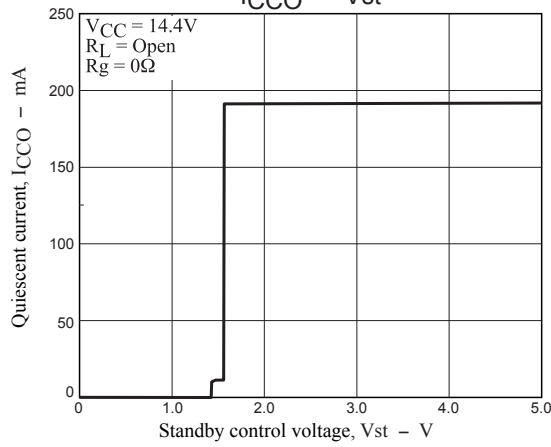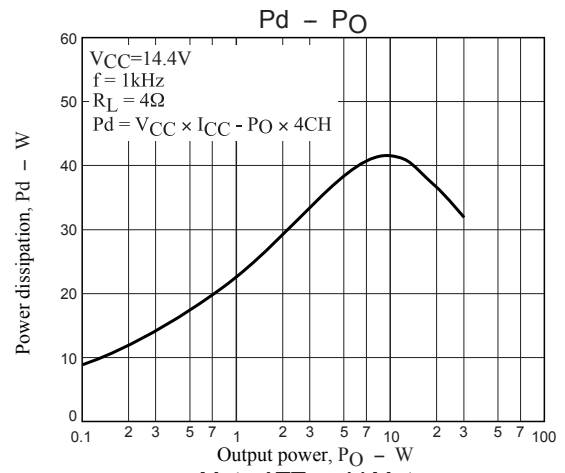  • Series connection of CR (0.1μF and 2.2Ω) between each output pin and GND.

8. EMC countermeasure

LV47022P has function that decrease of Electric mirror noise and GSM noise.

When you connect capacitor of more than 1000pF between out and GND because of EMC countermeasure, please add oscillation cut parts. Value of oscillation prevention parts recommends 2.2Ω + 0.1μF.

## $I_{CCO}$ – $V_{CC}$

$R_L$ = Open
$Rg$ = 0Ω

Quiescent current, $I_{CCO}$ – mA

Supply voltage, $V_{CC}$ – V

## $V_N$ – $V_{CC}$

$R_L$ = Open
$Rg$ = 0Ω

Output midpoint voltage, $V_N$ – V

Supply voltage, $V_{CC}$ – V

## $P_O$ – $V_{CC}$

f = 1kHz
$R_L$ = 4Ω
THD = 10%

Output power, $P_O$ – W

all channel is similar

Supply voltage, $V_{CC}$ – V

## $P_O$ – f

Output power, $P_O$ – W

all channel is similar

$V_{CC}$ = 14.4V
$R_L$ = 4Ω
THD = 1%

Frequency, f – Hz

## THD – $P_O$

$V_{CC}$ = 14.4V
$R_L$ = 4Ω
f = 1kHz

Total harmonic distortion, THD – %

CH2
CH4
CH3
CH1

Output power, $P_O$ – W

## THD – $P_O$

$V_{CC}$ = 14.4V
$R_L$ = 4Ω
f = 100Hz

Total harmonic distortion, THD – %

CH2
CH1 CH4 CH3

Output power, $P_O$ – W

## THD – $P_O$

$V_{CC}$ = 14.4V
$R_L$ = 4Ω
f = 10kHz

Total harmonic distortion, THD – %

CH3
CH1 CH2
CH4

Output power, $P_O$ – W

## THD – f

$V_{CC}$ = 14.4V
$R_L$ = 4Ω
$P_O$ = 4W

Total harmonic distortion, THD – %

CH1
CH2
CH3
CH4

Frequency, f – Hz

No.A2047-8/12

## Respomse – f



V_CC = 14.4V
R_L = 4Ω
V_O = 0dBm

all channel is similar

Response – dB

Frequency, f – Hz

## V_NO – Rg



V_CC = 14.4V
R_L = 4Ω

all channel is similar

Output noise voltage, V_NO – V

Rg – Ω

## CH.Sep – f



CH1→CH3
CH1→CH4
CH1→CH2

V_CC = 14.4V
R_L = 4Ω
Rg = 10kΩ
V_O = 0dBm
(CH1→)

Channel separation – dB

Frequency, f – Hz

## CH.Sep – f



CH2→CH3
CH2→CH4
CH2→CH1

V_CC = 14.4V
R_L = 4Ω
Rg = 10kΩ
V_O = 0dBm
(CH2→)

Channel separation – dB

Frequency, f – Hz

## CH.Sep – f



CH3→CH2
CH3→CH1
CH3→CH4

V_CC = 14.4V
R_L = 4Ω
Rg = 10kΩ
V_O = 0dBm
(CH3→)

Channel separation – dB

Frequency, f – Hz

## CH.Sep – f



CH4→CH3
CH4→CH2
CH4→CH1

V_CC = 14.4V
R_L = 4Ω
Rg = 10kΩ
V_O = 0dBm
(CH4→)

Channel separation – dB

Frequency, f – Hz

## SVRR – V_CC



all channel is similar

V_CCR = 0dBm
fR = 100Hz
Rg = 0Ω
R_L = 4Ω
V_O = 0dBm

Ripple rejection ratio, SVRR – dB

Supply voltage, V_CC – V

## SVRR – f_R



all channel is similar

V_CC = 14.4V
V_CCR = 0dBm
Rg = 0Ω
R_L = 4Ω
CV_CC = 0.1μF

Ripple rejection ratio, SVRR – dB

Ripple frequency, f_R – Hz

No.A2047-9/12

## Offset DIAG – $V_{CC}$

Detection threshold voltage, $V_{OSDET}$ - V

$R_g = 0\Omega$
$R_L = 4\Omega$

Detection Level

all channel is similar

Power supply, $V_{CC}$ - V

## $I_{CCO}$ – Vst

Quiescent current, $I_{CCO}$ – mA

$V_{CC} = 14.4V$
$R_L = $ Open
$R_g = 0\Omega$

Standby control voltage, Vst – V

## Pd – $P_O$

Power dissipation, Pd – W

$V_{CC} = 14.4V$
$f = 1kHz$
$R_L = 4\Omega$
$Pd = V_{CC} \times I_{CC} - P_O \times 4CH$

Output power, $P_O$ – W

## Mute ATT – V Mute

Mute attenuation, Mute ATT – dB

$V_{CC} = 14.4V$
$R_L = 4\Omega$
$V_O = 20dBm$

all channel is similar

Mute control voltage, V Mute – V

PS No.A2047-10/12

HZIP25 Heat sink attachment

Heat sinks are used to lower the semiconductor device junction temperature by leading the head generated by the device to the outer environment and dissipating that heat.

a.   Unless otherwise specified, for power ICs with tabs and power ICs with attached heat sinks, solder must not be applied to the heat sink or tabs.

b.   Heat sink attachment
     · Use flat-head screws to attach heat sinks.
     · Use also washer to protect the package.
     · Use tightening torques in the ranges 39-59Ncm(4-6kgcm) .
     · If tapping screws are used, do not use screws with a diameter larger than the holes in the semiconductor device itself.
     · Do not make gap, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
     · Take care a position of via hole .
     · Do not allow dirt, dust, or other contaminants to get between the semiconductor device and the tab or heat sink.
     · Verify that there are no press burrs or screw-hole burrs on  the heat sink.
     · Warping in heat sinks and printed circuit boards must be no more than 0.05 mm between screw holes, for either concave or convex warping.
     · Twisting  must be limited to under 0.05 mm.
     · Heat sink and semiconductor device are mounted in parallel.
       Take care of electric or compressed air drivers
     · The speed of these torque wrenches should never exceed 700 rpm, and should typically be about 400 rpm.

○                          ×

Binding head             Countersunk head
machine screw            mashine screw

Heat sink

gap

Via hole
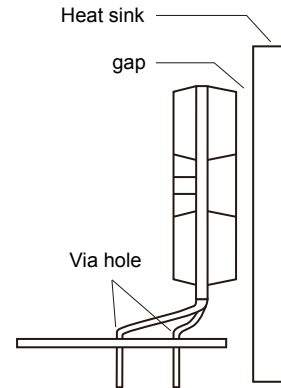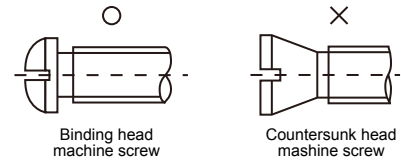
c.   Silicone grease
     · Spread the silicone grease evenly when mounting heat sinks.
     · Our company recommends YG-6260 (Momentive Performance Materials Japan LLC)

d.   Mount
     · First mount the heat sink on the semiconductor device, and then mount that assembly on the printed circuit board.
     · When attaching a heat sink after mounting a semiconductor device into the printed circuit board, when tightening up a heat sink with the screw, the mechanical stress which is impossible to the semiconductor device and the pin doesn't hang.

e.   When mounting the semiconductor device to the heat sink using jigs, etc.,
     · Take care not to allow the device to ride onto the jig or positioning dowel.
     · Design the jig so that no unreasonable mechanical stress is not applied to the semiconductor device.

f.   Heat sink screw holes
     · Be sure that chamfering and shear drop of heat sinks must not be larger than the diameter of screw head used.
     · When using nuts, do not make the heat sink hole diameters larger than the diameter of the head of the screws used. A hole diameter about 15% larger than the diameter of the screw is desirable.
     · When tap screws are used, be sure that the diameter of the holes in the heat sink are not too small. A diameter about 15% smaller than the diameter of the screw is desirable.

g.   There is a method to mount the semiconductor device to the heat sink by using a spring band.  But this method is not recommended because of possible displacement due to fluctuation of the spring force with time or vibration.