TFA9812

BTL stereo Class-D audio amplifier with I²S input

Rev. 02 — 22 January 2009 Preliminary data sheet

1. General description

The TFA9812 is a high-efficiency Bridge Tied Load (BTL) stereo Class-D audio amplifier with a digital I²S audio input. It is available in a HVQFN48 package with exposed die paddle. The exposed die paddle technology enhances the thermal and electrical performances of the device.

The TFA9812 features digital sound processing and audio power amplification. It supports I²C control mode and Legacy mode. In Legacy mode I²C involvement is not needed because the key features are controlled by hardware pin connections.

A continuous time output power of 2×12 W (R_L = 8 Ω, V_{DDP} = 15 V) is supported without an external heat sink. Due to the implementation of a programmable thermal foldback even for high supply voltages, higher ambient temperatures, and/or lower load impedances, the device operates without sound interrupting behavior.

TFA9812 is designed in such a way that it starts up easily (no special power-up sequence required). It features various soft and hard impact protection mechanisms to ensure an application that is both user friendly and robust.

A modulation technique is applied for the TFA9812, which supports common mode choke approach (1 common mode choke only per BTL amplifier stage). This minimizes the number of external components.

2. Features

2.1 General features

- 3.3 V and 8 V to 20 V external power supply
- High efficiency and low power dissipation
- Speaker outputs fully short circuit proof across load, to supply lines and ground
- Pop noise free at power-up/power-down and sample rate switching
- Low power Sleep mode
- Overvoltage and undervoltage protection on the 8 V to 20 V power supply
- Undervoltage protection on the 3.3 V power supply
- Overcurrent protection (no audible interruptions)
- Overdissipation protection
- Thermally protected and programmable thermal foldback
- Clock error protection
- I²C mode control or Legacy mode (i.e. no I²C) control
- Four different I²C addresses supported
- Internal Phase-Locked Loop (PLL) without using external components

- No high system clock required (PLL is able to lock on BCK)
- No external heat sink required
- 5 V tolerant digital inputs
- Supports dual coil inductor application
- Easy application and limited external components required

2.2 DSP features

- Digital parametric 10-band equalizer
- Digital volume control per channel
- Selectable +24 dB gain boost
- Analog interface to digital volume control in Legacy mode
- Digital clip level control
- Soft and hard mute
- Thermal foldback threshold temperature control
- De-emphasis
- Output power limiting control
- Polarity switch
- Four Pulse Width Modulation (PWM) switching frequency settings

2.3 Audio data input interface format support

- Master or slave Master Clock (MCLK), Bit Clock (BCK) and Word Select (WS) signals
- Philips I²S, standard I²S
- Japanese I²S, Most Significant Bit (MSB) justified
- Sony I²S, Least Significant Bit (LSB) justified
- Sample rates from 8 kHz to 192 kHz

3. Applications

- Digital-in Class-D audio amplifier applications
- CRT and flat-panel television sets
- Flat-panel monitors
- Multimedia systems
- Wireless speakers
- Docking stations for MP3 players

4. Quick reference data

Table 1. Quick reference table

Unless specified otherwise, $V_{DDA} = V_{DDP} = 12$ V, $V_{SSP1} = V_{SSP2} = 0$ V, $V_{DDA(3V3)} = V_{DDD(3V3)} = 3.3$ V, $V_{SS1} = V_{SS2} = REFD = REFA = 0$ V, $T_{amb} = 25$ °C, $R_L = 8\ \Omega$, $f_i = 1$ kHz, $f_s = 44.1$ kHz, $f_{sw} = 400$ kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
General							
V_{DDA}	analog supply voltage			8	12	20	V
V_{DDP}	power supply voltage			8	12	20	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)			3.0	3.3	3.6	V
I_P	supply current	soft mute mode, with load, filter and snubbers connected	[1]	-	38	45	mA
		sleep mode	[1]	-	160	270	µA
$I_{DDA(3V3)}$	analog supply current (3.3 V)	operating mode					
		I²S slave mode		-	2	4	mA
		I²S master mode		-	4	6	mA
		sleep mode					
		$V_{DDA} = V_{DDP} = 12$ V		-	120	-	µA
		$V_{DDA} = V_{DDP} = 1$ V		-	40	70	µA
$I_{DDD(3V3)}$	digital supply current (3.3 V)	operating mode					
		I²S slave mode		-	15	25	mA
		I²S master mode		-	25	40	mA
		sleep mode; DATA = WS = BCK = MCLK = 0 V		-	4	30	µA
$P_{o(RMS)}$	RMS output power	Continuous time output power per channel; THD = 10 %; $R_L = 8\ \Omega$					
		$V_{DDA} = V_{DDP} = 12$ V		-	8.3	-	W
		$V_{DDA} = V_{DDP} = 13.5$ V		-	10	-	W
		$V_{DDA} = V_{DDP} = 15$ V		-	12	-	W
		Short time (≤ 10 s) output power per channel; THD = 10 %; $R_L = 8\ \Omega$					
		$V_{DDA} = V_{DDP} = 17$ V		-	15	-	W
η_{po}	output power efficiency	$R_L = 8\ \Omega$; $P_{o(RMS)} = 8.3$ W		-	88	-	%

[1] I_P is the current through the analog supply voltage (V_{DDA}) pin added to the current through the power supply voltage (V_{DDP}) pin.

5. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
TFA9812HN	HVQFN48	plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 × 7 × 0.85 mm	SOT619-8

6. Block diagram

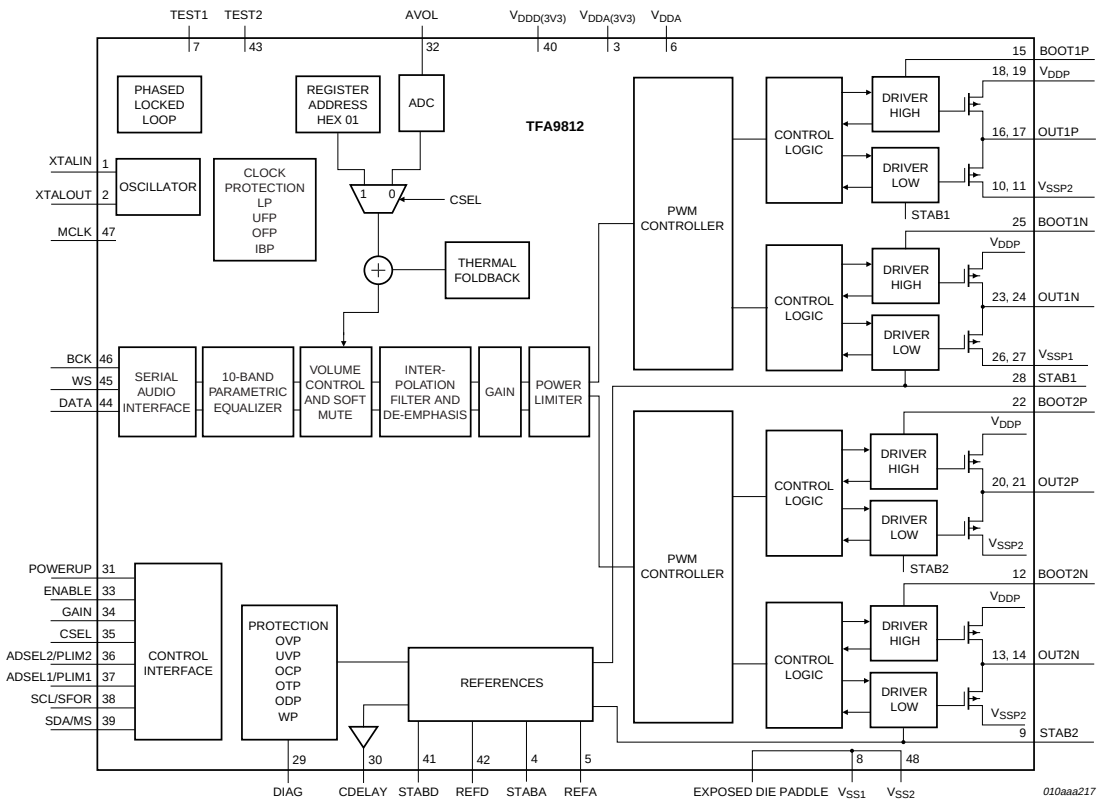


Fig 1. TFA9812 block diagram

Figure 1 shows the block diagram of the TFA9812. For a detailed description of the audio signal path see Section 8.1.

7. Pinning information

7.1 Pinning

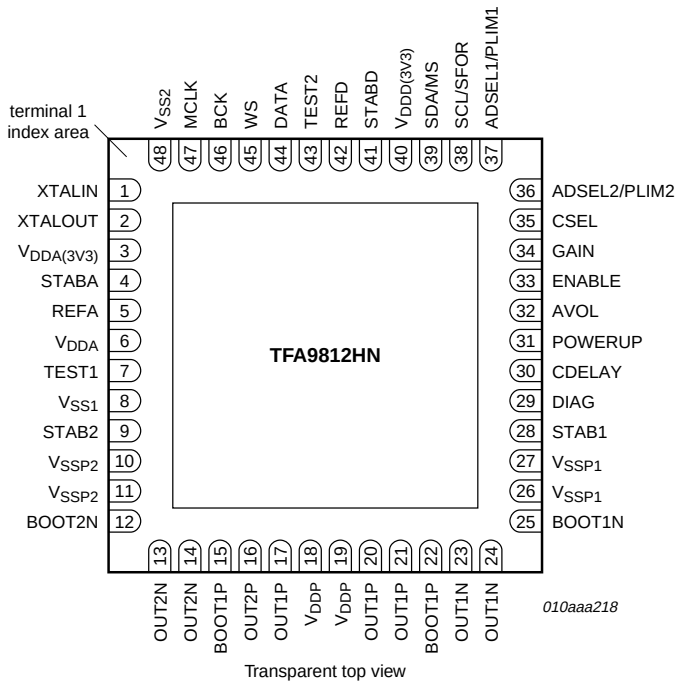


Fig 2. Pin configuration, transparent top view

Table 3. Pinning description TFA9812

Pin	Symbol	Type	Description
1	XTALIN	I	Crystal oscillator input
2	XTALOUT	O	Crystal oscillator output
3	$V_{DDA(3V3)}$	P	Analog supply voltage (3.3 V)
4	STABA	O	1.8 V analog stabilizer output
5	REFA	P	Analog reference voltage
6	V_{DDA}	P	Analog supply voltage (8 V to 20 V)
7	TEST1	I	Test signal input 1. For test purposes only (connect to V_{SS})
8	V_{SS1}	P	PCB ground reference
9	STAB2	O	Decoupling of internal 11 V regulator for channel 2 drivers
10	V_{SSP2}	P	Negative power supply voltage for channel 1 and channel 2
11	V_{SSP2}	P	Negative power supply voltage for channel 1 and channel 2
12	BOOT2N	O	Bootstrap high-side driver negative PWM output channel 2
13	OUT2N	O	Negative PWM output channel 2

Table 3. Pinning description TFA9812 *…continued*

Pin	Symbol	Type	Description
14	OUT2N	O	Negative PWM output channel 2
15	BOOT1P	O	Bootstrap high-side driver positive PWM output channel 1
16	OUT1P	O	Positive PWM output channel 1
17	OUT1P	O	Positive PWM output channel 1
18	V_{DDP}	P	Positive power supply voltage (8 V to 20 V)
19	V_{DDP}	P	Positive power supply voltage (8 V to 20 V)
20	OUT2P	O	Positive PWM output channel 2
21	OUT2P	O	Positive PWM output channel 2
22	BOOT2P	O	Bootstrap high-side driver positive PWM output channel 2
23	OUT1N	O	Negative PWM output channel 1
24	OUT1N	O	Negative PWM output channel 1
25	BOOT1N	O	Bootstrap high-side driver negative PWM output channel 1
26	V_{SSP1}	P	Negative power supply voltage for channel 1 and channel 2
27	V_{SSP1}	P	Negative power supply voltage for channel 1 and channel 2
28	STAB1	O	Decoupling of internal 11 V regulator for channel 1 drivers
29	DIAG	O	Fault mode indication output (open-drain pin)
30	CDELAY	I	Timing reference
31	POWERUP	I	Power-up pin to switch between Sleep and other operational modes
32	AVOL	I	Analog volume control (Legacy mode)
33	ENABLE	I	Enable input to switch between 3-state and other operational modes
34	GAIN	I	Gain selection input to select between 0 dB and +24 dB gain (Legacy mode)
35	CSEL	I	Control selection input to select between Legacy mode (no I²C bus control) and I²C bus control
36	ADSEL2/PLIM2	I	Address selection in I²C mode input 2, power limiter selection input 2 in Legacy mode
37	ADSEL1/PLIM1	I	Address selection in I²C mode input 1, power limiter selection input 1 in Legacy mode
38	SCL/SFOR	I	I²C bus clock input in I²C mode, I²S serial data format selection input in Legacy mode
39	SDA/MS	I/O	I²C bus data input and output in I²C mode, master/slave selection input in Legacy mode
40	$V_{DDD(3V3)}$	P	Digital supply voltage (3.3 V)
41	STABD	O	1.8 V digital stabilizer output
42	REFD	P	Digital reference voltage
43	TEST2	I	Test signal input 2; for test purposes only (connect to V_{SS})
44	DATA	I	I²S bus data input
45	WS	I/O	I²S bus word select input (I²S slave mode) or output (I²S master mode)
46	BCK	I/O	I²S bus bit clock input (I²S slave mode) or output (I²S master mode)

Table 3. Pinning description TFA9812 *…continued*

Pin	Symbol	Type	Description
47	MCLK	I/O	Master clock input (I²S slave mode) or output (I²S master mode)
48	V_{SS2}	P	PCB ground reference
Exposed die-paddle	-	P	PCB ground reference

8. Functional description

8.1 General

The TFA9812 is a high-efficiency stereo BTL Class-D amplifier with a digital I²S audio input. It supports all commonly used I²S formats.

Figure 1 shows the functional block diagram, which includes the key function blocks of the TFA9812. In the digital domain the audio signal is processed and converted to a pulse width modulated signal using BD modulation. A BTL configured power comparator carries out power amplification.

The audio signal processing path is as follows:

1. The Digital Audio Input (DAI) block translates the I²S (-like) input signal into a standard internal stereo audio stream.
2. The 10-band parametric equalizer can optionally equalize the stereo audio stream. Both channels have separate equalization streams. It can be used for speaker transfer curve compensation to optimize the audio performance of applied speakers.
3. Volume control in the TFA9812 is done by attenuation. The attenuation depends on the volume control settings and the thermal foldback value. Soft mute is also arranged at this part. In Legacy mode the volume control is done by an on-board Analog-to-Digital Converter (ADC) which measures the analog voltage on pin 32.
4. The interpolation filter interpolates from 1 fs to the PWM controller sample rate (2048 fs at 44.1 kHz) by cascading FIR filters.
5. The gain block can boost the signal with 0 dB or +24 dB. Four specific gain settings are also provided in this block. These specific gain settings are related to maximum clip levels of < 0.5 %, 10 %, 20 % or 30 % THD at the TFA9812 output. These maximum clip levels are only valid with the gain boost set to 0 dB and a 0 dBFS input signal.
6. The power limiter limits the maximum output signal of the TFA9812. The power limiter settings are 0 dB, –1.5 dB, –3 dB, and –4.5 dB. This function can be used to reduce the maximum output power delivered to the speakers at a fixed supply voltage and speaker impedance.
7. The PWM controller block transforms the audio signal into a BD-modulated PWM signal. The BD-modulation provides a high signal-to-noise performance and eliminates clock jitter noise.
8. Via four differential comparators the PWM signals are amplified by two BTL power output stages. By default the left audio signal is connected to channel 1 and the right audio signal to channel 2.

The block control defines the operational control settings of the TFA9812 in line with the actual I²C settings and the pin-controlled settings.

The PLL block creates the system clock and can take the I²S BCK, the MCLK or an external crystal as reference source.

The following protections are built into the TFA9812:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- Window Protection (WP)
- Lock Protection (LP)
- UnderFrequency Protection (UFP)
- OverFrequency Protection (OFP)
- Invalid BCK Protection (IBP)
- DC-blocking
- ElectroStatic Discharge (ESD)

8.2 Functional modes

8.2.1 Control modes

The two control modes of the TFA9812 are I²C and legacy.

- In I²C mode the I²C format control is enabled.
- In Legacy mode a pin-based subset of the control options is available. The control settings for features which are not available in Legacy mode are set to the default I²C register settings.

The control mode is selected via pin CSEL as shown in Table 4.

Table 4. Control mode selection

CSEL Pin value	Control mode
0	Legacy (no I²C)
1	I²C

In the functional descriptions below the control for the various functions will be described for each control mode. Section 9.6 summarizes the support given by each control mode for the various TFA9812 functions.

8.2.2 Key operating modes

There are six key operating modes:

- In **Sleep** mode the voltage supplies are present, but power consumption for the whole device is reduced to the minimum level. The output stages in Sleep mode are 3-state and I²C communication is disabled.

- In **Soft mute** mode the I²S input signal is overruled with a soft mute.
  - In Legacy control mode the analog input pin AVOL controls Soft mute mode.
  - In I²C control mode I²C control can be used to enable an automatic soft mute function. See also Section 8.5.3.
- In **Hard mute** mode the PWM controller is overruled with a 50 % duty cycle square pulse. The Hard mute mode is only available in I²C control mode.
- In **Operating** mode the TFA9812 amplifies the I²S audio input signal in line with the actual control setting.
- In **3-state** mode the output stages are switched off.
- **Fault** mode is entered when a fault condition is detected by one or more of the protection mechanisms implemented in the TFA9812. In Fault mode the actual device configuration depends on the fault detected: see Section 8.7 for more information. Fault mode is for a subset of the faults flagged on the DIAG output pin. When the DIAG pin is flagged the output stages will be forced to enter 3-state mode. In Sleep mode the DIAG pin will not flag fault modes.

Table 5. Operational mode selection

Pin:				DIAG Output	Operational mode selected:
POWERUP	ENABLE	CSEL	AVOL		
0	-	-	-	floating	Sleep mode
1	-	-	-	0 / floating	Fault mode (enabled by system)[1]
1	1	1	-	floating	Soft mute mode (in I²C control mode)[2]
1	1	0	< 0.8 V	floating	Soft mute (in Legacy control mode)
1	0	-	-	floating	3-state mode
1	1	-	-	floating	Operational mode

[1] Clocking faults do not trigger DIAG output.

[2] Under these conditions soft mute still has to be enabled by the appropriate I²C setting.

8.2.3 I²S master/slave modes and MCLK/BCK clock modes

The I²S interface can be set in master or in slave.

- In **I²S master** mode the PLL locks to the output signal of the internal crystal oscillator circuit which uses an external crystal. The BCK, WS and MCLK signals are generated by the TFA9812. On the MCLK pin the TFA9812 delivers a master clock running at the crystal frequency.
- In **I²S slave** mode the PLL can lock to:
  - The external MCLK signal on the MCLK pin called **MCLK clock** mode.
  - The I²S input BCK signal on the BCK pin called **BCK clock** mode.

The I²S master or slave mode can be selected:

- In I²C control mode by selecting the right I²C setting.
- In legacy control mode by selecting the right setting on the SDA/MS pin.

Table 6. I²S master/slave mode selection

Pin value		Clock mode	I²S mode
CSEL	SDA/MS		
0	0	legacy	slave
0	1	legacy	master
1	-	I²C	slave or master[1]

[1] Under these conditions the mode is enabled by the appropriate I²C setting.

In I²S slave mode selection between BCK and MCLK clock modes is automatic.

MCLK clock mode is given higher priority than BCK. If the MCLK clock is judged valid by the protection circuit then MCLK clock mode is enabled. BCK clock mode is enabled when the MCLK clock is invalid (e.g. not available) and the BCK clock is judged valid by the protection circuit (see Section 8.7.11).

Table 7 shows the supported crystal frequencies in I²S master mode.

Table 8 shows the supported MCLK frequencies in MCLK mode (I²S slave mode).

Table 9 shows the supported BCK frequencies in BCK mode (I²S slave mode).

Table 7. Valid crystal frequencies in I²S master mode

Control mode	f_s (kHz)	Crystal frequency (MHz)
I²C	8, 16, 32, 64, 128	8.192
	11.025, 22.05, 44.1, 88.2, 176.4	11.2896
	12, 24, 48, 96, 192	12.288
Legacy	32	8.192
	44.1	11.2896
	48	12.288

Table 8. Valid MCLK frequencies in I²S slave mode

Control mode	f_s (kHz)	MLCK frequency (MHz)
I²C	8, 16, 32, 64, 128	8.192
		12.288
	32	18.432 (576 f_s)
	11.025, 22.05, 44.1, 88.2, 176.4	11.2896
		16.9344
	44.1	25.4016 (576 f_s)
	12, 24, 48, 96, 192	12.288
		18.432
	48	27.648 (576 f_s)

Table 8. Valid MCLK frequencies in I²S slave mode

Control mode	f_s (kHz)	MLCK frequency (MHz)
Legacy	32	8.192
		12.288
		18.432 (576 f_s)
	44.1	11.2896
		16.9344
		25.4016 (576 f_s)
	48	12.288
		18.432
		27.648 (576 f_s)

Table 9. Valid BCK frequencies in I²S slave mode

Control mode	f_s (kHz)	BCK (x f_s input)
I²C	8 to 192[1]	32 f_s
	8 to 192[1]	48 f_s
	8 to 192[1]	64 f_s
Legacy	32, 44.1, 48	32 f_s
	32, 44.1, 48	48 f_s
	32, 44.1, 48	64 f_s

[1] The valid sample frequencies are shown in Section 9.5.7.

8.3 Power-up/power-down

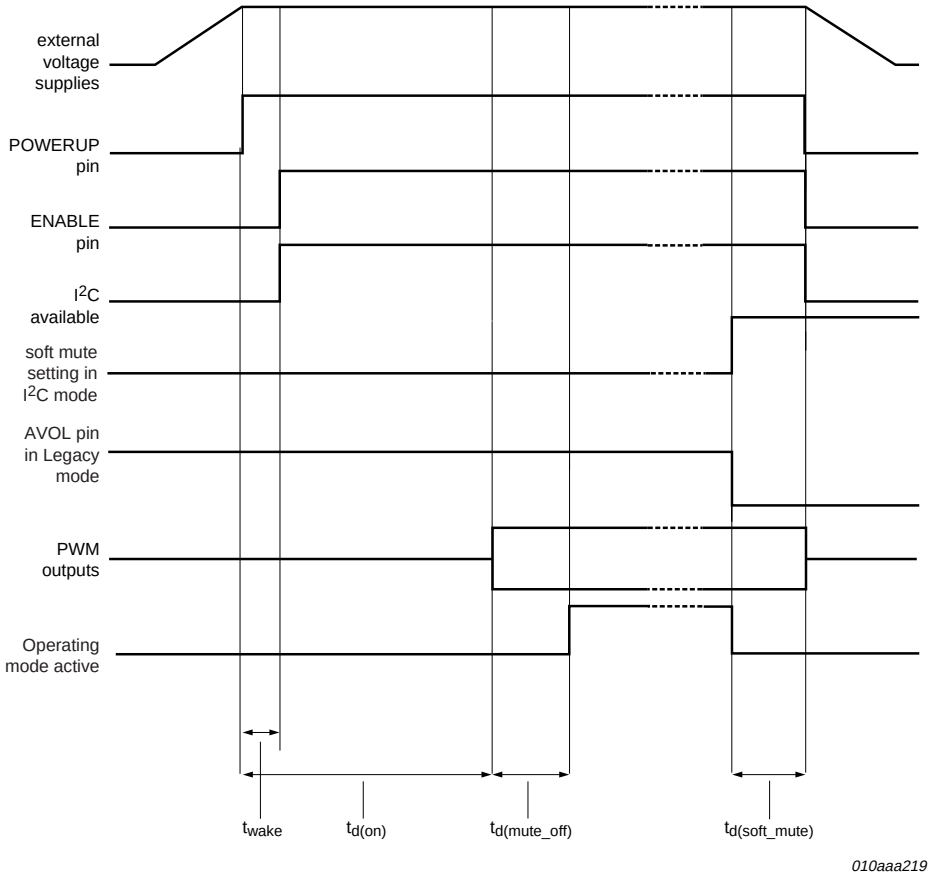


Fig 3. Power-up/power-down timing

8.3.1 Power-up

Figure 3 and Table 10 describe the power-up timing while Table 11 shows the pin control for initiating a power-up reset.

Table 10. Power-up/power-down timing

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{wake}	wake-up time	I²C control	-	4	-	ms
$t_{d(on)}$	turn-on delay time	-	70	-	135	ms
$t_{d(mute\_off)}$	mute off delay time	-	-	-	$128/f_s$	s
$t_{d(soft\_mute)}$	Soft mute delay time	I²C control	-	-	$128/f_s$	s
		legacy control[1]	-	15	-	ms

[1] Mute in Legacy mode is controlled by AVOL pin.

In I²C control mode communication is enabled after 4 ms. The preferred I²C settings can be made within 66 ms before the PLL starts running. Finally, the output stages are enabled and the audio level is increased via a demute sequence if mute has previously been disabled.

Remark: In I²C mode soft mute is enabled by default. It can be disabled at any time while I²C communication is valid. In order to prevent audio clicks volume control (default setting is 0 dB) should be set before soft mute is disabled.

Remark: For a proper start-up in I²S master mode and I²C mode the following sequence should be followed:

1. The I²S master setting should be set and keep the default sample rate setting active.
2. Next, another sample rate setting than the default one should be selected.
3. Finally, when the default sample rate is used the default sample rate setting should be selected again.

8.3.2 Power-down

Figure 3 includes the power-down timing while Table 11 shows the pin control for enabling power-down.

Table 11. Power-up/power-down selection

Power-up pin value	Description
0	Power-down (Sleep mode)
1	Power-up

Putting the TFA9812 into power-down is equivalent to enabling Sleep mode (see Section 8.2.2). This mode is entered immediately and no additional clock cycles are required.

In order to prevent audible clicks, soft mute should be enabled at least $T_{d(soft\_mute)}$ seconds before enabling Sleep mode.

The specified low current and power conditions in Table 1 are valid within 10 µs after enabling Sleep mode.

8.4 Digital audio data input

8.4.1 Digital audio data format support

The TFA9812 supports a commonly used range of I²S and I²S-like digital audio data input formats. These are listed in Table 12.

Table 12. Supported digital audio data formats

BCK frequency	Interface format (MSB first)	Supported in I²C control mode	Supported in Legacy control mode
32 f_s	I²S up to 16-bit data	yes	yes
32 f_s	MSB-justified 16-bit data	yes	yes
32 f_s	LSB-justified 16-bit data	yes	yes
48 f_s	I²S up to 24-bit data	yes	yes
48 f_s	MSB-justified up to 24-bit data	yes	yes

Table 12. Supported digital audio data formats

BCK frequency	Interface format (MSB first)	Supported in I²C control mode	Supported in Legacy control mode
48 f_s	LSB-justified 16-bit data	yes	no
48 f_s	LSB-justified 18-bit data	yes	no
48 f_s	LSB-justified 20-bit data	yes	no
48 f_s	LSB-justified 24-bit data	yes	yes
64 f_s	I²S up to 24-bit data	yes	yes
64 f_s	MSB-justified up to 24-bit data	yes	yes
64 f_s	LSB-justified 16-bit data	yes	no
64 f_s	LSB-justified 18-bit data	yes	no
64 f_s	LSB-justified 20-bit data	yes	no
64 f_s	LSB-justified 24-bit data	yes	no

Remark: Only MSB-first formats are supported.

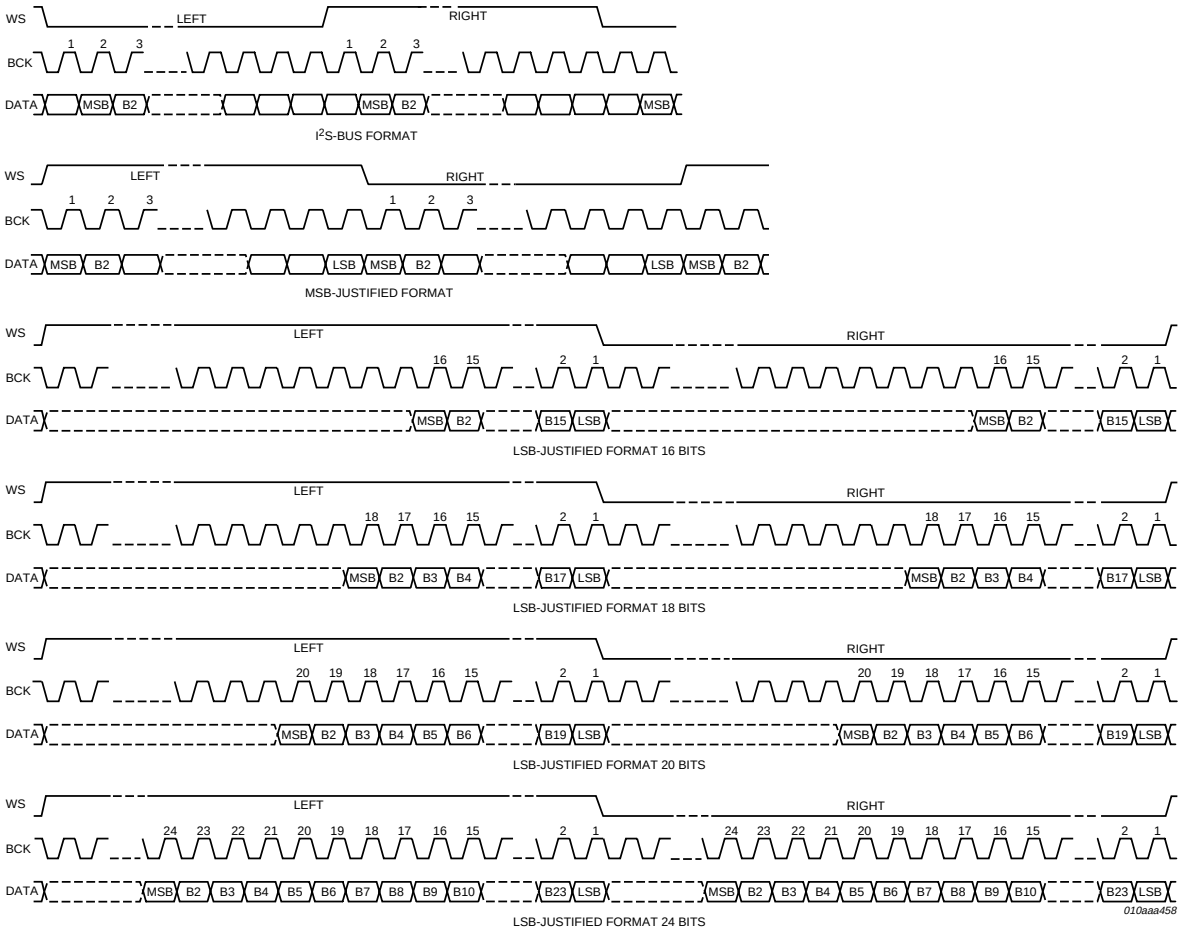


Fig 4. Serial interface input and output formats

In I²C control mode the following sample frequency f_s can be used: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz or 192 kHz. The I²C control for f_s selection can be found in Section 9.5.7.

In Legacy control mode the following sample frequencies (f_s) can be used: 32 kHz, 44.1 kHz or 48 kHz.

8.4.2 Digital audio data format control

The BCK-to-WS and MCLK-to-WS frequency ratios are automatically detected, so no control settings need to be configured for these.

In I²C control mode all the formats listed in Table 12 are supported. The appropriate I²C controls for selecting the supported formats can be found in Section 9. In the Legacy control mode only a subset of the supported formats can be used. These are shown in Table 12 and the required pin control is given in Table 13.

See Section 8.2.1 for details of how to enable Legacy control mode.

Table 13. Digital audio data format selection in Legacy control mode

SCL/SFOR pin value	Interface formats (MSB-first)
0	I²S
1	MSB-justified

8.5 Digital signal-processing features

8.5.1 Equalizer

8.5.1.1 Equalizer options

The equalizer function can be bypassed and the equalizer can be configured to either a 5-band or 10-band function. These settings are for both audio channels simultaneously.

There are 20 bands in the equalizer. These are distributed as follows:

- Bands A1 to A5 are bands 1 to 5 of output 1 (used in 5-band and 10-band configuration).
- Bands B1 to B5 are bands 1 to 5 of output 2 (used in 5-band and 10-band configuration).
- Bands C1 to C5 are bands 6 to 10 of output 1 (used in 10-band configuration only).
- Bands D1 to D5 are bands 6 to 10 of output 2 (used in 10-band configuration only).

In I²C control mode each band can be configured separately using I²C register settings.

In Legacy control mode the equalizer is bypassed.

8.5.1.2 Equalizer band function

The shape of each parametric equalizer band is determined by the three filter parameters:

- (Relative) center frequency $\omega = 2\pi(f_c / f_s)$.
- Quality factor Q.
- Gain factor G.

In the above equation f_c is the center frequency and f_s is the sample frequency.

The definition of the quality factor is the center frequency divided by the 3 dB bandwidth, see Equation 1. In parametric equalizers this is only valid when the gain is set very small (–30 dB).

$$Q = \frac{f_c}{f_2 - f_1}; \quad \begin{matrix} f_1: & 20^{10}log\left(\frac{A_{f_1}}{A_{f_c}}\right) & = 3\text{dB} & f_c > f_1 \\ f_2: & 20^{10}log\left(\frac{A_{f_2}}{A_{f_c}}\right) & = 3\text{dB} & , f_2 > f_c \end{matrix} \tag{1}$$

Each band filter can be programmed to perform a band-suppression (G < 1) or a band-amplification (G > 1) function around the center frequency.

Each band of the TFA9812 equalizer has a second-order Regalia-Mitra all-pass filter structure. The structure is shown in Figure 5.

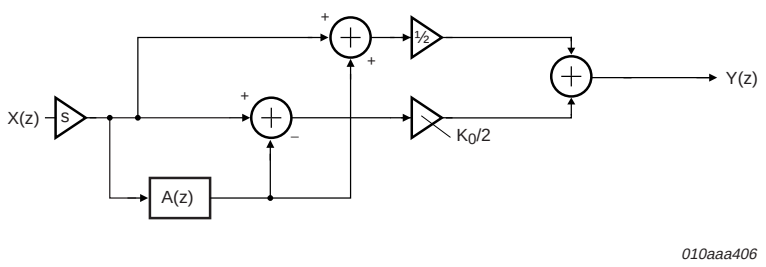


Fig 5. Regalia filter flow-diagram

The transfer function of this all-pass filter is shown in Equation 2:

$$H(z) = 1/2 \cdot (1 + A(z)) + K_0/2 \cdot (1 - A(z)) \tag{2}$$

A(z) is the second-order filter structure. The transfer function of A(z) is shown in Equation 3:

$$A(z) = \frac{K_1 + K_2 \cdot (1 + K_1) \cdot Z^{-1} + Z^{-2}}{1 + K_2 \cdot (1 + K_1) \cdot Z^{-1} + K_1 \cdot Z^{-2}} \tag{3}$$

The relationship between the programmable parameters K_0, K_1, and K_2 and the filter parameters G, ω, Q is shown in Equation 4 and Equation 5.

Use Equation 4 to calculate band suppression (G < 1) functions.

$$\left.\begin{matrix} K_0 = G \\ K_1 = -cos\omega \\ K_2 = (2Q \cdot G - sin\omega)/(2Q \cdot G + sin\omega) \end{matrix}\right|_{G<1} \tag{4}$$

Use Equation 5 to calculate band amplification (G ≥ 1) functions.

$$\left.\begin{aligned} K_0 &= G \\ K_1 &= -\cos\omega \\ K_2 &= (2Q - \sin\omega)/(2Q + \sin\omega) \end{aligned}\right|_{G \geq 1} \quad (5)$$

The ranges of the TFA9812 parametric equalizer settings for each band are:

- The Gain, G is from –30 dB to +12 dB.
- The center frequency, f_c is from 0.0004 * f_s to 0.49 * f_s.
- The quality factor Q is from 0.001 to 8.

Using I²C control, filter coefficients need to be entered for each filter stage to configure it as desired.

Figure 6, Figure 7 and Figure 8 show some of the possible transfer functions of the equalizer bands. The relations are symmetrical for the suppression and amplification functions. A skewing effect can be observed for the higher frequencies.

Different configurations are available for the same filter transfer function, thus allowing optimum numerical noise performance. The binary filter configuration parameters t_1 and t_2 control the actual configuration and should be chosen according to Equation 6.

$$t_1 = \begin{cases} 0 & \omega <= \pi/2 \\ 1 & \omega > \pi/2 \end{cases}$$
$$t_2 = \begin{cases} 0 & k_2 >= 0 \\ 1 & k_2 < 0 \end{cases} \quad (6)$$

A maximum of 12 dB amplification per equalizer stage can be achieved with respect to the input signal. Each band of the equalizer is provided with a –6 dB amplification, so in order to prevent numerical clipping for some filter settings with over 6 dB of amplification, band filters can be scaled by 0 dB or –6 dB. For optimum numerical noise performance steps of –6 dB amplification should be applied to the highest possible sections that are still within scale signal processing safeguards. Band filters can be scaled with the binary parameters listed in Table 14.

Table 14. Equalizer scale factor coding

s	scale factor (dB)
0	0
1	–6

8.5.1.3 Equalizer band control

For compact representation with positive signed parameters, parameters k_1' and k_2' are introduced in Equation 7.

The parameters k_0, k_1', k_2', t_1, t_2 and s must be combined in two 16-bit control words, word1 and word2, and must fit within the representation given in Table 15. Parameters k_1' and k_2' are unsigned floating-point representations in Equation 8.

$$k_1' = \begin{cases} 1 - k_1 & t_1 = 1 \\ 1 + k_1 & t_1 = 0 \end{cases}$$

$$k_2' = \begin{cases} 1 - k_2 & t_2 = 0 \\ 1 + k_2 & t_2 = 1 \end{cases} \quad (7)$$

$$k_x = M \cdot 2^{-E}\big|_{M<1} \quad (8)$$

In Equation 8, M is the unsigned mantissa and E the negative signed exponent. For example, in word2 bits [14:8] = [0111 010] represent $k_2' = (7/2^4) \times 2^{-2} = 1.09375 \quad 10^{-1}$.

Table 15. Equalizer control word construction

Word	Section	Data
word1	15	t_1
word1	[14:4]	11 mantissa bits of k_1'
word1	[3:0]	Four exponent bits of k_1'
word2	15	t_2
word2	[14:11]	Four mantissa bits of k_2'
word2	[10:8]	Three exponents bits of k_2'
word2	[7:1]	k_0
word2	0	s

Section 9.5.4 shows the I²C address locations of the controls for various bands of the equalizer.

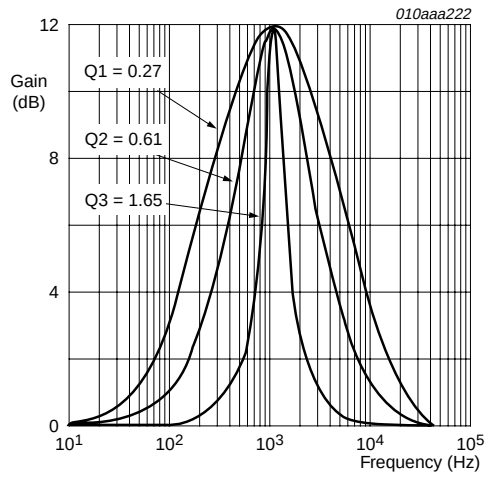


Fig 6. Transfer functions for several quality factors Q

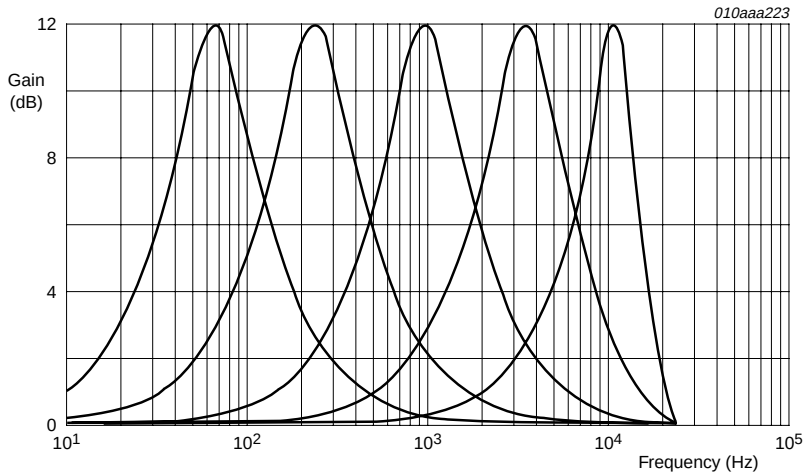


Fig 7. Transfer functions for several center frequencies f_c

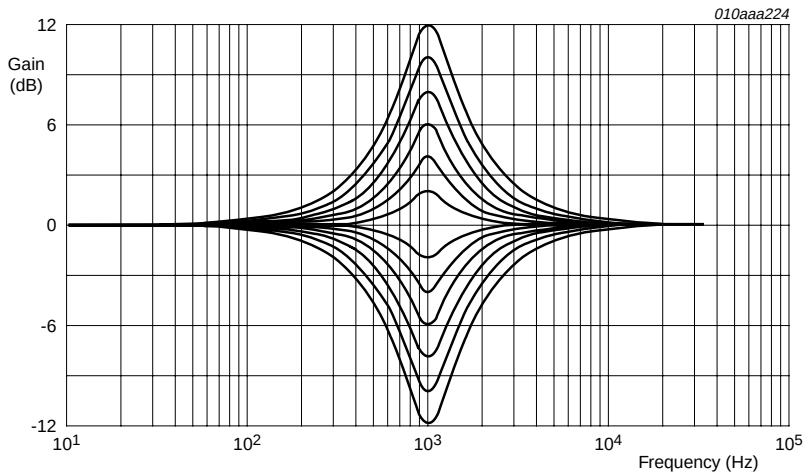


Fig 8. Transfer functions for several gain factors G

8.5.2 Digital volume control

In I²C control mode both audio channels have separate digital volume control. In Legacy control mode the volume control of both channels is common and the volume control setting depends on the supply voltage on the pin AVOL (32).

8-bit volume control is available per channel. This is dB-linear down to –124 dB in steps of 0.5 dB. The last step of the volume control is mute.

Table 16 shows the various settings and their related channel suppression:

Table 16. Volume control channel suppression table

[7:0] control value (hexadecimal)	Gain (dB)
00	0
01	–0.5
...	steps of 0.5 dB
F7	–123.5
F8	–124
F9	mute

Section 9 shows the I²C address locations for the digital gain control for both channels.

In Legacy mode the pin AVOL (32) can be used to control the volume.

Voltage levels of 0.8 V to 2.8 V correspond linearly to control values of 00h (0 dB) to F9h (mute). See Table 16.

An external pull-up resistor connected to the $V_{DDD(3V3)}$ can be applied to provide a default volume of 0 dB. Pin AVOL has no function in I²C mode.

8.5.3 Soft mute and mute

Soft mute is available in I²C and in Legacy control modes: hard mute can be enabled only in I²C control mode.

In I²C control mode the soft mute function smoothly reduces the gain setting for both channels to mute level over a duration of $128/f_s$ seconds. The smooth shape is implemented as a raised cosine function. Soft demute results in a similar gain increase. This implementation avoids audible plops.

A different soft mute and soft demute function is implemented in Legacy mode. This works via the analog gain control under the control of pin AVOL. The analog volume control input signal is first-order low-pass filtered with a time constant of 10 ms in the digital domain. Suddenly switching on or switching off volume by setting the control voltage to > 2.8 V or < 0.8 V respectively will result in a fading which lasts approximately 15 ms (switching between 0 V and 3.3 V at AVOL).

In Legacy mode the soft demute function that is part of the automatic power-up sequence is similar to the I²C mode soft demute function described above. The I²C control for the soft and hard mute functions can be found In Section 9.

8.5.4 Output signal and word-select polarity control

In I²C control mode the TFA9812 can switch the polarity of the stereo output signal. The effect is a 180 degree phase shift of both output signals.

The TFA9812 also has the option of switching the polarity of the WS signal. Without polarity inversion the left audio signal is connected to channel 1 and the right audio signal is connected to channel 2.

The I²C control for the polarity switch can be found in Section 9.5.1.

8.5.5 Gain boost and clip level control

An additional gain boost of +24 dB can be selected in the TFA9812. In Legacy mode this feature can be selected with the GAIN pin, see Table 17.

Table 17. GAIN pin functionality

GAIN pin value	Function
0	0 dB gain
1	+24 dB gain

The I²C controls for selecting the +24 dB gain can be found in Section 9.5.6. The GAIN pin has no function In I²C mode.

The TFA9812 features also specific gain settings which are related to < 0.5 %, 10 %, 20 % or 30 % clipping at the output of the TFA9812. These clipping values are only valid under the following conditions:

- The volume control is set to 0 dB.
- The gain boost is set to 0 dB.
- A 0 dBFs I²S input signal is obtained.

The I²C controls for selecting a specific clip level can be found in Section 9.5.6. In Legacy mode the clip level is set to 10 %.

8.5.6 Output power limiter

Output power can be limited to three discrete levels with respect to the maximum power. The maximum power output value is determined by the value of the high voltage supply. Clipping levels (see Section 8.5.5) still apply to the maximum levels of reduced output voltage swings.

In I²C control mode the same output power limiting levels can be selected, see Section 9.5.6. In Legacy control mode two pins can be used to select the output power limit level as shown in Table 18.

Table 18. Legacy mode output power limiter control

Pin value		Function
ADSEL2/PLIM2	ADSEL1/PLIM1	
0	0	Maximum power
0	1	Maximum power – 1.5 dB
1	0	Maximum power – 3.0 dB
1	1	Maximum power – 4.5 dB

8.5.7 PWM control for performance improvement

The PWM switching frequency of the TFA9812 is dependent on:

- The sampling frequency, f_s.
- The sampling frequency setting, f_s(selected) (see Section 9.5.7).
- The PWM switching frequency setting, f_{sw} (selected) (see Section 9.5.6).

Equation 9 shows the relationship between these settings and the PWM carrier frequency:

$$f_{sw} = \frac{f_s}{f_{s(selected))}} \cdot f_{sw(selected)} \quad (9)$$

The selected PWM switching frequency is 400 kHz by default and can be set to 350 kHz, 700 kHz and 750 kHz in I²C control mode. In Legacy mode 400 kHz is the only option and this scales linearly if 32 kHz or 48 kHz is used as f_s.

Remark: The selected sample frequency, f_s (selected) must be equal to the sample frequency (f_s) in I²C control mode.

Remark: The performance of AM radio reception can sometimes be improved by selecting non-interfering frequencies for the PWM signal.

8.6 Class-D amplification

The Class-D power amplification of the PWM signal is carried out in two BTL power stages. The output signal voltage level is determined by the values on the V_{DDP} pins.

The power amplifiers can be explicitly put into 3-state mode by using the pin ENABLE as shown in Table 19. The ENABLE pin is functional in Legacy mode and in I²C mode.

Table 19. ENABLE pin functionality

ENABLE pin value	Function
0	Output stages in 3-state mode.
1	Switching enabled [1].

[1] Can be overruled by a forced 3-state in Sleep or Fault mode.

8.7 Protection mechanisms

The TFA9812 has a wide range of protection mechanisms to facilitate optimal and safe application. All of these are active in both I²C and Legacy control modes.

The following protections are included in the TFA9812:

- Thermal Foldback (TF)
- OverTemperature Protection (OTP)
- OverCurrent Protection (OCP)
- OverVoltage Protection (OVP)
- UnderVoltage Protection (UVP)
- Window Protection (WP)
- Lock Protection (LP)
- UnderFrequency Protection (UFP)
- OverFrequency Protection (OFP)
- Invalid BCK Protection (IBP)
- DC-blocking
- ESD

The reaction of the device to the different fault conditions differs per protection.

8.7.1 Thermal foldback

If the junction temperature of the TFA9812 exceeds the programmable Thermal foldback threshold temperature the gain of the amplifier is decreased gradually to a level where the combination of dissipation (P) and the thermal resistance from junction to ambient ($R_{th(j-a)}$) results in a junction temperature around the threshold temperature.

This means that the device will not completely switch off, but remains operational at lower output power levels. Especially with music output signals this feature enables high peak output power while still operating without any external heat sink other than the printed-circuit board area. If the junction temperature still increases due to external causes, the OTP switches the amplifier to 3-state mode.

Under I²C control the Thermal foldback threshold temperature value can be lowered (see Section 9.5.8): In Legacy control mode the default threshold value of 125 °C is fixed.

8.7.2 Overtemperature protection

This is a 'hard' protection to prevent heat damage to the TFA9812. The overtemperature threshold level is the 160 °C junction temperature.

When the threshold temperature is exceeded the output stages are set to 3-state mode. The temperature is then checked at 1 µs intervals and the output stages will operate normally again once the temperature has dropped below the threshold level.

OTP is flagged by a low DIAG pin. The TFA9812 temperature is an I²C reading, see Section 9.5.9.

Under normal conditions thermal foldback prevents the overtemperature protection from being triggered.

8.7.3 Overcurrent protection

The output current of the power amplifiers is current-limited. When an output stage exceeds a current of 3 A typical, the output stages are set to 3-state mode and after 1 µs the stages will start operating normally again. These interruptions are not audible.

OCP is flagged by a low DIAG pin and by a high DIAG I²C status bit, see Section 9.5.10. I²C settings remain valid.

8.7.4 Overvoltage protection

The supply for the power stages (V_{DDA}, V_{DDP}) is protected against overvoltage. When a supply voltage exceeds 20 V the device will enter Sleep mode. When the supply voltage has fallen below 20 V again the power-up sequence is started.

OVP is flagged by a low DIAG pin and by a high DIAG I²C status bit, see Section 9.5.10. I²C settings remain valid.

8.7.5 Undervoltage protections

The supplies are protected against undervoltage. When this is detected the device will enter Sleep mode. When the supply voltage has risen to a sufficient level again the power-up sequence is started.

Table 20 shows the UVP trigger levels for the V_{DDA} and $V_{DDA(3V3)}$ supplies:

Table 20. Undervoltage trigger levels

Pin name	UVP level		DIAG pin (protection active)
	Min	Max	
V_{DDA}	≥ 7 V	< 8 V	LOW
$V_{DDA(3V3)}$	≥ 1.6 V	< 3 V	-

8.7.6 Overdissipation protection

When the output current of the power amplifiers exceeds a current value of 3 A and the temperature is above 140 °C, overdissipation protection is activated and the device enters Sleep mode. A restart will be initiated automatically when the two overdissipation conditions are both changed to 'false'.

Overdissipation is flagged by a low DIAG pin and by a high DIAG I²C status bit, see Section 9.5.10.

Under normal conditions thermal foldback prevents overdissipation protection from being triggered. I²C settings remain valid.

8.7.7 Window protection

Window protection is a feature for protecting the device against shorts from the outputs to the ground or supply lines. If during power-up one of the outputs is shorted to V_{SSPx} or V_{DDP}, power-up does not proceed any further. The trigger levels for these conditions are:

- OUTxx > V_{DDA} – 1 V, or
- OUTxx < REFA + 1 V.

The WP alarm is flagged by a low DIAG pin and by a high DIAG I²C status bit, see Section 9.5.10.

8.7.8 Lock protection

When the selected clock input source (MCLK, BCK or crystal) stops running, the TFA9812 is able to detect this and set the output stages to 3-state mode. Without this protection peripheral devices in an application might be damaged.

The PLL lock indication is an I²C reading and will be 'false' in the event of a clock interruption, see Section 9.5.10.

8.7.9 Underfrequency protection

UFP sets the output stages to 3-state mode when the clock input source is too low. The PWM switching frequency can becomes critically low when the clock input source is lower than specified. Without UFP peripheral devices in an application might be damaged.

The status of the UFP is shown in I²C reading register, see Section 9.5.10.

8.7.10 Overfrequency protection

OFP sets the output stages to 3-state mode when the clock input source is too high. The PWM controller can become unstable when the clock input source is higher than specified. Without OFP peripheral devices in an application might be damaged.

The status of the OFP is shown in I²C reading register, see Section 9.5.10.

8.7.11 Invalid BCK protection

The BCK clock signal is verified as being at one of the allowed relative frequencies: 32 f_s, 48 f_s or 64 f_s. If it is not at one of these frequencies the TFA9812 will set the output stages to 3-state mode to prevent audible effects.

The MCLK clock signal is also verified as being valid, see Section 8.2.3.

Detection of violation results in an automatic internal overruling of the MCLK assignment to BCK.

8.7.12 DC blocking

The TFA9812 features a high pass filter after the I²S input to block DC signals. DC values at the output can damage the peripheral devices. The high pass filter is always enabled.

8.7.13 Overview protections

Table 21 shows the overview of the protections.

Table 21. Overview protections

Protections					
Symbol	**Conditions**	**DIAG pin**	**I²C flag[1]**	**Output**	**Recovering**
TF	programmable max. T_j > 125 °C	Floating	-	Switching	Automatic, increasing volume control back to volume setting
OTP	T_j > 160 °C	LOW	DIAG	Floating	Automatic, after 1 µs and T_j < 160 °C
OCP	$I_O > I_{ORM}$	LOW	DIAG	Floating	Automatic, after 1 µs and $I_O < I_{ORM}$
OVP	V_{DDA} > 20 V	LOW	DIAG	Floating	Restart (fault to operating when V_{DDA} > 8 V and $V_{DDA(3V3)}$ > 3 V)
UVP	V_{DDA} < 8 V or $V_{DDA(3V3)}$ < 3 V	LOW	DIAG	Floating	Restart (fault to operating when V_{DDA} > 8 V and $V_{DDA(3V3)}$ > 3 V)
ODP	T_j > 140 °C and $I_O > I_{ORM}$	LOW	DIAG	Floating	Restart (fault to operating when T_j < 140 °C or IO < I_{ORM})
WP[2]	OUTX > V_{DDA} – 1 V or OUTX < REFA + 1 V	LOW	DIAG	Floating	Restart (fault to operating when OUTX < V_{DDA} – 1 V and OUTX > V_{SSA} + 1 V)
LP	PLL out of lock	Floating	LP	Floating	Restart (fault to operating when PLL is in lock)
UFP	PLL frequency < 45 MHz	Floating	UFP	Floating	Restart (fault to operating when PLL frequency > 45 MHz)

Table 21. Overview protections *...continued*

Protections					
Symbol	**Conditions**	**DIAG pin**	**I²C flag[1]**	**Output**	**Recovering**
OFP	PLL frequency > 140 MHz	Floating	OFP	Floating	Restart (fault to operating when PLL frequency < 140 MHz)
IBP	BCK/WS is not 32 ± 2, 48 2 or 64 2	Floating	-	Floating	Restart (fault to operating when BCK/WS is 32 ± 2, 48 2 or 64 2)

[1] See, Section 9.5.10.

[2] Window Protection is only checked at power-up.

9. I²C bus interface and register settings

9.1 I²C bus interface

The TFA9812 supports the 400 kHz I²C bus microcontroller interface mode standard. This can be used to control the TFA9812 and to exchange data with it when in I²C control mode, see Section 8.2.1.

The TFA9812 can operate in I²C slave mode only as slave receiver or a slave transmitter.

The serial hardware interface involves the pins of the TFA9812 as described in Table 22.

Table 22. I²C pins in I²C control mode

Pin name	Description
SCL/SFOR	I²C bus clock input
SDA/MS	I²C bus data input and output
ADSEL2/PLIM2	I²C bus device address bit A2
ADSEL1/PLIM1	I²C bus device address bit A1

Voltage values applied to the I²C bus device address pins are interpreted as described in Table 23.

Table 23. I²C pin voltages in I²C control mode

Logic value	Voltage A2/A1
0	$< V_{IL}$
1	$> V_{IH}$

9.2 I²C bus TFA9812 device addresses

Table 24 shows the register address options for the TFA9812 as part of the 8-bit byte that contains the device address as well as the bit indicator read/write_not R/!W. The TFA9812 supports four different addresses, each of which can be configured using the pins ADSEL1/PLIM1 and ADSEL2/PLIM2, see Table 22.

Table 24. I²C bus device address

(MSB)	Bit						(LSB)
1	1	0	1	0	A2	A1	R/!W

9.3 I²C write cycle description

Table 25 shows the cycle required for writing data to the I²C registers of the TFA9812. The byte size is 8 bits. The I²C registers of the TFA9812 store two data bytes. Data is always written in pairs of two bytes. Data transfer is always MSB first.

The cycle format for writing to the TFA9812 using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller sends the device address (7 bits) of the TFA9812 followed by the R/!W bit set to 0.
3. The TFA9812 asserts an acknowledge (A).
4. The microcontroller writes the 8-bit TFA9812 register address to which the first data byte will be written.
5. The TFA9812 asserts an acknowledge.
6. The microcontroller sends the first byte. This is the most significant byte of the register.
7. The TFA9812 asserts an acknowledge.
8. The microcontroller sends the second byte.
9. The TFA9812 asserts an acknowledgement.
10. The microcontroller can either assert the stop condition (P) or continue with a further pair of data bytes, repeating step 6. In the latter case the targeted register address will have been auto-increased by the TFA9812.

Table 25. I²C write cycle

Start	TFA9812 Address	R/!W		TFA9812 first register address		MS databyte		LS databyte	More data...	Stop
S	$11010A_2A_1$	0	A	ADDR	A	MS1	A	LS1	<....>	P

9.4 I²C read cycle description

Table 26 shows the cycle required for reading data from the I²C registers of the TFA9812. The byte size is 8 bits. The I²C registers of the TFA9812 store two data bytes. Data is always read in pairs of two bytes. Data transfer is always MSB-first.

The read cycle format for writing to the TFA9812 using SDA is as follows:

1. The microcontroller asserts a start condition (S).
2. The microcontroller sends the device address (7 bits) of the TFA9812 followed by the R/!W bit set to 0.
3. The TFA9812 asserts an acknowledge (A).
4. The microcontroller writes the 8-bit TFA9812 register address from which the first data byte will be read.
5. The TFA9812 asserts an acknowledge.
6. The microcontroller asserts a repeated start (Sr).
7. The microcontroller resends the device address (7 bits) of the TFA9812 followed by the R/!W bit set to 1.
8. The TFA9812 asserts an acknowledge.

9. The TFA9812 sends the first byte. This is the most significant byte of the register.
10. The microcontroller asserts an acknowledge.
11. The TFA9812 sends the second byte.
12. The microcontroller asserts either an acknowledge or a negative acknowledge (NA).
    - If the microcontroller has asserted an acknowledge, the targeted register address is auto-increased by the TFA9812 and steps 9 to 12 are repeated.
    - If the microcontroller has asserted a negative acknowledge, the TFA9812 frees the I²C bus and the microcontroller generates a stop condition (P).

Table 26. I²C read cycle

Start	TFA9812 address	R/!W		First register address			TFA9812 address	R/!W		MS data byte		LS data byte	More data...	More data...		Stop
S	$11010A_2A_1$	0	A	ADDR	A	Sr	$11010A_2A_1$	1	A	MS1	A	LS1	<A>	<....>	NA	P

9.5 Top-level register map

Table 27 describes the assignments of the various register addresses to the functional control or status areas at top level. There are 47 control registers and 2 status registers.

The following subsections give the individual register interpretations and bit level details.

Table 27. Top-level register map

Register address (hex)	Default (hex)	Access	See:	Description
0x00	0x0020; Legacy_mode	R/W	Section 9.5.1	Interpolator settings and soft mute
	0x0021; I²C_mode			
0x01	0x0000	R/W	Section 9.5.2	Volume control
0x02	0x0006	R/W	Section 9.5.3	Format digital in
0x03	0x0002	R/W	Section 9.5.4	Equalizer configuration
0x04	0x0058	R/W	Section 9.5.5	Equalizer_A1 word_1; word_1 for equalizer band A1, see Section 8.5.1.2
0x05	0x4F40	R/W	Section 9.5.5	Equalizer_A1 word_2; see Section 8.5.1.2
0x06	0x0058	R/W	Section 9.5.5	Equalizer_B1 word_1
0x07	0x4F40	R/W	Section 9.5.5	Equalizer_B1 word_2
0x08	0x0A63	R/W	Section 9.5.5	Equalizer_C1 word_1
0x09	0x4240	R/W	Section 9.5.5	Equalizer_C1 word_2
0x0A	0x0A63	R/W	Section 9.5.5	Equalizer_D1 word_1
0x0B	0x4240	R/W	Section 9.5.5	Equalizer_D1 word_2
0x0C	0x00B7	R/W	Section 9.5.5	Equalizer_A2 word_1
0x0D	0x4E40	R/W	Section 9.5.5	Equalizer_A2 word_2
0x0E	0x00B7	R/W	Section 9.5.5	Equalizer_B2 word_1
0x0F	0x4E40	R/W	Section 9.5.5	Equalizer_B2 word_2
0x10	0x14A2	R/W	Section 9.5.5	Equalizer_C2 word_1

Table 27. Top-level register map *…continued*

Register address (hex)	Default (hex)	Access	See:	Description
0x11	0x7A40	R/W	Section 9.5.5	Equalizer_C2 word_2
0x12	0x14A2	R/W	Section 9.5.5	Equalizer_D2 word_1
0x13	0x7A40	R/W	Section 9.5.5	Equalizer_D2 word_2
0x14	0x0156	R/W	Section 9.5.5	Equalizer_A3 word_1
0x15	0x4D40	R/W	Section 9.5.5	Equalizer_A3 word_2
0x16	0x0156	R/W	Section 9.5.5	Equalizer_B3 word_1
0x17	0x4D40	R/W	Section 9.5.5	Equalizer_B3 word_2
0x18	0x2871	R/W	Section 9.5.5	Equalizer_C3 word_1
0x19	0x7140	R/W	Section 9.5.5	Equalizer_C3 word_2
0x1A	0x2871	R/W	Section 9.5.5	Equalizer_D3 word_1
0x1B	0x7140	R/W	Section 9.5.5	Equalizer_D3 word_2
0x1C	0x02A5	R/W	Section 9.5.5	Equalizer_A4 word_1
0x1D	0x4C40	R/W	Section 9.5.5	Equalizer_A4 word_2
0x1E	0x02A5	R/W	Section 9.5.5	Equalizer_B4 word_1
0x1F	0x4C40	R/W	Section 9.5.5	Equalizer_B4 word_2
0x20	0x4A80	R/W	Section 9.5.5	Equalizer_C4 word_1
0x21	0x5040	R/W	Section 9.5.5	Equalizer_C4 word_2
0x22	0x4A80	R/W	Section 9.5.5	Equalizer_D4 word_1
0x23	0x5040	R/W	Section 9.5.5	Equalizer_D4 word_2
0x24	0x0534	R/W	Section 9.5.5	Equalizer_A5 word_1
0x25	0x4B40	R/W	Section 9.5.5	Equalizer_A5 word_2
0x26	0x0534	R/W	Section 9.5.5	Equalizer_B5 word_1
0x27	0x4B40	R/W	Section 9.5.5	Equalizer_B5 word_2
0x28	0xD961	R/W	Section 9.5.5	Equalizer_C5 word_1
0x29	0x4840	R/W	Section 9.5.5	Equalizer_C5 word_2
0x2A	0xD961	R/W	Section 9.5.5	Equalizer_D5 word_1
0x2B	0x4840	R/W	Section 9.5.5	Equalizer_D5 word_2
0x2C	0x0005	R/W	Section 9.5.6	PWM signal control
0x2D	0x000E	R/W	Section 9.5.7	Digital-in clock configuration
0x2E	0x0000	R/W	Section 9.5.8	Thermal foldback control
0x2F	-	R	Section 9.5.9	TFA9812 temperature
0x30	-	R	Section 9.5.10	Miscellaneous status

Reserved registers or bits will be indicated by RSD.

9.5.1 Interpolator settings and soft mute

Table 28. Register address 00h: miscellaneous I²C interpolator settings

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	INV_POL	ROFF1	ROFF0	FDEMP2	FDEMP1	FDEMP0	S_MUTE
Default	0	0	1	0	0	0	0	1/0

Table 29. Bit description of register 00h: miscellaneous I²C interpolator settings

Bit	Symbol	Description
6	INV_POL	Enable polarity inversion: 0 = No polarity inversion (left audio signal connected to channel 1; right signal to channel 2) 1 = Polarity inversion enabled
5 to 4	ROFF[1:0]	Filter roll-off sharpness: 0 = Slow filter roll-off (2 to 8 f_s) ≥ stop band > 0.7619 f_s 1 = Slow filter roll-off (2 to 8 f_s) ≥ stop band > 0.7619 f_s 2 = Fast filter roll-off (2 to 8 f_s) ≥ stop band > 0.6094 f_s 3 = Fast filter roll-off (2 to 8 f_s) ≥ stop band > 0.6094 f_s
3 to 1	FDEMP[2:0]	Digital de-emphasis setting: 0 = No digital de-emphasis 1 = Digital de-emphasis for f_s = 32 kHz 2 = Digital de-emphasis for f_s = 44.1 kHz 3 = Digital de-emphasis for f_s = 48 kHz 4 = Digital de-emphasis for f_s = 96 kHz 5 to 8 = No digital de-emphasis
0	S_MUTE	Soft mute: 0 = Soft mute disabled using raised cosine (default in Legacy control mode) 1 = Soft mute enabled using raised cosine (default in I²C control mode)

9.5.2 Volume control

Table 30. Register address 01h: volume control

Bit	15	14	13	12	11	10	9	8
Symbol	VOL_L7	VOL_L6	VOL_L5	VOL_L4	VOL_L3	VOL_L2	VOL_L1	VOL_L0
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VOL_R7	VOL_R6	VOL_R5	VOL_R4	VOL_R3	VOL_R2	VOL_R1	VOL_R0
Default	0	0	0	0	0	0	0	0

Table 31. Bit description of register 00h: miscellaneous I²C interpolator settings

Bit	Symbol	Description
15 to 8	VOL_L[15:8]	See Table 16 for suppression levels on left channel as function of data byte setting.
7 to 0	VOL_R[7:0]	See Table 16 for suppression levels on right channel as function of data byte setting.

9.5.3 Digital input format

Table 32. Register address 02h: digital input format

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	RSD	RSD	RSD	DI_FOR2	DI_FOR1	DI_FOR0	WS_POL
Default	0	0	0	0	0	1	1	0

Table 33. Bit description of register 02h: digital input format

Bit	Symbol	Description
3 to 1	DI_FOR[2:0]	Digital audio input format: 0 = RSD 1 = RSD 2 = MSB-justified data up to 24 bits 3 = I²S data up to 24 bits 4 = LSB-justified 16-bit data 5 = LSB-justified 18-bit data 6 = LSB-justified 20-bit data 7 = LSB-justified 24-bit data
0	WS_POL	Enable WS signal polarity inversion: 0 = No WS signal polarity inversion 1 = WS signal polarity inversion enabled

9.5.4 Equalizer configuration

Table 34. Register address 03h: equalizer configuration

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	EQ_BP	EQ_BND
Default	0	0	0	0	0	0	1	0

Table 35. Bit description of register 03h: equalizer configuration

Bit	Symbol	Description
1	EQ_BP	Equalizer bypass enable: 0 = Equalizer not bypassed 1 = Equalizer bypassed
0	EQ_BND	Equalizer 10-band or 5-band configuration selection: 0 = 10-band equalizer configuration enabled 1 = 5-band equalizer configuration enabled

9.5.5 Equalizer settings

Table 36. Register addresses xxh = 04, 06...2A
For word1 for equalizer 'yy' see Figure 9

Bit	15	14	13	12	11	10	9	8
Symbol	Eyy_t_1	Eyy_k_{1m}10	Eyy_k_{1m}9	Eyy_k_{1m}8	Eyy_k_{1m}7	Eyy_k_{1m}6	Eyy_k_{1m}5	Eyy_k_{1m}4
Default[1]	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Eyy_k_{1m}3	Eyy_k_{1m}2	Eyy_k_{1m}1	Eyy_k_{1m}0	Eyy_k_{1e}3	Eyy_k_{1e}2	Eyy_k_{1e}1	Eyy_k_{1e}0
Default[1]	-	-	-	-	-	-	-	-

[1] Default settings are shown in Table 27. The corresponding equalizer configuration is shown in Table 40.

Table 37. Register addresses xxh = 05, 07...2B
For word2 for equalizer 'yy' see Figure 9

Bit	15	14	13	12	11	10	9	8
Symbol	Eyy_t_2	Eyy_k_{2m}3	Eyy_k_{2m}2	Eyy_k_{2m}1	Eyy_k_{2m}0	Eyy_k_{2e}2	Eyy_k_{2e}1	Eyy_k_{2e}0
Default	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	Eyy_$k_0$6	Eyy_$k_0$5	Eyy_$k_0$4	Eyy_$k_0$3	Eyy_$k_0$2	Eyy_$k_0$1	Eyy_$k_0$0	Eyy_s
Default	-	-	-	-	-	-	-	-

[1] Default settings are shown in Table 27. The corresponding equalizer configuration is shown in Table 40.

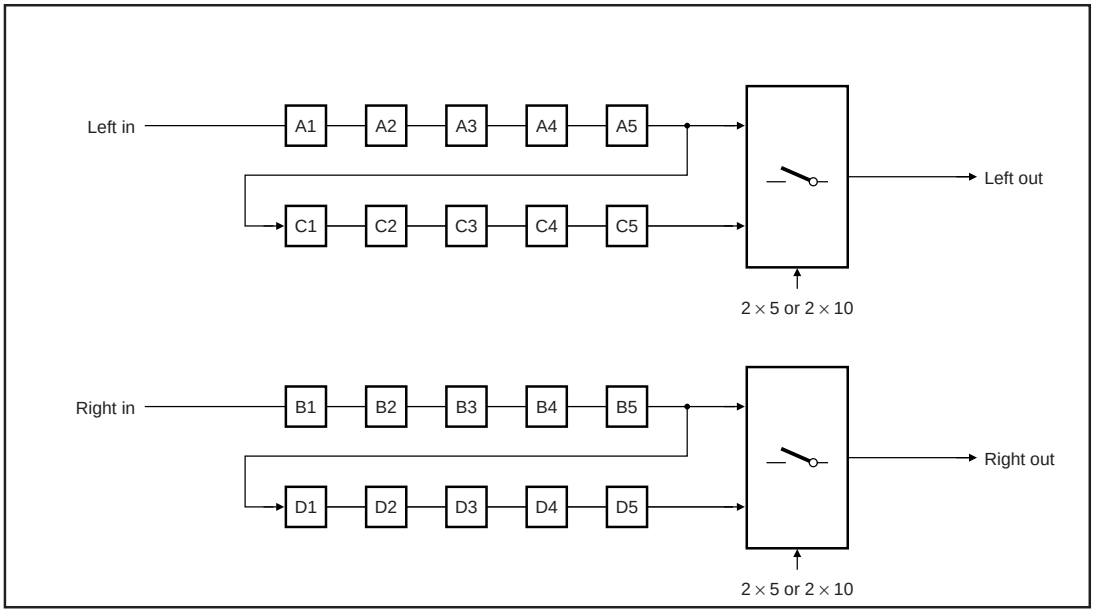


Fig 9. Equalizer configuration and register location mapping

Table 38. Bit description of registers xxh = 04, 06...2A

Bit	Symbol	Description
15	Eyy_t_1	The filter configuration bit t_1, see Section 8.5.1.2.
14 to 4	Eyy_$k1_m$[10:0]	The 11 mantissa bits of the filter parameter k_1, see Section 8.5.1.2.
3 to 0	Eyy_$k1_e$[3:0]	The four exponent bits of the filter parameter k_1, see Section 8.5.1.2.

Table 39. Bit description of registers xxh = 05, 07...2B

Bit	Symbol	Description
15	Eyy_t_2	The filter configuration bit t_2, see Section 8.5.1.2.
14 to 11	Eyy_k_{2m}[3:0]	The four mantissa bits of the filter parameter k_2, see Section 8.5.1.2.
10 to 8	Eyy_k_{2e}[2:0]	The three exponent bits of the filter parameter k_2, see Section 8.5.1.2.
7 to 1	Eyy_k_0[6:0]	The seven bits of the filter gain parameter k_0, see Section 8.5.1.2.
0	Eyy_s	The filter scale-factor bits, see Section 8.5.1.2: 0 = No scaling applied 1 = –6 dB amplification enabled

Table 40. Default configuration equalizer for f_s = 44.1 kHz

Band	A1/B1	A2/B2	A3/B3	A4/B4	A5/B5	C1/D1	C2/D2	C3/D3	C4/D4	C5/D5
Frequency (Hz)	31	63	125	250	500	1000	2000	4000	8000	16000
Q-factor	1	1	1	1	1	1	1	1	1	1
Gain (dB)	0	0	0	0	0	0	0	0	0	0

9.5.6 PWM signal control

Table 41. Register 2Ch: PWM signal control

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	PLIM1	PLIM0	PW_OFF	PW_SF1	PW_SF0	PW_CL1	PW_CL0
Default	0	0	0	0	0	1	0	1

Table 42. Bit description address 2Ch

Bit	Symbol	Description
7	GAIN	+24 dB gain boost: 0 = Gain boost 0 dB 1 = Gain boost +24 dB
6 to 5	PLIM[1:0]	Output power limitation: 0 = Maximum power 1 = Maximum power – 1.5 dB 2 = Maximum power – 3.0 dB 3 = Maximum power – 4.5 dB
4	PW_OFF	Hard mute control: 0 = No hard mute 1 = Hard mute enabled, implemented by PWM signal with 50 % duty cycle
3 to 2	PW_SF[1:0]	PWM switching frequency: 0 = 350 kHz 1 = 400 kHz 2 = 700 kHz 3 = 750 kHz
1 to 0	PW_CL[1:0]	PWM clip level: 0 = < 0.5 % THD 1 = 10 % THD 2 = 20 % THD 3 = 30 % THD

9.5.7 Digital-in clock configuration

Table 43. Register 2Dh: digital-in clock configuration

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	RSD	RSD	FSUB3	FSUB2	FSUB1	FSUB0	DI_MS
Default	0	0	0	0	1	1	1	0

Table 44. Bit description of register 2Dh:digital-in clock configuration

Bit	Symbol	Description
4 to 1	FSUB[3:0]	Sample frequency f_s of digital-in signal: 0 = 8 kHz 1 = 11.025 kHz 2 = 12 kHz 3 = 16 kHz 4 = 22.05 kHz 5 = 24 kHz 6 = 32 kHz 7 = 44.1 kHz 8 = 48 kHz 9 = 64 kHz 10 = 88.2 kHz 11 = 96 kHz 12 = 128 kHz 13 = 176.4 kHz 14 = 192 kHz 15 = RSD
0	DI_MS	TFA9812 digital-in Master/Slave mode selection: 0 = Slave mode 1 = Master mode

9.5.8 Thermal foldback control

Table 45. Register 2Eh: thermal foldback control

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	TP_THR9	TP_THR8
Default	0	0	0	0	0	0	0	0
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TP_THR7	TP_THR6	TP_THR5	TP_THR4	TP_THR3	TP_THR2	TP_THR1	TP_THR0
Default	0	0	0	0	0	0	0	0

Table 46. Bit description of register 2Dh: digital-in clock configuration

Bit	Symbol	Description
9 to 0	TP_THR[9:0]	Reduction on the maximum temperature of 125 °C. The reduction can be calculated by: $\text{reduction} = \text{INTEGER}\frac{(\text{TP\_THR}[9:0]}{2.4552}\text{in } °C$

9.5.9 TFA9812 temperature

Table 47. Register 2Fh: TFA9812 temperature

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	TEMP9	TEMP8
Default	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
Default	-	-	-	-	-	-	-	-

Table 48. Bit description of register 2Dh: digital-in clock configuration

Bit	Symbol	Description
9 to 0	TEMP[9:0]	Temperature of the TFA9812, which can be calculated in °C using: Temp TFA9812 = (1023 – TEMP[9:0]) / 2.4552

9.5.10 Miscellaneous status

Table 49. Register 30h: miscellaneous status

Bit	15	14	13	12	11	10	9	8
Symbol	RSD	RSD	RSD	RSD	RSD	RSD	RSD	RSD
Default	-	-	-	-	-	-	-	-
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	RSD	OFP	UFP	UVP1V8	UVP3V3	DIAG	LP	MUTE
Default	-	-	-	-	-	-	-	-

Table 50. Bit description of register 30h: miscellaneous status

Bit	Symbol	Description
6	OFP	PLL frequency-over-range indicator: 0 = PLL frequency in supported range 1 = PLL frequency exceeds highest supported frequency value
5	UFP	PLL frequency under-range indicator: 0 = PLL frequency in supported range 1 = PLL frequency below lowest supported frequency value
4	UVP1V8	Undervoltage detector for pins 4 and 41: 0 = No UVP has been detected 1 = A UVP has been detected since the last read-out of the register

Table 50. Bit description of register 30h: miscellaneous status *…continued*

Bit	Symbol	Description
3	UVP3V3	Undervoltage detector for pins 3 and 40: 0 = No UVP has been detected 1 = A UVP has been detected since the last read-out of the register
2	DIAG	Diagnostic pin flagging status[1]: 0 = Diagnostic pin has not been flagged low 1 = Diagnostic pin has been flagged low since the last read-out of the register
1	LP	PLL lock protection indicator: 0 = PLL is in locked status 1 = PLL is not in locked status
0	MUTE	Soft mute status: 0 = No soft-mute or soft mute/demute in progress 1 = Audio signal muted as result of a soft mute

[1] The diagnostic pin 30 DIAG is flagged when several protection mechanisms have been active, see Section 8.7.

9.6 Overview of functional control in each control mode

Table 51 shows the control level supported by either I²C or Legacy control mode for all functions described in Section 9. It summarizes the information provided in the detailed description of each function.

Table 51. Functional control support in I²C and Legacy control modes

D = fixed control setting, determined by default I²C register setting; N = not supported; Y = fully supported (i.e. all options implemented in the TFA9812).

Control function	Reference	I²C mode	Legacy mode
I²C register content	Section 9	Y	N/D
Sleep mode enable	Section 8.2.2	Y	Y
Operating mode enable	Section 8.2.2	Y	Y
3-state mode enable	Section 8.2.2	Y	Y
Master/Slave I²S	Section 8.2.3	Y	Y
MCLK/BCK master input clock selection	Section 8.2.3	Auto	Auto
Digital audio input format selection	Section 8.4	Y	Subset
Selection f_s = 8 kHz to192 kHz	Section 8.4.1	Y	D[1]
Equalizer enable and configuration	Section 8.5.1	Y	D[2]
Detailed equalizer settings	Section 8.5.1	Y	N
Digital volume control per channel	Section 8.5.2	Y	N
Analog volume control (shared for two channels)	Section 8.5.3	N	Y
De-emphasis for subset of allowed f_s	Section 8.5.3	Y	N
Soft mute	Section 8.5.3	Y	Y[3]
Hard mute	Section 8.5.3	Y	N
Polarity switch enable	Section 8.5.4	Y	N
+24 dB gain boost	Section 8.5.6	Y	Y

Table 51. Functional control support in I²C and Legacy control modes *...continued*

D = fixed control setting, determined by default I²C register setting; N = not supported; Y = fully supported (i.e. all options implemented in the TFA9812).

Control function	Reference	I²C mode	Legacy mode
Clip level control	Section 8.5.5	Y	D[4]
Output power limit level control	Section 8.5.6	Y	Y
PWM signal frequency selection	Section 8.5.7	Y	D[5]
Thermal foldback threshold temperature control	Section 8.7.1	Y	N

[1] 32 kHz, 44.1 kHz and 48 kHz supported

[2] Bypass.

[3] Special Legacy mode implementation.

[4] 10 % clip level.

[5] 400 kHz.

10. Internal circuitry

Table 52. Internal circuitry

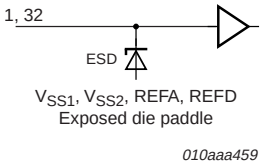
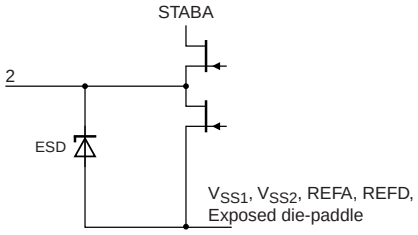
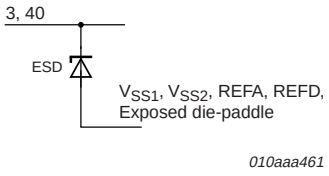
Pin	Symbol	Equivalent circuitry
1	XTALIN	
32	AVOL	
2	XTALOUT	
3	$V_{DDA(3V3)}$	
40	$V_{DDD(3V3)}$	

Table 52. Internal circuitry *…continued*

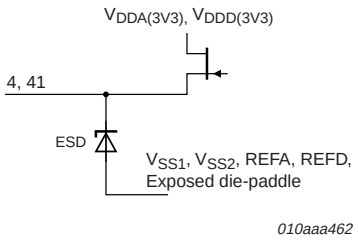
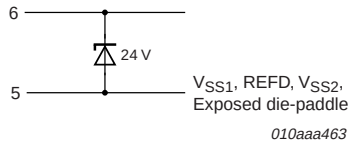
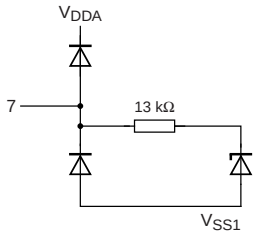
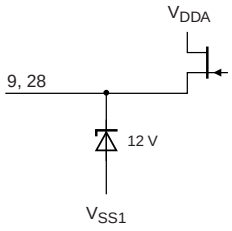
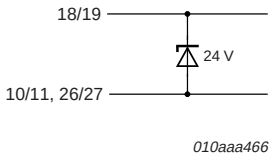
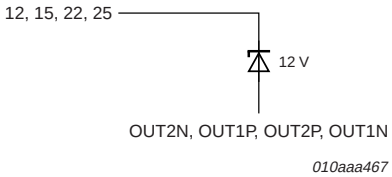
Pin	Symbol	Equivalent circuitry
4	STABA	
41	STABD	
5	REFA	
6	V_{DDA}	
7	TEST1	
9	STAB2	
28	STAB1	
10/11	V_{SSP2}	
18/19	V_{DDP}	
26/27	V_{SSP1}	
12	BOOT2N	
15	BOOT1P	
22	BOOT2P	
25	BOOT1N	

Table 52. Internal circuitry *…continued*

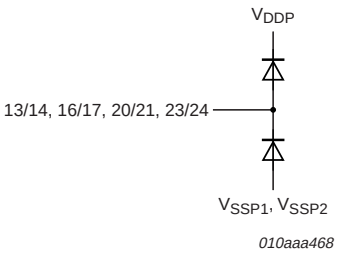
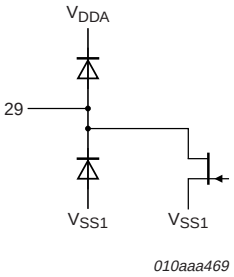
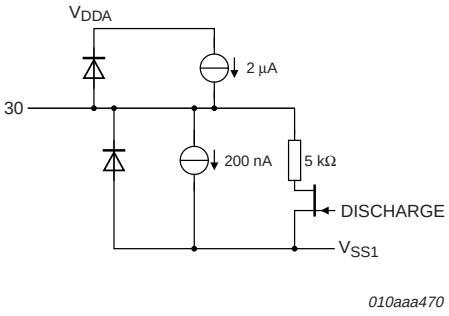
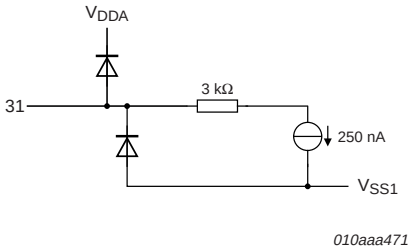
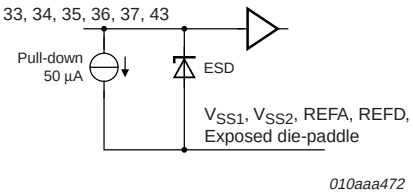
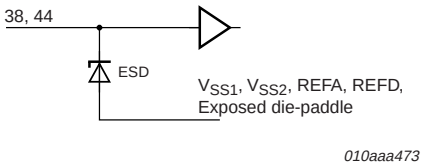
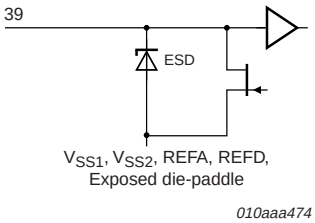
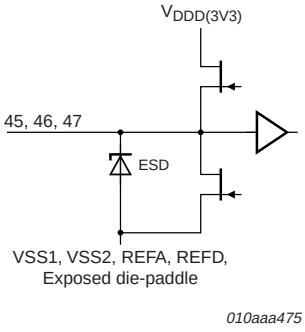
Pin	Symbol	Equivalent circuitry
13/14	OUT2N	
16/17	OUT1P	
20/21	OUT2P	
23/24	OUT1N	
29	DIAG	
30	CDELAY	
31	POWERUP	
33	ENABLE	
34	GAIN	
35	CSEL	
36	ADSEL2/PLIM2	
37	ADSEL1/PLIM1	
43	TEST2	

Table 52. Internal circuitry *…continued*

Pin	Symbol	Equivalent circuitry
38	SCL/SFOR	
39	SDA/MS	
45	WS	
46	BCK	
47	MCLK	

11. Limiting values

Table 53. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DDA}	analog supply voltage	$-V_{SS}$	[1]	–0.3	+24	V
V_{DDP}	power supply voltage	$-V_{SSPx}$; x = 1.2		–0.3	+24	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	$-V_{SS}$	[1]	–0.3	+4.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)	$-V_{SS}$	[1]	–0.3	+4.6	V
T_j	junction temperature			-	150	°C
T_{stg}	storage temperature			–55	+150	°C
T_{amb}	ambient temperature			–40	+85	°C
P	power dissipation				5	W

Table 53. Limiting values *...continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_x	voltage on pin x	DIAG	[1]	V_{SS} – 0.3	V_{SS} + 12	V
		POWERUP	[1]	V_{SS} – 0.3	V_{DDA} + 0.3	V
		ENABLE, GAIN, CSEL, ADSEL2/PLIM2, ADSEL2/PLIM1, SCL/SFOR, SDA/MS, DATA, WS, BCK, MCLK	[1]	V_{SS} – 0.5	V_{SS} + 5.5	V
		AVOL	[1]	V_{SS} – 0.5	V_{SS} + 4.6	V
V_{esd}	electrostatic discharge voltage	according to the human body model				
		STAB1 and STAB2 with respect to other pins		–1750	+1750	V
		all other pins		–2	+2	kV
		according to the charge device model		–500	+500	V

[1] $V_{ss} = V_{SS1} = V_{SS2} = REFA = REFD$

12. Thermal characteristics

Table 54. Thermal Characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	No air flow, JEDEC board	[1][2]	-	-	42	K/W
		No air flow; typical 4L board in the NXP 4L reference application	[2]	-	-	36	K/W
		No air flow; typical 2L board in the NXP 2L reference application	[2]	-	-	42	K/W
$R_{th(j-c)}$	thermal resistance from junction to case		[3]	5	-	-	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead	Worst-case pin		5	-	-	K/W

[1] Measured in a JEDEC high K-factor test board (standard EIA/JESD 51-7).

[2] Measured in free air with natural convection.

[3] Strongly depends on where measurement is made on the case: worst-case value stated.

13. Characteristics

13.1 DC Characteristics

Table 55. DC characteristics

Unless specified otherwise, V_{DDA} = V_{DDP} = 12 V, V_{SSP1} = V_{SSP2} = 0 V, $V_{DDA(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V, V_{SS1} = V_{SS2} = REFD = REFA = 0 V, T_{amb} = 25 °C, R_L = 8 Ω, f_i = 1 kHz, f_s = 44.1 kHz, f_{sw} = 400 kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Supply voltage							
V_{DDA}	analog supply voltage			8	12	20	V
V_{DDP}	power supply voltage			8	12	20	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)			3.0	3.3	3.6	V
$V_{DDD(3V3)}$	digital supply voltage (3.3 V)			3.0	3.3	3.6	V
I_P	supply current	soft mute mode, with load, filter and snubbers connected	[1]	-	38	45	mA
		sleep mode	[1]	-	160	270	µA
$I_{DDA(3V3)}$	analog supply current (3.3 V)	operating mode					
		I²S slave mode		-	2	4	mA
		I²S master mode		-	4	6	mA
		sleep mode					
		V_{DDA} = V_{DDP} = 12 V		-	120	-	µA
		V_{DDA} = V_{DDP} = 1 V		-	40	70	µA
$I_{DDD(3V3)}$	digital supply current (3.3 V)	operating mode					
		I²S slave mode		-	15	25	mA
		I²S master mode		-	25	40	mA
		sleep mode; DATA = WS = BCK = MLCK = 0 V		-	4	30	µA
Amplifier output pins; pins OUT1P, OUT1N, OUT2P and OUT2N							
$\lvert V_{O(offset)} \rvert$	output offset voltage	soft mute mode		-	-	5	mV
Power-up pin							
V_{IH}	HIGH-level input voltage	With respect to V_{SS1}		2.1	-	$V_{DDD(3V3)}$	V
V_{IL}	LOW-level input voltage	With respect to V_{SS1}		–0.3	-	+0.8	V
I_I	input current			-	0.1	20	µA
MCLK, BCK, WS, DATA pin							
V_{IH}	HIGH-level input voltage	With respect to V_{SS2}		0.7 × $V_{DDD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage	With respect to V_{SS2}		-	-	0.3 × $V_{DDD(3V3)}$	V
C_i	input capacitance			-	-	3	pF

Table 55. DC characteristics *…continued*

Unless specified otherwise, V_{DDA} = V_{DDP} = 12 V, V_{SSP1} = V_{SSP2} = 0 V, $V_{DDA(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V, V_{SS1} = V_{SS2} = REFD = REFA = 0 V, T_{amb} = 25 °C, R_L = 8 Ω, f_i = 1 kHz, f_s = 44.1 kHz, f_{sw} = 400 kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-level output voltage	At I_{OH} = –0.4 mA	$V_{DDD(3V3)}$ – 0.4 V	-	-	V
V_{OL}	LOW-level output voltage	At I_{OL} = 4 mA	-	-	400	mV
C_L	load capacitance		-	-	50	pF
SDA/MS, SCL/SFOR pin						
V_{IH}	HIGH-level input voltage	With respect to V_{SS2}	0.7 × $V_{DDD(3V3)}$	-	5.5	V
V_{IL}	LOW-level input voltage	With respect to V_{SS2}	–0.3	-	0.3 × $V_{DDD(3V3)}$	V
$V_{hys(i)}$	input hysteresis voltage	With respect to V_{SS2}	0.1 × $V_{DDD(3V3)}$	-	-	V
C_i	input capacitance		-	-	2.5	pF
V_{OL}	LOW-level output voltage	At I_{OL} = 3 mA	-	-	400	mV
ENABLE, GAIN, CSEL, ADSEL2/PLIM2, ASEL1/PLIM1 pin						
V_{IH}	HIGH-level input voltage	With respect to V_{SS2}	0.7 × $V_{DDD(3V3)}$	-	-	V
V_{IL}	LOW-level input voltage	With respect to V_{SS2}		-	0.3 × $V_{DDD(3V3)}$	V
$V_{hys(i)}$	input hysteresis voltage	With respect to V_{SS2}	0.1 × $V_{DDD(3V3)}$	-	-	V
I_I	input current		-	50	93	µA
Regulators						
V_o	output voltage	STAB1 – V_{SS1}	10	11	12	V
		STAB2 – V_{SS1}	10	11	12	V
		STABA – REFA	1.65	1.8	1.95	V
		STABD – REFD	1.65	1.8	1.95	V
CDELAY pin						
V_{CDELAY}	voltage on pin CDELAY	Relative to positive analog power supply	-	V_{DDA} –1	-	V
Crystal pins						
$V_{o(xtal)(p-p)}$	peak-to-peak crystal oscillator output voltage	With respect to V_{SS2}	-	1.8	-	V
AVOL pin						
V_i	input voltage	Mute level, with respect to V_{SS2}	0.77	0.8	0.83	V
		0 dB level with respect to V_{SS2}	2.74	2.8	2.86	V
I_I	input current		-	-	1	µA

Table 55. DC characteristics *…continued*

Unless specified otherwise, V_{DDA} = V_{DDP} = 12 V, V_{SSP1} = V_{SSP2} = 0 V, $V_{DDA(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V, V_{SS1} = V_{SS2} = REFD = REFA = 0 V, T_{amb} = 25 °C, R_L = 8 Ω, f_i = 1 kHz, f_s = 44.1 kHz, f_{sw} = 400 kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Condition		Min	Typ	Max	Unit
Thermal Foldback (TF)							
$T_{act(th\_fold)}$	thermal foldback activation temperature		[2]	118	125	132	°C
OverTemperature Protection (OTP)							
$T_{act(th\_prot)}$	thermal protection activation temperature			-	-	160	°C
OverVoltage Protection (OVP)							
$V_{P(ovp)}$	overvoltage protection supply voltage			20	22.3	24	V
UnderVoltage Protections (UVP)							
$V_{P(uvp)}$	undervoltage protection supply voltage	UVP on V_{DDA}		7	7.5	8	V
		UVP on $V_{DDA(3V3)}$		1.6	2.2	3.0	V
OverCurrent Protection (OCP)							
$I_{O(ocp)}$	overcurrent protection output current		[3]	3.0	3.3	3.6	A
Window Protection (WP)							
V_o	output voltage	high level		-	V_{DDA} − 1	-	V
		low level		-	REFA + 1	-	V
OverFrequency Protection (OFP)							
f_{OFP}	Overfrequency protection frequency	At PLL output frequency	[4]	100	140	185	MHz
UnderFrequency Protection (OFP)							
f_{UFP}	Underfrequency protection frequency	At PLL output frequency	[4]	30	45	60	MHz

[1] I_P is the current through the analog supply voltage (V_{DDA}) pin added to the current through the power supply voltage (V_{DDP}) pin.

[2] Thermal foldback temperature sensor is not located at hottest spot. Hottest spot is 12 °C higher.

[3] Current limiting concept: in overcurrent condition no interruption of the audio signal in case of impedance drop.

[4] PLL output frequency not external available.

13.2 AC characteristics

Table 56. AC characteristics

Unless specified otherwise, $V_{DDA} = V_{DDP} = 12$ V, $V_{DDA(3V3)} = V_{DDD(3V3)} = 3.3$ V, $T_{amb} = 25$ °C, $R_s < 0.1$ Ω[1], $R_L = 8$ Ω, $f_i = 1$ kHz, $f_s = 44.1$ kHz, $f_{sw} = 400$ kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Condition		Min.	Typ.	Max.	Unit
Output power per channel							
$P_{o(RMS)}$	RMS output power	Continuous time output power per channel; THD = 1 %, $R_L = 6$ Ω					
		$V_{DDA} = V_{DDP} = 12$ V		-	7.9	-	W
		$V_{DDA} = V_{DDP} = 15$ V		-	12	-	W
		Continuous time output power per channel; THD = 10 %, $R_L = 6$ Ω					
		$V_{DDA} = V_{DDP} = 12$ V		-	9.7	-	W
		Short time (≤ 10 s) output power per channel; THD = 10 %, $R_L = 6$ Ω					
		$V_{DDA} = V_{DDP} = 15$ V		-	15	-	W
		Continuous time output power per channel; THD = 1 %, $R_L = 8$ Ω					
		$V_{DDA} = V_{DDP} = 12$ V		-	6.6	-	W
		$V_{DDA} = V_{DDP} = 15$ V		-	10	-	W
		Continuous time output power per channel; THD = 10 %, $R_L = 8$ Ω					
		$V_{DDA} = V_{DDP} = 12$ V		-	8.3	-	W
		$V_{DDA} = V_{DDP} = 13.5$ V		-	10	-	W
		$V_{DDA} = V_{DDP} = 15$ V		-	12	-	W
		Short time (≤ 10 s) output power per channel; THD = 10 %, $R_L = 8$ Ω					
		$V_{DDA} = V_{DDP} = 17$ V		-	15	-	W
Performance							
THD+N	total harmonic distortion-plus-noise	$P_O = 1$ W; AES17 brick wall filter		-	0.07	0.1	%
S/N	signal-to-noise ratio	$V_O = 10$ V; A-weighted		-	103	-	dB
$V_{n(o)}$	output noise voltage	MCLK clock jitter < 200 ps; AES17 brick-wall filter					
		operating mode		-	70	-	μV
		soft mute mode		-	70	-	μV
		hard mute mode		-	30	-	μV
α_{cs}	channel separation	$P_{o(RMS)} = 1$ W; aggressor channel: $f_i = 1$ kHz		50	54	-	dB
SVRR	supply voltage ripple rejection	$V_{ripple} = 2\ V_{pp}$; $f_{ripple} = 100$ Hz		55	60	-	dB
η_{po}	output power efficiency	$R_L = 8$ Ω; $P_{o(RMS)} = 8.3$ W	[2]	-	88	-	%
		$R_L = 6$ Ω; $P_{o(RMS)} = 9.7$ W	[2]	-	83	-	%
Power-up times and delay times							
$t_{d(on)}$	turn-on delay time			-	-	155	ms

Table 56. AC characteristics *…continued*

Unless specified otherwise, V_{DDA} = V_{DDP} = 12 V, $V_{DDA(3V3)}$ = $V_{DDD(3V3)}$ = 3.3 V, T_{amb} = 25 °C, R_s < 0.1 Ω[1], R_L = 8 Ω, f_i = 1 kHz, f_s = 44.1 kHz, f_{sw} = 400 kHz, 24-bit I²S input data, MCLK clock mode, typical application diagram (Figure 13).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
t_{PD}	propagation delay	f_s =				
		8 kHz	-	3.6	-	ms
		11.025 kHz	-	2.58	-	ms
		12 kHz	-	2.39	-	ms
		16 kHz	-	1.78	-	ms
		22.05 kHz	-	1.3	-	ms
		24 kHz	-	1.18	-	ms
		32 kHz	-	892	-	µs
		44.1 kHz	-	664	-	µs
		48 kHz	-	600	-	µs
		64 kHz	-	458	-	µs
		88.2 kHz	-	320	-	µs
		96 kHz	-	306	-	µs
		128 kHz	-	67.2	-	µs
		176.4 kHz	-	48	-	µs
		192 kHz	-	40.8	-	µs
PWM output						
t_r	rise time	I_O = 0 A	-	10	-	ns
t_f	fall time	I_O = 0 A	-	10	-	ns
$t_{w(min)}$	minimum pulse width	I_O = 0 A	-	40	-	ns
R_{DSon}	drain-source on-state resistance	per output MOSFET, for low and high side	-	0.28	0.35	Ω
δ_{max}	maximum duty factor		-	-	0.96	-

[1] R_s is the series resistance of inductor of low-pass LC filter in the application.

[2] Output power measured across the loudspeaker load. This is based on indirect measurement of R_{DSon}.

13.3 Timing

Table 57. Characteristics I²C bus interface; see Figure 10

$V_{DDD(3V3)}$ = $V_{DDA(3V3)}$ = 2.7 V to 3.6 V; V_{DDA} = V_{DDP} = 8 V to 20 V; T_{amb} = −20 °C to +85 °C; all voltages referenced to ground; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{LOW}	LOW period of the SCL clock			1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	µs
t_r	rise time	SDA and SCL signals	[1]	20 + 0.1 C_b	-	-	ns
t_f	fall time	SDA and SCL signals	[1]	20 + 0.1 C_b	-	-	ns
$t_{HD;STA}$	hold time (repeated) START condition		[2]	0.6	-	-	µs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	µs

Table 57. Characteristics I²C bus interface; see Figure 10 *…continued*

$V_{DDD(3V3)}$ = $V_{DDA(3V3)}$ = 2.7 V to 3.6 V; V_{DDA} = V_{DDP} = 8 V to 20 V; T_{amb} = −20 °C to +85 °C; all voltages referenced to ground; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU;STO}$	set-up time for STOP condition		0.6	-	-	µs
t_{BUF}	bus free time between a STOP and START condition		1.3	-	-	µs
$t_{SU;DAT}$	data set-up time		100	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	µs
t_{SP}	pulse width of spikes that must be suppressed by the input filter	[3]	0	-	50	ns
C_b	capacitive load for each bus line		-	-	400	pF

[1] C_b is the total capacitance of one bus line in pF. The maximum capacitive load for each bus line is 400 pF.

[2] After this period, the first clock pulse is generated.

[3] To be suppressed by the input filter.

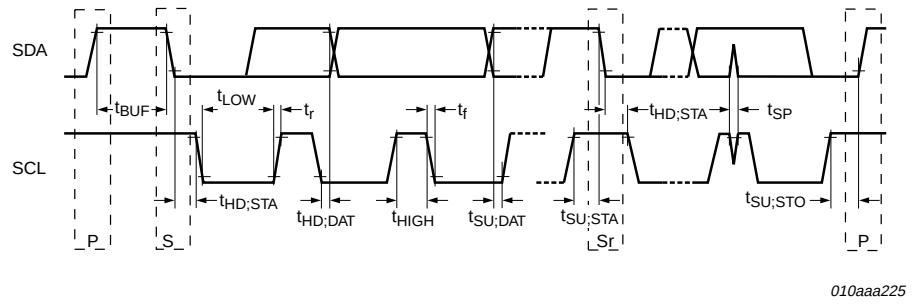


Fig 10. Timing

14. Application information

14.1 Output power estimation

The output power just before clipping can be estimated using Equation 10:

$$P_O(0.5\%) = \frac{\left(\left(\frac{R_L}{R_L + 2 \cdot (R_{DSon} + R_S)}\right) \cdot \delta_{max} \cdot V_P\right)^2}{2 \cdot R_L} \quad (10)$$

Where:

V_P = supply voltage (V) (V_{DDP}-V_{SSP}).

R_L = load impedance (Ω).

R_{DSon} = 'On' resistance power switch (Ω).

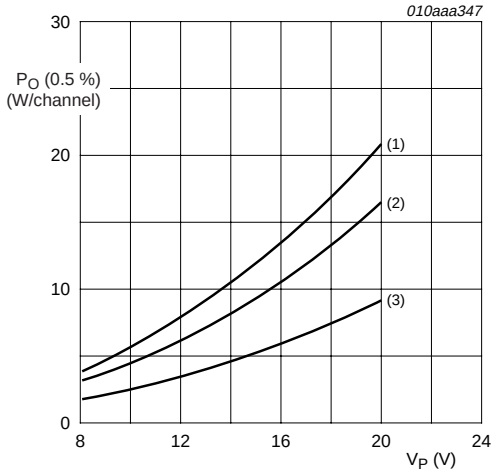
R_S = Series resistance output inductor (Ω).

δ_{max} = Maximum duty factor (0.96).

The output power at 10 % THD can be estimated using Equation 11:

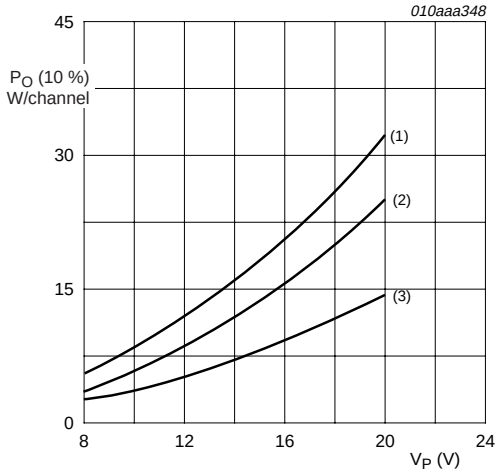
$$P_O(10\%) = 1.25 \cdot P_O(0.5\%) \quad (11)$$

Figure 11 and Figure 12 show the estimated output power at THD = 0.5 % and THD = 10 % as a function of BTL supply voltage for different load impedances.



(1) 6 Ω
(2) 8 Ω
(3) 16 Ω

Fig 11. BTL P_O (0.5 %) as a function of V_P



(1) 6 Ω
(2) 8 Ω
(3) 16 Ω

Fig 12. BTL P_O (10 %) as a function of V_P

14.2 Output current limiting

The peak output current is internally limited above a level of 3 A minimum. During normal operation the output current should not exceed this threshold level of 3 A otherwise the output signal will be distorted. The peak output current in BTL can be estimated using Equation 12:

$$I_{O(max)} \leq \frac{V_P}{R_L + 2 \cdot \langle R_{DSon} + R_S \rangle} \quad (12)$$

Where:

V_P= supply voltage (V) (V_{DDP}-V_{SSP})

R_L= load impedance (Ω)

R_{DSon}= 'On' resistance power switch (Ω)

R_S= series resistance output inductor (Ω)

Remark: A 4.8 Ω speaker (6 Ω speaker with 20 % spread) in BTL configuration can be used up to a supply voltage of 17 V without running into current limiting. Current limiting (clipping) will avoid audio holes, but it causes a distortion comparable to voltage clipping.

14.3 Speaker configuration and impedance

For a flat-frequency response (second-order Butterworth filter) it is necessary to change the low pass filter components L_{LC} and C_{LC} according to the speaker configuration and impedance.

Table 58. Filter component values

Impedance (Ω)	L_{LC} (μH)	C_{LC} (nF)
6	15	680
8	18	560
16	47	330

14.4 Typical application schematics

14.4.1 I²S slave mode and Legacy control mode

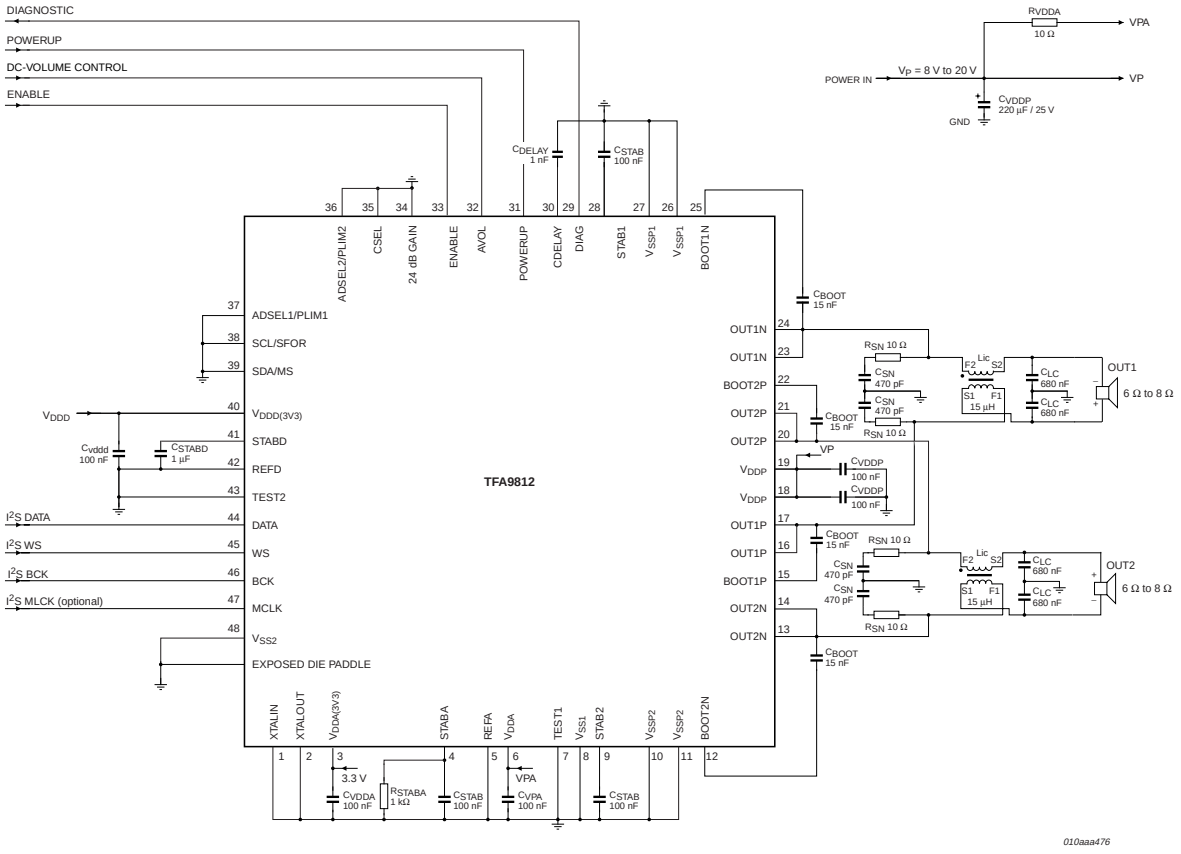


Fig 13. Simplified application diagram for I²S slave mode and Legacy control mode

14.4.2 I²S slave mode and I²C control mode

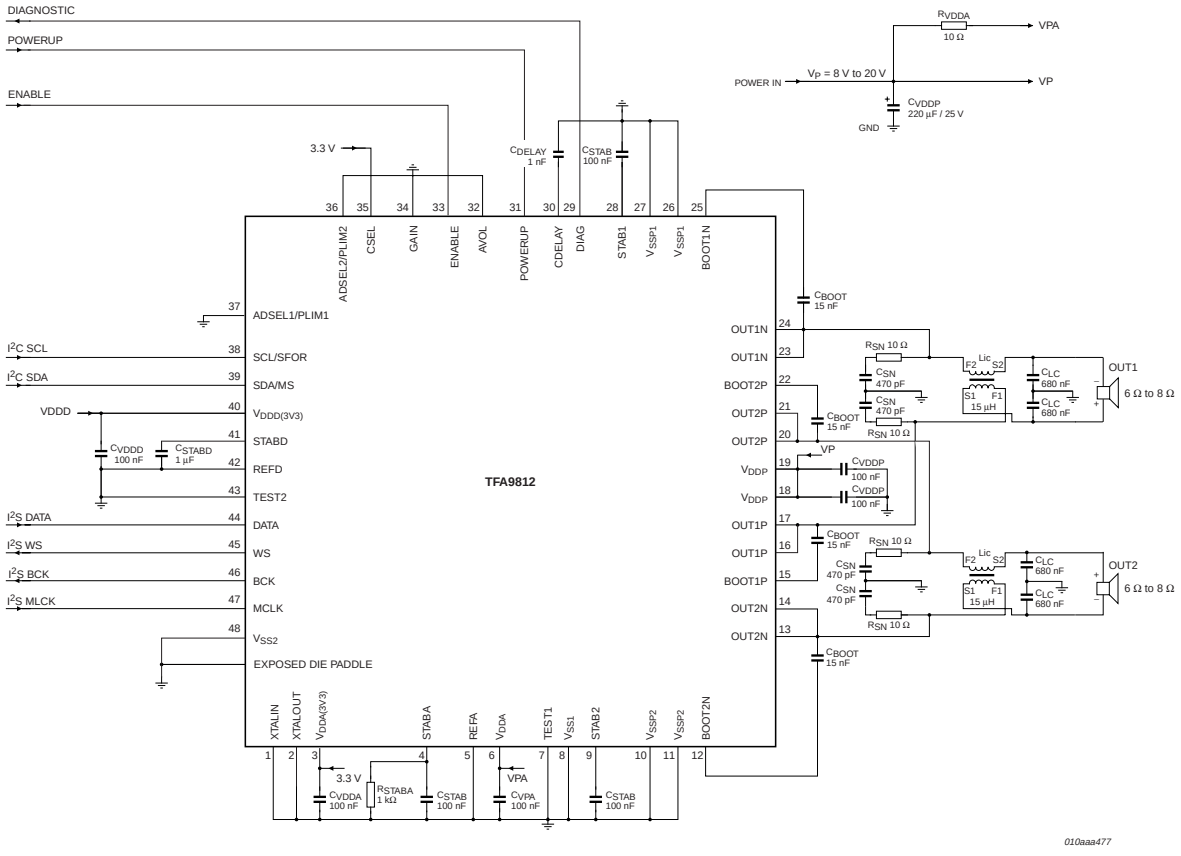


Fig 14. Simplified application diagram for I²S slave mode and I²C control mode

14.4.3 I²S master mode and Legacy control mode

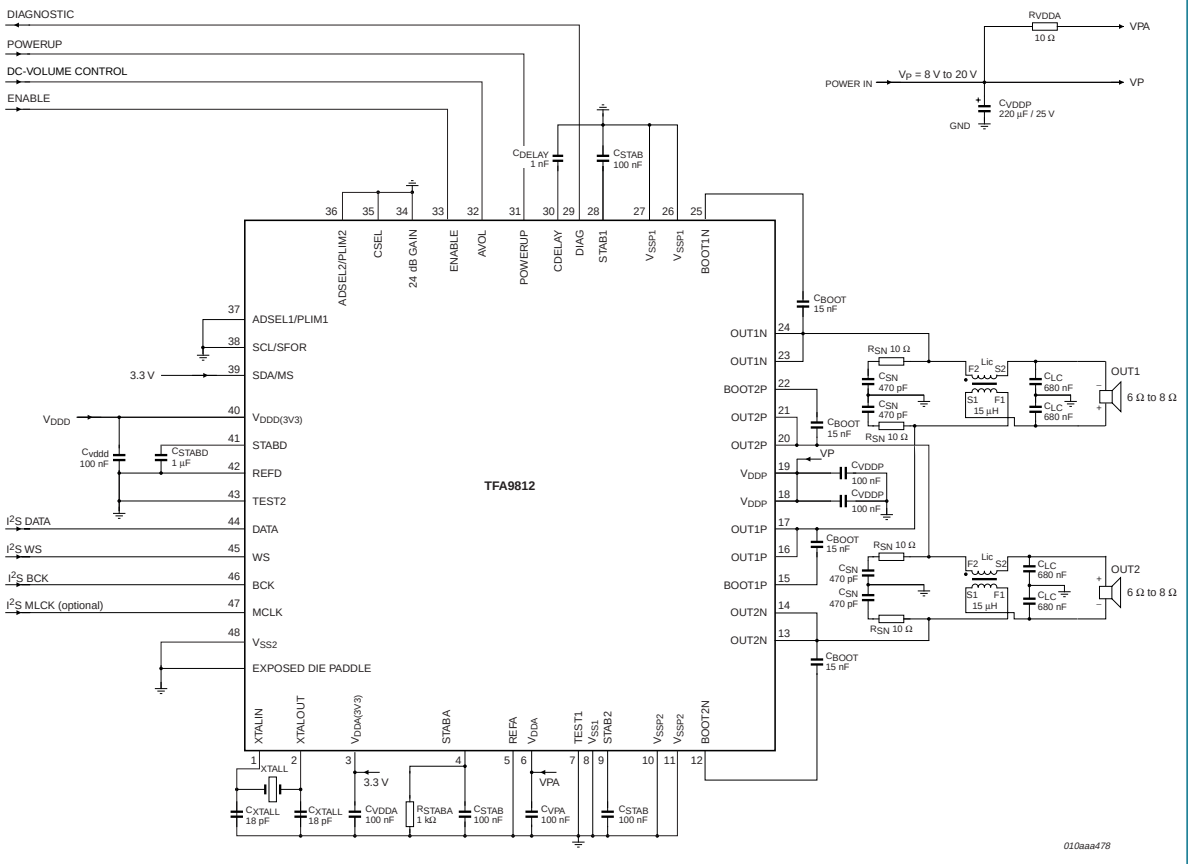


Fig 15. Simplified application diagram for I²S master mode and Legacy control mode

14.4.4 I²S master mode and I²C control mode

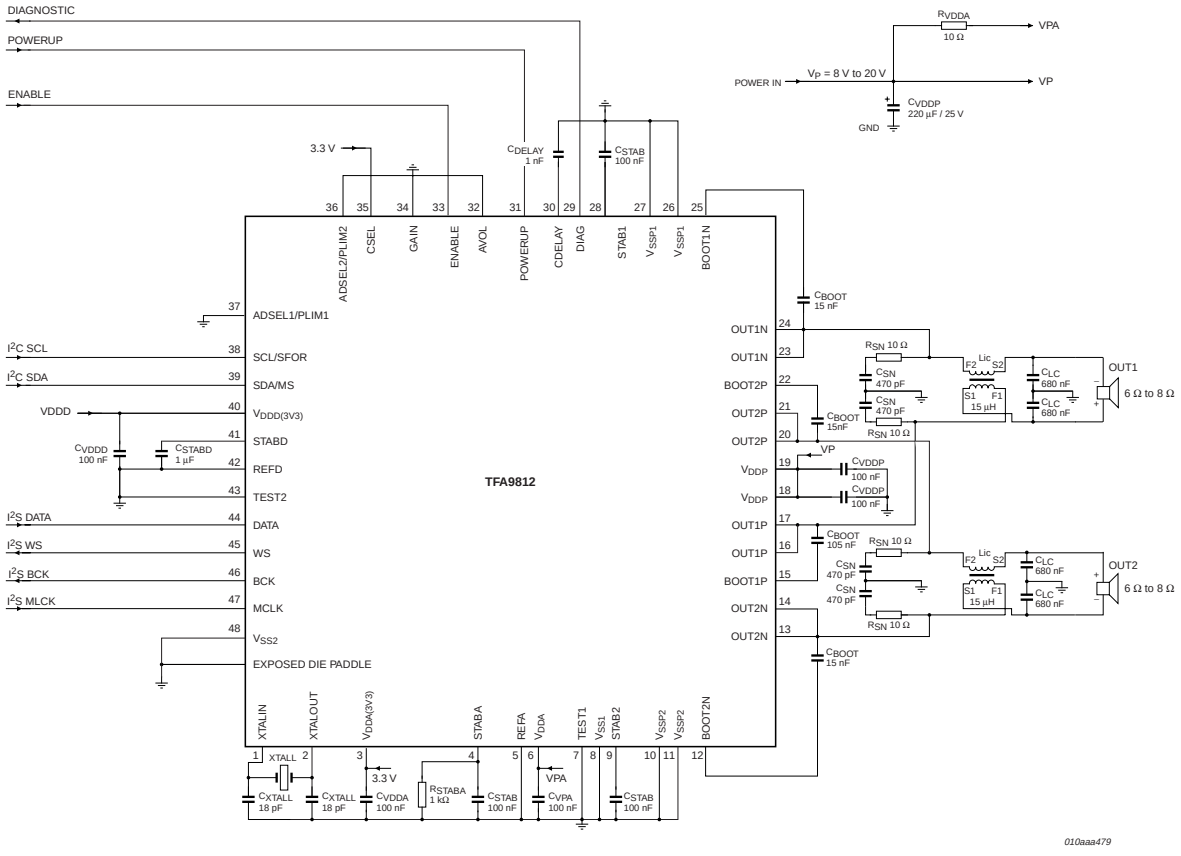
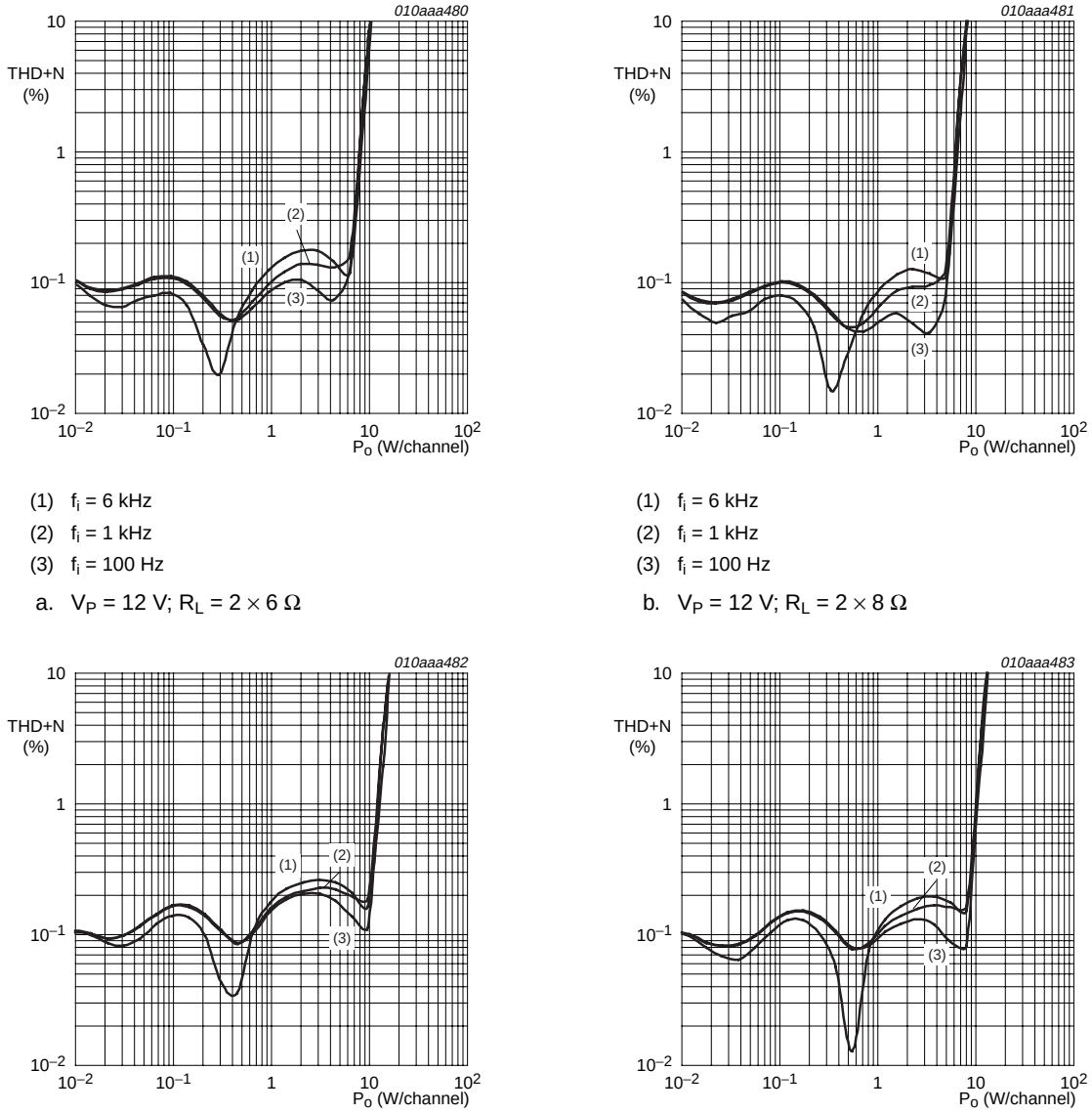


Fig 16. Simplified application diagram for I²S master mode and I²C control mode

14.5 Curves measured in typical application



(1) f_i = 6 kHz
(2) f_i = 1 kHz
(3) f_i = 100 Hz

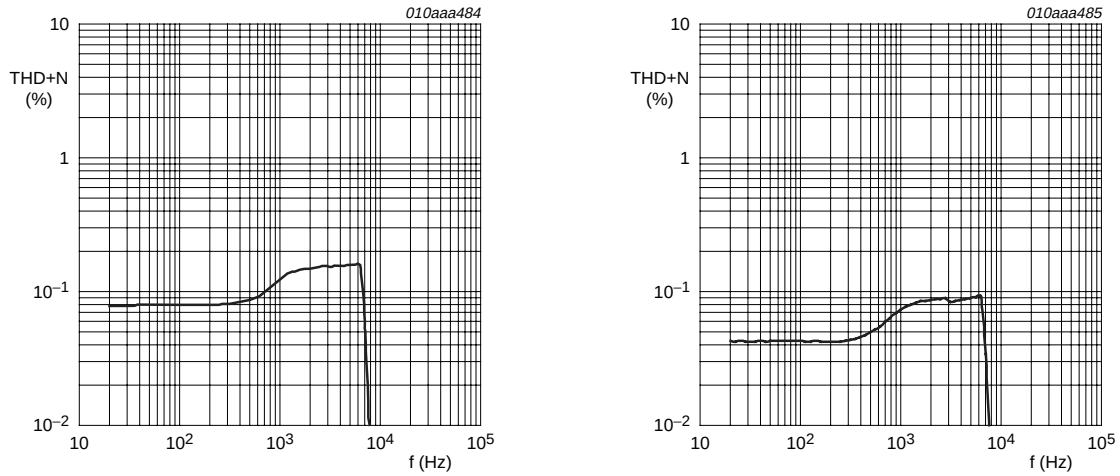
a. V_P = 12 V; R_L = 2 × 6 Ω

b. V_P = 12 V; R_L = 2 × 8 Ω

c. V_P = 15 V; R_L = 2 × 6 Ω

d. V_P = 15 V; R_L = 2 × 8 Ω

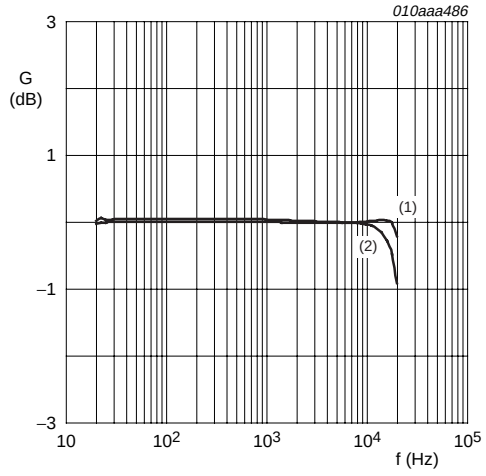
Fig 17. Total harmonic distortion-plus-noise as a function of output power



a. V_P = 12 V; R_L = 2 × 6 Ω; P_o = 1 W

b. V_P = 12 V; R_L = 2 × 8 Ω; P_o = 1 W

Fig 18. Total harmonic distortion-plus-noise as a function of frequency

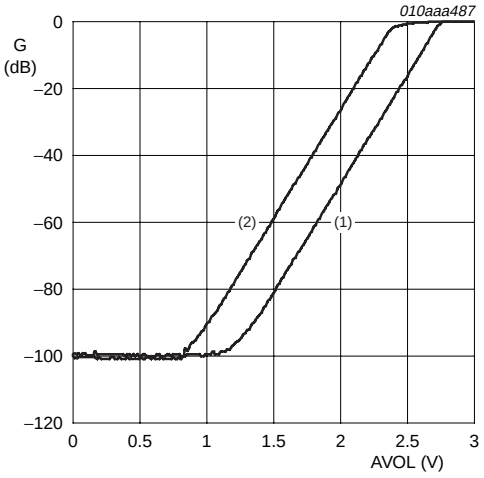


V_P = 12 V; P_O = 1 W

(1) R_L = 6 Ω 15 µH / 680 µF

(2) R_L = 8 Ω 15 µH / 680 µF

Fig 19. Gain as a function of frequency

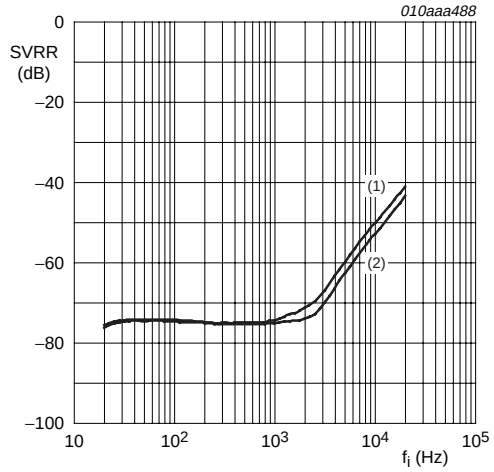


V_P = 12 V; R_L = 8 Ω; f_i = 1 kHz

(1) 0 dB

(2) 24 dB gain boost

Fig 20. Gain as a function of AVOL

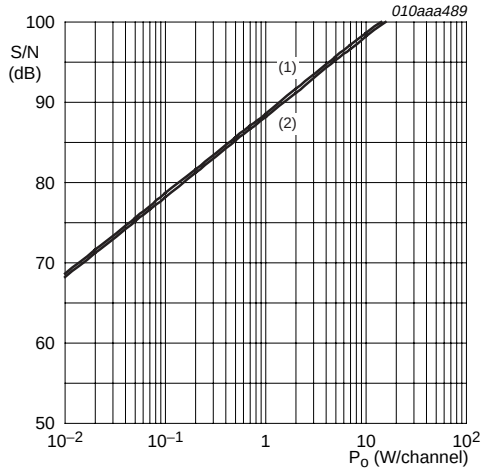


V_P = 12 V; V_{ripple} = 500 mV (RMS) reference to ground; No input signal

(1) R_L = 8 Ω

(2) R_L = 6 Ω

Fig 21. SVRR as a function of frequency

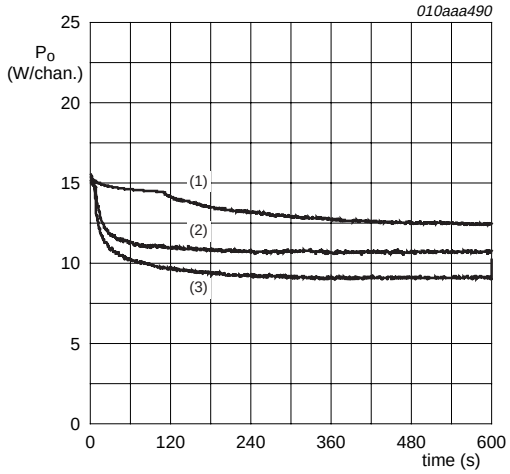


V_P = 15 V; 20 kHz AES17 filter

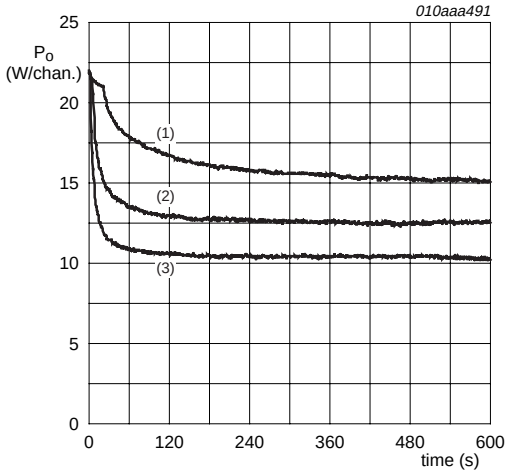
(1) R_L = 2 × 8 Ω

(2) R_L = 2 × 6 Ω

Fig 22. S/N ratio as a function of output power



a. V_P = 15 V; R_L = 2 × 6 Ω BTL; f_i = 1 kHz



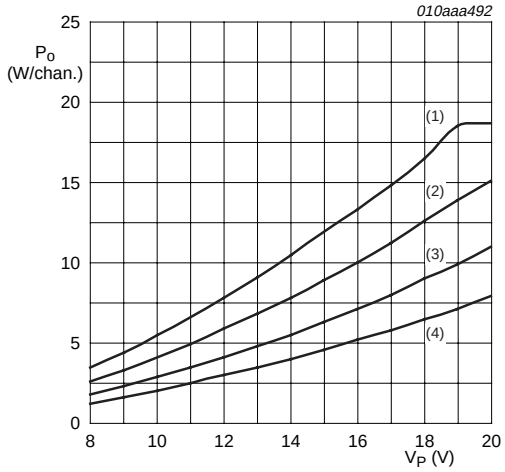
b. V_P = 20 V; R_L = 2 × 8 Ω BTL; f_i = 1 kHz

(1) $T_{act(th\_fold)}$ = 125 °C

(2) $T_{act(th\_fold)}$ = 105 °C

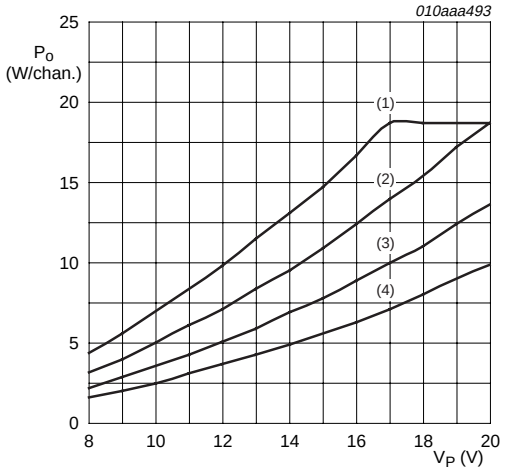
(3) $T_{act(th\_fold)}$ = 90 °C

Fig 23. Output power as a function of time



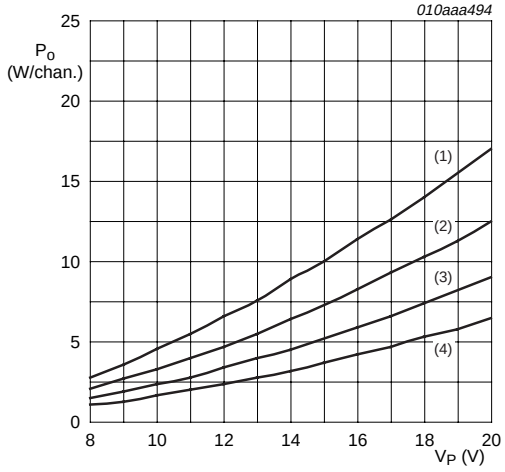
(1) Power limiter = 0 dB
(2) Power limiter = –1.5 dB
(3) Power limiter = –3 dB
(4) Power limiter = –4.5 dB

a. V_P = 12 V; R_L = 2 × 6 Ω; f_i = 1 kHz; THD = 1 %



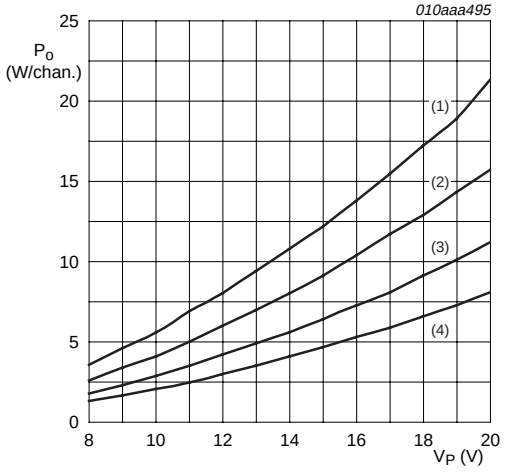
(1) Power limiter = 0 dB
(2) Power limiter = –1.5 dB
(3) Power limiter = –3 dB
(4) Power limiter = –4.5 dB

b. V_P = 12 V; R_L = 2 × 6 Ω; f_i = 1 kHz; THD = 10 %



(1) Power limiter = 0 dB
(2) Power limiter = –1.5 dB
(3) Power limiter = –3 dB
(4) Power limiter = –4.5 dB

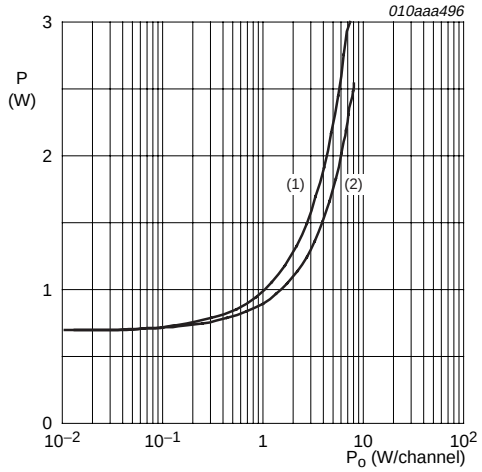
c. V_P = 15 V; R_L = 2 × 8 Ω; f_i = 1 kHz; THD = 1 %



(1) Power limiter = 0 dB
(2) Power limiter = –1.5 dB
(3) Power limiter = –3 dB
(4) Power limiter = –4.5 dB

d. V_P = 15 V; R_L = 2 × 8 Ω; f_i = 1 kHz; THD = 10 %

Fig 24. Output power as a function of supply voltage

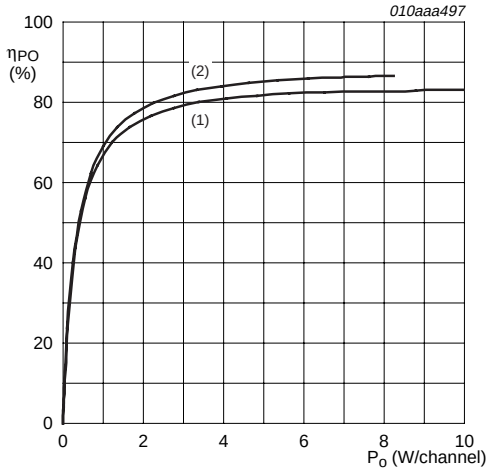


V_P = 12 V; f_i = 1 kHz; Power dissipation in junction only

(1) $R_L = 2 \times 6\ \Omega$

(2) $R_L = 2 \times 8\ \Omega$

Fig 25. Power dissipation as a function of output power

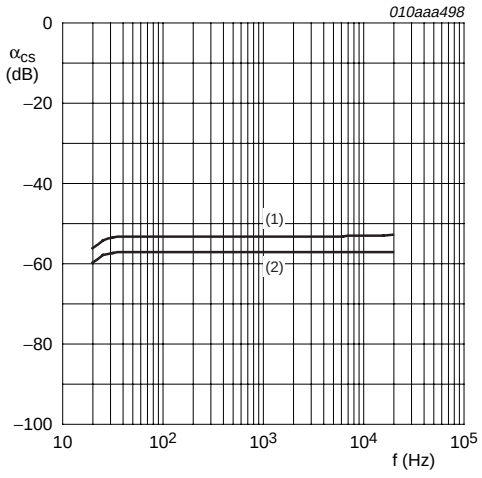


V_P = 12 V; f_i = 1 kHz; $\eta_{po} = (2 \times P_o) / (2 \times P_o + P_d)$

(1) $R_L = 2 \times 6\ \Omega$

(2) $R_L = 2 \times 8\ \Omega$

Fig 26. Efficiency as a function of output power



V_P = 12 V; P_O = 1 W

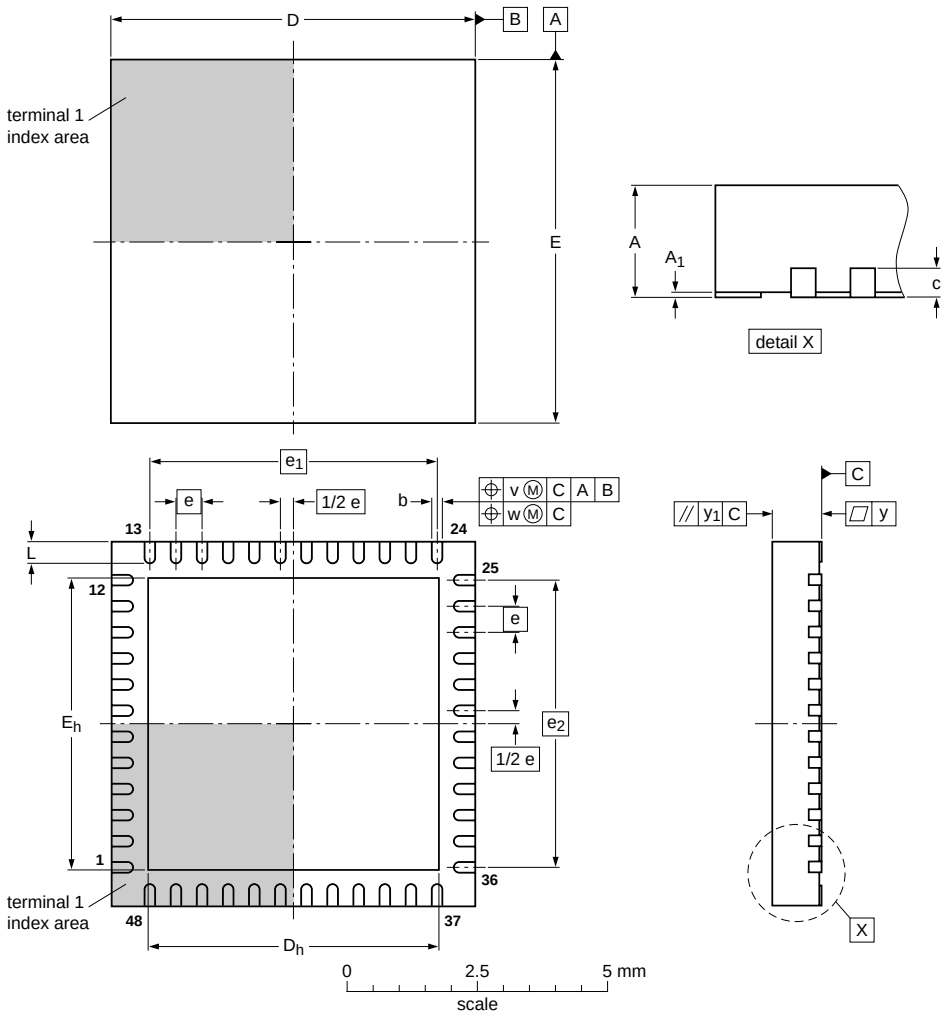
(1) $R_L = 2 \times 6\ \Omega$

(2) $R_L = 2 \times 8\ \Omega$

Fig 27. Channel separation as a function of frequency

15. Package outline

HVQFN48: plastic thermal enhanced very thin quad flat package; no leads; 48 terminals; body 7 x 7 x 0.85 mm **SOT619-8**



DIMENSIONS (mm are the original dimensions)

UNIT	$A^{(1)}$ max	A_1	b	c	$D^{(1)}$	D_h	$E^{(1)}$	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	7.1 6.9	5.75 5.45	7.1 6.9	5.75 5.45	0.5	5.5	5.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT619-8	- - -	MO-220	- - -			~~07-01-10~~ 07-01-30

Fig 28. Package outline SOT619-8 (HVQFN48)

16. Handling information

It is advisable to abide by the normal precautions appropriate to handling MOS devices.

17. Revision history

Table 59. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TFA9812_2	20090122	Preliminary data sheet	-	TFA9812_1
Modifications:	• Table 55 “DC characteristics” V_{IH} maximum value updated.			
TFA9812_1	2008/10/30	Preliminary data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents

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