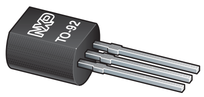


MAC97A8; MAC97A6

Logic level triac

Rev. 2 — 14 September 2011 **Product data sheet**

1. Product profile

1.1 General description

Logic level sensitive gate triac intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

Product availability:

MAC97A8 in SOT54 (TO-92)

MAC97A6 in SOT54 (TO-92).

1.2 Features and benefits

- Blocking voltage to 600 V (MAC97A8)
- Sensitive gate in all four quadrants
- RMS on-state current to 0.6 A
- Low cost package.

1.3 Applications

- General purpose bidirectional switching
- Solid state relays.
- Phase control applications

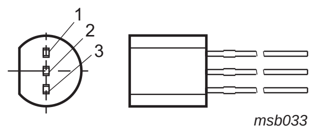
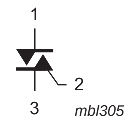
1.4 Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	MAC97A8	T_j = 25 to 125 °C	–	600	V
	MAC97A6	T_j = 25 to 125 °C	–	400	V
$I_{T(RMS)}$	on-state current (RMS value)	full sine wave; $T_{lead} \leq 50$ °C; Figure 5	–	0.6	A
I_{TSM}	non-repetitive peak on-state current		–	8.0	A

2. Pinning information

Table 2. Pinning - SOT54 (TO-92), simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	main terminal 2		
2	gate		
3	main terminal 1		
		SOT54 (TO-92)	

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
MAC97A8	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54
MAC97A6	TO-92	Plastic single-ended leaded (through hole) package; 3 leads	SOT54

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage				
	MAC97A8	T_j = 25 to 125 °C	–	600	V
	MAC97A6	T_j = 25 to 125 °C	–	400	V
$I_{T(RMS)}$	on-state current (RMS value)	full sine wave; T_{lead} ≤ 50 °C; Figure 5	–	0.6	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; T_j = 25 °C prior to surge			
		t = 20 ms	–	8.0	A
		t = 16.7 ms	–	8.8	A
I^2t	I^2t for fusing	t = 10 ms	–	0.32	A^2s
dI_T/dt	repetitive rate of rise of on-state current after triggering	I_{TM} = 1.0 A; I_G = 0.2 A; dI_G/dt = 0.2 A/µs			
		T2+ G+	–	50	A/µs
		T2+ G–	–	50	A/µs
		T2– G–	–	50	A/µs
		T2– G+	–	10	A/µs
I_{GM}	gate current (peak value)	t = 2 µs max	–	1	A
V_{GM}	gate voltage (peak value)	t = 2 µs max		5	V
P_{GM}	gate power (peak value)	t = 2 µs max	–	5	W
$P_{G(AV)}$	average gate power	T_{case} = 80 °C; t = 2 µs max	–	0.1	W
T_{stg}	storage temperature		–40	+150	°C
T_j	operating junction temperature		–40	+125	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	full cycle	60	K/W
		half cycle	80	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; lead length = 4 mm; Figure 1	150	K/W

5.1 Transient thermal impedance

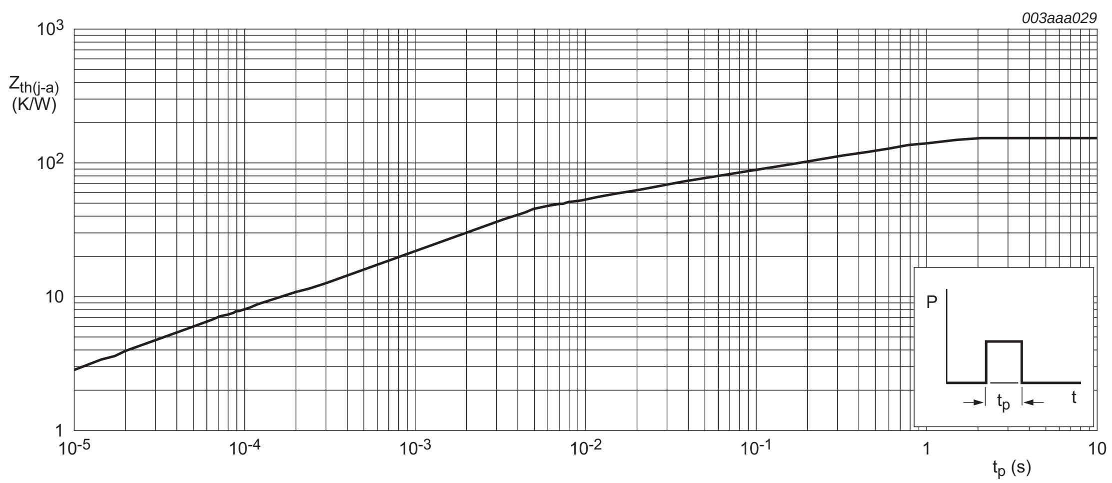
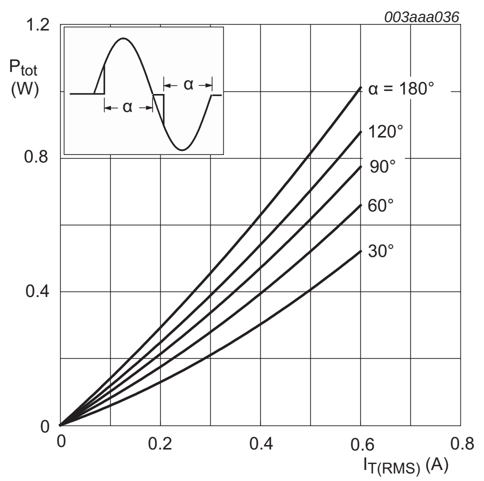


Fig 1. Transient thermal impedance from junction to ambient as a function of pulse duration.

6. Characteristics

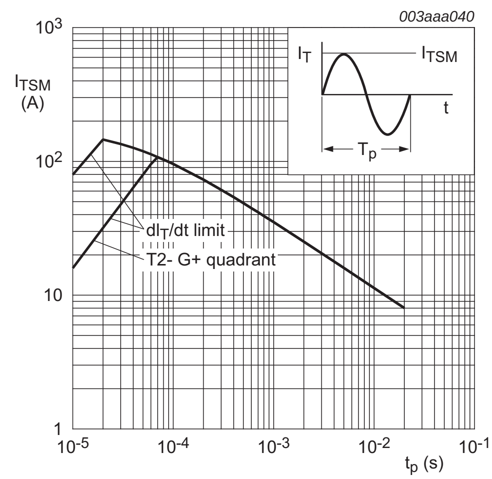
Table 6. Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; Figure 8				
		T2+ G+	–	1	5	mA
		T2+ G–	–	2	5	mA
		T2– G–	–	2	5	mA
		T2– G+	–	4	7	mA
I_L	latching current	V_D = 12 V; I_{GT} = 0.1 A; Figure 9				
		T2+ G+	–	1	10	mA
		T2+ G–	–	5	10	mA
		T2– G–	–	1	10	mA
		T2– G+	–	2	10	mA
I_H	holding current	V_D = 12 V; I_{GT} = 0.1 A; Figure 10	–	1	10	mA
V_T	on-state voltage	I_T = 0.85 A; Figure 11	–	1.4	1.9	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; Figure 7	–	0.9	2	V
		$V_D = V_{DRM}$; I_T = 0.1 A; T_j = 110 °C	0.1	0.7	–	V
I_D	off-state leakage current	$V_D = V_{DRM\ (max)}$; T_j = 110 °C	–	3	100	µA
Dynamic characteristics						
dV_D/dt	critical rate of rise of off-state voltage	V_D = 67% of $V_{DM(max)}$; T_{case} = 110 °C; exponential waveform; gate open circuit; Figure 12	30	45	–	V/µs
dV_{com}/dt	critical rate of rise of commutation voltage	V_D = rated V_{DRM}; T_{case} = 50 °C; I_{TM} = 0.84 A; commutating dI/dt = 0.3 A/ms	–	5	–	V/µs
t_{gt}	gate controlled turn-on time	I_{TM} = 1.0 A; $V_D = V_{DRM(max)}$; I_G = 25 mA; dI_G/dt = 5 A/µs	–	2	–	µs



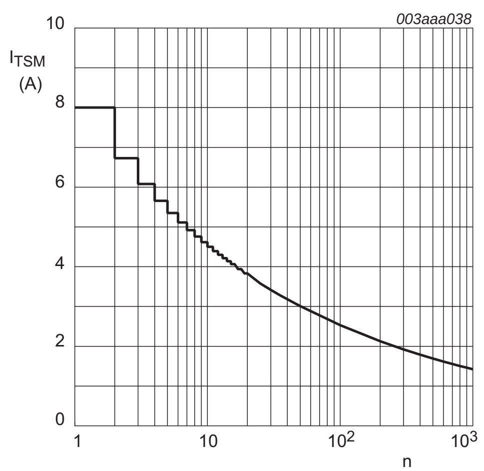
α = conduction angle

Fig 2. Maximum on-state dissipation as a function of RMS on-state current; typical values.



$t_p \leq 20$ ms

Fig 3. Maximum permissible non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; typical values.



n = number of cycles at f = 50 Hz

Fig 4. Maximum permissible non-repetitive peak on-state current as a function of number of cycles for sinusoidal currents; typical values.

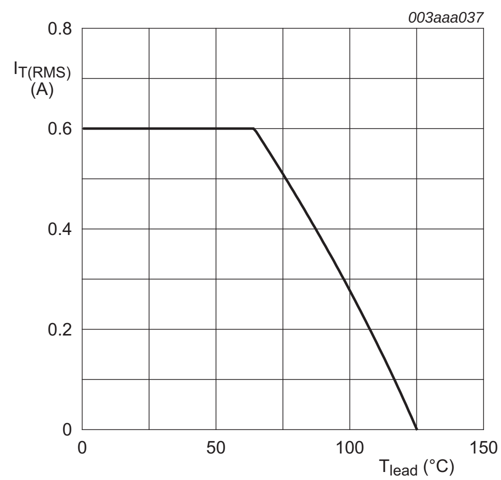
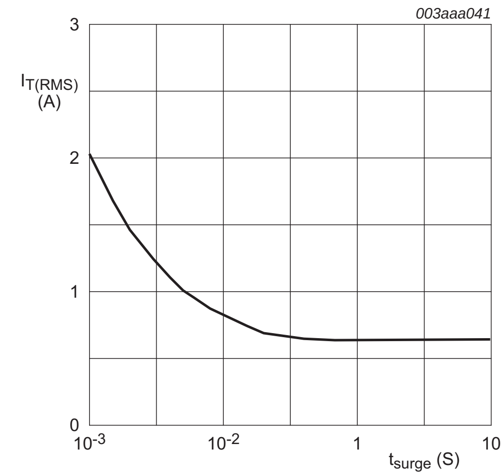
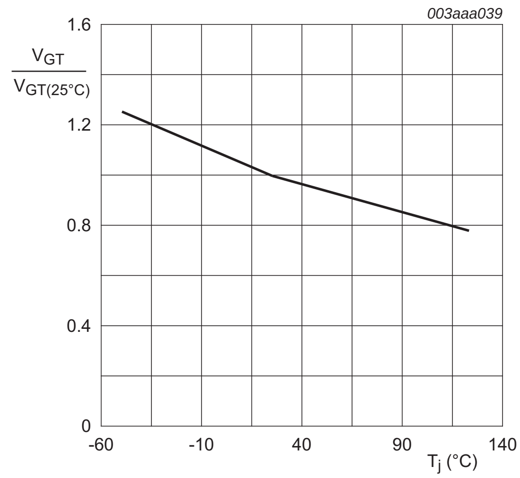


Fig 5. Maximum permissible RMS current as a function of lead temperature; typical values.



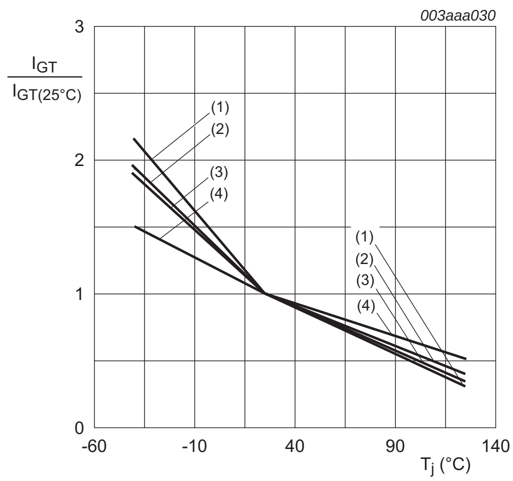
f = 50 Hz; $T_{lead} \leq 50$ °C

Fig 6. **Maximum permissible repetitive RMS on-state current as a function of surge duration for sinusoidal currents; typical values.**



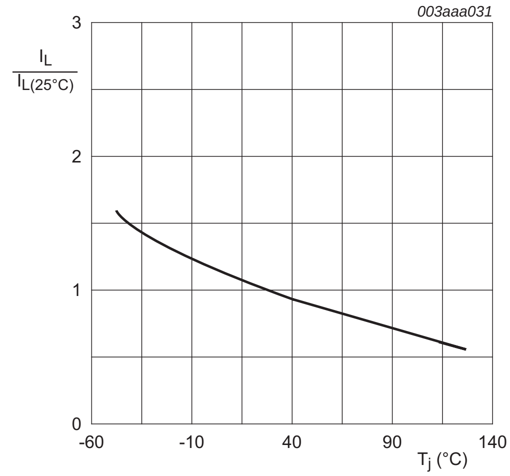
$$a = \frac{V_{GT(Tj)}}{V_{GT(25^\circ C)}}$$

Fig 7. **Normalized gate trigger voltage as a function of junction temperature; typical values.**



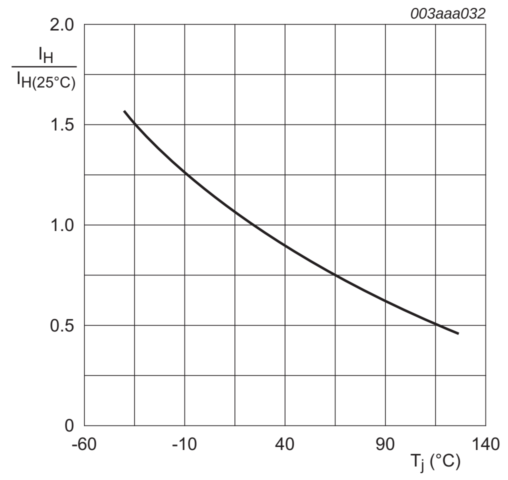
$$a = \frac{I_{GT(Tj)}}{I_{GT(25^\circ C)}}$$

Fig 8. **Normalized gate trigger current as a function of junction temperature; typical values.**



$$a = \frac{I_{L(Tj)}}{I_{L(25^\circ C)}}$$

Fig 9. **Normalized latching current as a function of junction temperature; typical values.**



$$a = \frac{I_{H(Tj)}}{I_{H(25^{\circ}C)}}$$

Fig 10. Normalized holding current as a function of junction temperature; typical values.

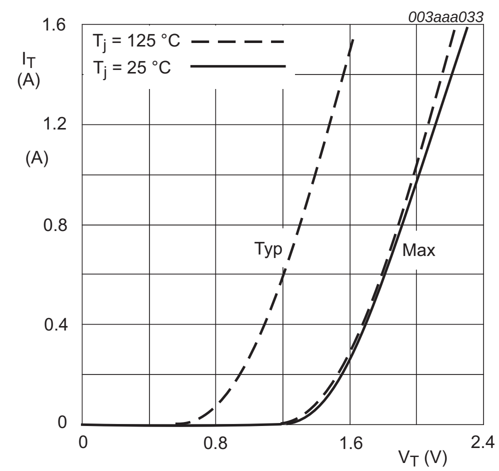


Fig 11. On-state current as a function of on-state voltage; typical and maximum values.

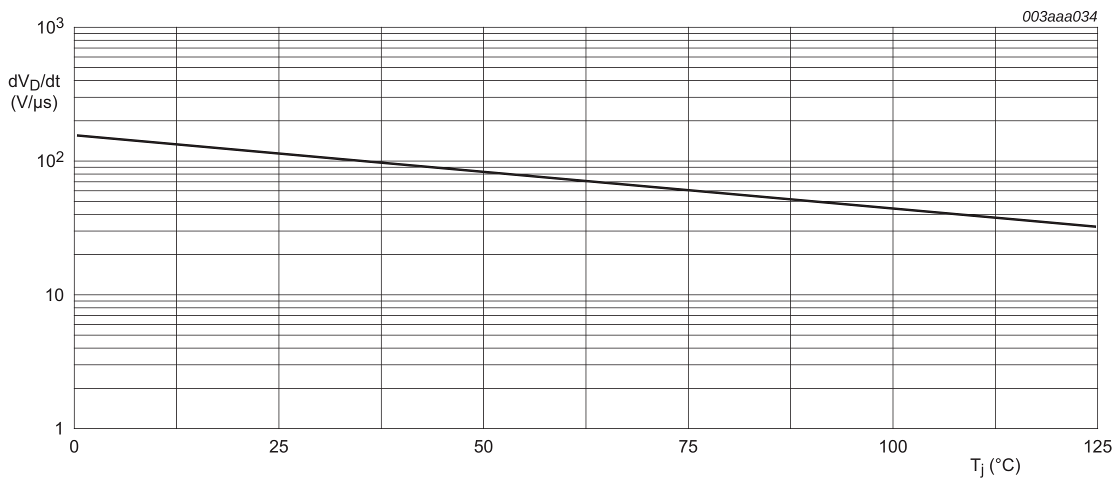
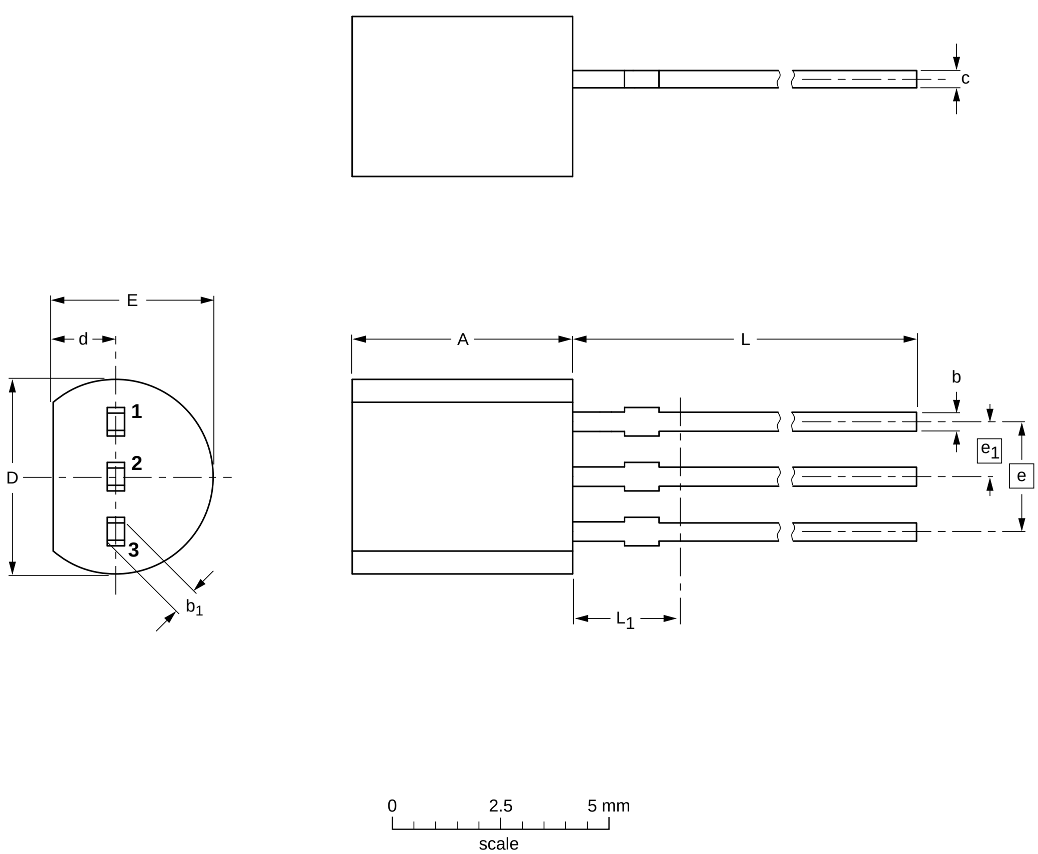


Fig 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values.

7. Package outline

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max.
mm	5.2 5.0	0.48 0.40	0.66 0.55	0.45 0.38	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

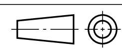
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT54		TO-92	SC-43A			~~04-06-28~~ 04-11-16

Fig 13. SOT54 (TO-92).

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MAC97A8_A6 v.2	20110914	Product data sheet	-	MAC97A8_A6 v.1 (9397 750 07917)
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Package outline drawings have been updated to the latest version. • Section 3 "Ordering information" added.			
MAC97A8_A6 v.1 (9397 750 07917)	20010329	Product specification	-	-

9. Legal information

9.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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