DATA SHEET

BF1202; BF1202R; BF1202WR

N-channel dual-gate PoLo MOS-FETs

Product specification

Supersedes data of 2000 Mar 29

2010 Sep 16

N-channel dual-gate PoLo MOS-FETs BF1202; BF1202R; BF1202WR

FEATURES

- Short channel transistor with high forward transfer admittance to input capacitance ratio
- Low noise gain controlled amplifier
- Partly internal self-biasing circuit to ensure good cross-modulation performance during AGC and good DC stabilization.

APPLICATIONS

- VHF and UHF applications with 3 to 9 V supply voltage, such as digital and analogue television tuners and professional communications equipment.

DESCRIPTION

Enhancement type N-channel field-effect transistor with source and substrate interconnected. Integrated diodes between gates and source protect against excessive input voltage surges. The BF1202, BF1202R and BF1202WR are encapsulated in the SOT143B, SOT143R and SOT343R plastic packages respectively.

PINNING

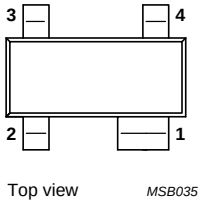
PIN	DESCRIPTION
1	source
2	drain
3	gate 2
4	gate 1

Marking code legend:

* = - : made in Hong Kong

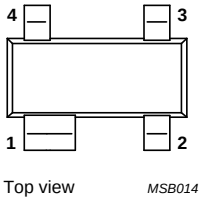
* = p : made in Hong Kong

* = t : made in Malaysia



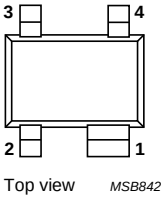
BF1202R marking code: LE*

Fig.2 Simplified outline (SOT143R).



BF1202 marking code: LD*

Fig.1 Simplified outline (SOT143B).



BF1202WR marking code: LE*

Fig.3 Simplified outline (SOT343R).

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{DS}	drain-source voltage		–	–	10	V
I_D	drain current		–	–	30	mA
P_{tot}	total power dissipation		–	–	200	mW
$\lvert y_{fs} \rvert$	forward transfer admittance		25	30	40	mS
$C_{ig1\text{-}ss}$	input capacitance at gate 1		–	1.7	2.2	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 800 MHz	–	1.1	1.8	dB
X_{mod}	cross-modulation	input level for k = 1% at 40 dB AGC	100	105	–	dBμV
T_j	operating junction temperature		–	–	150	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

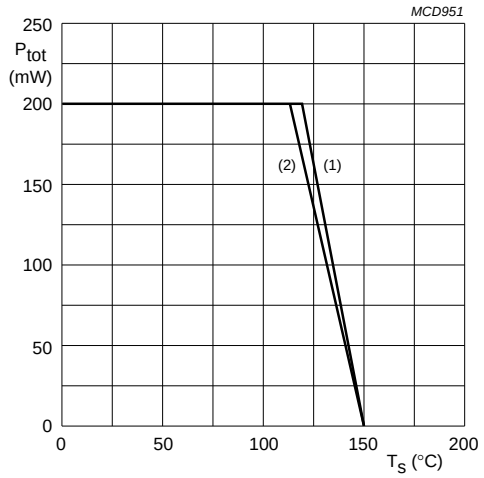
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage		–	10	V
I_D	drain current		–	30	mA
I_{G1}	gate 1 current		–	±10	mA
I_{G2}	gate 2 current		–	±10	mA
P_{tot}	total power dissipation				
	BF1202; BF1202R	$T_s \leq 113$ °C; note 1	–	200	mW
	BF1202WR	$T_s \leq 119$ °C; note 1	–	200	mW
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	150	°C

Note

1. T_s is the temperature of the soldering point of the source lead.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}s}$	thermal resistance from junction to soldering point		
	BF1202; BF1202R	185	K/W
	BF1202WR	155	K/W



(1) BF1202WR.
(2) BF1202; BF1202R.

Fig.4 Power derating curve.

STATIC CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{G1-S} = V_{G2-S} = 0$; I_D = 10 μA	10	–	V
$V_{(BR)G1-SS}$	gate 1-source breakdown voltage	$V_{G2-S} = V_{DS} = 0$; I_{G1-S} = 10 mA	6	–	V
$V_{(BR)G2-SS}$	gate 2-source breakdown voltage	$V_{G1-S} = V_{DS} = 0$; I_{G2-S} = 10 mA	6	–	V
$V_{(F)S-G1}$	forward source-gate 1 voltage	$V_{G2-S} = V_{DS} = 0$; I_{S-G1} = 10 mA	0.5	1.5	V
$V_{(F)S-G2}$	forward source-gate 2 voltage	$V_{G1-S} = V_{DS} = 0$; I_{S-G2} = 10 mA	0.5	1.5	V
$V_{G1-S(th)}$	gate 1-source threshold voltage	V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 100 μA	0.3	1.0	V
$V_{G2-S(th)}$	gate 2-source threshold voltage	V_{G1-S} = 5 V; V_{DS} = 5 V; I_D = 100 μA	0.3	1.2	V
I_{DSX}	drain-source current	V_{G2-S} = 4 V; V_{DS} = 5 V; R_{G1} = 120 kΩ; note 1	8	16	mA
I_{G1-SS}	gate 1 cut-off current	$V_{G2-S} = V_{DS} = 0$; V_{G1-S} = 5 V	–	50	nA
I_{G2-SS}	gate 2 cut-off current	$V_{G1-S} = V_{DS} = 0$; V_{G2-S} = 4 V	–	20	nA

Note

1. R_{G1} connects G_1 to V_{GG} = 5 V.

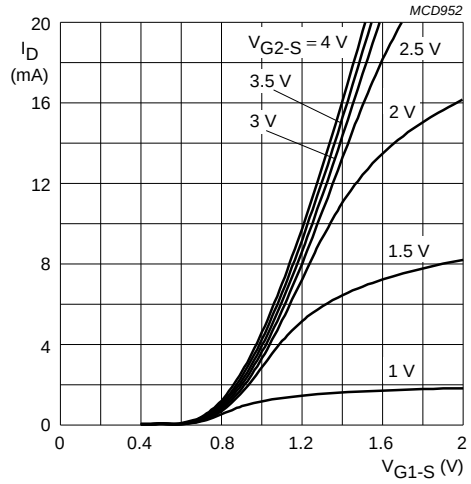
DYNAMIC CHARACTERISTICS

Common source; T_{amb} = 25 °C; V_{G2-S} = 4 V; V_{DS} = 5 V; I_D = 12 mA; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$\lvert y_{fs} \rvert$	forward transfer admittance	pulsed; T_j = 25 °C	25	30	40	mS
C_{ig1-ss}	input capacitance at gate 1	f = 1 MHz	–	1.7	2.2	pF
C_{ig2-ss}	input capacitance at gate 2	f = 1 MHz	–	1	–	pF
C_{oss}	output capacitance	f = 1 MHz	–	0.85	–	pF
C_{rss}	reverse transfer capacitance	f = 1 MHz	–	15	30	fF
F	noise figure	f = 10.7 MHz; G_S = 20 mS; B_S = 0	–	9	11	dB
		f = 400 MHz; $Y_S = Y_{S\ opt}$	–	0.9	1.5	dB
		f = 800 MHz; $Y_S = Y_{S\ opt}$	–	1.1	1.8	dB
G_{tr}	power gain	f = 200 MHz; G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 0.5 mS; $B_L = B_{L\ opt}$	–	34.5	–	dB
		f = 400 MHz; G_S = 2 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$	–	30.5	–	dB
		f = 800 MHz; G_S = 3.3 mS; $B_S = B_{S\ opt}$; G_L = 1 mS; $B_L = B_{L\ opt}$	–	26.5	–	dB
X_{mod}	cross-modulation	input level for k = 1%; f_w = 50 MHz; f_{unw} = 60 MHz; note 1				
		at 0 dB AGC	90	–	–	dBμV
		at 10 dB AGC	–	92	–	dBμV
		at 40 dB AGC	100	105	–	dBμV

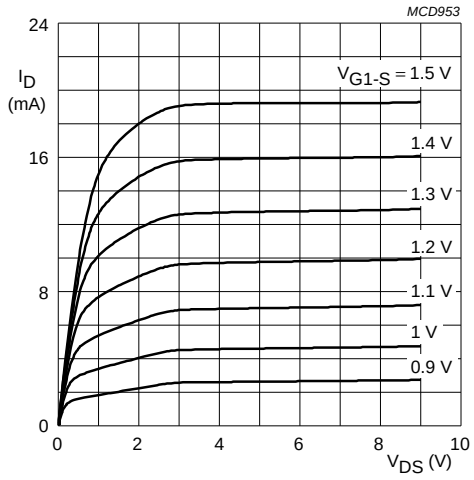
Note

1. Measured in Fig.21 test circuit.



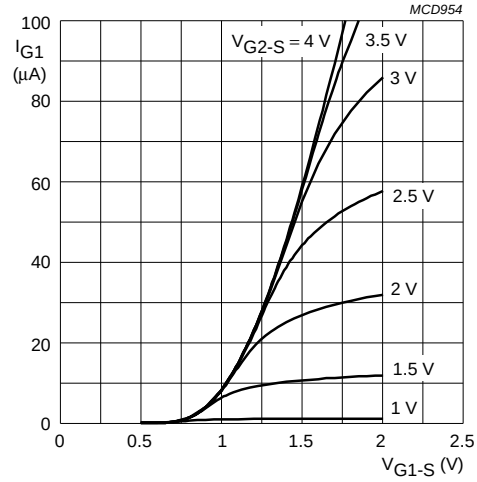
V_{DS} = 5 V.
T_j = 25 °C.

Fig.5 Transfer characteristics; typical values.



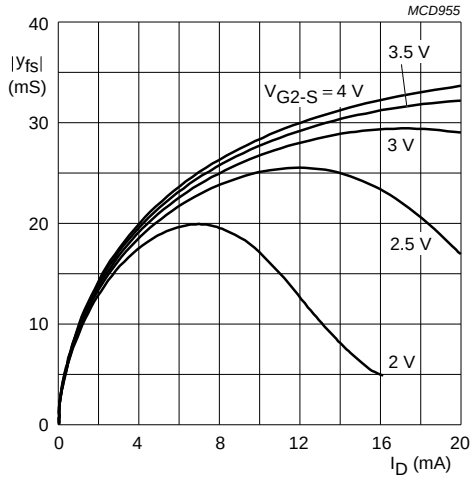
V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.6 Output characteristics; typical values.



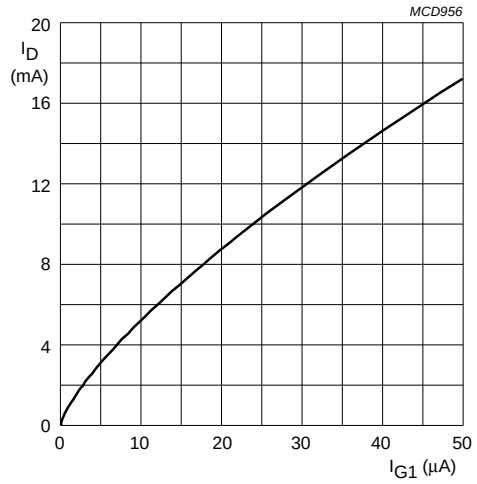
V_{DS} = 5 V.
T_j = 25 °C.

Fig.7 Gate 1 current as a function of gate 1 voltage; typical values.



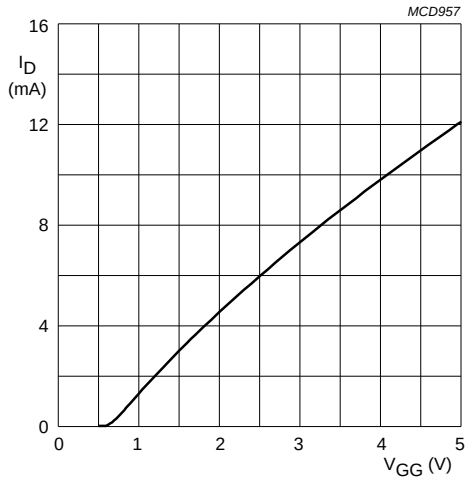
V_{DS} = 5 V.
T_j = 25 °C.

Fig.8 Forward transfer admittance as a function of drain current; typical values.



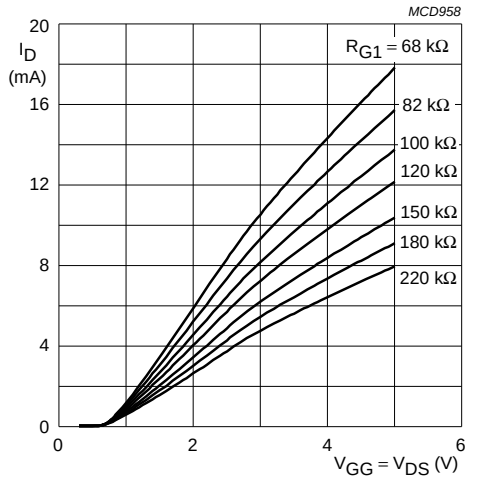
V_{DS} = 5 V; V_{G2-S} = 4 V.
T_j = 25 °C.

Fig.9 Drain current as a function of gate 1 current; typical values.



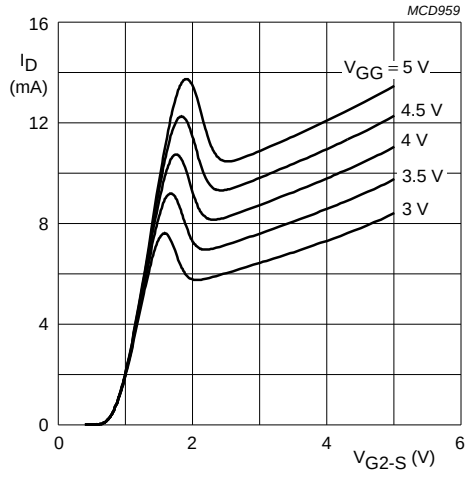
V_{DS} = 5 V; V_{G2-S} = 4 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.21.

Fig.10 Drain current as a function of gate 1 supply voltage (= V_{GG}); typical values.



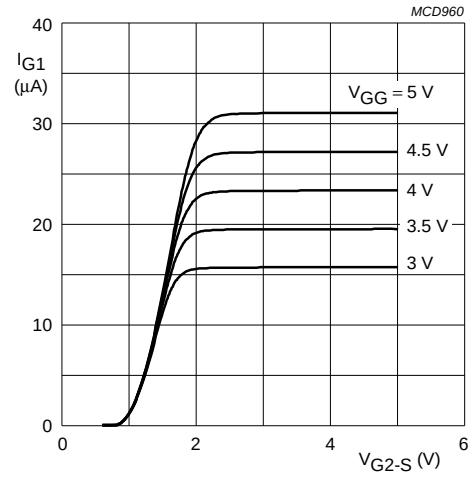
V_{G2-S} = 4 V; T_j = 25 °C.
R_{G1} connected to V_{GG}; see Fig.21.

Fig.11 Drain current as a function of gate 1 (= V_{GG}) and drain supply voltage; typical values.



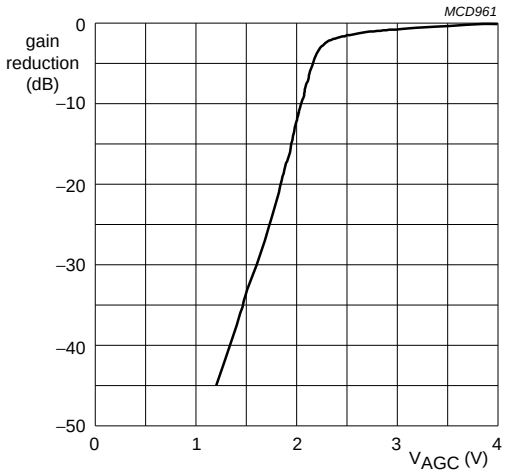
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.21.

Fig.12 Drain current as a function of gate 2 voltage; typical values.



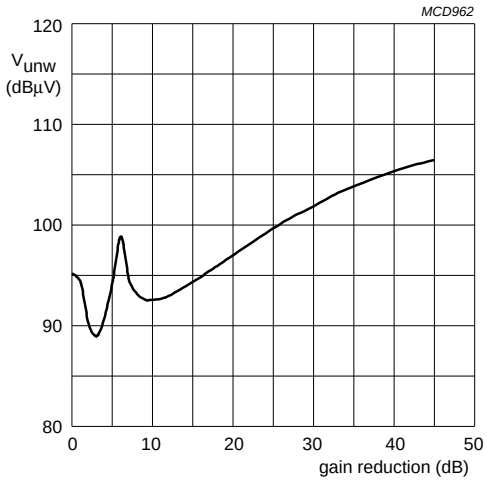
V_{DS} = 5 V; T_j = 25 °C.
R_{G1} = 120 kΩ (connected to V_{GG}); see Fig.21.

Fig.13 Gate 1 current as a function of gate 2 voltage; typical values.



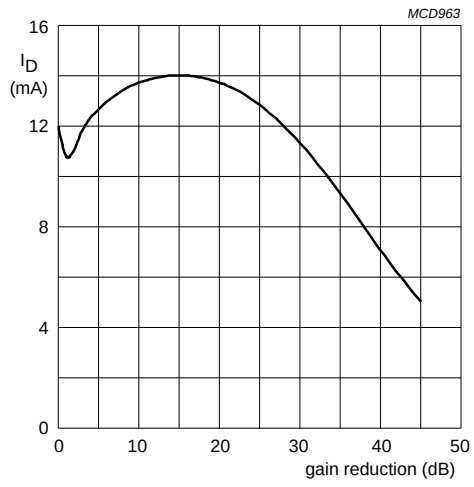
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.14 Typical gain reduction as a function of the AGC voltage; see Fig.21.



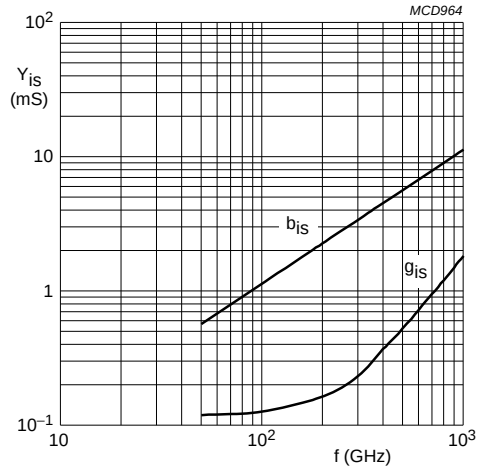
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f= 50 MHz; f_{unw} = 60 MHz; T_{amb} = 25 °C.

Fig.15 Unwanted voltage for 1% cross-modulation as a function of gain reduction; typical values; Fig.21.



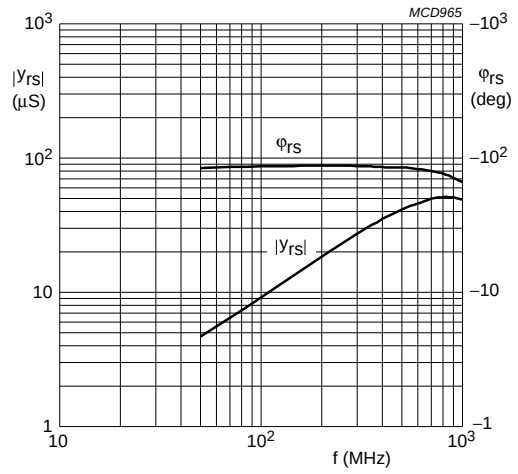
V_{DS} = 5 V; V_{GG} = 5 V; R_{G1} = 120 kΩ;
f = 50 MHz; T_{amb} = 25 °C.

Fig.16 Drain current as a function of gain reduction; typical values; see Fig.21.



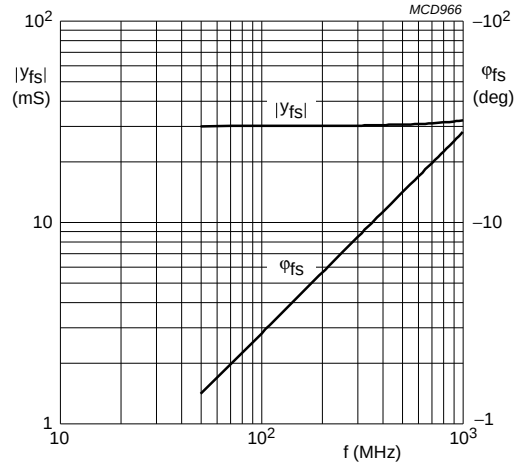
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.17 Input admittance as a function of frequency; typical values.



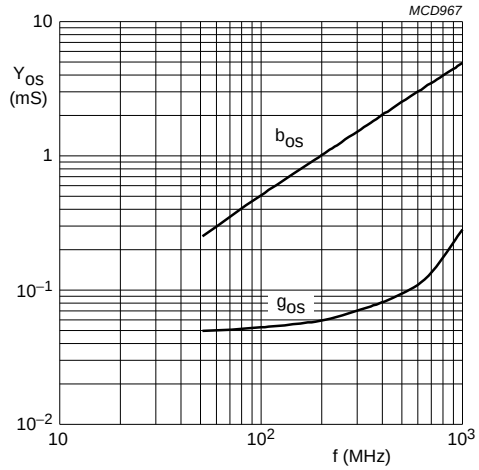
V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.18 Reverse transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.19 Forward transfer admittance and phase as a function of frequency; typical values.



V_{DS} = 5 V; V_{G2} = 4 V.
I_D = 12 mA; T_{amb} = 25 °C.

Fig.20 Output admittance as a function of frequency; typical values.

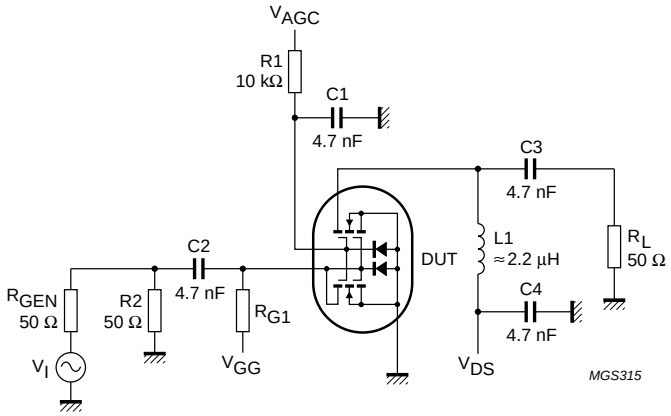


Fig.21 Cross-modulation test set-up.

Table 1 Scattering parameters: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA; T_{amb} = 25 °C

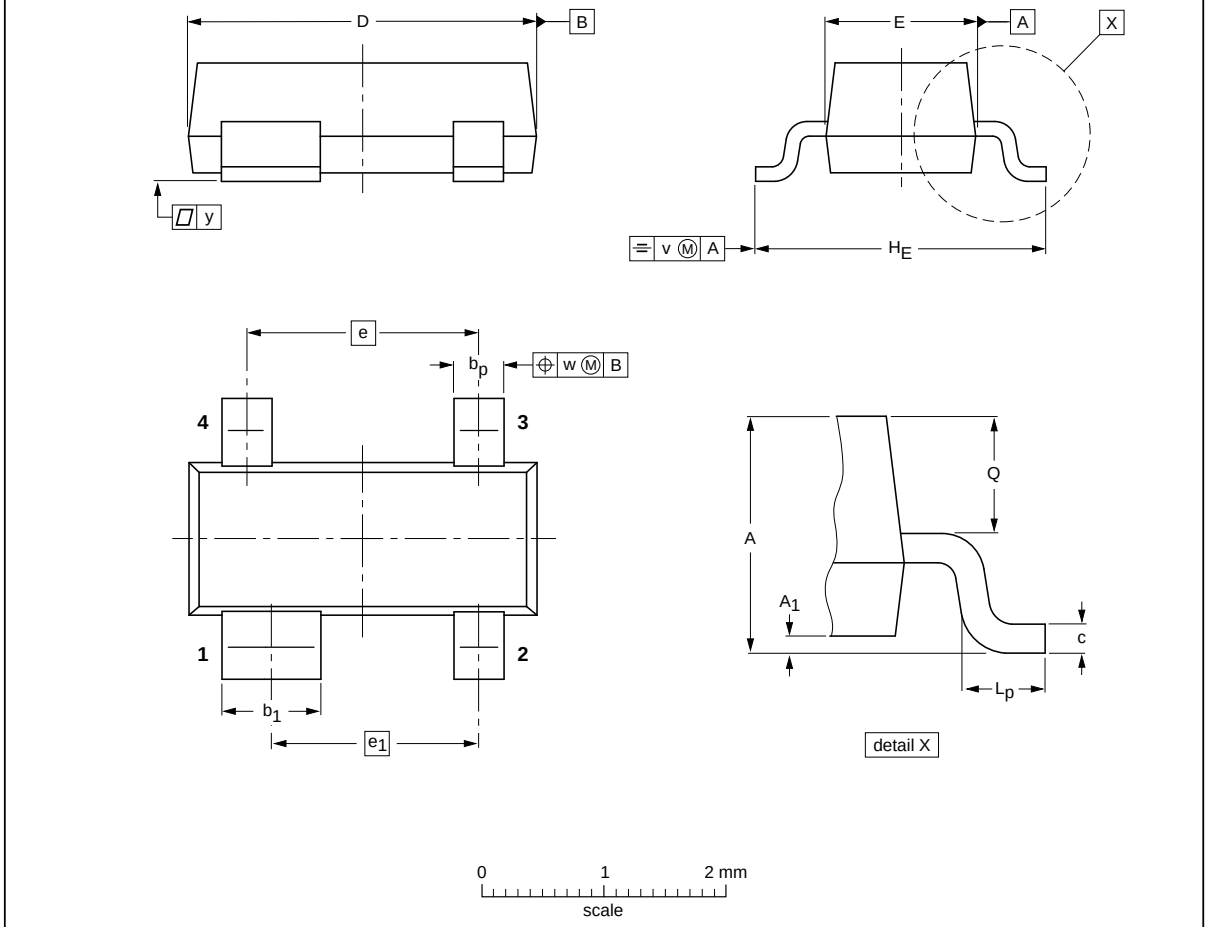
f (MHz)	s_{11}		s_{21}		s_{12}		s_{22}	
	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)	MAGNITUDE (ratio)	ANGLE (deg)
50	0.988	–3.26	2.989	176.2	0.0005	92.6	0.995	–1.50
100	0.988	–6.52	3.017	172.5	0.0009	88.0	0.995	–3.01
200	0.984	–12.99	2.990	165.0	0.0018	82.5	0.994	–5.95
300	0.977	–19.39	2.949	157.6	0.0027	78.2	0.992	–8.86
400	0.965	–25.65	2.913	150.3	0.0036	75.4	0.990	–11.79
500	0.951	–31.76	2.853	143.2	0.0039	71.8	0.988	–14.65
600	0.936	–37.68	2.793	136.3	0.0042	69.9	0.986	–17.41
700	0.919	–43.42	2.727	129.5	0.0044	68.9	0.984	–20.10
800	0.903	–48.94	2.664	123.0	0.0043	68.5	0.980	–22.69
900	0.887	–54.25	2.593	116.7	0.0041	70.7	0.975	–25.27
1000	0.870	–59.34	2.518	110.5	0.0038	72.4	0.970	–27.90

Table 2 Noise data: V_{DS} = 5 V; $V_{G2\text{-}S}$ = 4 V; I_D = 12 mA; T_{amb} = 25 °C

f (MHz)	F_{min} (dB)	Γ_{opt}		R_n (Ω)
		(ratio)	(deg)	
400	0.9	0.805	28.5	50
800	1.1	0.725	47.2	40

PACKAGE OUTLINES

Plastic surface-mounted package; 4 leads **SOT143B**

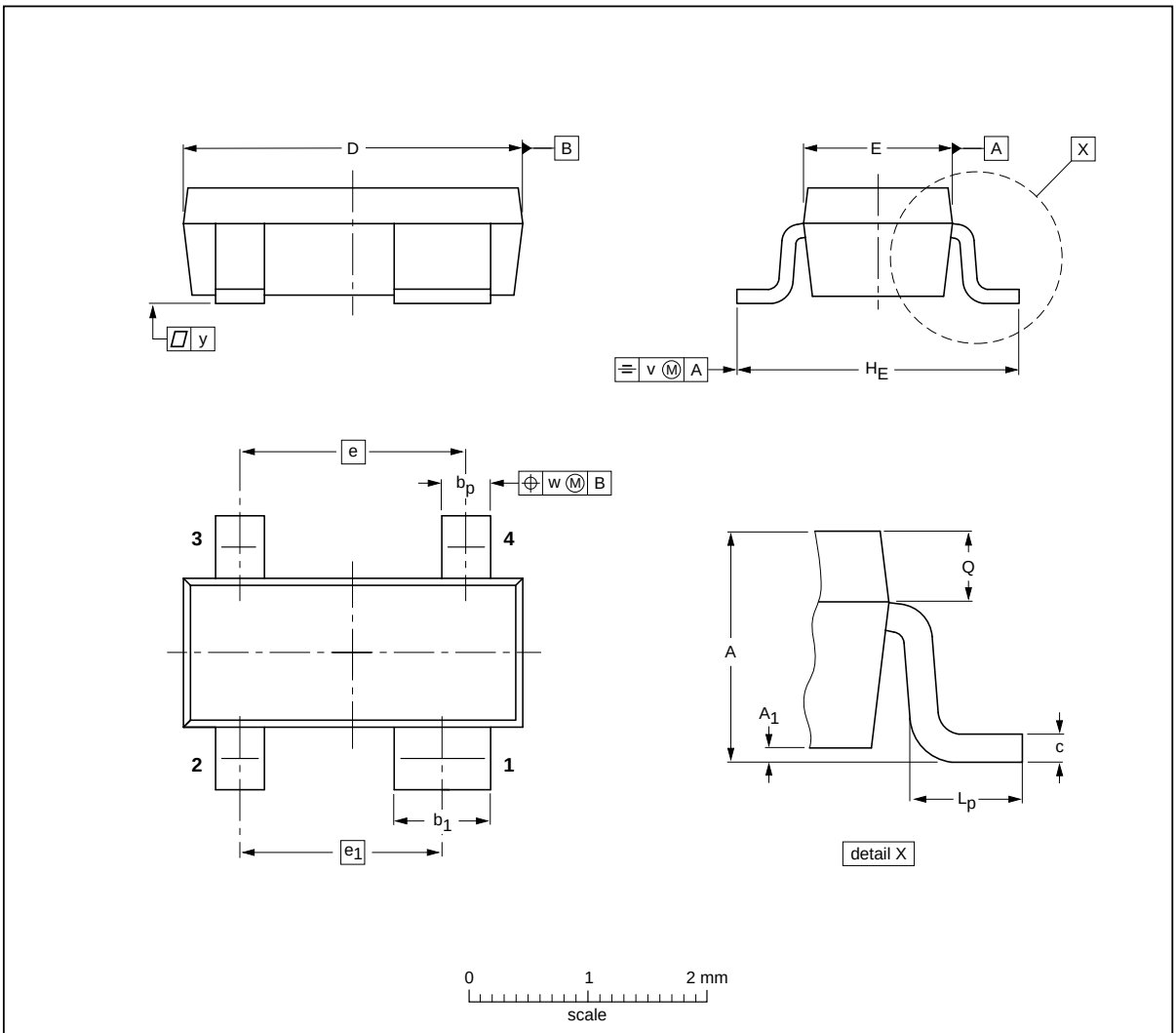


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143B						~~04-11-16~~ 06-03-16

Plastic surface-mounted package; reverse pinning; 4 leads **SOT143R**

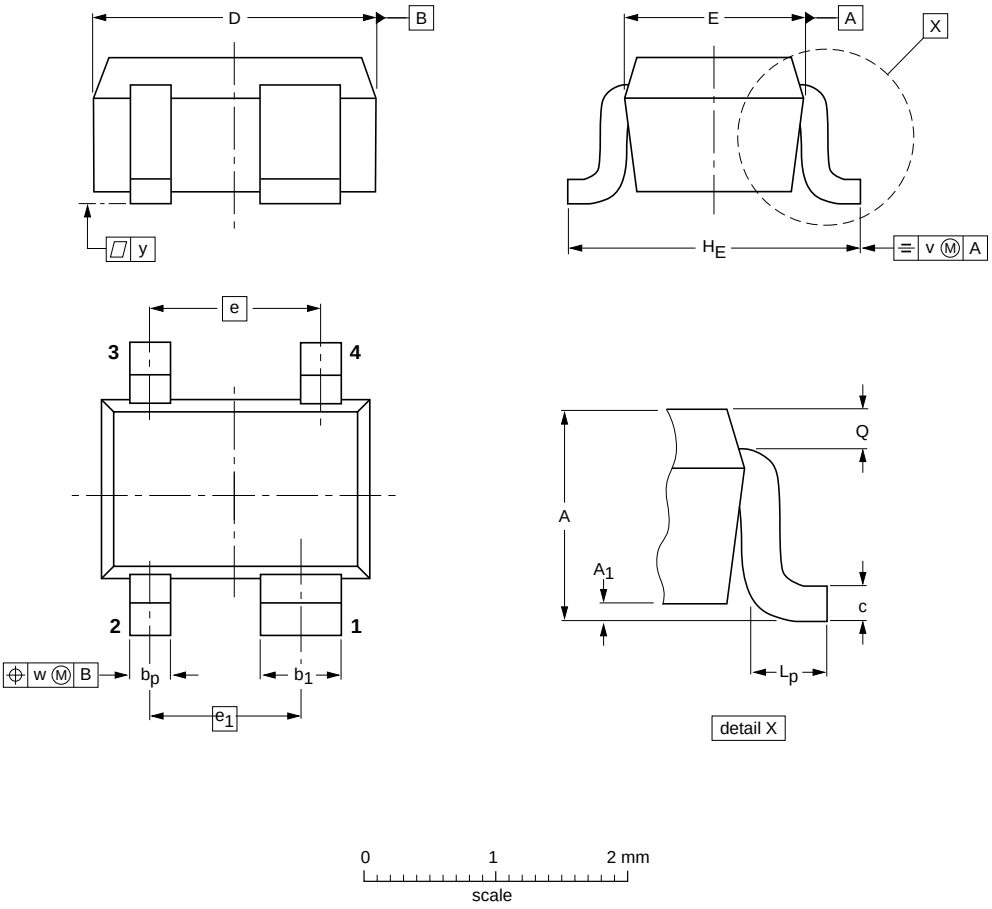


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT143R			SC-61AA			~~04-11-16~~ 06-03-16

Plastic surface-mounted package; reverse pinning; 4 leads **SOT343R**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						~~97-05-21~~ 06-03-16

DATA SHEET STATUS

DOCUMENT STATUS[1]	PRODUCT STATUS[2]	DEFINITION
Objective data sheet	Development	This document contains data from the objective specification for product development.
Preliminary data sheet	Qualification	This document contains data from the preliminary specification.
Product data sheet	Production	This document contains the product specification.

Notes

1. Please consult the most recently issued document before initiating or completing a design.
2. The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Customer notification

This data sheet was changed to reflect the new company name NXP Semiconductors, including new legal definitions and disclaimers. No changes were made to the technical content, except for the marking codes and the package outline drawings which were updated to the latest version.

Contact information

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