

Product Number Change Notice

Notification Date: Dec. 6, 2010

Dear Customers:

Thanks for your full support to Nuvoton Microcontroller Products in the past years.

This notice is to inform you that the part numbers listed in the following will be changed by Nuvoton.

NUC100LC1AN, NUC100LD1AN, NUC100LD2AN, NUC100RC1AN, NUC100RD1AN,
NUC100RD2AN, NUC120LC1AN, NUC120LD1AN, NUC120LD2AN, NUC120RC1AN,
NUC120RD1AN and NUC120RD2AN

Nuvoton provides more features in the new parts. The different features are listed in the Appendix. You can replace the corresponding part by B version without any concern. The new part numbers are listed in the following:

**NUC100LC1BN, NUC100LD1BN, NUC100LD2BN, NUC100RC1BN, NUC100RD1BN,
NUC100RD2BN, NUC120LC1BN, NUC120LD1BN, NUC120LD2BN, NUC120RC1BN,
NUC120RD1BN and NUC120RD2BN**

Nuvoton will provide the best service to you continuously.

Yours truly,

Kevin S.F. Hsieh

Microcontroller Marketing Division Director

Appendix

1. The different features list:

| Item | NUC100LC1AN, NUC100LD1AN, NUC100LD2AN, NUC100RC1AN, NUC100RD1AN, NUC100RD2AN, NUC120LC1AN, NUC120LD1AN, NUC120LD2AN, NUC120RC1AN, NUC120RD1AN, NUC120RD2AN | NUC100LC1BN, NUC100LD1BN, NUC100LD2BN, NUC100RC1BN, NUC100RD1BN, NUC100RD2BN, NUC120LC1BN, NUC120LD1BN, NUC120LD2BN, NUC120RC1BN, NUC120RD1BN, NUC120RD2BN |
|-----------------------|--|--|
| GPIO | <ul style="list-style-type: none"> Max. GPIO toggle cycle is 7 HCLK | <ul style="list-style-type: none"> Max. GPIO toggle cycle is improved from 7 HCLK to 4 HCLK. Add single bit control, all pin can be read/write individually. |
| UART | - | <ul style="list-style-type: none"> Add RS485 mode |
| EBI | <ul style="list-style-type: none"> Did not support this feature. | <ul style="list-style-type: none"> Support 8/16-bit bus width and byte write for 16-bit data bus width Only 64-pin package with EBI function |
| High performance mode | - | <ul style="list-style-type: none"> HPMEN bit in CPR0[0] (@0x50000010) is used to enable flash sequential address code fetch, SRAM read access and GPIO pin toggle speed improvement logic. HPMEN=0, flash controller, SRAM read access, and GPIO pin toggle behavior are fully compatible with NUC1XXAN. HPMEN=1, CPU performance is improved about 10% and GPIO pin toggle cycles is improved from 7 HCLK to 4 HCLK. |

2. The part number and alternate replacement part number list:

| Part number | Alternate Replacement P/N |
|-------------|---------------------------|
| NUC100LC1AN | NUC100LC1BN |
| NUC100LD1AN | NUC100LD1BN |
| NUC100LD2AN | NUC100LD2BN |
| NUC100RC1AN | NUC100RC1BN |
| NUC100RD1AN | NUC100RD1BN |
| NUC100RD2AN | NUC100RD2BN |
| NUC120LC1AN | NUC120LC1BN |
| NUC120LD1AN | NUC120LD1BN |
| NUC120LD2AN | NUC120LD2BN |
| NUC120RC1AN | NUC120RC1BN |
| NUC120RD1AN | NUC120RD1BN |
| NUC120RD2AN | NUC120RD2BN |

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